



T-46-07-11

74FCT825A 8-Bit D Flip-Flop

General Description

The 74FCT825A is an 8-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

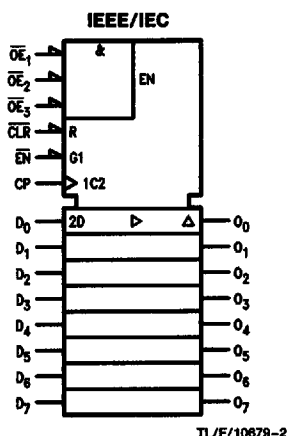
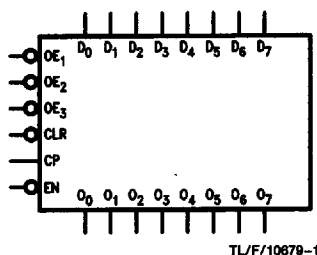
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 74FCT825A is pin and functionally equivalent to IDT 74FCT825A
- High-speed parallel registers with positive edge-triggered D-type flip flops
- Buffered common clock enable (EN) and asynchronous Clear input (CLR)
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- $I_{OL} = 48 \text{ mA (Com)}$
- CMOS power levels
- 4 kV minimum ESD immunity

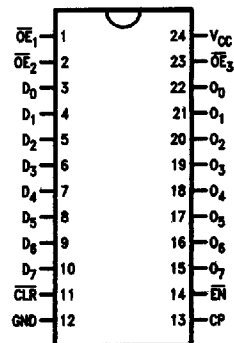
Ordering Code: See Section 8

Logic Symbols



Connection Diagram

Pin Assignment
for DIP, Flatpak and SOIC



Pin Names	Description
D ₀ -D ₇	Data Inputs
O ₀ -O ₇	Data Outputs
OE ₁ , OE ₂ , OE ₃	Output Enables
EN	Clock Enable
CLR	Clear
CP	Clock Input

Functional Description

The 'FCT825A consists of eight D-type edge-triggered flip-flops. These devices have TRI-STATE® outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable (OE) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With OE₁, OE₂ and OE₃ LOW, the contents of the flip-flops are available at the outputs. When one of OE₁, OE₂ or OE₃ is HIGH, the outputs go to the high impedance state.

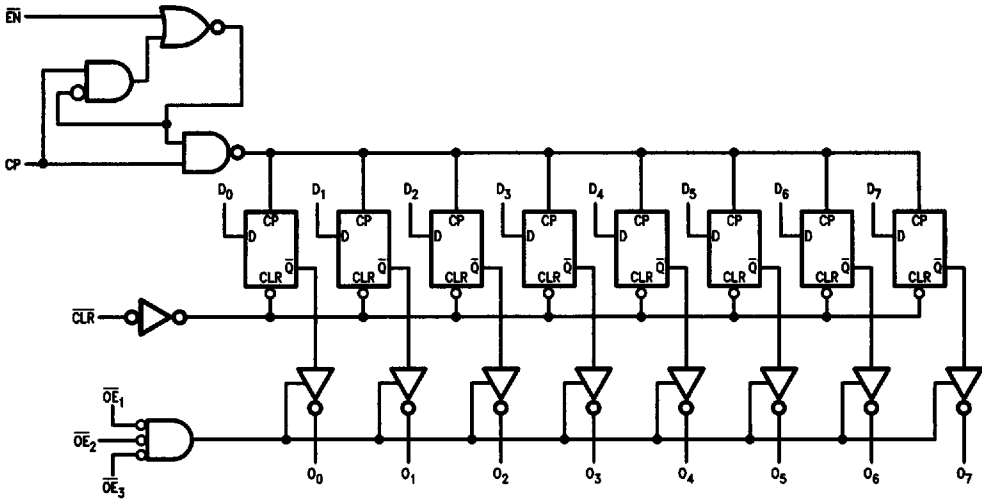
Operation of the OE input does not affect the state of the flip-flops. The 'FCT825A has Clear (CLR) and Clock Enable (EN) pins. These pins are ideal for parity bus interfacing in high performance systems. When CLR is LOW and OE is LOW, the outputs are LOW. When CLR is HIGH, data can be entered into the flip-flops. When EN is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When EN is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

inputs					Internal	Output	Function
OE	CLR	EN	CP	D _n	Q	O	
H	X	L	↗	L	L	Z	High-Z
H	X	L	↗	H	H	Z	High-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/10678-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

825A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})

74FCTA -0.5V to 7.0V

Temperature Under Bias (T_{BIAS})

74FCTA -55°C to +125°C

Storage Temperature (T_{STG})

74FCTA -55°C to +125°C

Power Dissipation (P_T) 0.5W

DC Output Current (I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})

74FCTA 4.75V to 5.25V

Input Voltage 0V to V_{CC}

Output Voltage 0V to V_{CC}

Operating Temperature (T_A)

74FCTA 0°C to +70°C

Junction Temperature (T_J)

PDIP 140°C

Note: Plastic DIP packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to 125°C.

DC Characteristics for 'FCTA Family Devices

Typical values are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type. Com: $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$; $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCTA			Units	Conditions	
		Min	Typ	Max			
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	$V_{CC} = \text{Max}$	$V_I = V_{CC}$ $V_I = 2.7V$ (Note 2)
I_{IL}	Input Low Current			-5.0 -5.0	μA	$V_{CC} = \text{Max}$	$V_I = 0.5V$ (Note 2) $V_I = GND$
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 -10.0 -10.0	μA	$V_{CC} = \text{Max}$	$V_O = V_{CC}$ $V_O = 2.7V$ (Note 2) $V_O = 0.5V$ (Note 2) $V_O = GND$
V_{IK}	Clamp Diode Voltage	-0.7	-1.2		V	$V_{CC} = \text{Min}; I_N = -18 \text{ mA}$	
I_{OS}	Short Circuit Current	-75	-120		mA	$V_{CC} = \text{Max}$ (Note 1); $V_O = GND$	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OH} = -32 \mu A$	
		V_{HC}	V_{CC}			$V_{CC} = \text{Min}$	
		2.4	4.3			$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300 \mu A$ $I_{OH} = -24 \text{ mA}$ (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OL} = 300 \mu A$	
			GND	0.2		$V_{CC} = \text{Min}$	
			0.3	0.5		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300 \mu A$ $I_{OL} = 48 \text{ mA}$ (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	$V_{CC} = \text{Max}$ $V_{IN} \geq V_{HC}; V_{IN} \leq 0.2V$ $f_I = f_{CP} = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	$V_{CC} = \text{Max}$ $V_{IN} = 3.4V$ (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)			0.35	mA/MHz	$V_{CC} = \text{Max}$ Outputs Open OE = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$

825A

DC Characteristics for 'FCTA Family Devices

Typical values are at $V_{CC} = 5.0V$, $25^{\circ}C$ ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$; $V_{HC} = V_{CC} - 0.2V$. (Continued)

Symbol	Parameter	74FCTA			Units	Conditions	
		Min	Typ	Max			
I_C	Total Power Supply Current (Note 6)			4.0	mA	$V_{CC} = \text{Max}$ Outputs Open $f_{CP} = 10 \text{ MHz}$ $OE = GND$ $f_I = 5 \text{ MHz}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				6.0			$V_{IN} = 3.4V$ $V_{IN} = GND$
				11.0		(Note 5) $V_{CC} = \text{Max}$ Outputs Open $f_{CP} = 10 \text{ MHz}$ $OE = EN = GND$ $f_I = 2.5 \text{ MHz}$ Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				16.8			$V_{IN} = 3.4V$ $V_{IN} = GND$

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + F_I N_I)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs High
 N_T = Number of Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_I = Input Frequency
 N_I = Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.

825A

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	Test Conditions	74FCTA		Units	Fig. No.
			$T_A, V_{CC} = \text{Com}$			
			Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to O_n ($\overline{OE} = \text{Low}$)	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$		10.0	ns	2-8
		$C_L = 300 \text{ pF}$ (Note 1) $R_L = 500\Omega$		20.0	ns	2-9
t_{SU}	Data to CP Setup Time	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$	4.0		ns	2-10
t_H	Data CP Hold Time		2.0		ns	2-10
t_{SU}	Enable $\overline{EN}$ to CP Setup Time		4.0		ns	2-10
t_H	Enable ($\overline{EN}$) Hold Time		2.0		ns	2-10
t_{PHL}	Propagation Delay Clear to O_1			14.0	ns	2-10
t_{REC}	Clear Recover ($\overline{CLR}$) Time		6.0		ns	2-9
t_P	Clock Pulse Width		7.0		ns	2-9
t_P	Clear ($\overline{CLR} = \text{Low}$) Pulse Width		6.0		ns	2-9
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	$C_L = 50 \text{ pF}$ $R_L = 500\Omega$		12.0	ns	2-11
		$C_L = 300 \text{ pF}$ (Note 1) $R_L = 500\Omega$		23.0	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	$C_L = 5 \text{ pF}$ (Note 1) $R_L = 500\Omega$		7.0	ns	2-11
		$C_L = 50 \text{ pF}$ $R_L = 500\Omega$		8.0	ns	2-11

Note 1: This parameter is guaranteed but not tested.

Capacitance $T_A = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$

Symbol	Parameter (Note)	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	8	12	pF

Note: This parameter is measured at characterization but not tested.