



High Speed CMOS 16-Bit Bus Register Transceiver (3-State)

QS74FCT16952T
QS74FCT162952T

FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <1 μ W typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5 ns tsk(o)
- Flow-through pinout for easy layout
- Power off disable allows hot plugging
- Extended commercial temperature: -40°C to +85°C
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise

FCT16952T

- High drive standard FCT-T outputs: IOL = +64 mA, IOH = -32 mA
- Incident switching for driving buses and large loads

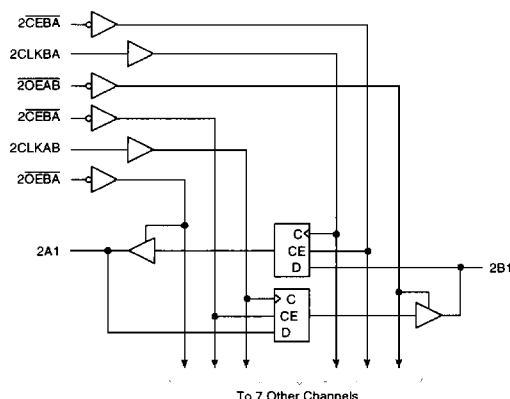
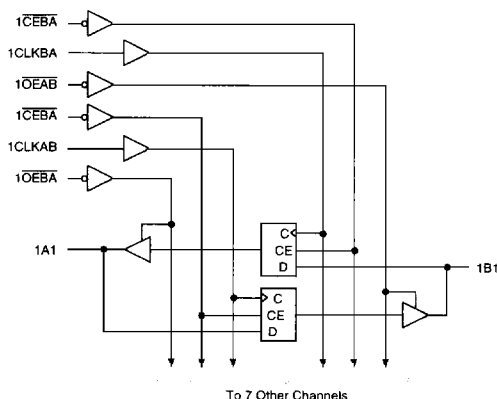
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- Balanced output drivers: ± 24 mA
- Reduced switching noise for point to point signals

DESCRIPTION

The FCT16952 family of products are 16-bit bus register transceivers with three-state outputs that are ideal for driving address and data buses. Two independent 8-bit registered transceivers are used to permit independent control of data flow in either direction. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01) and many power and ground pins provide low ground bounce. To accommodate hot-plug or live insertion applications, both versions of this product were designed not to load an active bus when Vcc is removed. In applications where bus signals are point-to-point or driving light capacitance loads, the balanced drive FCT162952 is recommended.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
(All Pins Top View)

SSOP, TSSOP

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
VCC	7	50	VCC
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
VCC	22	35	VCC
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2CEAB	26	31	2CEBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

PIN DESCRIPTION

Name	Description
xOEAB	A to B Output Enable Inputs (Active LOW)
xOEBA	B to A Output Enable Inputs (Active LOW)
xCEAB	A to B Enable Inputs (Active LOW)
xCEBA	B to A Enable Inputs (Active LOW)
xCLKAB	A to B Clock Inputs
xCLKBA	B to A Clock Inputs
xAx	A to B Data Inputs or B to A 3 State Outputs
xBx	B to A Data Inputs or A to B 3 State Outputs