HARRIS

HA-5101/883

Low Noise, High Performance Operational Amplifier

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Noise Voltage @ 1kHz..... 4.5nV/$\sqrt{Hz}$ Max
- Low Noise Current @ 1kHz.....3pA/$\sqrt{Hz}$ Max
- Wide Unity Gain Bandwidth .....10MHz Min
- High Gain (Full Temp)..... 100kV/V Min
  (Room Temp) .....1MV/V Typ
- Slew Rate .....6V/μs Min
- High CMRR/PSRR (Full Temp)..... 80dB Min
- High Output Drive Capability (Full Temp) 25mA

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators

Description

The HA-5101/883 is a dielectrically isolated operational amplifier featuring low noise and high performance. This amplifier has a excellent noise voltage density of 4.5nV/$\sqrt{Hz}$ (max) at 1kHz. The unity gain stable HA-5101/883 yields a 10MHz unity gain bandwidth and a 6V/μs slew rate.

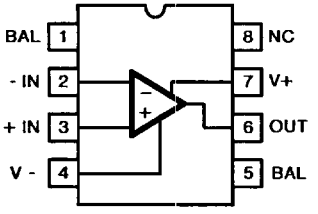
D.C. characteristics of the HA-5101/883 assure accurate performance. The 3mV (max) offset voltage is externally adjustable and offset voltage drift is just 3μV/°C. Low offset currents (200nA max) reduces input errors and with high open loop voltage gain of 100kV/V over temperature, increases the loop gain for low distortion amplification.

The HA-5101/883 is ideal for audio applications, expecially low-level signal amplifiers such as microphone, tape head, and preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators, and high Q filters.

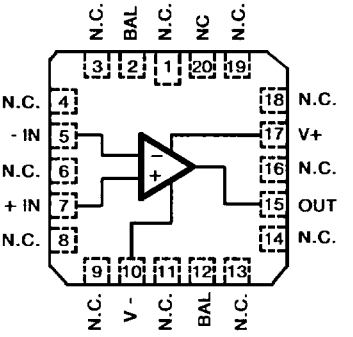
The HA-5101/883 has guaranteed operation from -55°C to +125°C, is available in Ceramic Mini-DIP, TO-99 Metal Can and 20 pin Ceramic LCC packages.

Pinouts

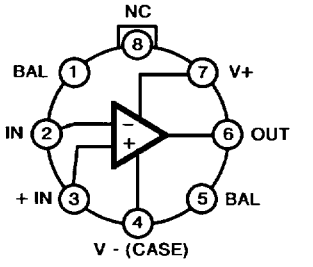
HA7-5101/883 (CERAMIC MINI-DIP)
TOP VIEW



HA4-5101/883 (CERAMIC LCC)
TOP VIEW



HA2-5101/883 (METAL CAN)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal ..... V+ to V-
Input Current 25mA
Output Short Circuit Duration ..... Indefinite
Junction Temperature (T_J) ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... <2000V
Lead Temperature (Soldering 10 sec) ..... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	82°C/W	23°C/W
Ceramic LCC Package	74°C/W	20°C/W
Metal Can Package	121°C/W	36°C/W

Package Power Dissipation Limit at +75°C for $T_J \leq +175°C$
Ceramic DIP Package 1.22W
Ceramic LCC Package 1.35W
Metal Can Package 830mW
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 12.2mW/°C
Ceramic LCC Package ..... 13.5mW/°C
Metal Can Package ..... 8.3mW/°C

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±5V to ±15V

$V_{INCm} \leq 1/2 (V+ - V-)$
$R_L \geq 500\Omega$

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, $R_{SOURCE} = 100\Omega$, $R_{LOAD} = 500k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	$V_{CM} = 0V$	1	+25°C	-3	3	mV
			2, 3	+125°C, -55°C	-4	4	mV
Input Bias Current	$+I_B$	$V_{CM} = 0V$ $+R_S = 100k\Omega$ $-R_S = 100\Omega$	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
	$-I_B$	$V_{CM} = 0V$ $+R_S = 100\Omega$ $-R_S = 100k\Omega$	1	+25°C	-200	200	nA
			2, 3	+125°C, -55°C	-325	325	nA
Input Offset Current	I_{IO}	$V_{CM} = 0V$ $+R_S = 100k\Omega$ $-R_S = 100k\Omega$	1	+25°C	-75	75	nA
			2, 3	+125°C, -55°C	-125	125	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	$V_{OUT} = 0V$ and $+10V$ $R_L = 2k\Omega$	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
	$-A_{VOL}$	$V_{OUT} = 0V$ and $-10V$ $R_L = 2k\Omega$	4	+25°C	100	-	kV/V
			5, 6	+125°C, -55°C	100	-	kV/V
Common Mode Rejection Ratio	+CMRR	$\Delta V_{CM} = +10V$ +V = +5V -V = -25V $V_{OUT} = -10V$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	$\Delta V_{CM} = -10V$ +V = +25V -V = -5V $V_{OUT} = +10V$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 100Ω, R_{LOAD} = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	$-V_{OUT1}$	R_L = 2kΩ	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
	$+V_{OUT2}$	V_{SUPPLY} = ±18V R_L = 600Ω	1	+25°C	15	-	V
			2, 3	+125°C, -55°C	15	-	V
	$-V_{OUT2}$	V_{SUPPLY} = ±18V R_L = 600Ω	1	+25°C	-	-15	V
			2, 3	+125°C, -55°C	-	-15	V
Output Current	$+I_{OUT}$	V_{OUT} = -15V V_{SUPPLY} = ±18V	1	+25°C	25	-	mA
			2, 3	+125°C, -55°C	25	-	mA
	$-I_{OUT}$	V_{OUT} = +15V V_{SUPPLY} = ±18V	1	+25°C	-	-25	mA
			2, 3	+125°C, -55°C	-	-25	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-	6	mA
			2, 3	+125°C, -55°C	-	6	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25°C	-6	-	mA
			2, 3	+125°C, -55°C	-6	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = 10V +V = +10V, -V = -15V +V = +20V, -V = -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	ΔV_{SUP} = 10V +V = +15V, -V = -10V +V = +15V, -V = -20V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Offset Voltage Adjustment	$+V_{IO}$Adj	Note 5 R_L = 2kΩ, C_L = 50pF A_V = +1V/V	1	+25°C	V_{IO}-1	-	mV
			2, 3	+125°C, -55°C	V_{IO}-1	-	mV
	$-V_{IO}$Adj		1	+25°C	V_{IO}+1	-	mV
			2, 3	+125°C, -55°C	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	4	+25°C	6	-	V/µs
	-SR	V_{OUT} = +3V to -3V	4	+25°C	6	-	V/µs
Rise & Fall Time	T_R	V_{OUT} = 0 to +200mV 10% ≤ T_R ≤ 90%	4	+25°C	-	200	ns
			5, 6	+125°C, -55°C	-	400	ns
	T_F	V_{OUT} = 0 to -200mV 10% ≤ T_R ≤ 90%	4	+25°C	-	200	ns
			5, 6	+125°C, -55°C	-	400	ns
Overshoot	+OS	V_{OUT} = 0 to +200mV	4	+25°C	-	35	%
			5, 6	+125°C, -55°C	-	35	%
	-OS	V_{OUT} = 0 to -200mV	4	+25°C	-	35	%
			5, 6	+125°C, -55°C	-	35	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_{LOAD} = 2kΩ, C_{LOAD} = 50pF, A_V = +1, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25°C	250	-	kΩ
Low Frequency Peak-to-Peak Noise	E_{np-p}	0.1Hz to 10Hz	1	+25°C	-	0.2	μV_{p-p}
Input Noise Voltage Density	E_n	R_S = 20Ω, f_O = 1000Hz	1, 4	+25°C	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_O = 1000Hz	1, 4	+25°C	-	3	$pA/\sqrt{Hz}$
Unity Gain Bandwidth	UGBW	V_O = 100mV	1	+25°C	10	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25°C	95	-	kHz
Minimum Closed Loop Stable Gain	CLSG	R_L = 2kΩ, C_L = 50pF	1	-55°C to +125°C	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	150	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55°C to +125°C	-	180	mW

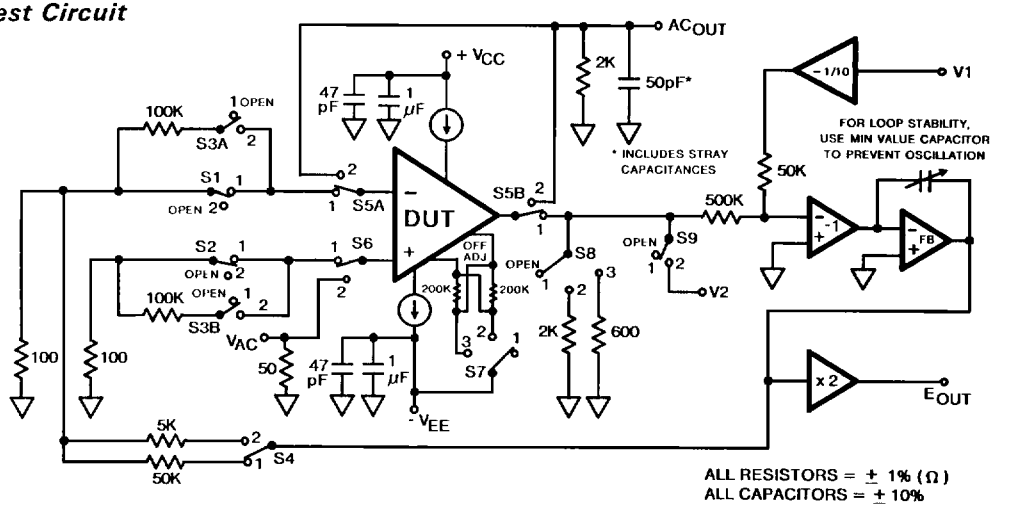
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Input Noise Voltage Density and Input Noise Current Density is sample tested on every lot.
5. Offset adjustment range is [V_{IO} (Measured) ± 1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

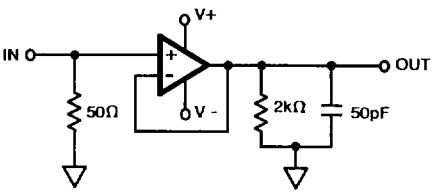
Test Circuit



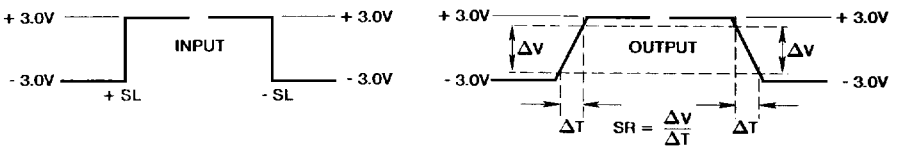
For Detailed Information, Refer to HA-5101/883 Test Tech Brief

Test Waveforms

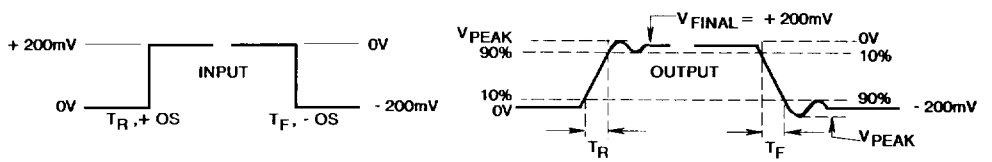
SIMPLIFIED TEST CIRCUIT (Applies To Tables 2 And 3)



SLEW RATE WAVEFORMS

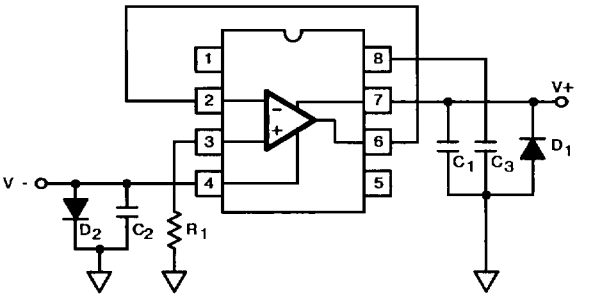


OVERSHOOT, RISE/FALL TIME WAVEFORMS

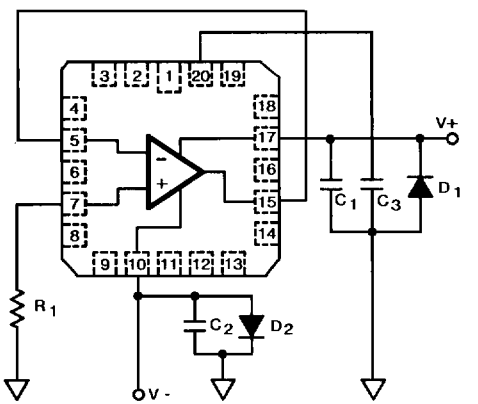


Burn-In Circuits

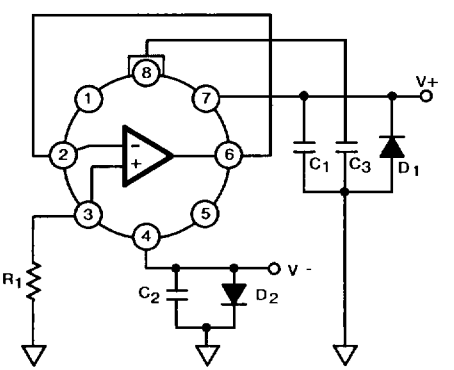
HA7-5101/883 CERAMIC MINI-DIP



HA4-5101/883 CERAMIC LCC



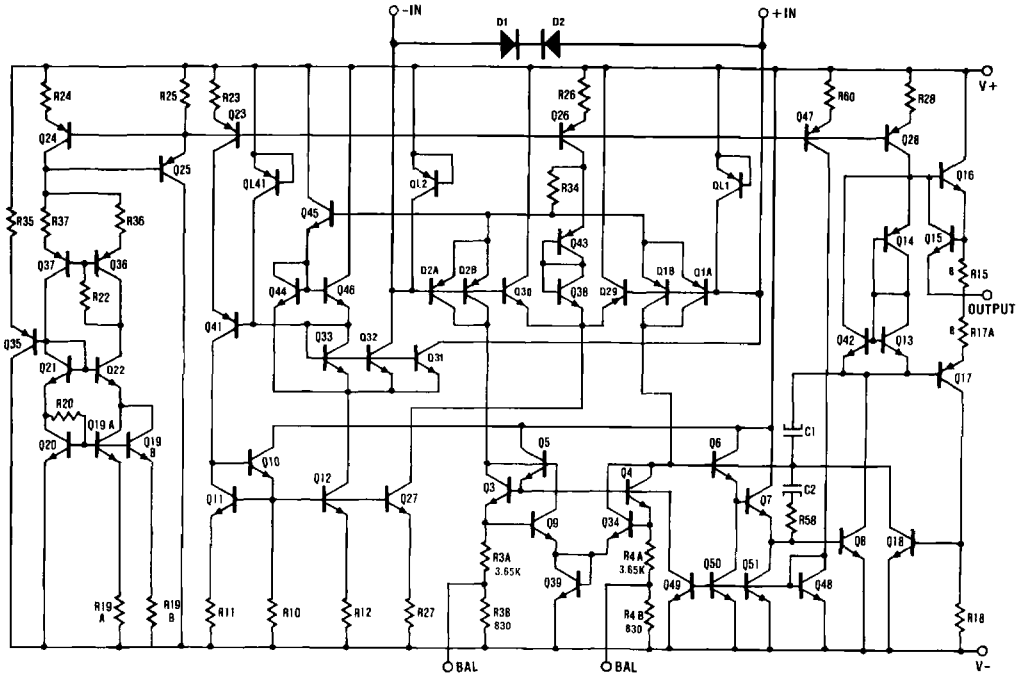
HA2-5101/883 (TO-99) METAL CAN



NOTES:

R_1 = 1MΩ, ±5%, 1/4W (Min)
C_1 = C_2 = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)
C_3 = 0.01μF/Socket, 10%
D_1 = D_2 = IN4002 or Equivalent/Board
$|(V+) - (V-)|$ = 30V

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
68.9 x 69.3 x 19 mils
(1750 x 1760 x 483 µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
1.38 x 10^5A/cm^2 at 30mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

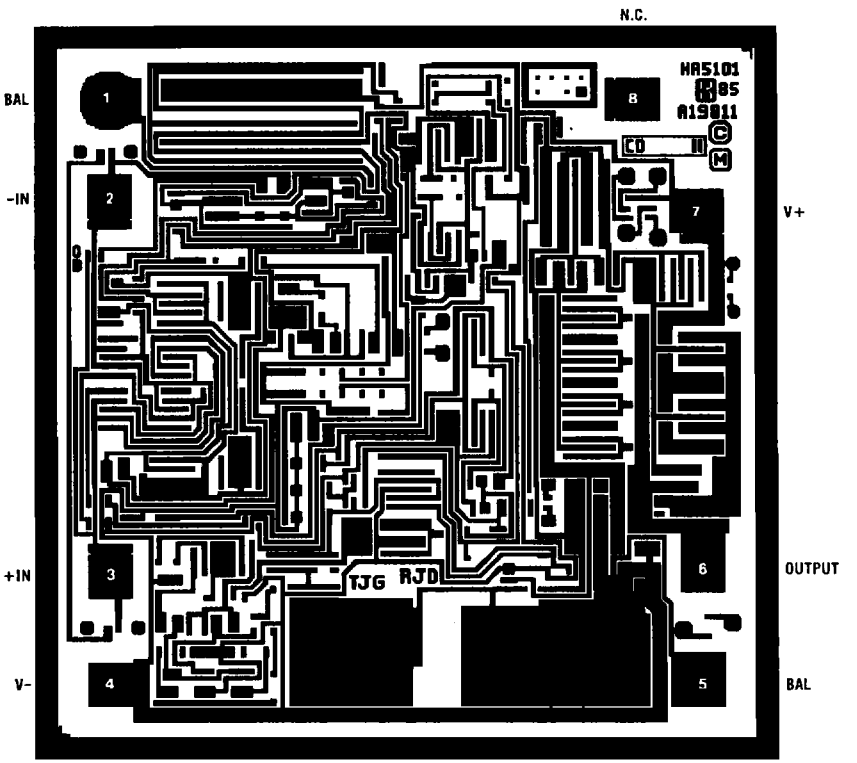
TRANSISTOR COUNT: 54

PROCESS: HFSB Bipolar Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)
Metal Can — 420°C (Max)

Metallization Mask Layout

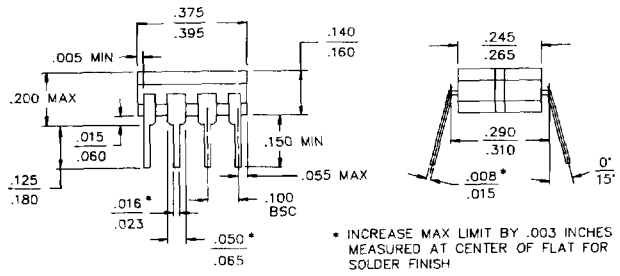
HA-5101/883



NOTE: Pin Numbers Correspond to Ceramic Mini-DIP and Metal Can Packages Only.

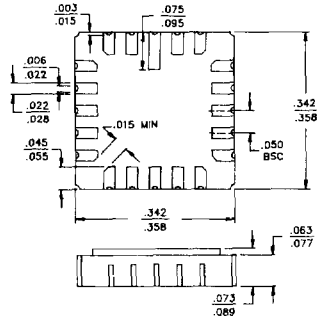
Packaging †

8 PIN CERAMIC DIP



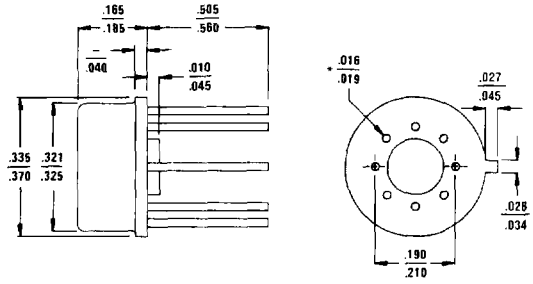
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-4

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic, 90% Al_2O_3
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

8 PIN TO-99 METAL CAN



*Dimension Maximum Limits Are Increased by 0.003 inches for Solder Dip Finish

LEAD MATERIAL: Type A
LEAD FINISH: Type C
PACKAGE MATERIAL: Kovar Header with Nickel Can
PACKAGE SEAL:
Material: No Seal Material
Temperature: Room Temperature
Method: Resistance Weld
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic Bonded
COMPLIANT OUTLINE: 38510 A-1

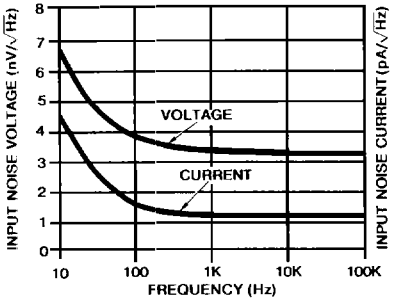
NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

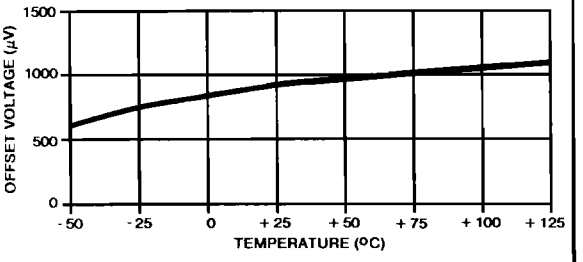
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Curves Unless Otherwise Specified: V± = ±15V, T_A = +25°C

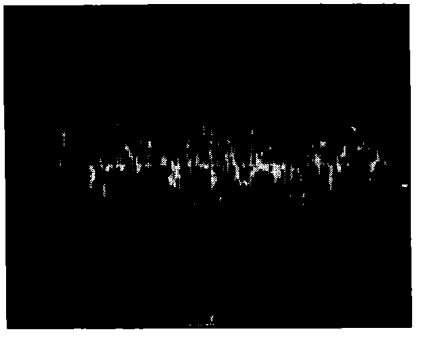
HA-5101 NOISE SPECTRUM



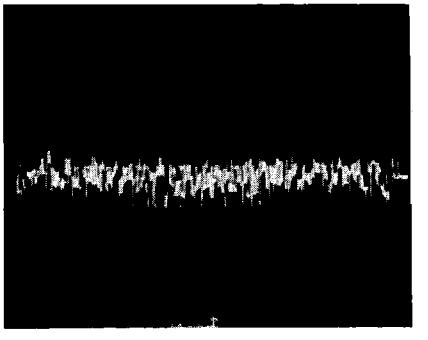
OFFSET VOLTAGE vs. TEMPERATURE



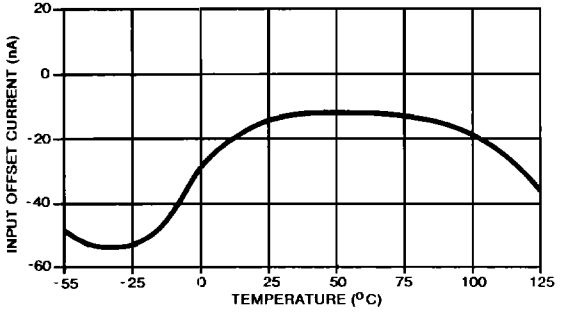
PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
A_V = 25,000, V_{CC} = ±15V
(0.09μV_{p-p} RTI)



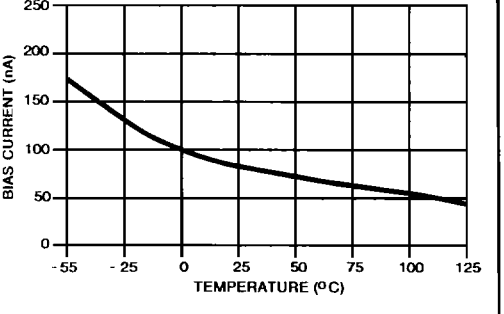
PEAK-TO-PEAK TOTAL NOISE 0.1Hz TO 1MHz
A_V = 25,000, V_{CC} = ±15V
(12.89mV_{p-p} RTO or 0.52μV_{p-p} RTI)



INPUT OFFSET CURRENT vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE



DESIGN INFORMATION (Continued)

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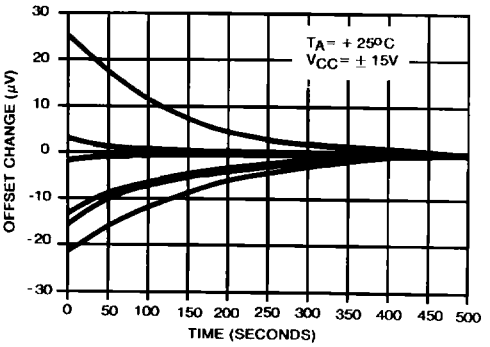
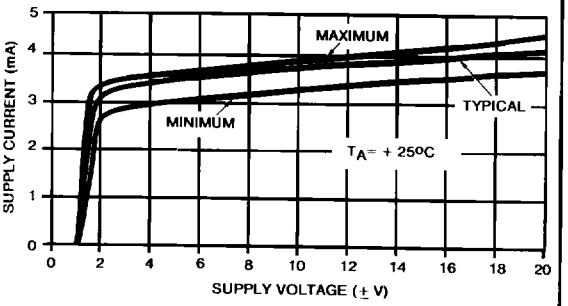
Typical Performance Curves Unless Otherwise Specified: V± = ±15V, T_A = +25°C

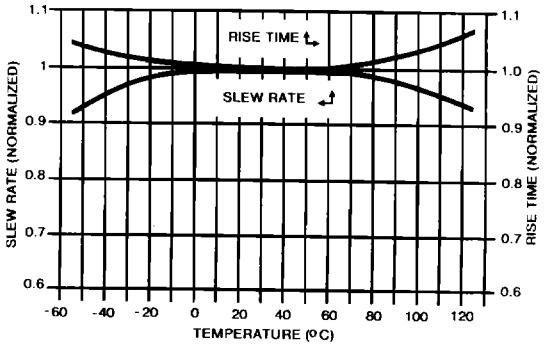
INPUT OFFSET WARMUP DRIFT vs. TIME
(Normalized to Zero Final Value)
(Six Representative Units)



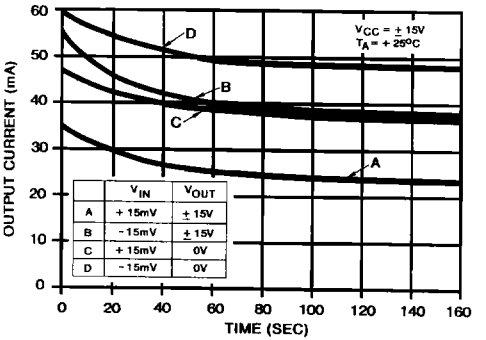
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SLEW RATE/RISE TIME vs. TEMPERATURE
R_L = 2K, C_L = 50pF, V_{CC} = ±15V

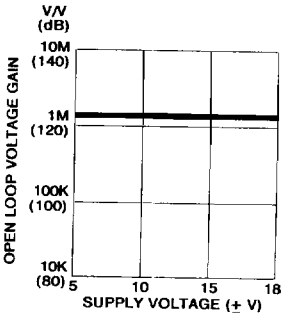


SHORT CIRCUIT CURRENT vs. TIME

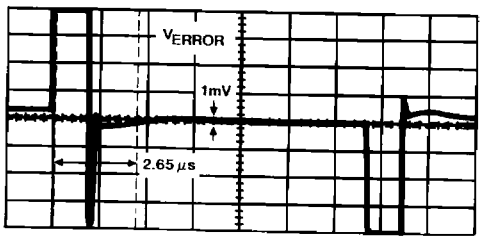


	V_{IN}	V_{OUT}
A	+ 15mV	± 15V
B	- 15mV	± 15V
C	+ 15mV	0V
D	- 15mV	0V

D.C. OPEN LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE



HA-5101 SETTLING WAVEFORM
1.5ms/DIV.



DESIGN INFORMATION (Continued)

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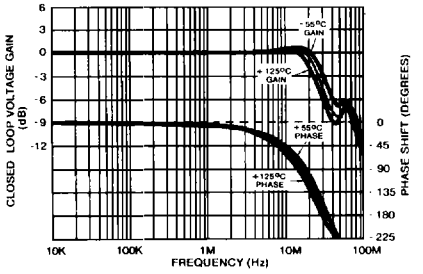
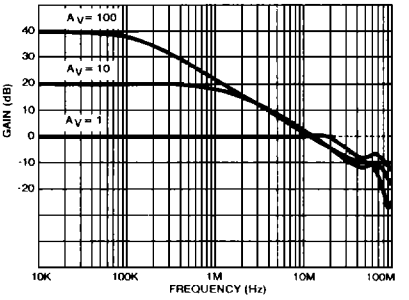
Typical Performance Curves Unless Otherwise Specified: V± = ±15V, T_A = +25°C

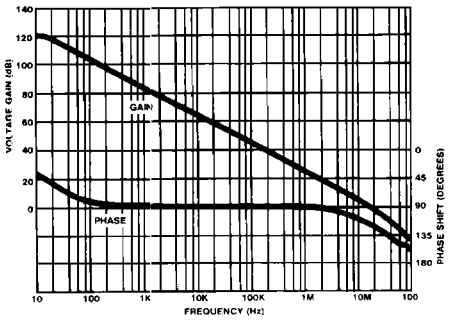
HA-5101 CLOSED LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE
(Typical Response of One Amplifier)
V_{CC} = ±15V, A_V = 1V/V, R_L = 2K, C_L = 50pF



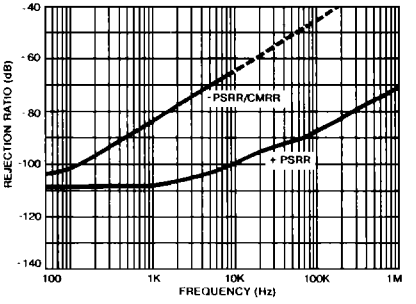
HA-5101 CLOSED LOOP VOLTAGE GAIN vs. FREQUENCY AT DIFFERENT CLOSED LOOP GAINS
T_A = +25°C, V_{CC} = ±15V, R_L = 2K, C_L = 50pF



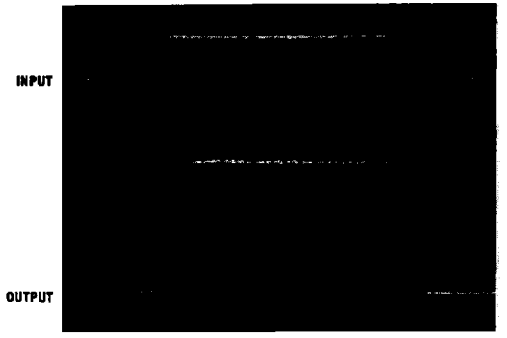
OPEN LOOP GAIN/PHASE vs. FREQUENCY



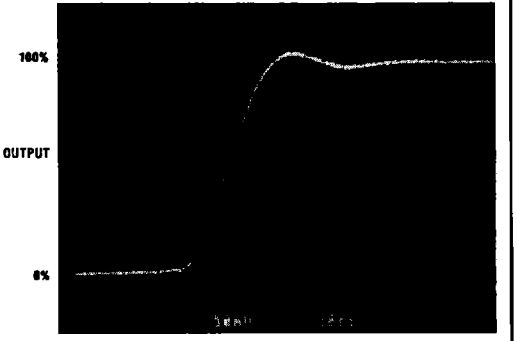
HA-5101 REJECTION RATIOS vs. FREQUENCY
T_A = +25°C, V_{CC} = ±15V



SLEW RATE WAVEFORM
V_{IN} = V_{OUT} = ±3V, A_V = +1, R_L = 2kΩ, C_L = 50pF
Timescale = 500ns/Div., Scale: Input = 5V/Div., Output = 2V/Div.



SMALL SIGNAL WAVEFORM
Rise Time and Overshoot
V_{IN} = V_{OUT} = 0V to +200mV, A_V = +1, R_L = 2K, C_L = 50pF
Timescale = 20ns/Div.



DESIGN INFORMATION (Continued)

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Applications Information

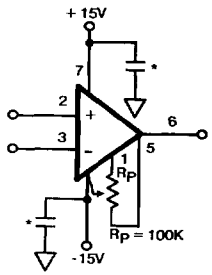
OPERATION AT ±5V SUPPLY

The HA-5101 performs well at V_{CC} = ±5V exhibiting typical characteristics as listed below:

I_{CC}	3.7	mA
V_{IO}	0.5	mV
I_{BIAS}	56	nA
A_{VOL} (V_O = ±3V)	106	KV/V
V_{OUT}	3.7	V
I_{OUT}	13	mA
CMRR (ΔV_{CM} = ±2.5V)	90	dB
PSRR (ΔV_{CC} = 0.5V)	90	dB
Unity Bandwidth (5101)	10	MHz
Slew Rate (5101)	7	V/µs

OFFSET ADJUSTMENT

The following is the recommended V_{IO} adjust configuration:

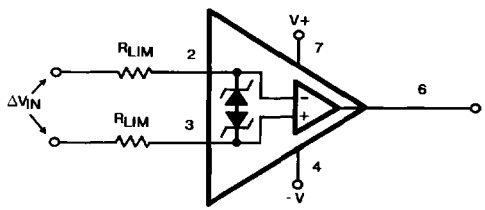


* Proper decoupling is always recommended, 0.1µF high quality capacitors should be at or vary near the device's supply pins.

INPUT PROTECTION

The HA-5101 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the HA-5101 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5101 input.

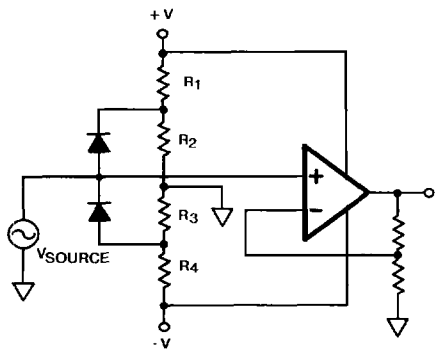
COMPARATOR CIRCUIT



Choose R_{LIM} Such That $\frac{(\Delta V_{IN}MAX - 7V)}{25mA} \leq 2R_{LIM}$

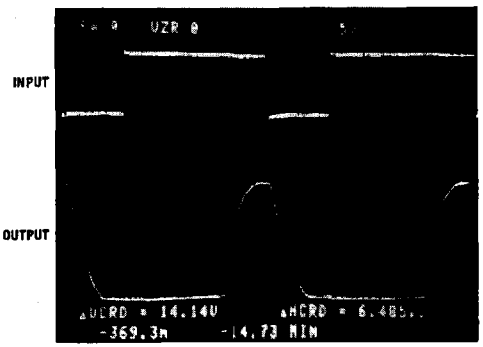
OUTPUT SATURATION

When an operational amplifier is overdriven, output devices can saturate and and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



If saturation cannot be avoided the HA-5101 recovers from a 25% overdrive in about 6.5µs (see photo).

Top: Input
Bottom: Output, 5V/Div., 2µs/Div.



Output is overdriven negative, recovers after 6µs.

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, R_L = 2kΩ, C_L = 50pF, A_{VCL} = +1V/V Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMITS	UNITS
Offset Voltage	V_{CM} = 0V	+25°C	0.8	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	-55°C to +125°C	3	7	µV/°C
Offset Current Average Drift	Versus Temperature	-55°C to +125°C	100	250	pA/°C
Input Bias Current	V_{CM} = 0V	+25°C	65	Table 1	nA
Input Offset Current	V_{CM} = 0V	+25°C	35	Table 1	nA
Differential Input Resistance	V_{CM} = 0V	+25°C	500	Table 3	kΩ
Input Noise Voltage Density	f_O = 10Hz	+25°C	5.4	9	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	3.4	5.5	$nV/\sqrt{Hz}$
	f_O = 1kHz	+25°C	3.2	Table 3	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O = 10Hz	+25°C	6	20	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	1.5	5	$pA/\sqrt{Hz}$
	f_O = 1kHz	+25°C	0.52	Table 3	$pA/\sqrt{Hz}$
Large Signal Voltage Gain	V_{OUT} = ±10V	-55°C	400K	Table 1	V/V
		+25°C	1M	Table 1	V/V
		+125°C	1M	Table 1	V/V
Slew Rate	V_{OUT} = ±3V	-55°C to +125°C	10	5.4	V/µs
Full Power Bandwidth	Note 2, V_{peak} = 10V	-55°C to +125°C	159	85	kHz
Rise and Fall Times	V_{OUT} = ±200mV	-55°C to +125°C	50	Table 2	ns
Overshoot	V_{OUT} = ±200mV	-55°C to +125°C	20	35	%
Settling Time	To 0.1% for 10V Step	+25°C	4.5	6	µs
	To 0.01% for 10V Step	+25°C	6	10	µs
Output Short Circuit Current	t <10 Seconds, V_{OUT} = ±15V	+25°C	±35	±50	mA
Output Resistance	Open Loop	+25°C	110	Table 3	Ω
Supply Current	No Load	+25°C	4.3	Table 1	mA
Minimum Supply Voltage	Functional Operation Only, Other Parameters Will Vary	+25°C	±4	±5	V