

## 8-bit AVR Microcontroller with 8K Bytes In-System Programmable Flash

### DATASHEET SUMMARY

#### Features

- High Performance, Low Power Atmel® AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 123 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
- Non-volatile Program and Data Memories
  - 8K Bytes of In-System Programmable Flash Program Memory
    - Endurance: 10,000 Write/Erase Cycles
  - 256 Bytes of In-System Programmable EEPROM
    - Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Optional Boot Code Section with Independent Lock Bits
  - Data Retention: 20 Years at 85°C / 100 Years at 25°C
- Peripheral Features
  - One 8-bit and one 16-bit Timer/Counter with Two PWM Channels, Each
  - Programmable Ultra Low Power Watchdog Timer
  - On-chip Analog Comparator
  - 10-bit Analog to Digital Converter
    - 28 External and 4 Internal, Single-ended Input Channels
  - Full Duplex USART with Start Frame Detection
  - Master/Slave SPI Serial Interface
  - Slave I<sup>2</sup>C Serial Interface
- Special Microcontroller Features
  - Low Power Idle, ADC Noise Reduction, and Power-down Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-out Detection Circuit with Supply Voltage Sampling
  - External and Internal Interrupt Sources
    - Pin Change Interrupt on 28 Pins
  - Calibrated 8MHz Oscillator with Temperature Calibration Option
  - Calibrated 32kHz Ultra Low Power Oscillator
  - High-Current Drive Capability on 8 I/O Pins
- I/O and Packages
  - 32-lead TQFP, and 32-pad QFN/MLF: 28 Programmable I/O Lines
- Speed Grade
  - 0 – 2 MHz @ 1.7 – 1.8V
  - 0 – 4 MHz @ 1.8 – 5.5V
  - 0 – 10 MHz @ 2.7 – 5.5V
  - 0 – 20 MHz @ 4.5 – 5.5V

- Low Power Consumption
  - Active Mode: 0.2 mA at 1.8V and 1MHz
  - Idle Mode: 30  $\mu$ A at 1.8V and 1MHz
  - Power-Down Mode (WDT Enabled): 1  $\mu$ A at 1.8V
  - Power-Down Mode (WDT Disabled): 100 nA at 1.8V

## 1. Pin Configurations

Figure 1. ATtiny828 Pinout in MLF32.

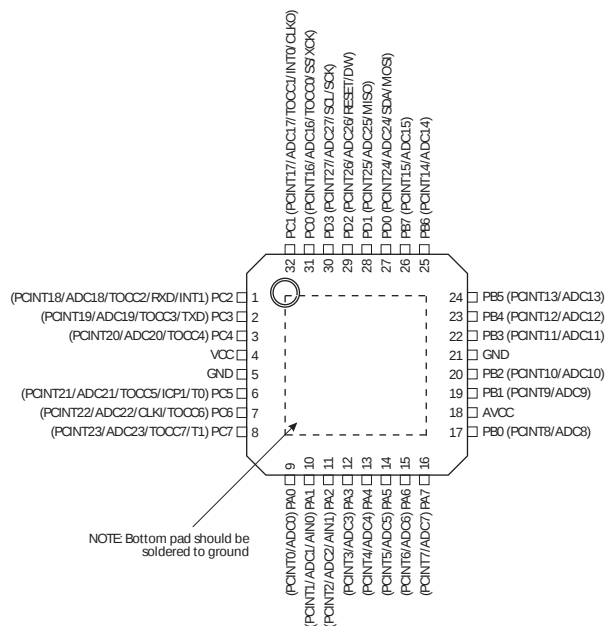
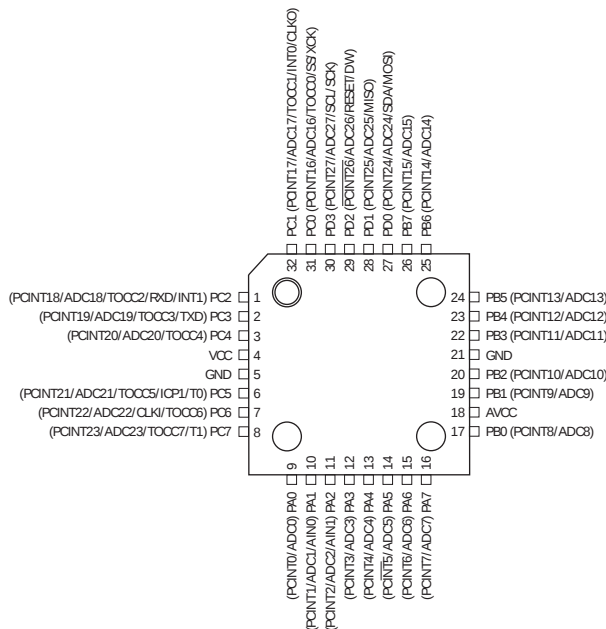


Figure 2. ATtiny828 Pinout in TQFP32.



## 1.1 Pin Description

### 1.1.1 VCC

Supply voltage.

### 1.1.2 AVCC

AV<sub>CC</sub> is the supply voltage pin for the A/D converter and a selection of I/O pins. This pin should be externally connected to V<sub>CC</sub> even if the ADC is not used. If the ADC is used, it is recommended this pin is connected to V<sub>CC</sub> through a low-pass filter, as described in [“Noise Canceling Techniques” on page 145](#).

All pins of Port A and Port B are powered by AV<sub>CC</sub>. All other I/O pins take their supply voltage from V<sub>CC</sub>.

### 1.1.3 GND

Ground.

### 1.1.4 RESET

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in [Table 107 on page 250](#). Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

### 1.1.5 Port A (PA7:PA0)

This is an 8-bit, bi-directional I/O port with internal pull-up resistors (selected for each bit). Output buffers have high sink and standard source capability. See [Table 107 on page 250](#) for port drive strength.

As inputs, port pins that are externally pulled low will source current provided that pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port has alternative pin functions for pin change interrupts, the analog comparator, and ADC. See [“Alternative Port Functions” on page 63](#).

### 1.1.6 Port B (PB7:PB0)

This is an 8-bit, bi-directional I/O port with internal pull-up resistors (selected for each bit). Output buffers have high sink and standard source capability. See [Table 103 on page 247](#) for port drive strength.

As inputs, port pins that are externally pulled low will source current provided that pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port has alternative pin functions for pin change interrupts, and ADC. See [“Alternative Port Functions” on page 63](#).

### 1.1.7 Port C (PC7:PC0)

This is an 8-bit, bi-directional I/O port with internal pull-up resistors (selected for each bit). Output buffers have high sink and standard source capability. Optionally, extra high sink capability can be enabled. See [Table 103 on page 247](#) for port drive strength.

As inputs, port pins that are externally pulled low will source current provided that pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port has alternative pin functions for pin change interrupts, ADC, timer/counter, external interrupts, and serial interfaces. See [“Alternative Port Functions” on page 63](#).

### 1.1.8 Port D (PD3:PD0)

This is a 4-bit, bi-directional I/O port with internal pull-up resistors (selected for each bit). Output buffers of PD0 and PD3 have symmetrical drive characteristics, with both sink and source capability. Output buffer PD1 has high sink and

standard source capability, while PD2 only has weak drive characteristics due to its use as a reset pin. See [Table 103 on page 247](#) for port drive strength.

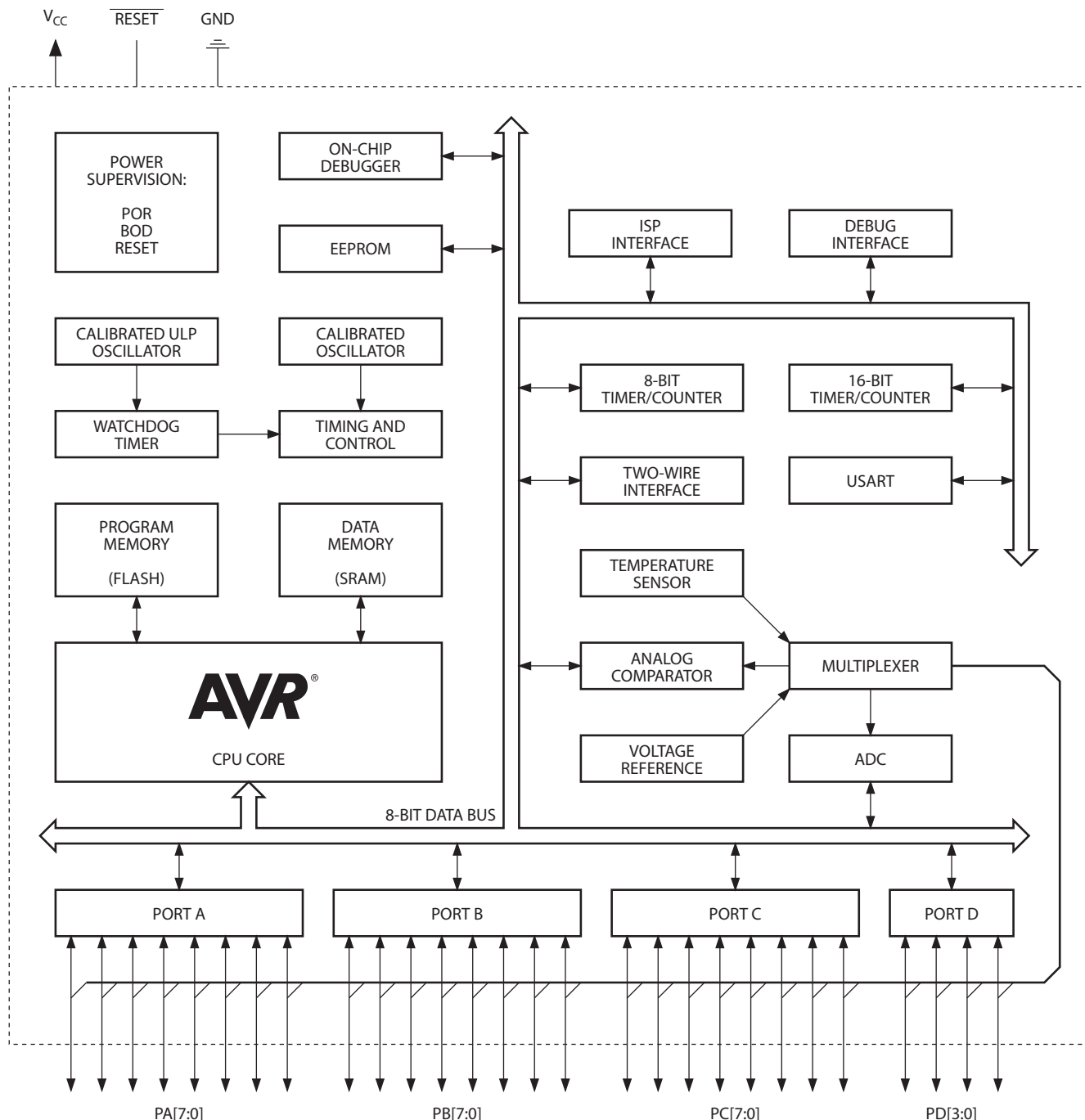
As inputs, port pins that are externally pulled low will source current provided that pull-up resistors are activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

This port has alternative pin functions for pin change interrupts, ADC, serial interfaces, and debugWire. See [“Alternative Port Functions” on page 63](#).

## 2. Overview

ATtiny828 is a low-power CMOS 8-bit microcontrollers based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny828 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

**Figure 3. Block Diagram**



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is compact and code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

ATtiny828 provides the following features:

- 8K bytes of in-system programmable Flash
- 512 bytes of SRAM data memory
- 256 bytes of EEPROM data memory
- 28 general purpose I/O lines
- 32 general purpose working registers
- An 8-bit timer/counter with two PWM channels
- A 16-bit timer/counter with two PWM channels
- Internal and external interrupts
- A 10-bit ADC with 4 internal and 28 external channels
- An ultra-low power, programmable watchdog timer with internal oscillator
- A programmable USART with start frame detection
- A slave, I<sup>2</sup>C compliant Two-Wire Interface (TWI)
- A master/slave Serial Peripheral Interface (SPI)
- A calibrated 8MHz oscillator
- A calibrated 32kHz, ultra low power oscillator
- Three software selectable power saving modes.

The device includes the following modes for saving power:

- Idle mode: stops the CPU while allowing the timer/counter, ADC, analog comparator, SPI, TWI, and interrupt system to continue functioning
- ADC Noise Reduction mode: minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC
- Power-down mode: registers keep their contents and all chip functions are disabled until the next interrupt or hardware reset

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash program memory can be re-programmed in-system through a serial interface, by a conventional non-volatile memory programmer or by an on-chip boot code, running on the AVR core. The boot program can use any interface to download the application program to the Flash memory. Software in the boot section of the Flash executes while the application section of the Flash is updated, providing true read-while-write operation.

The ATtiny828 AVR is supported by a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators and evaluation kits.

## **3. General Information**

### **3.1 Resources**

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at <http://www.atmel.com/avr>.

### **3.2 Code Examples**

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

### **3.3 Data Retention**

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

## 4. Register Summary

| Address | Name      | Bit 7                                          | Bit 6   | Bit 5   | Bit 4   | Bit 3                    | Bit 2     | Bit 1     | Bit 0   | Page(s)        |
|---------|-----------|------------------------------------------------|---------|---------|---------|--------------------------|-----------|-----------|---------|----------------|
| (0xFF)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xFE)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xFD)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xFC)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xFB)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xFA)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF9)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF8)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF7)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF6)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF5)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF4)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF3)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF2)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xF1)  | OSCTCAL0B | Oscillator Temperature Compensation Register B |         |         |         |                          |           |           |         | Page 33        |
| (0xF0)  | OSCTCAL0A | Oscillator Temperature Compensation Register A |         |         |         |                          |           |           |         | Page 33        |
| (0xEF)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xEE)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xED)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xEC)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xEB)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xEA)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xE9)  | TOCPMSA1  | TOCC7S1                                        | TOCC7S0 | TOCC6S1 | TOCC6S0 | TOCC5S1                  | TOCC5S0   | TOCC4S1   | TOCC4S0 | Page 127       |
| (0xE8)  | TOCPMSA0  | TOCC3S1                                        | TOCC3S0 | TOCC2S1 | TOCC2S0 | TOCC1S1                  | TOCC1S0   | TOCC0S1   | TOCC0S0 | Page 127       |
| (0xE7)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xE6)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xE5)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xE4)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xE3)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xE2)  | TOCPMCOE  | TOCC7OE                                        | TOCC6OE | TOCC5OE | TOCC4OE | TOCC3OE                  | TOCC2OE   | TOCC1OE   | TOCC0OE | Page 128       |
| (0xE1)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xE0)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xDF)  | DIDR3     | –                                              | –       | –       | –       | ADC27D                   | ADC26D    | ADC25D    | ADC24D  | Page 154       |
| (0xDE)  | DIDR2     | ADC23D                                         | ADC22D  | ADC21D  | ADC20D  | ADC19D                   | ADC18D    | ADC17D    | ADC16D  | Page 154       |
| (0xDD)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xDC)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xDB)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xDA)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD9)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD8)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD7)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD6)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD5)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD4)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD3)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD2)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD1)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xD0)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xCF)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xCE)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xCD)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xCC)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xCB)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xCA)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xC9)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xC8)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xC7)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xC6)  | UDR       | USART Data Register                            |         |         |         |                          |           |           |         | Pages 184, 195 |
| (0xC5)  | UBRRH     | –                                              | –       | –       | –       | USART Baud Register High |           |           |         | Page 189, 198  |
| (0xC4)  | UBRRL     | USART Baud Rate Register Low                   |         |         |         |                          |           |           |         | Page 189, 198  |
| (0xC3)  | UCSRD     | RXSIE                                          | RXS     | SFDE    | –       | –                        | –         | –         | –       | Page 188       |
| (0xC2)  | UCSRC     | UMSEL1                                         | UMSEL0  | UPM1    | UPM0    | USBS                     | UCSZ1/UDO | UCSZ0/UCP | UCPOL   | Page 186, 197  |
| (0xC1)  | UCSRB     | RXCIE                                          | TXCIE   | UDRIE   | RXEN    | TXEN                     | UCSZ2     | RXB8      | TXB8    | Page 185, 196  |
| (0xC0)  | UCSRA     | RXC                                            | TXC     | UDRE    | FE      | DOR                      | UPE       | U2X       | MPCM    | Page 184, 196  |
| (0xBF)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |
| (0xBE)  | Reserved  | –                                              | –       | –       | –       | –                        | –         | –         | –       |                |

| Address | Name     | Bit 7                                                | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Page(s)                                         |
|---------|----------|------------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|-------------------------------------------------|
| (0xBD)  | TWSD     | TWI Slave Data Register                              |        |        |        |        |        |        |        | Page <a href="#">211</a>                        |
| (0xBC)  | TWSA     | TWI Slave Address Register                           |        |        |        |        |        |        |        | Page <a href="#">210</a>                        |
| (0xBB)  | TWSAM    | TWI Slave Address Mask Register                      |        |        |        |        |        |        |        | Page <a href="#">211</a>                        |
| (0xBA)  | TWSSRA   | TWDIF                                                | TWASIF | TWCH   | TWRA   | TWC    | TWBE   | TWDIR  | TWAS   | Page <a href="#">209</a>                        |
| (0xB9)  | TWSCRB   | –                                                    | –      | –      | –      | –      | TWAA   | TWCMD1 | TWCMD0 | Page <a href="#">208</a>                        |
| (0xB8)  | TWSCRA   | TWSHE                                                | –      | TWDIE  | TWASIE | TWEN   | TWSIE  | TWPME  | TWSME  | Page <a href="#">207</a>                        |
| (0xB7)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xB6)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xB5)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xB4)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xB3)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xB2)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xB1)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xB0)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xAF)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xAE)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xAD)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xAC)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xAB)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xAA)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA9)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA8)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA7)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA6)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA5)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA4)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA3)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA2)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA1)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0xA0)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x9F)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x9E)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x9D)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x9C)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x9B)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x9A)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x99)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x98)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x97)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x96)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x95)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x94)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x93)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x92)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x91)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x90)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x8F)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x8E)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x8D)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x8C)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x8B)  | OCR1BH   | Timer/Counter1 – Output Compare Register B High Byte |        |        |        |        |        |        |        | Page <a href="#">128</a>                        |
| (0x8A)  | OCR1BL   | Timer/Counter1 – Output Compare Register B Low Byte  |        |        |        |        |        |        |        | Page <a href="#">128</a>                        |
| (0x89)  | OCR1AH   | Timer/Counter1 – Output Compare Register A High Byte |        |        |        |        |        |        |        | Page <a href="#">128</a>                        |
| (0x88)  | OCR1AL   | Timer/Counter1 – Output Compare Register A Low Byte  |        |        |        |        |        |        |        | Page <a href="#">128</a>                        |
| (0x87)  | ICR1H    | Timer/Counter1 – Input Capture Register High Byte    |        |        |        |        |        |        |        | Page <a href="#">129</a>                        |
| (0x86)  | ICR1L    | Timer/Counter1 – Input Capture Register Low Byte     |        |        |        |        |        |        |        | Page <a href="#">129</a>                        |
| (0x85)  | TCNT1H   | Timer/Counter1 – Counter Register High Byte          |        |        |        |        |        |        |        | Page <a href="#">128</a>                        |
| (0x84)  | TCNT1L   | Timer/Counter1 – Counter Register Low Byte           |        |        |        |        |        |        |        | Page <a href="#">128</a>                        |
| (0x83)  | Reserved | –                                                    | –      | –      | –      | –      | –      | –      | –      |                                                 |
| (0x82)  | TCCR1C   | FOC1A                                                | FOC1B  | –      | –      | –      | –      | –      | –      | Page <a href="#">127</a>                        |
| (0x81)  | TCCR1B   | ICNC1                                                | ICES1  | –      | WGM13  | WGM12  | CS12   | CS11   | CS10   | Page <a href="#">125</a>                        |
| (0x80)  | TCCR1A   | COM1A1                                               | COM1A0 | COM1B1 | COM1B0 | –      | –      | WGM11  | WGM10  | Page <a href="#">123</a>                        |
| (0x7F)  | DIDR1    | ADC15D                                               | ADC14D | ADC13D | ADC12D | ADC11D | ADC10D | ADC9D  | ADC8D  | Page <a href="#">154</a>                        |
| (0x7E)  | DIDR0    | ADC7D                                                | ADC6D  | ADC5D  | ADC4D  | ADC3D  | ADC2D  | ADC1D  | ADC0D  | Pages <a href="#">136</a> , <a href="#">154</a> |
| (0x7D)  | ADMUXB   | –                                                    | –      | REFS   | –      | –      | –      | –      | MUX5   | Page <a href="#">150</a>                        |
| (0x7C)  | ADMUXA   | –                                                    | –      | –      | MUX4   | MUX3   | MUX2   | MUX1   | MUX0   | Page <a href="#">149</a>                        |
| (0x7B)  | ADCSRB   | –                                                    | –      | –      | –      | ADLAR  | ADTS2  | ADTS1  | ADTS0  | Page <a href="#">153</a>                        |
| (0x7A)  | ADCSRA   | ADEN                                                 | ADSC   | ADATE  | ADIF   | ADIE   | ADPS2  | ADPS1  | ADPS0  | Page <a href="#">151</a>                        |

| Address     | Name     | Bit 7                                      | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1    | Bit 0   | Page(s)                  |
|-------------|----------|--------------------------------------------|---------|---------|---------|---------|---------|----------|---------|--------------------------|
| (0x79)      | ADCH     | ADC – Conversion Result High Byte          |         |         |         |         |         |          |         | Page <a href="#">151</a> |
| (0x78)      | ADCL     | ADC – Conversion Result Low Byte           |         |         |         |         |         |          |         | Page <a href="#">151</a> |
| (0x77)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x76)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x75)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x74)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x73)      | PCMSK3   | –                                          | –       | –       | –       | PCINT27 | PCINT26 | PCINT25  | PCINT24 | Page <a href="#">54</a>  |
| (0x72)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x71)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x70)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x6F)      | TIMSK1   | –                                          | –       | ICIE1   | –       | –       | OCIE1B  | OCIE1A   | TOIE1   | Page <a href="#">129</a> |
| (0x6E)      | TIMSK0   | –                                          | –       | –       | –       | –       | OCIE0B  | OCIE0A   | TOIE0   | Page <a href="#">102</a> |
| (0x6D)      | PCMSK2   | PCINT23                                    | PCINT22 | PCINT21 | PCINT20 | PCINT19 | PCINT18 | PCINT17  | PCINT16 | Page <a href="#">54</a>  |
| (0x6C)      | PCMSK1   | PCINT15                                    | PCINT14 | PCINT13 | PCINT12 | PCINT11 | PCINT10 | PCINT9   | PCINT8  | Page <a href="#">54</a>  |
| (0x6B)      | PCMSK0   | PCINT7                                     | PCINT6  | PCINT5  | PCINT4  | PCINT3  | PCINT2  | PCINT1   | PCINT0  | Page <a href="#">55</a>  |
| (0x6A)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x69)      | EICRA    | –                                          | –       | –       | –       | ISC11   | ISC10   | ISC01    | ISC00   | Page <a href="#">55</a>  |
| (0x68)      | PCICR    | –                                          | –       | –       | –       | PCIE3   | PCIE2   | PCIE1    | PCIE0   | Page <a href="#">56</a>  |
| (0x67)      | OSCCAL1  | –                                          | –       | –       | –       | –       | –       | CAL11    | CAL10   | Page <a href="#">33</a>  |
| (0x66)      | OSCCAL0  | CAL07                                      | CAL06   | CAL05   | CAL04   | CAL03   | CAL02   | CAL01    | CAL00   | Page <a href="#">32</a>  |
| (0x65)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x64)      | PRR      | PRTWI                                      | –       | PRTIM0  | –       | PRTIM1  | PRSPI   | PRUSART0 | PRADC   | Page <a href="#">37</a>  |
| (0x63)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x62)      | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| (0x61)      | CLKPR    | –                                          | –       | –       | –       | CLKPS3  | CLKPS2  | CLKPS1   | CLKPS0  | Page <a href="#">31</a>  |
| (0x60)      | WDTCR    | WDIF                                       | WDIE    | WDP3    | –       | WDE     | WDP2    | WDP1     | WDP0    | Page <a href="#">46</a>  |
| 0x3F (0x5F) | SREG     | I                                          | T       | H       | S       | V       | N       | Z        | C       | Page <a href="#">15</a>  |
| 0x3E (0x5E) | SPH      | –                                          | –       | –       | –       | –       | –       | SP9      | SP8     | Page <a href="#">14</a>  |
| 0x3D (0x5D) | SPL      | SP7                                        | SP6     | SP5     | SP4     | SP3     | SP2     | SP1      | SP0     | Page <a href="#">14</a>  |
| 0x3C (0x5C) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x3B (0x5B) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x3A (0x5A) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x39 (0x59) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x38 (0x58) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x37 (0x57) | SPMCSR   | SPMIE                                      | RWWBSB  | RSIG    | RWWWSRE | RWFLB   | PGWRT   | PGERS    | SPMEN   | Page <a href="#">223</a> |
| 0x36 (0x56) | CCP      | CPU Change Protection Register             |         |         |         |         |         |          |         | Page <a href="#">14</a>  |
| 0x35 (0x55) | MCUCR    | –                                          | –       | –       | –       | –       | –       | IVSEL    | –       | Page <a href="#">53</a>  |
| 0x34 (0x54) | MCUSR    | –                                          | –       | –       | –       | WDRF    | BORF    | EXTRF    | PORF    | Page <a href="#">45</a>  |
| 0x33 (0x53) | SMCR     | –                                          | –       | –       | –       | –       | SM1     | SM0      | SE      | Page <a href="#">37</a>  |
| 0x32 (0x52) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x31 (0x51) | DWDR     | debugWire Data Register                    |         |         |         |         |         |          |         | Page <a href="#">213</a> |
| 0x30 (0x50) | ACSR     | ACD                                        | ACPMUX2 | ACO     | ACI     | ACIE    | ACIC    | ACIS1    | ACIS0   | Page <a href="#">134</a> |
| 0x2F (0x4F) | ACSRB    | HSEL                                       | HLEV    | ACLP    | –       | ACNMUX1 | ACNMUX0 | ACPMUX1  | ACPMUX0 | Page <a href="#">135</a> |
| 0x2E (0x4E) | SPDR     | SPI Data Register                          |         |         |         |         |         |          |         | Page <a href="#">163</a> |
| 0x2D (0x4D) | SPSR     | SPIF                                       | WCOL    | –       | –       | –       | –       | –        | SPI2X   | Page <a href="#">162</a> |
| 0x2C (0x4C) | SPCR     | SPIE                                       | SPE     | DORD    | MSTR    | CPOL    | CPHA    | SPR1     | SPR0    | Page <a href="#">161</a> |
| 0x2B (0x4B) | GPOR2    | General Purpose I/O Register 2             |         |         |         |         |         |          |         | Page <a href="#">25</a>  |
| 0x2A (0x4A) | GPOR1    | General Purpose I/O Register 1             |         |         |         |         |         |          |         | Page <a href="#">25</a>  |
| 0x29 (0x49) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x28 (0x48) | OCR0B    | Timer/Counter0 – Output Compare Register B |         |         |         |         |         |          |         | Page <a href="#">102</a> |
| 0x27 (0x47) | OCR0A    | Timer/Counter0 – Output Compare Register A |         |         |         |         |         |          |         | Page <a href="#">102</a> |
| 0x26 (0x46) | TCNT0    | Timer/Counter0 – Counter Register          |         |         |         |         |         |          |         | Page <a href="#">101</a> |
| 0x25 (0x45) | TCCR0B   | FOC0A                                      | FOC0B   | –       | –       | WGM02   | CS02    | CS01     | CS00    | Page <a href="#">100</a> |
| 0x24 (0x44) | TCCR0A   | COM0A1                                     | COM0A0  | COM0B1  | COM0B0  | –       | –       | WGM01    | WGM00   | Page <a href="#">97</a>  |
| 0x23 (0x43) | GTCCR    | TSM                                        | –       | –       | –       | –       | –       | –        | PSR     | Page <a href="#">132</a> |
| 0x22 (0x42) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x21 (0x41) | EEARL    | EEPROM Address Register Low Byte           |         |         |         |         |         |          |         | Page <a href="#">23</a>  |
| 0x20 (0x40) | EEDR     | EEPROM Data Register                       |         |         |         |         |         |          |         | Page <a href="#">24</a>  |
| 0x1F (0x3F) | EECR     | –                                          | –       | EEP1    | EEP0    | EERIE   | EEMPE   | EEPE     | EERE    | Page <a href="#">24</a>  |
| 0x1E (0x3E) | GPOR0    | General Purpose I/O register 0             |         |         |         |         |         |          |         | Page <a href="#">26</a>  |
| 0x1D (0x3D) | EIMSK    | –                                          | –       | –       | –       | –       | –       | INT1     | INT0    | Page <a href="#">56</a>  |
| 0x1C (0x3C) | EIFR     | –                                          | –       | –       | –       | –       | –       | INT1     | INTF0   | Page <a href="#">57</a>  |
| 0x1B (0x3B) | PCIFR    | –                                          | –       | –       | –       | PCIF3   | PCIF2   | PCIF1    | PCIF0   | Page <a href="#">57</a>  |
| 0x1A (0x3A) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x19 (0x39) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x18 (0x38) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x17 (0x37) | Reserved | –                                          | –       | –       | –       | –       | –       | –        | –       |                          |
| 0x16 (0x36) | TIFR1    | –                                          | –       | ICF1    | –       | –       | OCF1B   | OCF1A    | TOV1    | Page <a href="#">130</a> |

| Address     | Name     | Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Page(s)                  |
|-------------|----------|--------|--------|--------|--------|--------|--------|--------|--------|--------------------------|
| 0x15 (0x35) | TIFR0    | –      | –      | –      | –      | –      | OCF0B  | OCF0A  | TOV0   | Page <a href="#">103</a> |
| 0x14 (0x34) | PHDE     | –      | –      | –      | –      | –      | PHDEC  | –      | –      | Page <a href="#">81</a>  |
| 0x13 (0x33) | Reserved | –      | –      | –      | –      | –      | –      | –      | –      |                          |
| 0x12 (0x32) | Reserved | –      | –      | –      | –      | –      | –      | –      | –      |                          |
| 0x11 (0x31) | Reserved | –      | –      | –      | –      | –      | –      | –      | –      |                          |
| 0x10 (0x30) | Reserved | –      | –      | –      | –      | –      | –      | –      | –      |                          |
| 0x0F (0x2F) | PUED     | –      | –      | –      | –      | PUED3  | PUED2  | PUED1  | PUED0  | Page <a href="#">82</a>  |
| 0x0E (0x2E) | PORTD    | –      | –      | –      | –      | PORTD3 | PORTD2 | PORTD1 | PORTD0 | Page <a href="#">82</a>  |
| 0x0D (0x2D) | DDRD     | –      | –      | –      | –      | DDD3   | DDD2   | DDD1   | DDD0   | Page <a href="#">82</a>  |
| 0x0C (0x2C) | PIND     | –      | –      | –      | –      | PIND3  | PIND2  | PIND1  | PIND0  | Page <a href="#">83</a>  |
| 0x0B (0x2B) | PUEC     | PUEC7  | PUEC6  | PUEC5  | PUEC4  | PUEC3  | PUEC2  | PUEC1  | PUEC0  | Page <a href="#">83</a>  |
| 0x0A (0x2A) | PORTC    | PORTC7 | PORTC6 | PORTC5 | PORTC4 | PORTC3 | PORTC2 | PORTC1 | PORTC0 | Page <a href="#">83</a>  |
| 0x09 (0x29) | DDRC     | DDC7   | DDC6   | DDC5   | DDC4   | DDC3   | DDC2   | DDC1   | DDC0   | Page <a href="#">83</a>  |
| 0x08 (0x28) | PINC     | PINC7  | PINC6  | PINC5  | PINC4  | PINC3  | PINC2  | PINC1  | PINC0  | Page <a href="#">84</a>  |
| 0x07 (0x27) | PUEB     | PUEB7  | PUEB6  | PUEB5  | PUEB4  | PUEB3  | PUEB2  | PUEB1  | PUEB0  | Page <a href="#">84</a>  |
| 0x06 (0x26) | PORTB    | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | Page <a href="#">84</a>  |
| 0x05 (0x25) | DDRB     | DDB7   | DDB6   | DDB5   | DDB4   | DDB3   | DDB2   | DDB1   | DDB0   | Page <a href="#">84</a>  |
| 0x04 (0x24) | PINB     | PINB7  | PINB6  | PINB5  | PINB4  | PINB3  | PINB2  | PINB1  | PINB0  | Page <a href="#">85</a>  |
| 0x03 (0x23) | PUEA     | PUEA7  | PUEA6  | PUEA5  | PUEA4  | PUEA3  | PUEA2  | PUEA1  | PUEA0  | Page <a href="#">85</a>  |
| 0x02 (0x22) | PORTA    | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTA3 | PORTA2 | PORTA1 | PORTA0 | Page <a href="#">85</a>  |
| 0x01 (0x21) | DDRA     | DDA7   | DDA6   | DDA5   | DDA4   | DDA3   | DDA2   | DDA1   | DDA0   | Page <a href="#">85</a>  |
| 0x00 (0x20) | PINA     | PINA7  | PINA6  | PINA5  | PINA4  | PINA3  | PINA2  | PINA1  | PINA0  | Page <a href="#">86</a>  |

- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
  2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
  3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

## 5. Instruction Set Summary

| Mnemonics                                | Operands | Description                            | Operation                                                          | Flags      | #Clocks |
|------------------------------------------|----------|----------------------------------------|--------------------------------------------------------------------|------------|---------|
| <b>ARITHMETIC AND LOGIC INSTRUCTIONS</b> |          |                                        |                                                                    |            |         |
| ADD                                      | Rd, Rr   | Add two Registers                      | $Rd \leftarrow Rd + Rr$                                            | Z,C,N,V,H  | 1       |
| ADC                                      | Rd, Rr   | Add with Carry two Registers           | $Rd \leftarrow Rd + Rr + C$                                        | Z,C,N,V,H  | 1       |
| ADIW                                     | Rdl,K    | Add Immediate to Word                  | $Rdh:Rdl \leftarrow Rdh:Rdl + K$                                   | Z,C,N,V,S  | 2       |
| SUB                                      | Rd, Rr   | Subtract two Registers                 | $Rd \leftarrow Rd - Rr$                                            | Z,C,N,V,H  | 1       |
| SUBI                                     | Rd, K    | Subtract Constant from Register        | $Rd \leftarrow Rd - K$                                             | Z,C,N,V,H  | 1       |
| SBC                                      | Rd, Rr   | Subtract with Carry two Registers      | $Rd \leftarrow Rd - Rr - C$                                        | Z,C,N,V,H  | 1       |
| SBCI                                     | Rd, K    | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$                                         | Z,C,N,V,H  | 1       |
| SBIW                                     | Rdl,K    | Subtract Immediate from Word           | $Rdh:Rdl \leftarrow Rdh:Rdl - K$                                   | Z,C,N,V,S  | 2       |
| AND                                      | Rd, Rr   | Logical AND Registers                  | $Rd \leftarrow Rd \bullet Rr$                                      | Z,N,V      | 1       |
| ANDI                                     | Rd, K    | Logical AND Register and Constant      | $Rd \leftarrow Rd \bullet K$                                       | Z,N,V      | 1       |
| OR                                       | Rd, Rr   | Logical OR Registers                   | $Rd \leftarrow Rd \vee Rr$                                         | Z,N,V      | 1       |
| ORI                                      | Rd, K    | Logical OR Register and Constant       | $Rd \leftarrow Rd \vee K$                                          | Z,N,V      | 1       |
| EOR                                      | Rd, Rr   | Exclusive OR Registers                 | $Rd \leftarrow Rd \oplus Rr$                                       | Z,N,V      | 1       |
| COM                                      | Rd       | One's Complement                       | $Rd \leftarrow 0xFF - Rd$                                          | Z,C,N,V    | 1       |
| NEG                                      | Rd       | Two's Complement                       | $Rd \leftarrow 0x00 - Rd$                                          | Z,C,N,V,H  | 1       |
| SBR                                      | Rd,K     | Set Bit(s) in Register                 | $Rd \leftarrow Rd \vee K$                                          | Z,N,V      | 1       |
| CBR                                      | Rd,K     | Clear Bit(s) in Register               | $Rd \leftarrow Rd \bullet (0xFF - K)$                              | Z,N,V      | 1       |
| INC                                      | Rd       | Increment                              | $Rd \leftarrow Rd + 1$                                             | Z,N,V      | 1       |
| DEC                                      | Rd       | Decrement                              | $Rd \leftarrow Rd - 1$                                             | Z,N,V      | 1       |
| TST                                      | Rd       | Test for Zero or Minus                 | $Rd \leftarrow Rd \bullet Rd$                                      | Z,N,V      | 1       |
| CLR                                      | Rd       | Clear Register                         | $Rd \leftarrow Rd \oplus Rd$                                       | Z,N,V      | 1       |
| SER                                      | Rd       | Set Register                           | $Rd \leftarrow 0xFF$                                               | None       | 1       |
| <b>BRANCH INSTRUCTIONS</b>               |          |                                        |                                                                    |            |         |
| RJMP                                     | k        | Relative Jump                          | $PC \leftarrow PC + k + 1$                                         | None       | 2       |
| IJMP                                     |          | Indirect Jump to (Z)                   | $PC \leftarrow Z$                                                  | None       | 2       |
| RCALL                                    | k        | Relative Subroutine Call               | $PC \leftarrow PC + k + 1$                                         | None       | 3       |
| ICALL                                    |          | Indirect Call to (Z)                   | $PC \leftarrow Z$                                                  | None       | 3       |
| RET                                      |          | Subroutine Return                      | $PC \leftarrow STACK$                                              | None       | 4       |
| RETI                                     |          | Interrupt Return                       | $PC \leftarrow STACK$                                              | I          | 4       |
| CPSE                                     | Rd,Rr    | Compare, Skip if Equal                 | if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3                         | None       | 1/2/3   |
| CP                                       | Rd,Rr    | Compare                                | $Rd - Rr$                                                          | Z, N,V,C,H | 1       |
| CPC                                      | Rd,Rr    | Compare with Carry                     | $Rd - Rr - C$                                                      | Z, N,V,C,H | 1       |
| CPI                                      | Rd,K     | Compare Register with Immediate        | $Rd - K$                                                           | Z, N,V,C,H | 1       |
| SBRC                                     | Rr, b    | Skip if Bit in Register Cleared        | if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3                         | None       | 1/2/3   |
| SBRS                                     | Rr, b    | Skip if Bit in Register is Set         | if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3                         | None       | 1/2/3   |
| SBIC                                     | P, b     | Skip if Bit in I/O Register Cleared    | if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3                          | None       | 1/2/3   |
| SBIS                                     | P, b     | Skip if Bit in I/O Register is Set     | if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3                          | None       | 1/2/3   |
| BRBS                                     | s, k     | Branch if Status Flag Set              | if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$                 | None       | 1/2     |
| BRBC                                     | s, k     | Branch if Status Flag Cleared          | if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$                 | None       | 1/2     |
| BREQ                                     | k        | Branch if Equal                        | if $(Z = 1)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRNE                                     | k        | Branch if Not Equal                    | if $(Z = 0)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRCS                                     | k        | Branch if Carry Set                    | if $(C = 1)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRCC                                     | k        | Branch if Carry Cleared                | if $(C = 0)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRSH                                     | k        | Branch if Same or Higher               | if $(C = 0)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRLO                                     | k        | Branch if Lower                        | if $(C = 1)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRMI                                     | k        | Branch if Minus                        | if $(N = 1)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRPL                                     | k        | Branch if Plus                         | if $(N = 0)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRGE                                     | k        | Branch if Greater or Equal, Signed     | if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$              | None       | 1/2     |
| BRLT                                     | k        | Branch if Less Than Zero, Signed       | if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$              | None       | 1/2     |
| BRHS                                     | k        | Branch if Half Carry Flag Set          | if $(H = 1)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRHC                                     | k        | Branch if Half Carry Flag Cleared      | if $(H = 0)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRTS                                     | k        | Branch if T Flag Set                   | if $(T = 1)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRTC                                     | k        | Branch if T Flag Cleared               | if $(T = 0)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRVS                                     | k        | Branch if Overflow Flag is Set         | if $(V = 1)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRVC                                     | k        | Branch if Overflow Flag is Cleared     | if $(V = 0)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRIE                                     | k        | Branch if Interrupt Enabled            | if $(I = 1)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| BRID                                     | k        | Branch if Interrupt Disabled           | if $(I = 0)$ then $PC \leftarrow PC + k + 1$                       | None       | 1/2     |
| <b>BIT AND BIT-TEST INSTRUCTIONS</b>     |          |                                        |                                                                    |            |         |
| SBI                                      | P,b      | Set Bit in I/O Register                | $I/O(P,b) \leftarrow 1$                                            | None       | 2       |
| CBI                                      | P,b      | Clear Bit in I/O Register              | $I/O(P,b) \leftarrow 0$                                            | None       | 2       |
| LSL                                      | Rd       | Logical Shift Left                     | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$                     | Z,C,N,V    | 1       |
| LSR                                      | Rd       | Logical Shift Right                    | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$                     | Z,C,N,V    | 1       |
| ROL                                      | Rd       | Rotate Left Through Carry              | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V    | 1       |
| ROR                                      | Rd       | Rotate Right Through Carry             | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V    | 1       |

| Mnemonics                         | Operands | Description                      | Operation                                                              | Flags   | #Clocks |
|-----------------------------------|----------|----------------------------------|------------------------------------------------------------------------|---------|---------|
| ASR                               | Rd       | Arithmetic Shift Right           | $Rd(n) \leftarrow Rd(n+1), n=0..6$                                     | Z,C,N,V | 1       |
| SWAP                              | Rd       | Swap Nibbles                     | $Rd(3..0) \leftrightarrow Rd(7..4), Rd(7..4) \leftrightarrow Rd(3..0)$ | None    | 1       |
| BSET                              | s        | Flag Set                         | $SREG(s) \leftarrow 1$                                                 | SREG(s) | 1       |
| BCLR                              | s        | Flag Clear                       | $SREG(s) \leftarrow 0$                                                 | SREG(s) | 1       |
| BST                               | Rr, b    | Bit Store from Register to T     | $T \leftarrow Rr(b)$                                                   | T       | 1       |
| BLD                               | Rd, b    | Bit load from T to Register      | $Rd(b) \leftarrow T$                                                   | None    | 1       |
| SEC                               |          | Set Carry                        | $C \leftarrow 1$                                                       | C       | 1       |
| CLC                               |          | Clear Carry                      | $C \leftarrow 0$                                                       | C       | 1       |
| SEN                               |          | Set Negative Flag                | $N \leftarrow 1$                                                       | N       | 1       |
| CLN                               |          | Clear Negative Flag              | $N \leftarrow 0$                                                       | N       | 1       |
| SEZ                               |          | Set Zero Flag                    | $Z \leftarrow 1$                                                       | Z       | 1       |
| CLZ                               |          | Clear Zero Flag                  | $Z \leftarrow 0$                                                       | Z       | 1       |
| SEI                               |          | Global Interrupt Enable          | $I \leftarrow 1$                                                       | I       | 1       |
| CLI                               |          | Global Interrupt Disable         | $I \leftarrow 0$                                                       | I       | 1       |
| SES                               |          | Set Signed Test Flag             | $S \leftarrow 1$                                                       | S       | 1       |
| CLS                               |          | Clear Signed Test Flag           | $S \leftarrow 0$                                                       | S       | 1       |
| SEV                               |          | Set Twos Complement Overflow.    | $V \leftarrow 1$                                                       | V       | 1       |
| CLV                               |          | Clear Twos Complement Overflow   | $V \leftarrow 0$                                                       | V       | 1       |
| SET                               |          | Set T in SREG                    | $T \leftarrow 1$                                                       | T       | 1       |
| CLT                               |          | Clear T in SREG                  | $T \leftarrow 0$                                                       | T       | 1       |
| SEH                               |          | Set Half Carry Flag in SREG      | $H \leftarrow 1$                                                       | H       | 1       |
| CLH                               |          | Clear Half Carry Flag in SREG    | $H \leftarrow 0$                                                       | H       | 1       |
| <b>DATA TRANSFER INSTRUCTIONS</b> |          |                                  |                                                                        |         |         |
| MOV                               | Rd, Rr   | Move Between Registers           | $Rd \leftarrow Rr$                                                     | None    | 1       |
| MOVW                              | Rd, Rr   | Copy Register Word               | $Rd+1:Rd \leftarrow Rr+1:Rr$                                           | None    | 1       |
| LDI                               | Rd, K    | Load Immediate                   | $Rd \leftarrow K$                                                      | None    | 1       |
| LD                                | Rd, X    | Load Indirect                    | $Rd \leftarrow (X)$                                                    | None    | 2       |
| LD                                | Rd, X+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (X), X \leftarrow X + 1$                                | None    | 2       |
| LD                                | Rd, -X   | Load Indirect and Pre-Dec.       | $X \leftarrow X - 1, Rd \leftarrow (X)$                                | None    | 2       |
| LD                                | Rd, Y    | Load Indirect                    | $Rd \leftarrow (Y)$                                                    | None    | 2       |
| LD                                | Rd, Y+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (Y), Y \leftarrow Y + 1$                                | None    | 2       |
| LD                                | Rd, -Y   | Load Indirect and Pre-Dec.       | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$                                | None    | 2       |
| LDD                               | Rd, Y+q  | Load Indirect with Displacement  | $Rd \leftarrow (Y + q)$                                                | None    | 2       |
| LD                                | Rd, Z    | Load Indirect                    | $Rd \leftarrow (Z)$                                                    | None    | 2       |
| LD                                | Rd, Z+   | Load Indirect and Post-Inc.      | $Rd \leftarrow (Z), Z \leftarrow Z + 1$                                | None    | 2       |
| LD                                | Rd, -Z   | Load Indirect and Pre-Dec.       | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$                                | None    | 2       |
| LDD                               | Rd, Z+q  | Load Indirect with Displacement  | $Rd \leftarrow (Z + q)$                                                | None    | 2       |
| LDS                               | Rd, k    | Load Direct from SRAM            | $Rd \leftarrow (k)$                                                    | None    | 2       |
| ST                                | X, Rr    | Store Indirect                   | $(X) \leftarrow Rr$                                                    | None    | 2       |
| ST                                | X+, Rr   | Store Indirect and Post-Inc.     | $(X) \leftarrow Rr, X \leftarrow X + 1$                                | None    | 2       |
| ST                                | -X, Rr   | Store Indirect and Pre-Dec.      | $X \leftarrow X - 1, (X) \leftarrow Rr$                                | None    | 2       |
| ST                                | Y, Rr    | Store Indirect                   | $(Y) \leftarrow Rr$                                                    | None    | 2       |
| ST                                | Y+, Rr   | Store Indirect and Post-Inc.     | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$                                | None    | 2       |
| ST                                | -Y, Rr   | Store Indirect and Pre-Dec.      | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$                                | None    | 2       |
| STD                               | Y+q, Rr  | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$                                                | None    | 2       |
| ST                                | Z, Rr    | Store Indirect                   | $(Z) \leftarrow Rr$                                                    | None    | 2       |
| ST                                | Z+, Rr   | Store Indirect and Post-Inc.     | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$                                | None    | 2       |
| ST                                | -Z, Rr   | Store Indirect and Pre-Dec.      | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$                                | None    | 2       |
| STD                               | Z+q, Rr  | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$                                                | None    | 2       |
| STS                               | k, Rr    | Store Direct to SRAM             | $(k) \leftarrow Rr$                                                    | None    | 2       |
| LPM                               |          | Load Program Memory              | $R0 \leftarrow (Z)$                                                    | None    | 3       |
| LPM                               | Rd, Z    | Load Program Memory              | $Rd \leftarrow (Z)$                                                    | None    | 3       |
| LPM                               | Rd, Z+   | Load Program Memory and Post-Inc | $Rd \leftarrow (Z), Z \leftarrow Z + 1$                                | None    | 3       |
| SPM                               |          | Store Program Memory             | $(Z) \leftarrow R1:R0$                                                 | None    | -       |
| IN                                | Rd, P    | In Port                          | $Rd \leftarrow P$                                                      | None    | 1       |
| OUT                               | P, Rr    | Out Port                         | $P \leftarrow Rr$                                                      | None    | 1       |
| PUSH                              | Rr       | Push Register on Stack           | $STACK \leftarrow Rr$                                                  | None    | 2       |
| POP                               | Rd       | Pop Register from Stack          | $Rd \leftarrow STACK$                                                  | None    | 2       |
| <b>MCU CONTROL INSTRUCTIONS</b>   |          |                                  |                                                                        |         |         |
| NOP                               |          | No Operation                     |                                                                        | None    | 1       |
| SLEEP                             |          | Sleep                            | (see specific descr. for Sleep function)                               | None    | 1       |
| WDR                               |          | Watchdog Reset                   | (see specific descr. for WDR/timer)                                    | None    | 1       |
| BREAK                             |          | Break                            | For On-chip Debug Only                                                 | None    | N/A     |

## 6. Ordering Information

### 6.1 ATtiny828

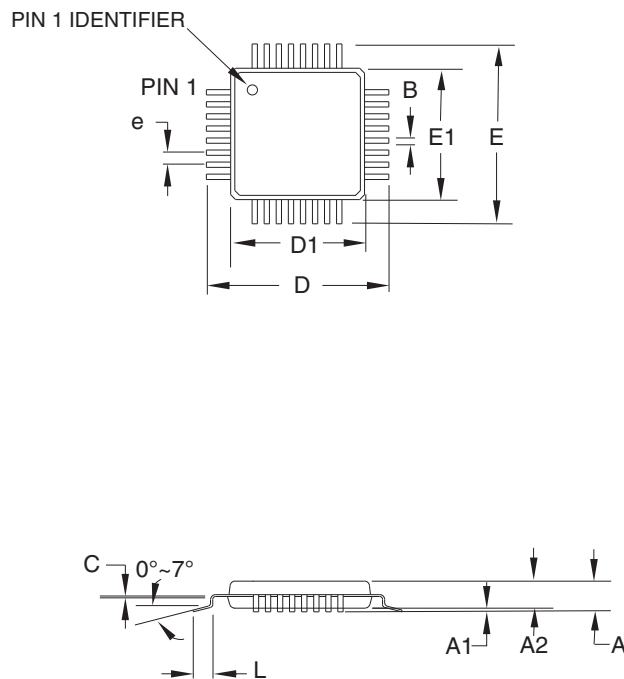
| Speed (MHz) <sup>(1)</sup> | Supply Voltage (V) <sup>(1)</sup> | Temperature Range                             | Package <sup>(2)</sup> | Accuracy <sup>(3)</sup> | Ordering Code <sup>(4)</sup> |
|----------------------------|-----------------------------------|-----------------------------------------------|------------------------|-------------------------|------------------------------|
| 20 MHz                     | 1.7 – 5.5V                        | Industrial <sup>(5)</sup><br>(-40°C to +85°C) | 32A                    | ±10%                    | ATtiny828-AU                 |
|                            |                                   |                                               |                        | ±2%                     | ATtiny828R-AU                |
|                            |                                   |                                               |                        | ±10%                    | ATtiny828-AUR                |
|                            |                                   |                                               |                        | ±2%                     | ATtiny828R-AUR               |
|                            |                                   |                                               | 32M1-A                 | ±10%                    | ATtiny828-MU                 |
|                            |                                   |                                               |                        | ±2%                     | ATtiny828R-MU                |
|                            |                                   |                                               |                        | ±10%                    | ATtiny828-MUR                |
|                            |                                   |                                               |                        | ±2%                     | ATtiny828R-MUR               |

- Notes:
1. For speed vs. supply voltage, see section [“Speed” on page 249](#).
  2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
  3. Indicates accuracy of internal oscillator. See [“Accuracy of Calibrated Internal Oscillator” on page 249](#).
  4. Code indicators:
    - U: matte tin
    - R: tape & reel
  5. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

| Package Type |                                                                       |
|--------------|-----------------------------------------------------------------------|
| 32A          | 32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)               |
| 32M1-A       | 32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm, Quad Flat No-Lead (QFN) |

## 7. Packaging Information

### 7.1 32A



**COMMON DIMENSIONS**  
(Unit of measure = mm)

| SYMBOL | MIN      | NOM  | MAX  | NOTE   |
|--------|----------|------|------|--------|
| A      | —        | —    | 1.20 |        |
| A1     | 0.05     | —    | 0.15 |        |
| A2     | 0.95     | 1.00 | 1.05 |        |
| D      | 8.75     | 9.00 | 9.25 |        |
| D1     | 6.90     | 7.00 | 7.10 | Note 2 |
| E      | 8.75     | 9.00 | 9.25 |        |
| E1     | 6.90     | 7.00 | 7.10 | Note 2 |
| B      | 0.30     | —    | 0.45 |        |
| C      | 0.09     | —    | 0.20 |        |
| L      | 0.45     | —    | 0.75 |        |
| e      | 0.80 TYP |      |      |        |

**Notes:**

1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**32A**, 32-lead, 7 x 7mm body size, 1.0mm body thickness,  
0.8mm lead pitch, thin profile plastic quad flat package (TQFP)

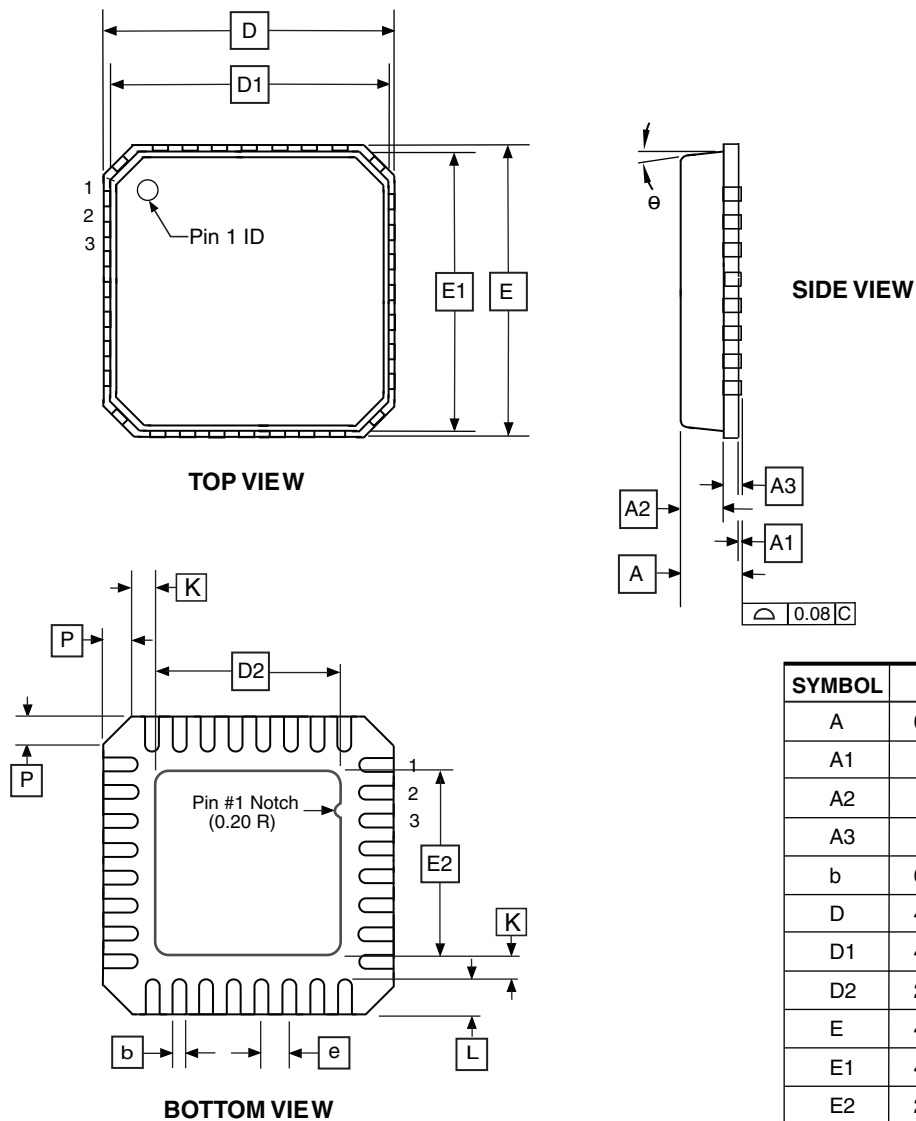
**DRAWING NO.**

32A

**REV.**

C

## 7.2 32M1-A



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL   | MIN      | NOM  | MAX             | NOTE |
|----------|----------|------|-----------------|------|
| A        | 0.80     | 0.90 | 1.00            |      |
| A1       | —        | 0.02 | 0.05            |      |
| A2       | —        | 0.65 | 1.00            |      |
| A3       | 0.20 REF |      |                 |      |
| b        | 0.18     | 0.23 | 0.30            |      |
| D        | 4.90     | 5.00 | 5.10            |      |
| D1       | 4.70     | 4.75 | 4.80            |      |
| D2       | 2.95     | 3.10 | 3.25            |      |
| E        | 4.90     | 5.00 | 5.10            |      |
| E1       | 4.70     | 4.75 | 4.80            |      |
| E2       | 2.95     | 3.10 | 3.25            |      |
| e        | 0.50 BSC |      |                 |      |
| L        | 0.30     | 0.40 | 0.50            |      |
| P        | —        | —    | 0.60            |      |
| $\theta$ | —        | —    | 12 <sup>0</sup> |      |
| K        | 0.20     | —    | —               |      |

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**32M1-A**, 32-pad, 5 x 5 x 1.0mm Body, Lead Pitch 0.50mm,  
3.10mm Exposed Pad, Micro Lead Frame Package (MLF)

### DRAWING NO.

32M1-A

### REV.

E

## 8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny828 device.

### 8.1 Rev. A

- Port Pin Restrictions When ULP Oscillator Is Disabled

#### 1. Port Pin Restrictions When ULP Oscillator Is Disabled

Port pin PD3 is not guaranteed to perform as a reliable input when the Ultra Low Power (ULP) oscillator is not running. In addition, the pin is pulled down internally when ULP oscillator is disabled. TWI and SPI use may be limited when ULP is not running since pin PD3 is used by SCL and SCK signals.

##### Problem Fix / Workaround

The ULP oscillator is automatically activated when required. To use PD3 as an input or clock signal of TWI/SPI, activate the watchdog timer. The watchdog timer automatically enables the ULP oscillator.

## 9. Revision History

| Doc. Rev. | Date    | Comments                  |
|-----------|---------|---------------------------|
| 8371A     | 08/2012 | Initial document release. |





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