

# NCN2500

## USB Single Channel Transceiver

The NCN2500 Integrated Circuit is a single channel transceiver designed to accommodate the physical USB Port with a microcontroller digital I/O. The part is fully USB compliant and supports the full 12 Mbps speed. On the other hand, the NCN2500 device includes the pullup resistors as defined by the USB-ECN new specifications.

### Features

- Compliant to the USB Specification, Version 2.0, Low and Full Speed
- Very Small Footprint Due to the QFN-16 Package
- Integrated D+/D- Pullup Resistors
- Operates Over the Full 1.5 V to 3.6 V Supply
- Pb-Free Package is Available\*

### Typical Applications

- Portable Computer
- Cellular Phone

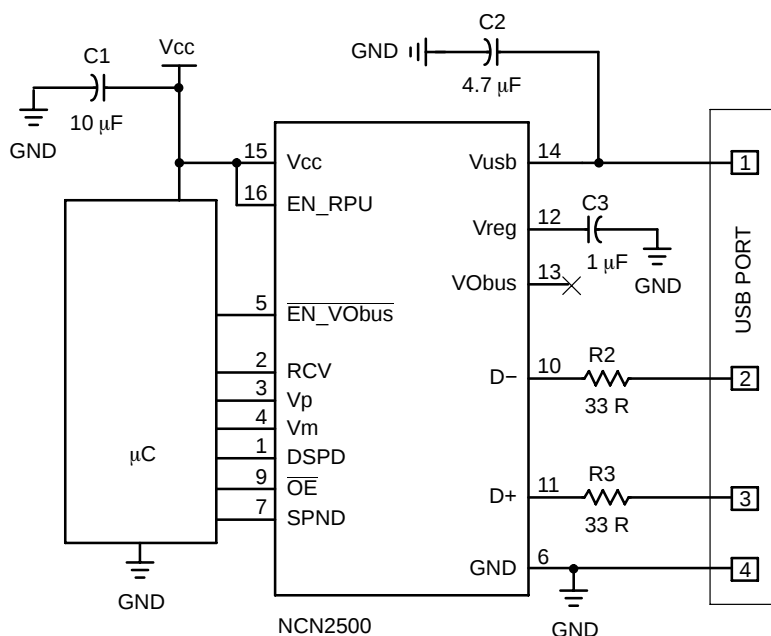


Figure 1. Typical Application

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



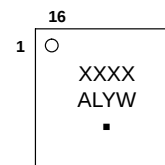
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### MARKING DIAGRAM

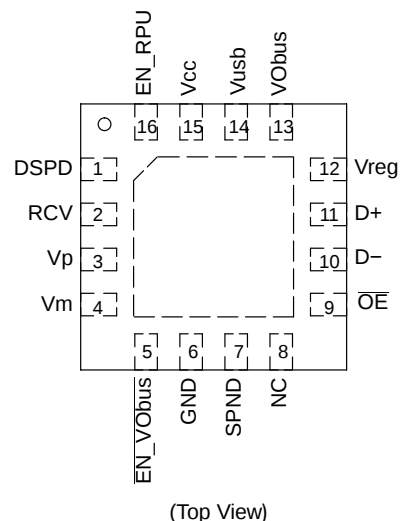


**QFN-16**  
**MNR SUFFIX**  
**CASE 485G**



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

| Device       | Package          | Shipping†        |
|--------------|------------------|------------------|
| NCN2500MNR2  | QFN-16           | 3000 Tape & Reel |
| NCN2500MNR2G | QFN-16 (Pb-Free) | 3000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCN2500

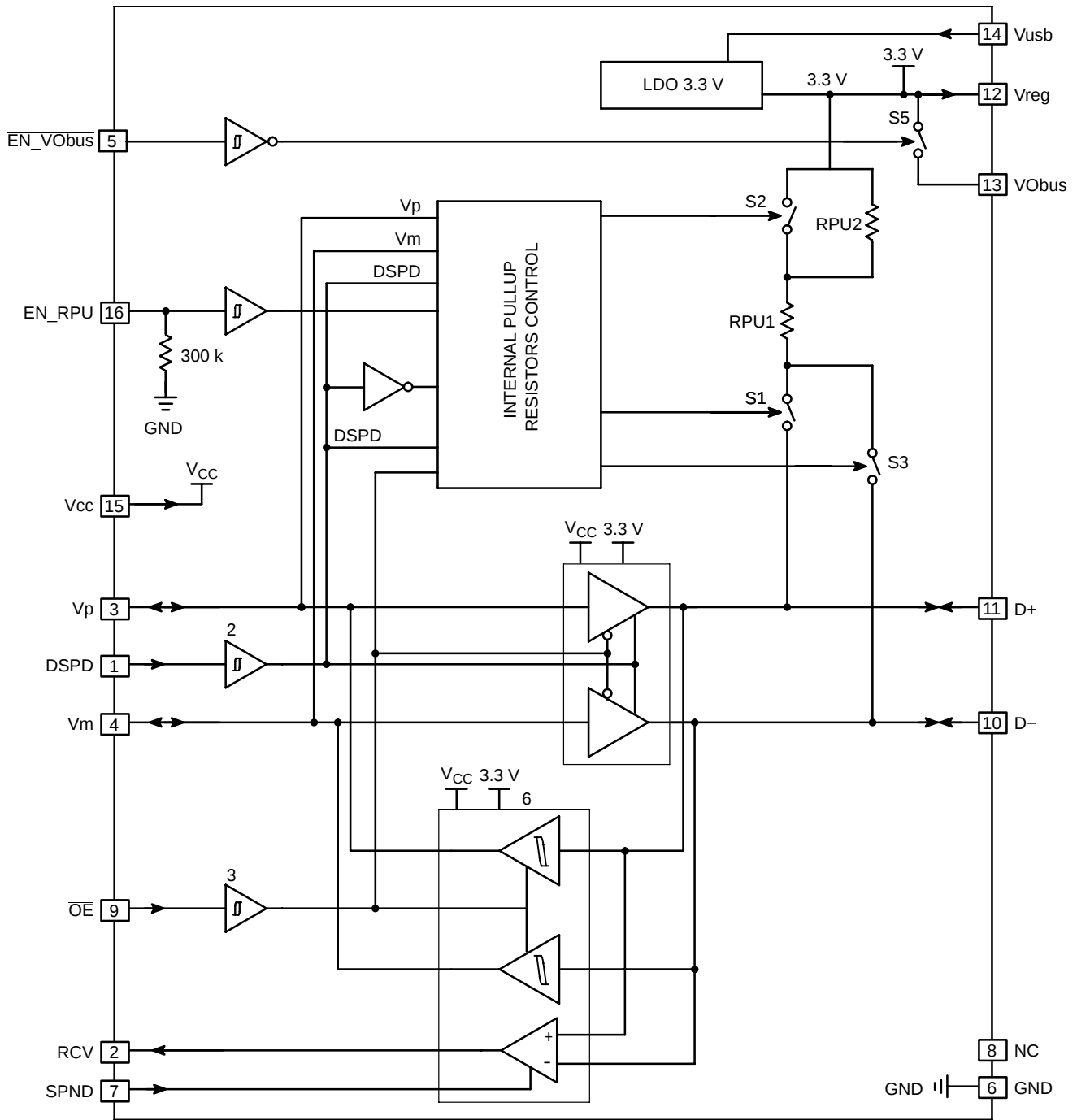


Figure 2. Block Diagram

# NCN2500

## PIN FUNCTION DESCRIPTION

| Pin | Symbol                 | Function    | Description                                                                                                                                                                                                                                                                           |
|-----|------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | DSPD                   | INPUT       | The DSPD logic level (Data Speed) activates the Low or the High speed operation on the USB port.<br>DSPD = Low    Low Speed, RPU1 and RPU2 connected to D-<br>DSPD = High    Full Speed, RPU1 and RPU2 connected to D+                                                                |
| 2   | RCV                    | OUTPUT      | This pin interfaces the USB signals with the microcontroller digital line. The data present on the D+/D- pins are translated onto this signal.                                                                                                                                        |
| 3   | Vp                     | I/O         | This pin, associated with Vm, is an I/O system interface signal depending upon the $\overline{OE}$ logic state:<br>$\overline{OE}$ = Low    Vp is a Plus driver Input (from $\mu$ C to USB bus)<br>$\overline{OE}$ = High    Vp is a Plus receiver Output (from USB bus to $\mu$ C)   |
| 4   | Vm                     | I/O         | This pin, associated with Vp, is an I/O system interface signal depending upon the $\overline{OE}$ logic state:<br>$\overline{OE}$ = Low    Vm is a Minus driver Input (from $\mu$ C to USB bus)<br>$\overline{OE}$ = High    Vm is a Minus receiver Output (from USB bus to $\mu$ C) |
| 5   | $\overline{EN\_VObus}$ | INPUT       | Digital input to control the VObus voltage.<br>$\overline{EN\_VObus}$ = Low    VObus connected to Vreg<br>$\overline{EN\_VObus}$ = High    VObus disconnected from Vreg (Hi Z)                                                                                                        |
| 6   | GND                    | PWR         | This pin carries the digital and USB ground level. High Quality PCB design shall be observed to avoid uncontrolled voltage spikes.                                                                                                                                                    |
| 7   | SPND                   | INPUT       | The SPND digital signal (SUSPEND) selects the operation mode to reduce the power supply current.<br>SPND = Low    Normal operation<br>SPND = High    Suspend mode, no activity takes place                                                                                            |
| 8   | NC                     | -           | No Connection, shall be neither grounded, nor connected to Vcc or Vbus.                                                                                                                                                                                                               |
| 9   | $\overline{OE}$        | INPUT       | This pin activates the operating mode of the D-/D+ signals.<br>$\overline{OE}$ = Low logic level    Data are transmitted onto the USB bus<br>$\overline{OE}$ = High logic level    Data are received from the USB bus                                                                 |
| 10  | D-                     | I/O         | This pin is connected to the USB Minus Data line I/O. The data direction depends upon the $\overline{OE}$ logic state.                                                                                                                                                                |
| 11  | D+                     | I/O         | This pin is connected to the USB Plus Data line I/O. The data direction depends upon the $\overline{OE}$ logic state.                                                                                                                                                                 |
| 12  | Vreg                   | PWR         | This pin provides a 3.3 V regulated voltage to supply the internal USB blocks and the external termination bias resistor. An external circuit can be connected to this LDO, assuming the current does not extend the maximum rating (50 mA).                                          |
| 13  | VObus                  | OUTPUT, PWR | This pin connects the Vreg voltage to the 1.5 k external pullup resistor. The VObus voltage is controlled by the logic states present Pin 5. The $R_{DSon}$ of the internal PMOS device (reference S5 in the Block Diagram) is 10 $\Omega$ typical.                                   |
| 14  | Vusb                   | PWR         | This pin is connected to the USB port +Vcc supply voltage.                                                                                                                                                                                                                            |
| 15  | Vcc                    | PWR         | This pin provides the interface power supply. The power source can be an external supply or can be derived from the USB + Vusb voltage.                                                                                                                                               |
| 16  | EN_RPU                 | INPUT       | This pin activates or deactivate the internal RPU1 and RPU2 pullup resistors:<br>EN_RPU = H    RPU1 and RPU2 activated<br>EN_RPU = L    RPU1 and RPU2 deactivated                                                                                                                     |

**MAXIMUM RATINGS**

| Rating                                                                                                        | Symbol                              | Value                                                           | Unit          |
|---------------------------------------------------------------------------------------------------------------|-------------------------------------|-----------------------------------------------------------------|---------------|
| Power Supply Voltage                                                                                          | V <sub>CC</sub>                     | 6.0                                                             | V             |
| Digital Input Pins                                                                                            | V <sub>IND</sub>                    | -0.5 V < V <sub>IN</sub> < V <sub>CC</sub> + 0.5 V, but < 6.0 V | V             |
| Digital Input Pins                                                                                            | V <sub>ID</sub>                     | -0.5 V < V <sub>IN</sub> < AGND + 0.5 V, but < 6.0 V            | V             |
| Digital Input Pins                                                                                            | I <sub>BIAS</sub>                   | -35 mA < I <sub>BIAS</sub> < 35 mA                              | mA            |
| ESD Capability, HBM (Note 1)<br>V <sub>usb</sub> , D+, D-, GND<br>Any Other Pins<br>Machine Model, Any Pins   | V <sub>ESD</sub>                    | 10<br>2.0<br>200                                                | kV<br>kV<br>V |
| QFN-16 Package<br>Power Dissipation @ Tamb = +85°C<br>Thermal Resistance, Junction-to-Air (R <sub>θJA</sub> ) | P <sub>DS</sub><br>R <sub>θJA</sub> | 470<br>85                                                       | mW<br>°C/W    |
| Operating Ambient Temperature Range                                                                           | T <sub>A</sub>                      | -40 to +85                                                      | °C            |
| Operating Junction Temperature Range                                                                          | T <sub>J</sub>                      | -40 to +125                                                     | °C            |
| Maximum Junction Temperature (Note 2)                                                                         | T <sub>Jmax</sub>                   | +150                                                            | °C            |
| Storage Temperature Range                                                                                     | T <sub>sg</sub>                     | -65 to +150                                                     | °C            |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

- Human Body Model, R = 1500 Ω, C = 100 pF; Machine Model.
- Absolute Maximum Rating beyond which damage(s) to the device may occur.

**ELECTRICAL CHARACTERISTICS**

| Characteristic | Symbol | Pin | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|-----|------|

**DIGITAL PARAMETERS SECTION @ 1.5 V < Vcc < 3.6 V** (–40°C to +85°C ambient temperature, unless otherwise noted.)

NOTE: Digital inputs undershoot < –0.3 V to ground, digital inputs overshoot < 0.3 V to Vcc.

|                                                                                                              |                 |                      |          |     |          |    |
|--------------------------------------------------------------------------------------------------------------|-----------------|----------------------|----------|-----|----------|----|
| High Level Input Voltage DSPD, Vp, Vm, $\overline{\text{EN\_VObus}}$ , SPND, $\overline{\text{OE}}$ , EN_RPU | V <sub>IH</sub> | 1, 3, 4, 5, 7, 9, 16 | 0.80*Vcc | –   | –        | V  |
| Low Level Input Voltage DSPD, Vp, Vm, $\overline{\text{EN\_VObus}}$ , SPND, OE, EN_RPU                       | V <sub>IL</sub> | 1, 3, 4, 5, 7, 9, 16 | –        | –   | 0.20*Vcc | V  |
| High Level Output Voltage RCV, Vp, Vm @ I <sub>OH</sub> = 1.0 mA                                             | V <sub>OH</sub> | 2, 3, 4              | 0.80*Vcc | –   | –        | V  |
| Low Level Output Voltage RCV, Vp, Vm @ I <sub>OL</sub> = 1.0 mA                                              | V <sub>OL</sub> | 2, 3, 4              | –        | –   | 0.20*Vcc | V  |
| Input Leakage Current DSPD, Vp, Vm, $\overline{\text{EN\_VObus}}$ , SPND, $\overline{\text{OE}}$ , EN_RPU    | I <sub>IL</sub> | 1, 3, 4, 5, 7, 9, 16 | –        | –   | ± 5.0    | μA |
| Input EN_RPU Pulldown Resistor @VCC = 3.3 V                                                                  | RPU             | –                    | –        | 300 | –        | kΩ |

**TRANSCEIVER SECTION @ 1.5 V < Vcc < 3.6 V** (–40°C to +85°C ambient temperature, unless otherwise noted.)

|                                                                                           |                    |        |     |     |      |    |
|-------------------------------------------------------------------------------------------|--------------------|--------|-----|-----|------|----|
| Static Output High, D–, D+ @ $\overline{\text{OE}}$ = Low, R <sub>L</sub> = 15 kΩ to GND  | V <sub>OH</sub>    | 10, 11 | 2.8 | –   | 3.6  | V  |
| Static Output Low, D–, D+ @ $\overline{\text{OE}}$ = Low, R <sub>L</sub> = 1.5 kΩ to Vreg | V <sub>OL</sub>    | 10, 11 | –   | –   | 0.3  | V  |
| Single Input Receiver Threshold                                                           | V <sub>SE</sub>    | 10, 11 | 0.8 | –   | 2.0  | V  |
| Single Ended Receiver Hysteresis (Note 3)                                                 | –                  | –      | –   | 200 | –    | mV |
| Differential Input Sensitivity   D+ – D–   @ 0.8 V < V <sub>CM</sub> < 2.5 V (Note 3)     | V <sub>DI</sub>    | 10, 11 | 0.2 | –   | –    | V  |
| Differential Common Mode Including the V <sub>DI</sub>                                    | V <sub>CM</sub>    | 10, 11 | 0.8 | –   | 2.5  | V  |
| Differential Receiver Hysteresis (Note 3)                                                 | –                  | 10, 11 | –   | 70  | –    | mV |
| D+ and D– Transceiver Hi-Z State Leakage Current @ OE = 1, 0 V < Vusb < 3.3 V             | I <sub>LO</sub>    | 10, 11 | –   | –   | ± 10 | μA |
| Transceiver Input Capacitance (Note 3)                                                    | C <sub>in</sub>    | 10, 11 | –   | –   | 20   | pF |
| Transceiver Output Resistance (Note 3)                                                    | Z <sub>DRV</sub>   | 10, 11 | 28  | –   | 44   | Ω  |
| Transceiver Input Impedance (Note 3)                                                      | Z <sub>IN</sub>    | 10, 11 | 10  | –   | –    | MΩ |
| Internal RPU1 Pull Resistor                                                               | R <sub>RPU-1</sub> | 10, 12 | 900 | –   | 1575 | Ω  |
| Internal RPU2 Pull Up Resistor                                                            | R <sub>RPU-2</sub> | 10, 12 | 525 | –   | 1515 | Ω  |

**LOW SPEED DRIVER OPERATION** (Note 3)

|                                                                               |                                 |        |          |        |            |     |
|-------------------------------------------------------------------------------|---------------------------------|--------|----------|--------|------------|-----|
| Transition Rise Time<br>@ C <sub>L</sub> = 50 pF<br>@ C <sub>L</sub> = 600 pF | t <sub>r</sub>                  | 10, 11 | 75<br>75 | –<br>– | 300<br>300 | ns  |
| Transition Fall Time<br>@ C <sub>L</sub> = 50 pF<br>@ C <sub>L</sub> = 600 pF | t <sub>f</sub>                  | 10, 11 | 75<br>75 | –<br>– | 300<br>300 | ns  |
| Rise and Fall Time Matching                                                   | t <sub>r</sub> , t <sub>f</sub> | 10, 11 | 80       | –      | 125        | %   |
| Output Signal Crossover Voltage                                               | V <sub>CRS</sub>                | 10, 11 | 1.3      | –      | 2.0        | V   |
| Data Transaction Rate                                                         | Drate                           | 10, 11 | –        | –      | 1.5        | Mbs |

3. Parameter guaranteed by design, not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

| Characteristic | Symbol | Pin | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|-----|------|

**FULL SPEED DRIVER OPERATION (Note 4)**

|                                              |            |        |     |   |     |     |
|----------------------------------------------|------------|--------|-----|---|-----|-----|
| Transition Rise Time @ $C_L = 50 \text{ pF}$ | $t_r$      | 10, 11 | 4.0 | – | 20  | ns  |
| Transition Fall Time @ $C_L = 50 \text{ pF}$ | $t_f$      | 10, 11 | 4.0 | – | 20  | ns  |
| Rise and Fall Time Matching                  | $t_r, t_f$ | 10, 11 | 90  | – | 110 | %   |
| Output Signal Crossover Voltage              | $V_{CRS}$  | 10, 11 | 1.3 | – | 2.0 | V   |
| Data Transaction Rate                        | Drate      | 10, 11 | –   | – | 12  | Mbs |

**TRANSCEIVER TIMING (Note 4)**

|                                                                                                                                        |           |              |    |   |     |    |
|----------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------|----|---|-----|----|
| $\overline{OE}$ to RCVR Hi-Z Delay (see Figure 3)                                                                                      | $t_{PVZ}$ | 9            | –  | – | 15  | ns |
| Receiver Hi-Z to Transmit Delay (see Figure 3)                                                                                         | $t_{PZD}$ | –            | 15 | – | –   | ns |
| $\overline{OE}$ to DRVR Hi-Z Delay (see Figure 3)                                                                                      | $t_{PDZ}$ | –            | –  | – | 15  | ns |
| Driver Hi-Z to Receiver Delay (see Figure 3)                                                                                           | $t_{PZV}$ | –            | 15 | – | –   | ns |
| Vp/Vm to D+/D– Propagation Delay (see Figure 6)                                                                                        | $t_{PLH}$ | 3, 4, 10, 11 | –  | – | 15  | ns |
| Vp/Vm to D+/D– Propagation Delay (see Figure 6)                                                                                        | $t_{PHL}$ | 3, 4, 10, 11 | –  | – | 15  | ns |
| D+/D– to RCV Propagation Delay @ $1.5 < V_{CC} < 5.5 \text{ V}$<br>(see Figure 5) $C_L = 25 \text{ pF}$ $t_r = t_f = 3.0 \text{ ns}$   | $t_{PLH}$ | 11, 10, 2    | –  | – | 15  | ns |
| D+/D– to RCV Propagation Delay @ $1.5 < V_{CC} < 5.5 \text{ V}$<br>(see Figure 5) $C_L = 25 \text{ pF}$ $t_r = t_f = 3.0 \text{ ns}$   | $t_{PHL}$ | 11, 10, 2    | –  | – | 15  | ns |
| D+/D– to Vp/D– Propagation Delay @ $1.5 < V_{CC} < 5.5 \text{ V}$<br>(see Figure 5) $C_L = 25 \text{ pF}$ $t_r = t_f = 3.0 \text{ ns}$ | $t_{PLH}$ | 11, 10, 3    | –  | – | 8.0 | ns |
| D+/D– to Vm/D– Propagation Delay @ $1.5 < V_{CC} < 5.5 \text{ V}$<br>(see Figure 5) $C_L = 25 \text{ pF}$ $t_r = t_f = 3.0 \text{ ns}$ | $t_{PHL}$ | 11, 10, 4    | –  | – | 8.0 | ns |

**POWER SUPPLY SECTION @  $1.5 \text{ V} < V_{CC} < 3.6 \text{ V}$  ( $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  ambient temperature, unless otherwise noted.)**

|                                                                                                                                                                                                           |            |    |     |            |        |                              |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|----|-----|------------|--------|------------------------------|
| Digital Supply Voltage                                                                                                                                                                                    | $V_{CC}$   | 15 | 1.5 | –          | 3.6    | V                            |
| USB Port Input Supply Voltage                                                                                                                                                                             | $V_{USB}$  | 14 | 4.0 | –          | 5.25   | V                            |
| Output Regulated Voltage @ $4.0 \text{ V} < V_{USB} < 5.25 \text{ V}$ ,<br>$C_{in} = 4.7 \text{ }\mu\text{F}$ , $C_{out} = 1.0 \text{ }\mu\text{F}$ , $I_{reg} = 100 \text{ mA}$                          | $V_{reg}$  | 12 | 3.0 | 3.3        | 3.6    | V                            |
| Output Switched Voltage @ $I_o = 1.0 \text{ mA}$ , $C_{in} = 4.7 \text{ }\mu\text{F}$                                                                                                                     | $V_{obus}$ | 13 | 3.0 | 3.3        | 3.6    | V                            |
| Line Regulation Output Voltage                                                                                                                                                                            | $V_{reg}$  | 12 | –   | 0.1        | –      | %                            |
| Standby Current @ $V_{USB} = 5.25 \text{ V}$ , $\overline{OE} = H$ , $SPND = H$ ,<br>D+ and D– are Idle, $V_{CC} = 3.6 \text{ V}$                                                                         | $I_{VCC}$  | 14 | –   | 1.0        | –      | $\mu\text{A}$                |
| Standby Current @ $V_{USB} = 5.25 \text{ V}$ , $\overline{OE} = H$ , $SPND = L$ ,<br>D+ and D– are Idle, $V_{CC} = 3.6 \text{ V}$                                                                         | $I_{VCC}$  | 14 | –   | 1.0        | –      | $\mu\text{A}$                |
| Operating Current $\overline{OE} = L$ , D– and D+ Active, $SPND = L$<br>(Note 4), Transmitter Mode<br>@ $F = 6.0 \text{ MHz}$ , $C_L = 50 \text{ pF}$<br>@ $F = 750 \text{ kHz}$ , $C_L = 600 \text{ pF}$ | $I_{VCC}$  | 14 | –   | 300<br>40  | –<br>– | $\mu\text{A}$                |
| Operating Current $\overline{OE} = H$ , D– and D+ Active, $SPND = L$<br>(Note 4), Receiver Mode<br>@ $F = 6.0 \text{ MHz}$ , $C_L = 25 \text{ pF}$<br>@ $F = 750 \text{ kHz}$ , $C_L = 25 \text{ pF}$     | $I_{VCC}$  | 14 | –   | 1.5<br>250 | –<br>– | $\text{mA}$<br>$\mu\text{A}$ |

4. Parameter guaranteed by design, not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

| Characteristic                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Symbol | Pin | Min                                            | Typ                                                  | Max                                      | Unit                                         |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|------------------------------------------------|------------------------------------------------------|------------------------------------------|----------------------------------------------|
| <b>POWER SUPPLY SECTION @ 1.5 V &lt; Vcc &lt; 3.6 V (continued)</b> (–40°C to +85°C ambient temperature, unless otherwise noted.)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |     |                                                |                                                      |                                          |                                              |
| USB Supply Current @ D– and D+ are Idle,<br>Vusb = 5.25 V and:<br>@ SPND = 1, $\overline{OE}$ = 1, DSPD = 0, EN_RPU = 0<br>@ SPND = 0, $\overline{OE}$ = 1, DSPD = 1, EN_RPU = 0<br>@ SPND = 0, $\overline{OE}$ = 0, DSPD = 0, EN_RPU = 0<br><br>@ SPND = 1, $\overline{OE}$ = 1, DSPD = 0, EN_RPU = 1<br><br>@ D– and D+ are Active, CL = 50 pF, Vusb = 5.25 V,<br>SPND = 0, $\overline{OE}$ = 0, DSPD = 1, F = 6.0 MHz (Note 5)<br>@ EN_RPU = Low<br>@ EN_RPU = High<br>@ D– and D+ are Active (Note 5)<br>Vusb = 5.25 V, SPND = 0, $\overline{OE}$ = 0, DSPD = 1,<br>F = 750 kHz, CL = 600 pF<br>F = 750 kHz, CL = 300 pF | IBUS   | 14  | –<br>–<br>–<br>–<br>–<br>–<br>–<br>–<br>–<br>– | 120<br>1.7<br>1.7<br>320<br>8.3<br>9.4<br>5.4<br>3.9 | 200<br>–<br>–<br>500<br>–<br>–<br>–<br>– | μA<br>mA<br>mA<br>μA<br>mA<br>mA<br>mA<br>mA |

5. Parameter guaranteed by design, not production tested.

**Table 1. Internal RPU1 and RPU2 Pullup Resistors Control**

| EN_RPU | DSPD | S1     | S2    | S3    | Data Line | USB        | Note                                                |
|--------|------|--------|-------|-------|-----------|------------|-----------------------------------------------------|
| 0      | X    | X      | X     | X     | X         | X          | Internal RPU Deactivated, S1 and S3 are Forced OPEN |
| 1      | 1    | Open   | X     | Open  | Vbus Off  | X          | Internal RPU disabled                               |
| 1      | 1    | Close  | Close | Open  | Idle      | Full Speed | Internal RPU Activated                              |
| 1      | 1    | Closed | Open  | Open  | Receiving | Full Speed | Internal RPU Activated                              |
| 1      | 0    | Open   | X     | Open  | Vbus Off  | X          | Internal RPU disabled                               |
| 1      | 0    | Open   | Close | Close | Idle      | Low Speed  | Internal RPU Activated                              |
| 1      | 0    | Open   | Open  | Close | Receiving | Low Speed  | Internal RPU Activated                              |

6. See Figure 8 and Figure 9.

**Table 2. Transmit Mode Interface Control ( $\overline{OE} = 0 \rightarrow$  Transmit Mode)**

| SPND | Vp | Vm | D+ | D- | RCV | STATE     |
|------|----|----|----|----|-----|-----------|
| 0    | 0  | 0  | 0  | 0  | X   | SE0       |
| 0    | 0  | 1  | 0  | 1  | 0   | Low       |
| 0    | 1  | 0  | 1  | 0  | 1   | High      |
| 0    | 1  | 1  | 1  | 1  | X   | Undefined |
| 1    | 0  | 0  | 0  | 0  | 0   | Suspend   |
| 1    | 0  | 1  | 0  | 1  | 0   | Suspend   |
| 1    | 1  | 0  | 1  | 0  | 0   | Suspend   |
| 1    | 1  | 1  | 1  | 1  | 0   | Suspend   |

**Table 3. Receive Mode Interface Control ( $\overline{OE} = 1 \rightarrow$  Receive Mode)**

| SPND | D+ | D- | Vp | Vm | RCV | STATE     |
|------|----|----|----|----|-----|-----------|
| 0    | 0  | 0  | 0  | 0  | X   | SE0       |
| 0    | 0  | 1  | 0  | 1  | 0   | Low       |
| 0    | 1  | 0  | 1  | 0  | 1   | High      |
| 0    | 1  | 1  | 1  | 1  | X   | Undefined |
| 1    | 0  | 0  | 0  | 0  | 0   | Suspend   |
| 1    | 0  | 1  | 0  | 1  | 0   | Suspend   |
| 1    | 1  | 0  | 1  | 0  | 0   | Suspend   |
| 1    | 1  | 1  | 1  | 1  | 0   | Suspend   |

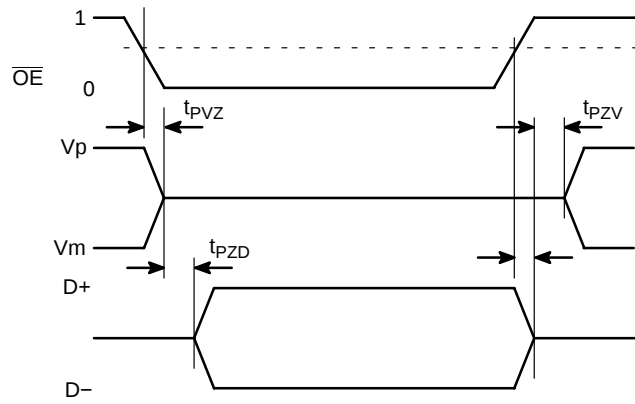


Figure 3. Enable and Disable USB Times

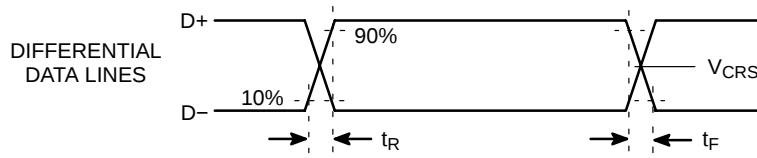


Figure 4. USB Line Rise and Fall Times

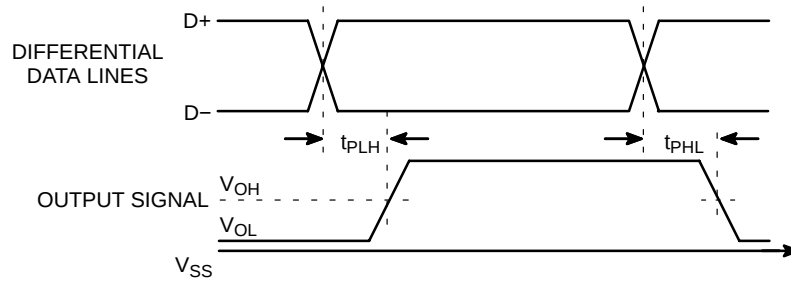


Figure 5. Receiver Propagation Delays

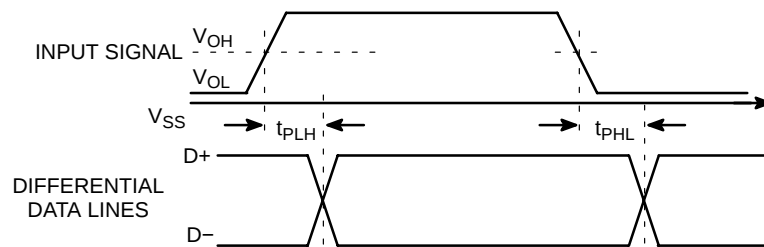


Figure 6. Driver Propagation Delays

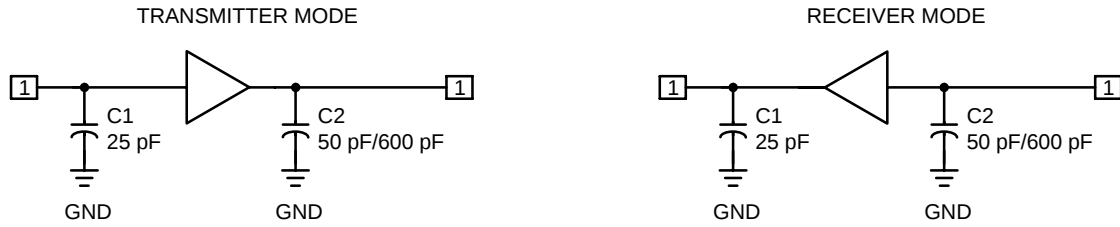


Figure 7. Input/Output Stray Capacitance Definitions

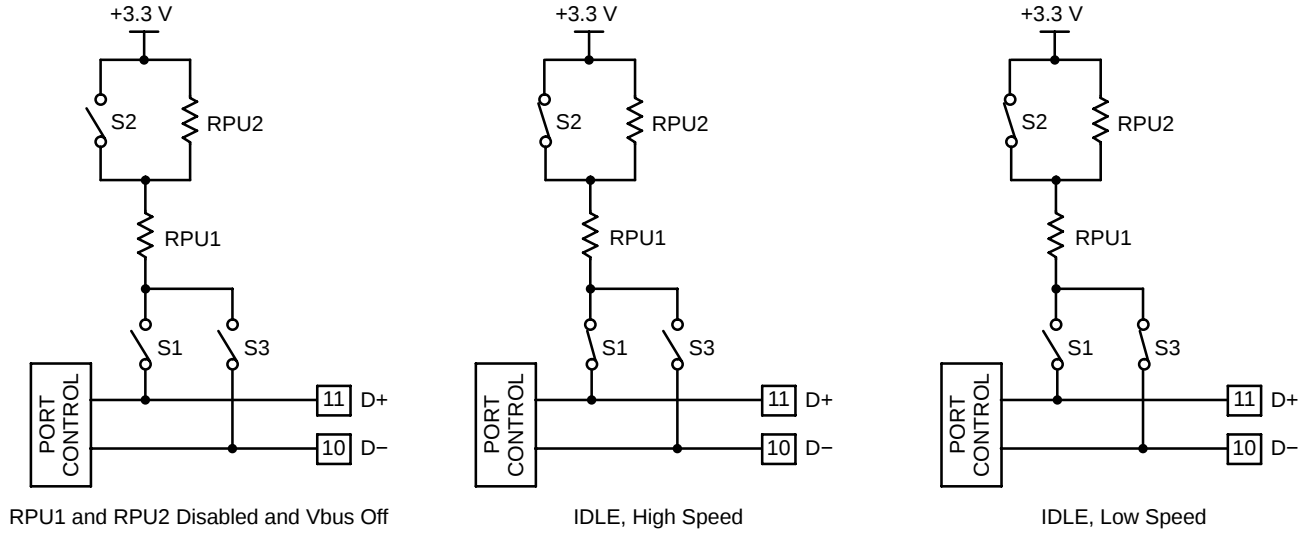
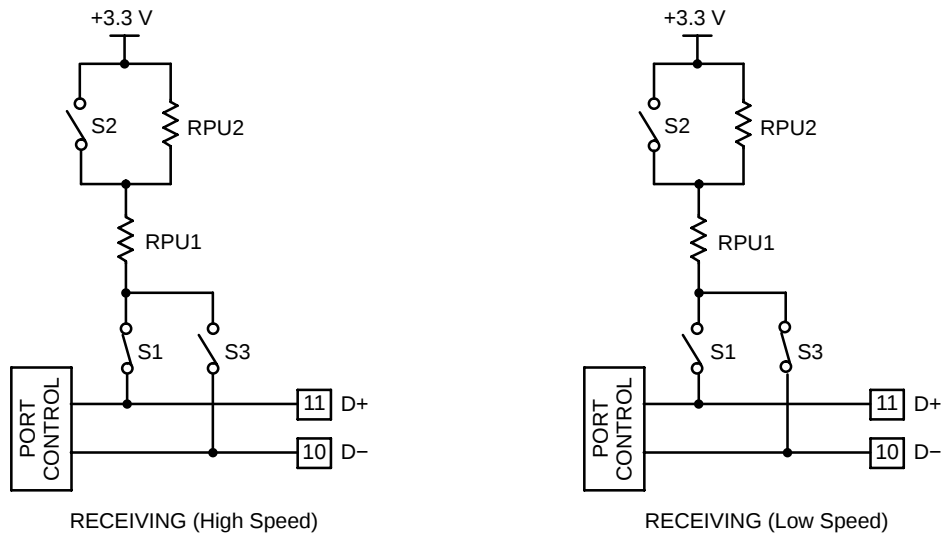


Figure 8. Internal RPU1 and RPU2 Pullup Resistors Operation, IDLE Mode

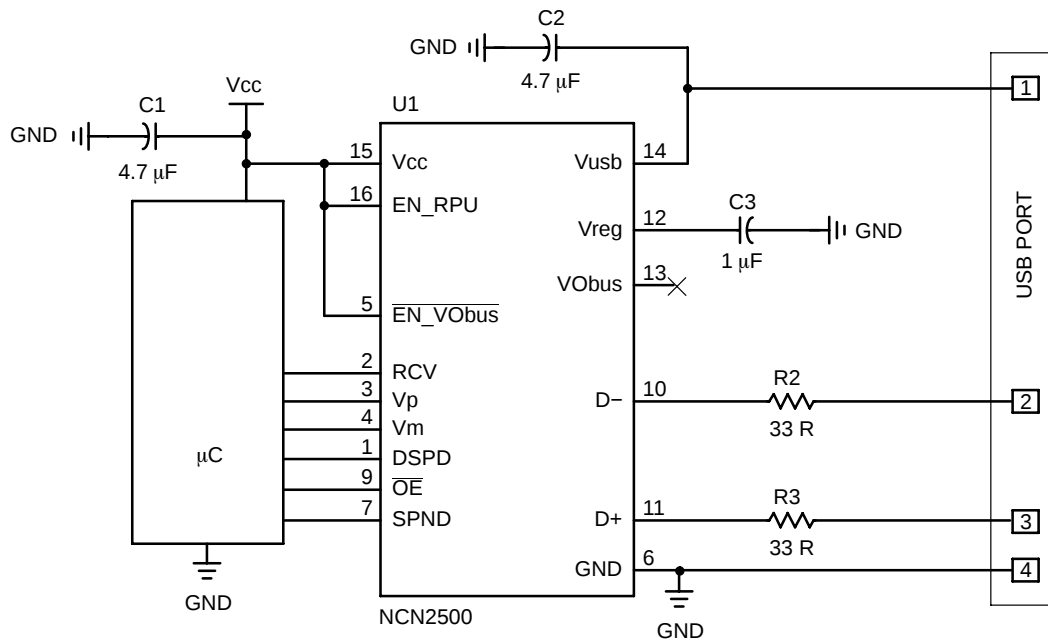


NOTE: Internal Pullup Resistor Range: RPU1: 900  $\Omega$  min–1575  $\Omega$  max, RPU2: 525  $\Omega$  min–1515  $\Omega$  max

Figure 9. Internal RPU1 and RPU2 Pullup Resistors Activated, RECEIVING Mode

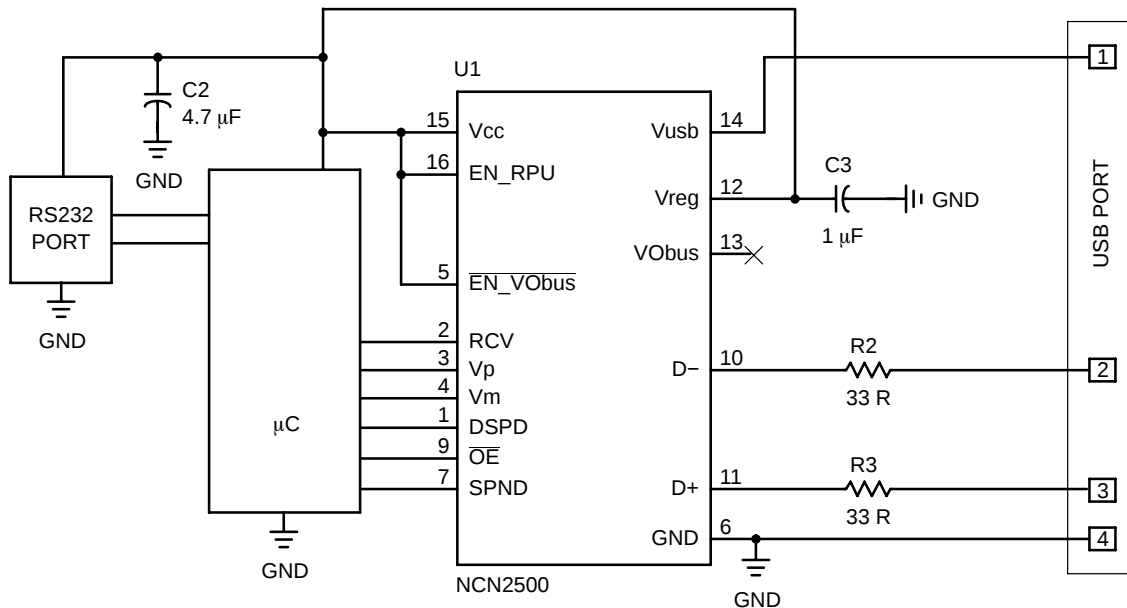
# NCN2500

## TYPICAL APPLICATIONS



In this application, the two internal pullup resistors (RPU1 and RPU2) are used to bias the USB line. Consequently, the VObus voltage is deactivated (Pin 5 connected to Vcc).

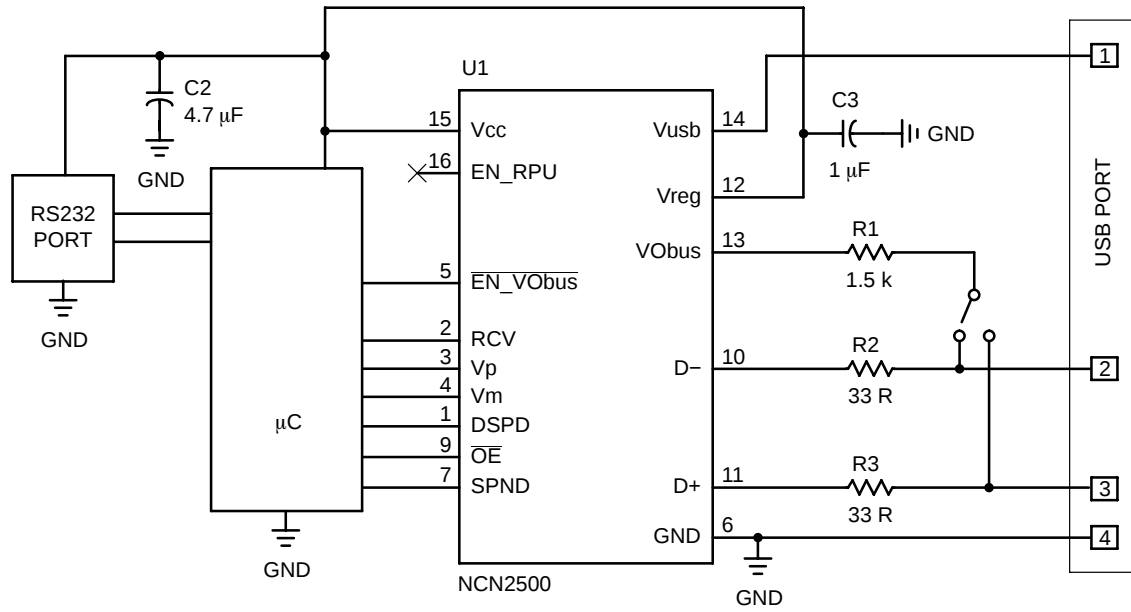
**Figure 10. Fully Independent Power Supplies**



**Figure 11. Peripheral are Powered by the Vreg Supply**

# NCN2500

## TYPICAL APPLICATIONS



Note: Pin 16 can be left open, due to the internal pull-down resistor, or connected to ground.

**Figure 12. Using External Pullup Resistors**

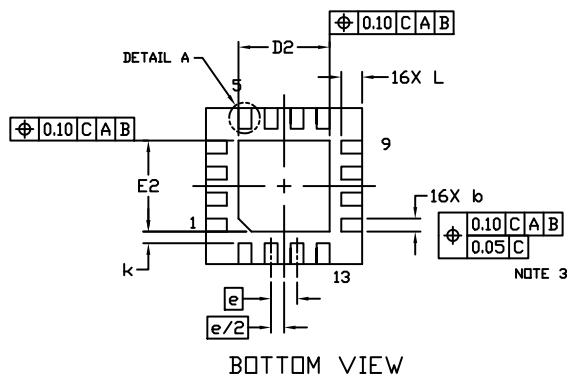
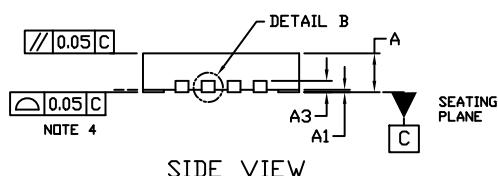
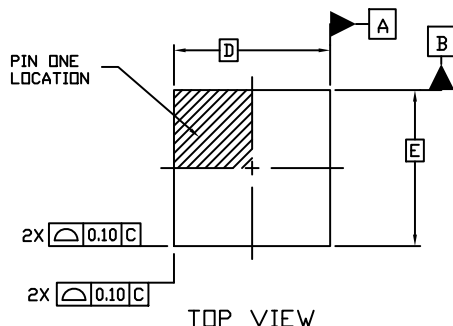
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

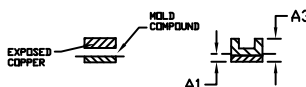
## QFN16 3x3, 0.5P CASE 485G ISSUE G

DATE 08 OCT 2021

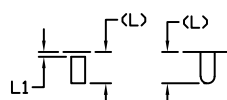


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



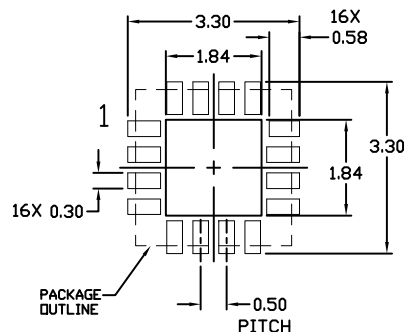
DETAIL B  
ALTERNATE  
CONSTRUCTIONS



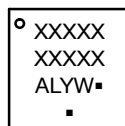
DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NDM. | MAX. |
| A   | 0.80        | 0.90 | 1.00 |
| A1  | 0.00        | 0.03 | 0.05 |
| A3  | 0.20 REF    |      |      |
| b   | 0.18        | 0.24 | 0.30 |
| D   | 3.00 BSC    |      |      |
| D2  | 1.65        | 1.75 | 1.85 |
| E   | 3.00 BSC    |      |      |
| E2  | 1.65        | 1.75 | 1.85 |
| e   | 0.50 BSC    |      |      |
| k   | 0.18 TYP    |      |      |
| L   | 0.30        | 0.40 | 0.50 |
| L1  | 0.00        | 0.08 | 0.15 |

### MOUNTING FOOTPRINT



### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                  |                 |                                                                                                                                                                                     |
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| DESCRIPTION:     | QFN16 3X3, 0.5P | PAGE 1 OF 1                                                                                                                                                                         |

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