

74LVTN16244B

3.3 V 16-bit buffer/driver; 3-state

Rev. 02 — 23 March 2010

Product data sheet

1. General description

The 74LVTN16244B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-state bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

2. Features and benefits

- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
 - ◆ JESD78B Class II exceeds 500 mA
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

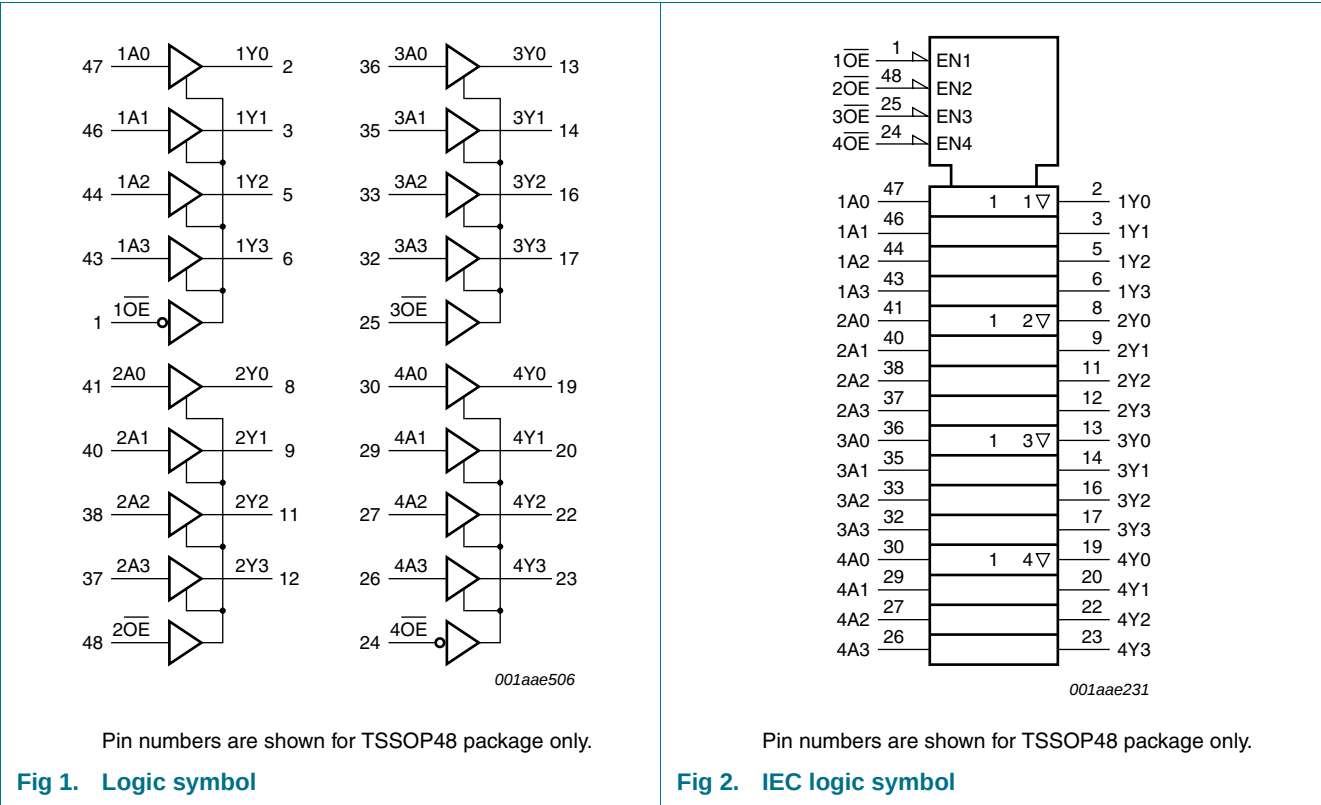
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVTN16244BDGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVTN16244BBQ	–40 °C to +85 °C	HXQFN60U	plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 × 6 × 0.5 mm	SOT1134-1



4. Functional diagram



5. Pinning information

5.1 Pinning

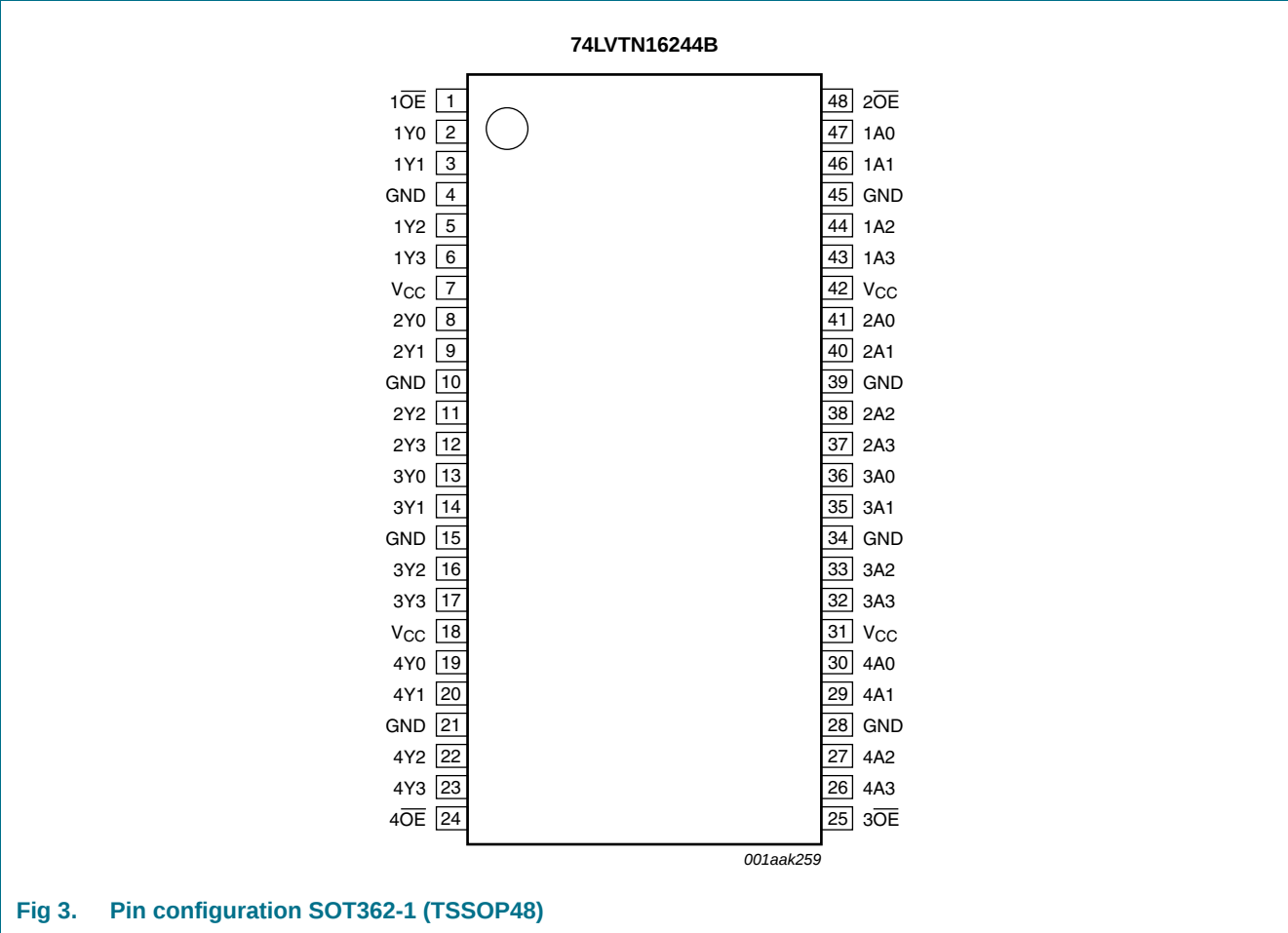
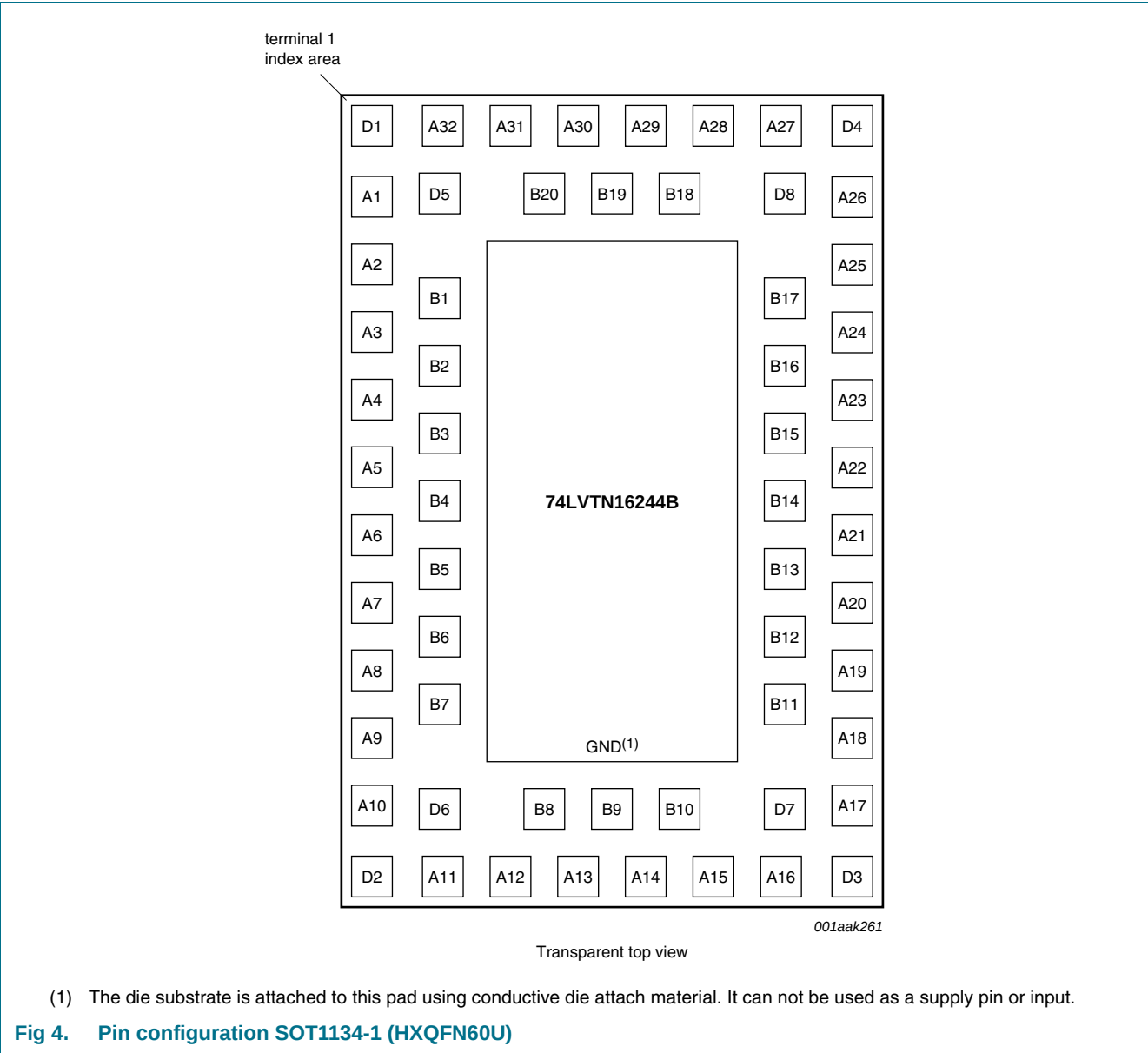


Fig 3. Pin configuration SOT362-1 (TSSOP48)



5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT362-1	SOT1134-1	
$\overline{1OE}$, $\overline{2OE}$, $\overline{3OE}$, $\overline{4OE}$	1, 48, 25, 24	A30, A29, A14, A13	output enable input (active LOW)
1Y0 to 1Y3	2, 3, 5, 6	B20, A31, D5, D1	data output
2Y0 to 2Y3	8, 9, 11, 12	A2, B2, B3, A5	data output
3Y0 to 3Y3	13, 14, 16, 17	A6, B5, B6, A9	data output
4Y0 to 4Y3	19, 20, 22, 23	D2, D6, A12, B8	data output

Table 2. Pin description ...continued

Symbol	Pin		Description
	SOT362-1	SOT1134-1	
GND	4, 10, 15, 21, 28, 34, 39, 45	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V _{CC}	7, 18, 31, 42	A1, A10, A17, A26	supply voltage
1A0 to 1A3	47, 46, 44, 43	B18, A28, D8, D4	data input
2A0 to 2A3	41, 40, 38, 37	A25, B16, B15, A22	data input
3A0 to 3A3	36, 35, 33, 32	A21, B13, B12, A18	data input
4A0 to 4A3	30, 29, 27, 26	D3, D7, A15, B10	data input
n.c.	-	A4, A7, A20, A23, B1, B4, B7, B9, B11, B14, B17, B19	not connected

6. Functional description

Table 3. Function table^[1]

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		^[1] -0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	^[1] -0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		^[2] -	150	°C

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$;			
		TSSOP48 package	[3] -	500	mW
		HXQFN60U package	[4] -	1000	mW

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
- [3] Above $60\text{ }^{\circ}\text{C}$ the value of P_{tot} derates linearly with 5.5 mW/K .
- [4] Above $70\text{ }^{\circ}\text{C}$ the value of P_{tot} derates linearly with 1.8 mW/K .

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_{I}	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$; $f_i \geq 1\text{ kHz}$	-	-	64	mA
T_{amb}	ambient temperature	in free-air	-40	-	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-0.85	-	V
V _{OH}	HIGH-level output voltage	I _{OH} = -100 µA; V _{CC} = 2.7 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _{OH} = -8 mA; V _{CC} = 2.7 V	2.4	2.5	-	V
		I _{OH} = -32 mA; V _{CC} = 3.0 V	2.0	2.3	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V				
		I _{OL} = 100 µA	-	0.07	0.2	V
		I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V				
		I _{OL} = 16 mA	-	0.25	0.4	V
		I _{OL} = 32 mA	-	0.3	0.5	V
I _I	input leakage current	V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	0.1	10	µA
		control pins; V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	0.1	±1.0	µA
		data pins; unused pins at V _{CC} or GND				
		V _I = V _{CC} ; V _{CC} = 3.6 V	-	0.1	1	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	0.1	±100	µA
		V _I = 0 V; V _{CC} = 3.6 V	-5	-0.1	-	µA
I _{LO}	output leakage current	output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	50	125	µA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; nOE = don't care	-	1	±100	µA
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL}				
		output HIGH: V _O = 3.0 V	-	0.5	5	µA
		output LOW: V _O = 0.5 V	-5	+0.5	-	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A				
		output HIGH	-	0.07	0.12	mA
		output LOW	-	4.0	6.0	mA
		outputs disabled	[3]	0.07	0.12	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; one input at V _{CC} - 0.6 V other inputs at V _{CC} or GND	[4]	0.1	0.2	mA
C _I	input capacitance	V _I = 0 V or 3.0 V	-	3	-	pF
C _O	output capacitance	outputs disabled; V _O = 0 V or 3.0 V	-	9	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and at T_{amb} = 25 °C.

[2] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[3] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[4] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C^[1]						
t _{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Figure 5				
		V _{CC} = 2.7 V	-	-	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	1.8	3.2	ns
t _{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Figure 5				
		V _{CC} = 2.7 V	-	-	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	1.7	3.2	ns
t _{PZH}	OFF-state to HIGH propagation delay	nOE to nYn; see Figure 6				
		V _{CC} = 2.7 V	-	-	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	4.0	ns
t _{PZL}	OFF-state to LOW propagation delay	nOE to nYn; see Figure 6				
		V _{CC} = 2.7 V	-	-	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.1	4.0	ns
t _{PHZ}	HIGH to OFF-state propagation delay	nOE to nYn; see Figure 6				
		V _{CC} = 2.7 V	-	-	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.2	4.5	ns
t _{PLZ}	LOW to OFF-state propagation delay	nOE to nYn; see Figure 6				
		V _{CC} = 2.7 V	-	-	4.4	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.9	4.0	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Waveforms

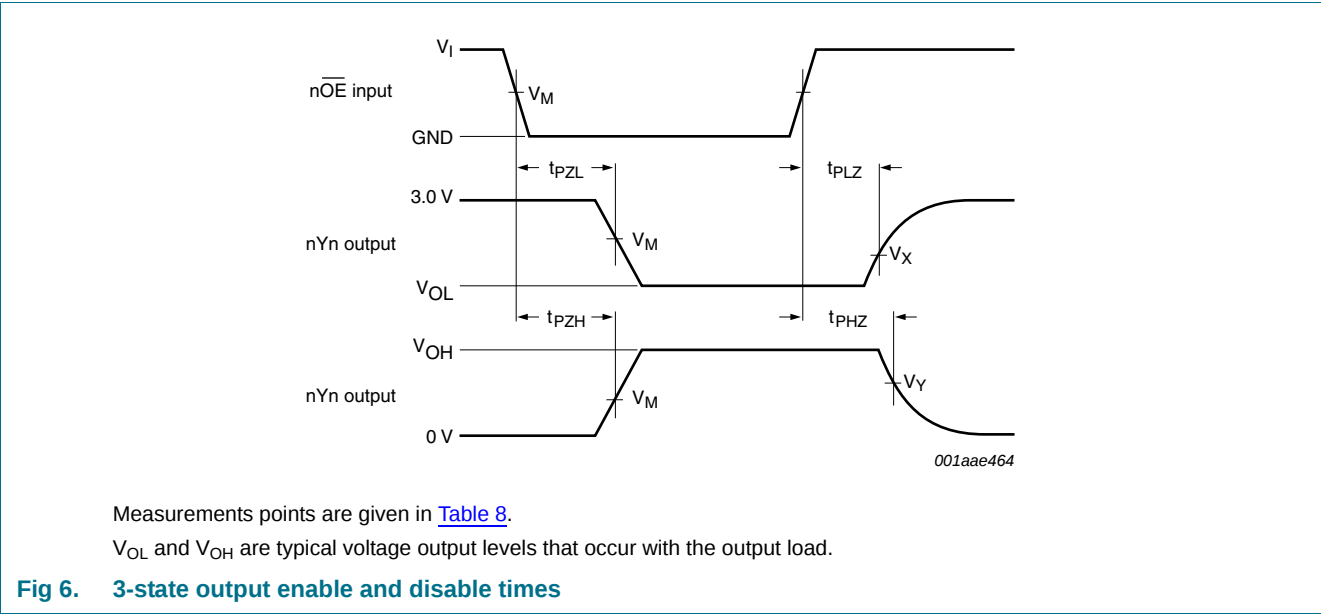
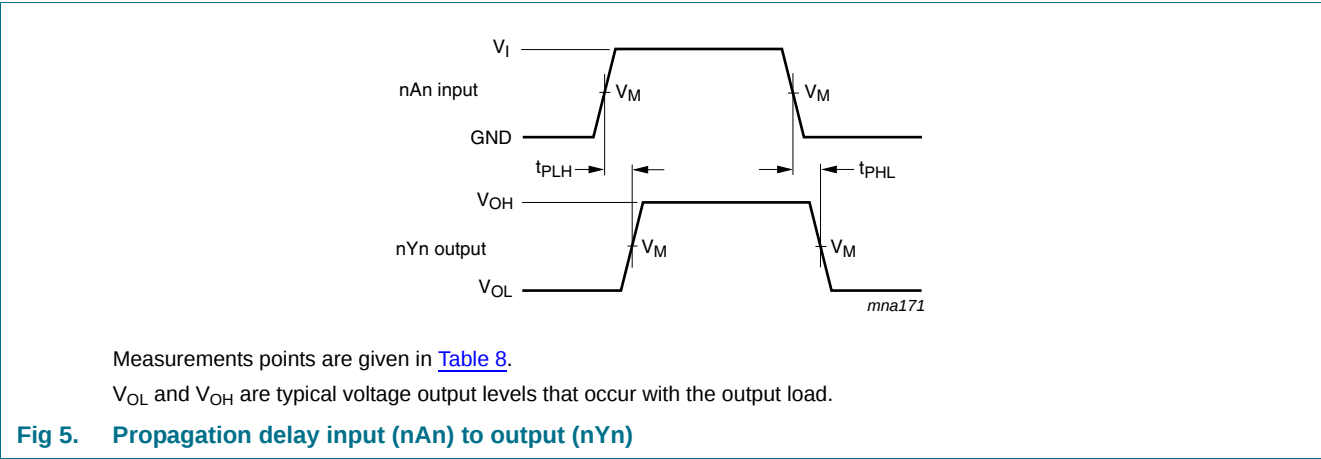
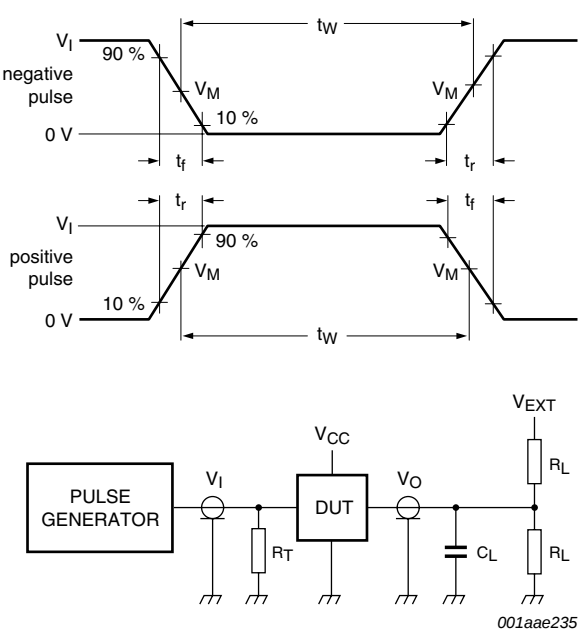


Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 7. Load circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

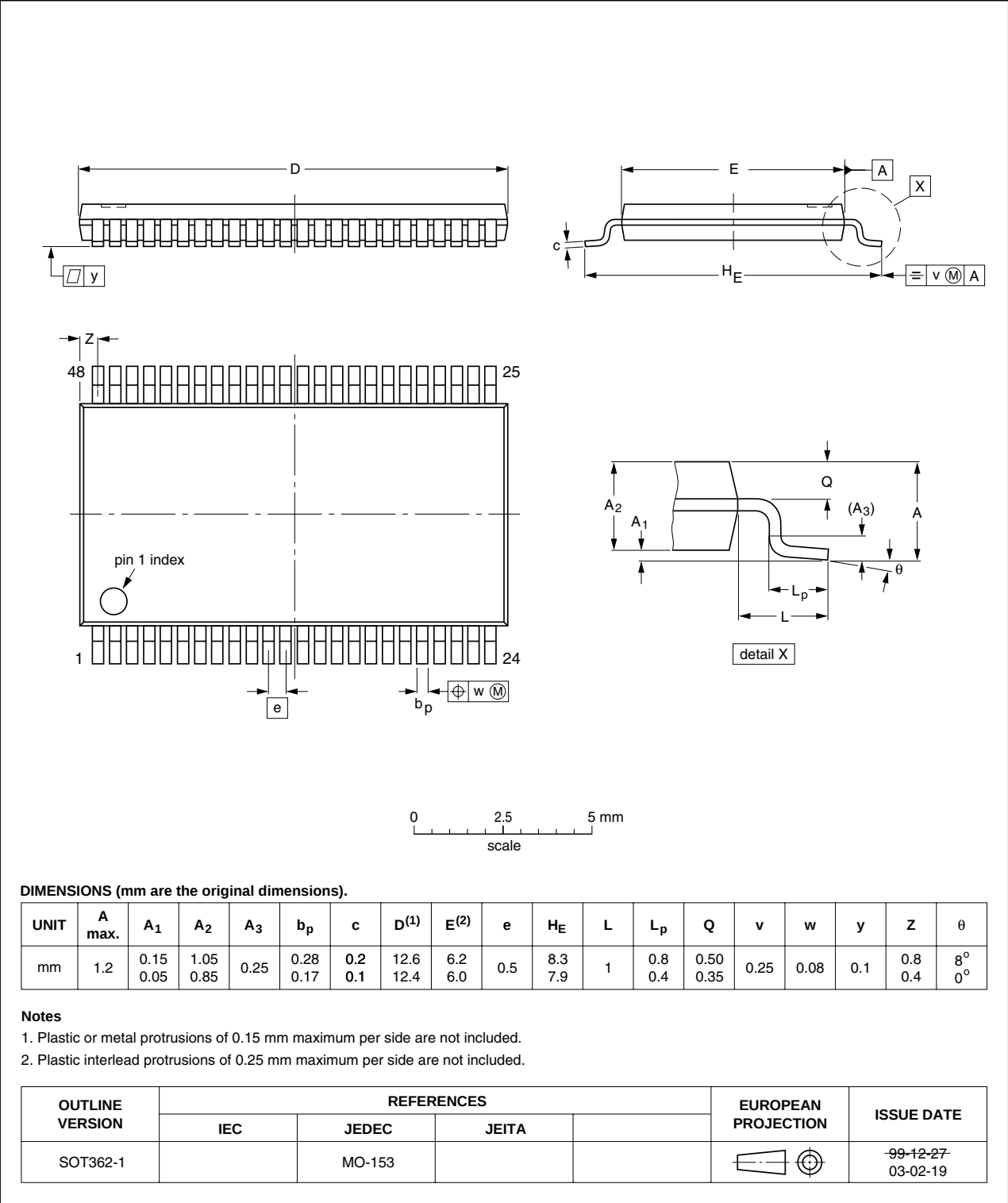


Fig 8. Package outline SOT362-1 (TSSOP48)

HXQFN60U: plastic thermal enhanced extremely thin quad flat package; no leads;

60 terminals; UTLP based; body 4 x 6 x 0.5 mm

SOT1134-1

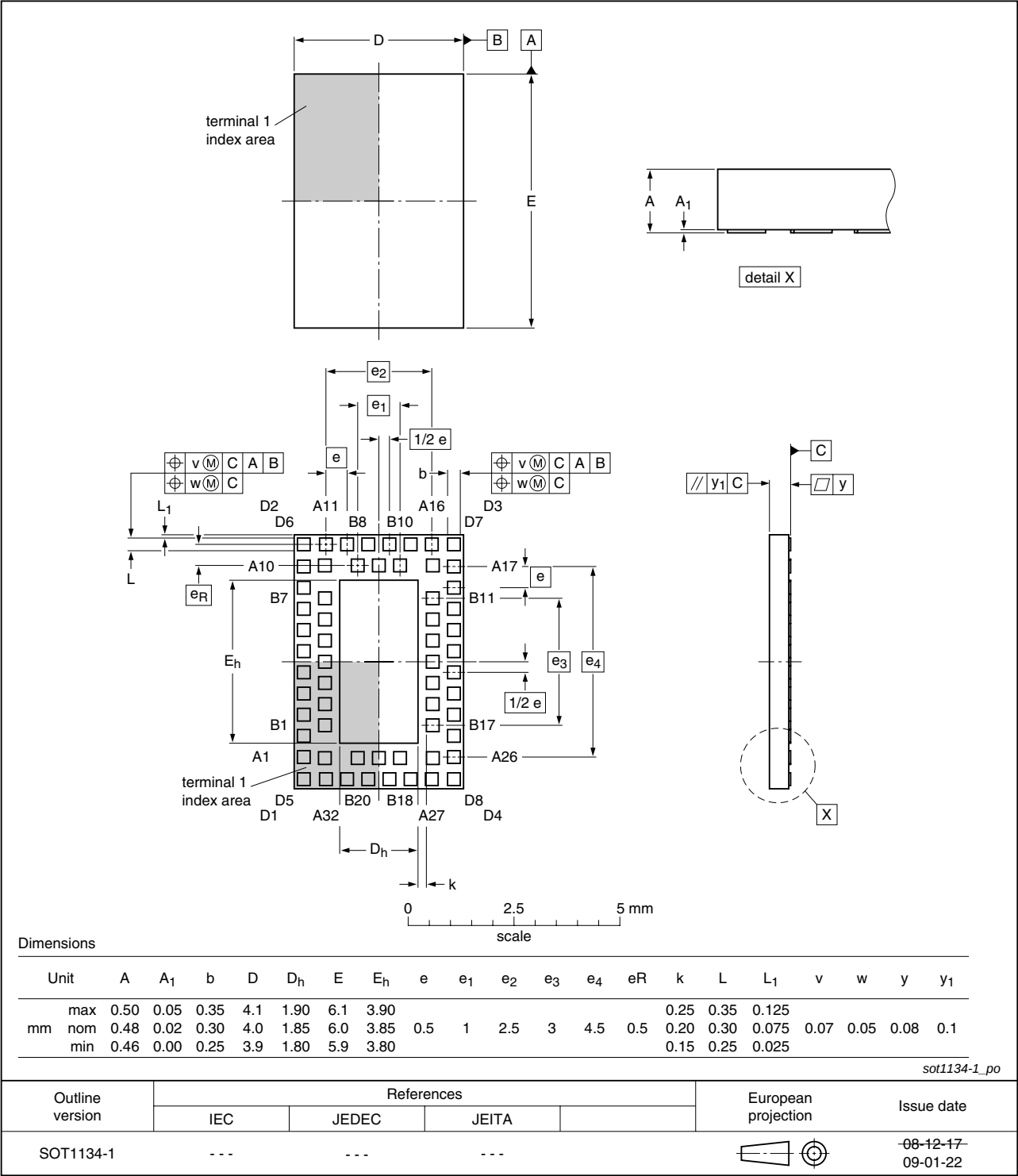


Fig 9. Package outline SOT1134-1 (HXQFN60U)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BICMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVTN16244B_2	20100323	Product data sheet	-	74LVTN16244B_1
Modifications:	74LVTN16244BBQ changed from HUQFN60U (SOT1025-1) to HXQFN60U (SOT1134-1) package.			
74LVTN16244B_1	20090713	Product data sheet	-	-

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Document status ^{[1][2]}	Product status ^[3]	Definition
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[2] The term 'short data sheet' is explained in section "Definitions".

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