



PUSBMxX4-TL series

High-speed USB OTG ESD protection diode arrays

Rev. 3 — 14 June 2012

Product data sheet

1. Product profile

1.1 General description

PUSBMxX4-TL is a series of four 4-channel ElectroStatic Discharge (ESD) diode arrays for USB 2.0 (On-The-Go (OTG)) interfaces. The devices provide protection to downstream components from ESD voltages up to ± 8 kV contact discharge. They offer three low capacitance ESD protection pins and one V_{BUS} protection diode. They are encapsulated in an ultra thin DFN1616-6 (SOT1189-1/XSON6) plastic package with 0.5 mm pitch. These features make the devices ideal for use in applications requiring component miniaturization, such as mobile phone handsets.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) and Dark Green compliant
- ESD protection according to IEC 61000-4-2 level 4: ± 8 kV contact discharge
- Electrical Fast Transients (EFT) protection according to IEC 61000-4-4 40A (5/50 ns)
- Three pairs of ultra low capacitance (1.1 pF typ.) rail-to-rail ESD protection diodes
- Ultra thin DFN1616-6 (SOT1189-1/XSON6) plastic package; 0.5 mm pitch

1.3 Applications

High-speed USB 2.0 and USB OTG connector ESD protection in:

- Cellular phone and Personal Communication System (PCS) mobile handsets
- Mobile internet devices
- Digital still cameras
- Portable media players

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	low capacitance ESD protection	Transparent top view	018aaa140
2	low capacitance ESD protection		
3	low capacitance ESD protection		
4	not connected		
5	not connected		
6	V_{BUS} ESD protection		
7	ground (GND)		



3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PUSBM5V5X4-TL	DFN1616-6	plastic, thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.6 × 1.6 × 0.5 mm	SOT1189-1
PUSBM12VX4-TL			
PUSBM15VX4-TL			
PUSBM30VX4-TL			

4. Marking

Table 3. Marking codes

Type number	Marking code
PUSBM5V5X4-TL	XE
PUSBM12VX4-TL	XL
PUSBM15VX4-TL	XO
PUSBM30VX4-TL	30

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{RWM}	reverse standoff voltage	pins 1, 2, 3	-0.5	+5.5	V
		PUSBM5V5X4-TL pin 6 (V_{BUS})	-0.5	+5.5	V
		PUSBM12VX4-TL pin 6 (V_{BUS})	-0.5	+12	V
		PUSBM15VX4-TL pin 6 (V_{BUS})	-0.5	+15	V
		PUSBM30VX4-TL pin 6 (V_{BUS})	-0.5	+30	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; pins 1, 2, 3, 6 to GND; [1] contact discharge	-	± 8	kV
P_{PP}	peak pulse power	$t_p = 8/20 \mu s$			
		pins 1, 2, 3; $V_{CL} = 12$ V	-	35	W
		PUSBM5V5X4-TL pin 6 (V_{BUS}); $V_{CL} = 9.2$ V	-	100	W
		PUSBM12VX4-TL pin 6 (V_{BUS}); $V_{CL} = 16$ V	-	100	W
		PUSBM15VX4-TL pin 6 (V_{BUS}); $V_{CL} = 22$ V	-	100	W
		PUSBM30VX4-TL pin 6 (V_{BUS}); $V_{CL} = 43$ V	-	100	W
I_{PP}	peak pulse current	$t_p = 8/20 \mu s$			
		pins 1, 2, 3	-	3	A
		PUSBM5V5X4-TL pin 6 (V_{BUS})	-	12	A
		PUSBM12VX4-TL pin 6 (V_{BUS})	-	6	A
		PUSBM15VX4-TL pin 6 (V_{BUS})	-	3	A
		PUSBM30VX4-TL pin 6 (V_{BUS})	-	2	A

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{\text{reflow(peak)}}$	peak reflow temperature	$t_p \leq 10$ s	-	+260	°C
T_{amb}	ambient temperature		-30	+85	°C
T_{stg}	storage temperature		-55	+150	°C

[1] Device is qualified with 1000 pulses of ± 8 kV contact discharges each, according to IEC61000-4-2 far exceeding level 4 (± 8 kV contact discharge).

6. Characteristics

Table 5. Characteristics $T_{\text{amb}} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_F	forward voltage		0.6	-	1.2	V
Low capacitance ESD protection						
V_{BRzd}	Zener diode breakdown voltage	$I_{\text{test}} = 1$ mA	6	-	10	V
$C_{(\text{I/O-GND})}$	input/output to ground capacitance	$V_{\text{bias(DC)}} = 0.5$ V; $f = 1$ MHz; pins 1, 2, 3 to GND	[1] -	1.1	1.3	pF
$\Delta C_{(\text{I/O-GND})}$	input/output to ground capacitance variation	$V_{\text{bias(DC)}} = 0.5$ V; $f = 1$ MHz	-	0.02	-	pF
$C_{(\text{I/O-I/O})}$	input/output to input/output capacitance	$V_{\text{bias(DC)}} = 0.5$ V; $f = 1$ MHz; pins 1 to 2, 1 to 3, 2 to 3	-	0.5	-	pF
I_{RM}	reverse leakage current	pins 1, 2, 3 to GND; $V_{\text{RWM}} = 5.5$ V	-	100	1000	nA
V_{BUS} ESD protection						
V_{BR}	breakdown voltage	pin 6 (V_{BUS}) to GND; $I_{\text{test}} = 1$ mA				
	PUSBM5V5X4-TL		6.4	6.8	7.2	V
	PUSBM12VX4-TL		12.5	14.5	16	V
	PUSBM15VX4-TL		17	18	19	V
	PUSBM30VX4-TL		32	36	40	V
C_d	diode capacitance	$V_{\text{bias(DC)}} = 0.5$ V; $f = 1$ MHz; pin 6 (V_{BUS}) to GND				
	PUSBM5V5X4-TL		-	165	220	pF
	PUSBM12VX4-TL		-	73	100	pF
	PUSBM15VX4-TL		-	60	90	pF
	PUSBM30VX4-TL		-	50	70	pF
I_{RM}	reverse leakage current	pin 6 (V_{BUS}) to GND				
	PUSBM5V5X4-TL	$V_{\text{RWM}} = 5.5$ V	-	200	500	nA
	PUSBM12VX4-TL	$V_{\text{RWM}} = 12$ V	-	1	100	nA
	PUSBM15VX4-TL	$V_{\text{RWM}} = 15$ V	-	1	100	nA
	PUSBM30VX4-TL	$V_{\text{RWM}} = 30$ V	-	1	100	nA

[1] Guaranteed by design.

7. Application information

7.1 Typical application

The devices are designed to protect USB interfaces from downstream ESD. They offer three low capacitance ESD protection channels for D⁻, D⁺ and ID and a high-voltage ESD protection channel for V_{BUS}.

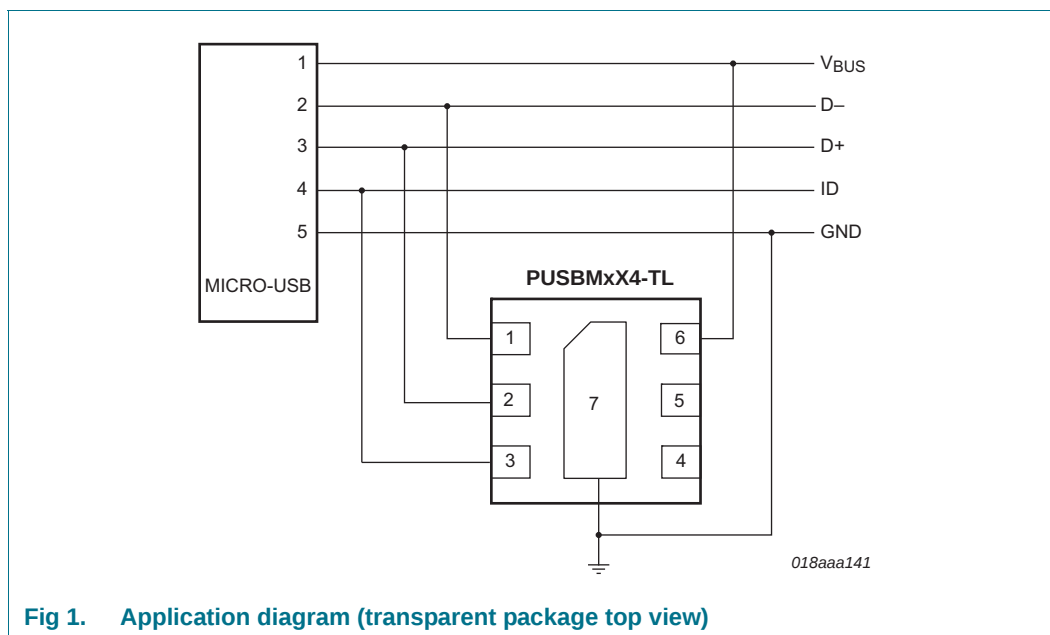


Fig 1. Application diagram (transparent package top view)

7.2 Insertion loss

The setup for measuring frequency response curves in a 50 Ω system is shown in [Figure 2](#). The frequency response curves for the low capacitance ESD protection channels (pins 1 to 3) are depicted in [Figure 3](#).

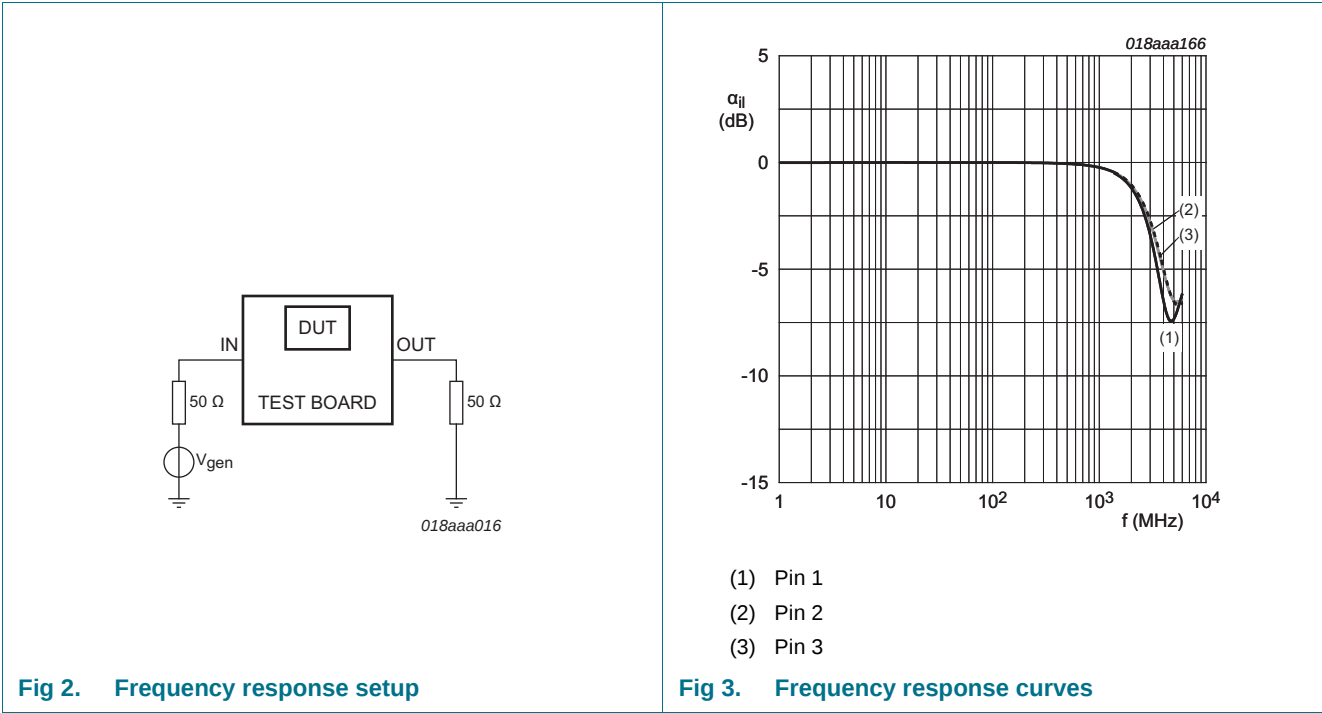


Fig 2. Frequency response setup

Fig 3. Frequency response curves

8. Package outline

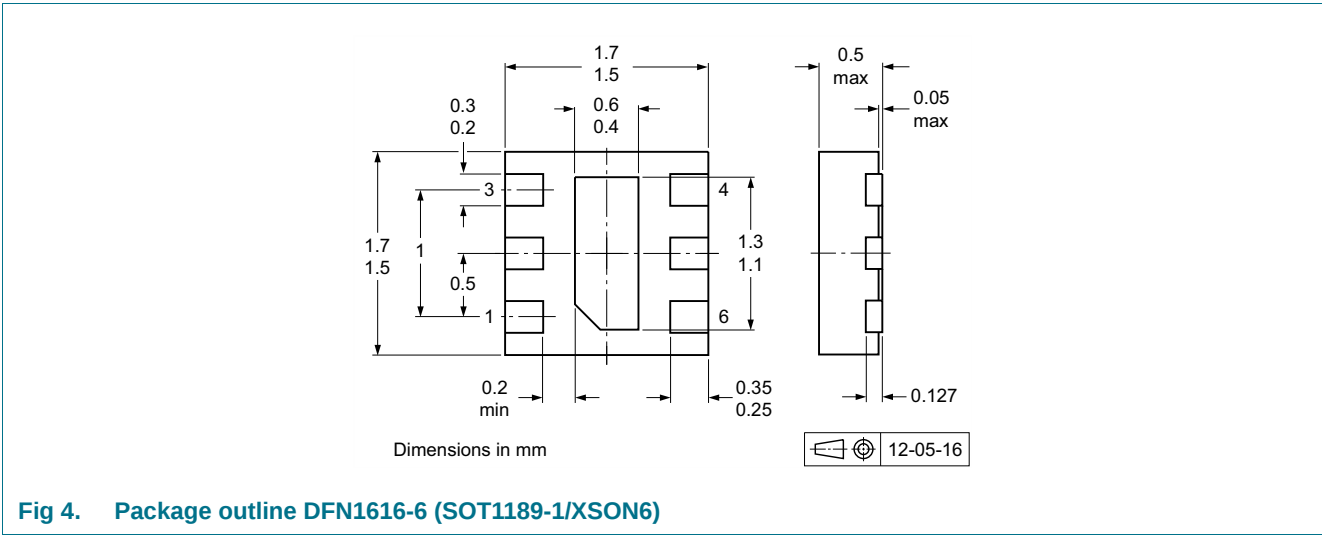


Fig 4. Package outline DFN1616-6 (SOT1189-1/XSON6)

9. Soldering

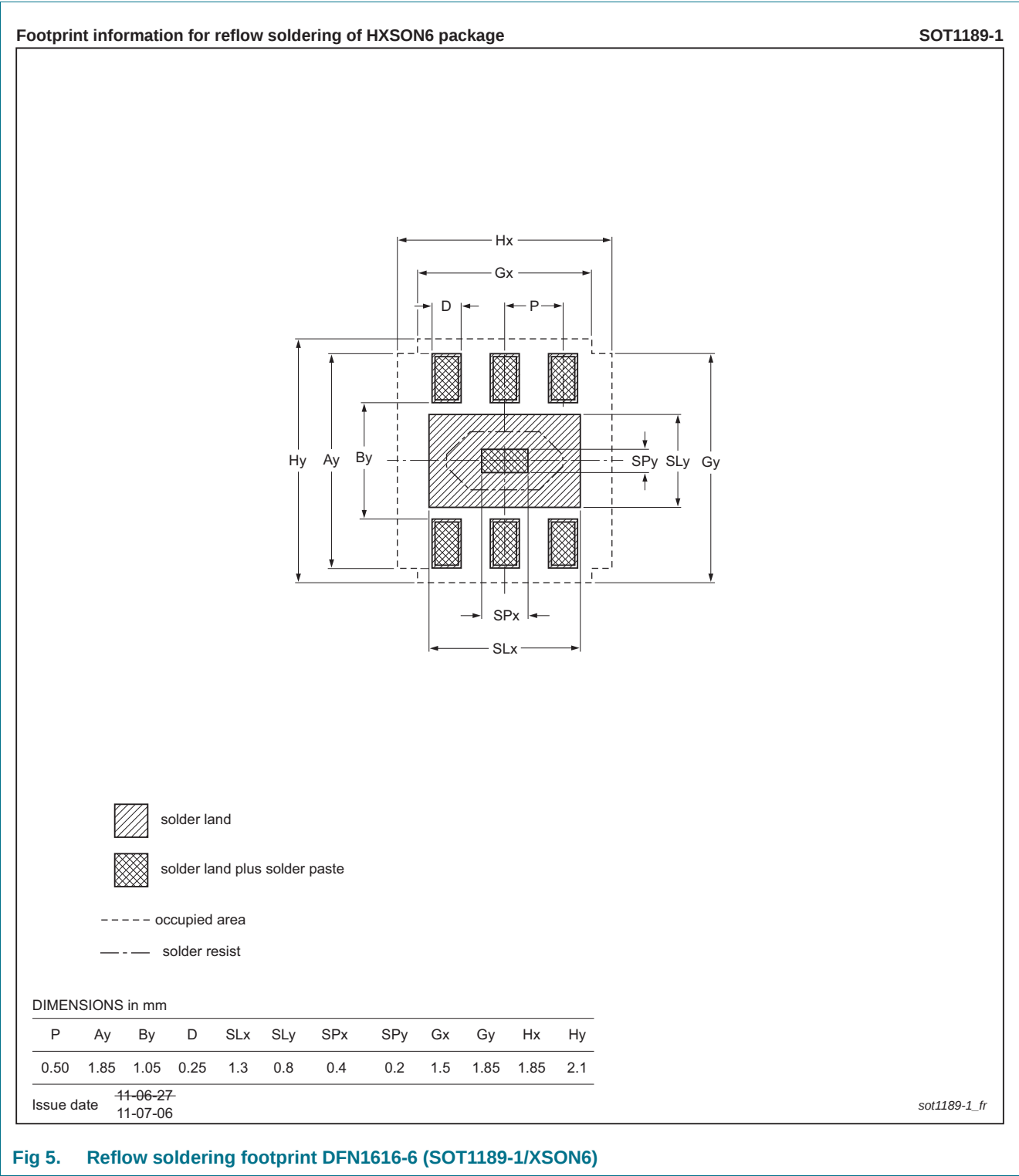


Fig 5. Reflow soldering footprint DFN1616-6 (SOT1189-1/XSON6)

10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSBMXX4-TL_SER v.3	20120614	Product data sheet	-	PUSBMXX4-TL_SER v.2
Modifications:				
• Section 2 "Pinning information": simplified outline graph updated • Figure 1 updated • Figure 4 replaced by minimized package outline				
PUSBMXX4-TL_SER v.2	20120416	Preliminary data sheet	-	PUSBMXX4-TL_SER v.1
PUSBMXX4-TL_SER v.1	20111209	Preliminary data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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