

The ABLIC Inc. HDL6V5541HF is a quad, five-level RTZ, high-voltage, ultra high-speed pulser. The HDL6V5541HF consists of logic interfaces, level translators, MOSFET gate drive buffers, and high-voltage, high-current MOSFETs.

Functions

- Quad 5-level pulser with 3-input per channel

Features

- 0 to $\pm 100\text{V}$ output voltage
- $\pm 2.5\text{A}$ source and sink peak current for the 1st and 2nd high-voltage pulses (V_{PP1}/V_{NN1} , V_{PP2}/V_{NN2})
- $\pm 1.0\text{A}$ source and sink peak current for active ground clamp
- 500Ω ($\pm 50\text{mA}$) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- 15V/ns output slew rate
- Up to 100MHz CMOS clock (transparent mode available)
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- 1.8V to 5V CMOS logic interface
- Noise-cut diodes at each high-voltage output
- Embedded high-voltage clamp diodes
- 4-mode output current control for the 2nd high-voltage rail
- Automatic thermal protection with indicator
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 64-lead $9\times 9\text{mm}$ QFN package (RoHS compliant)

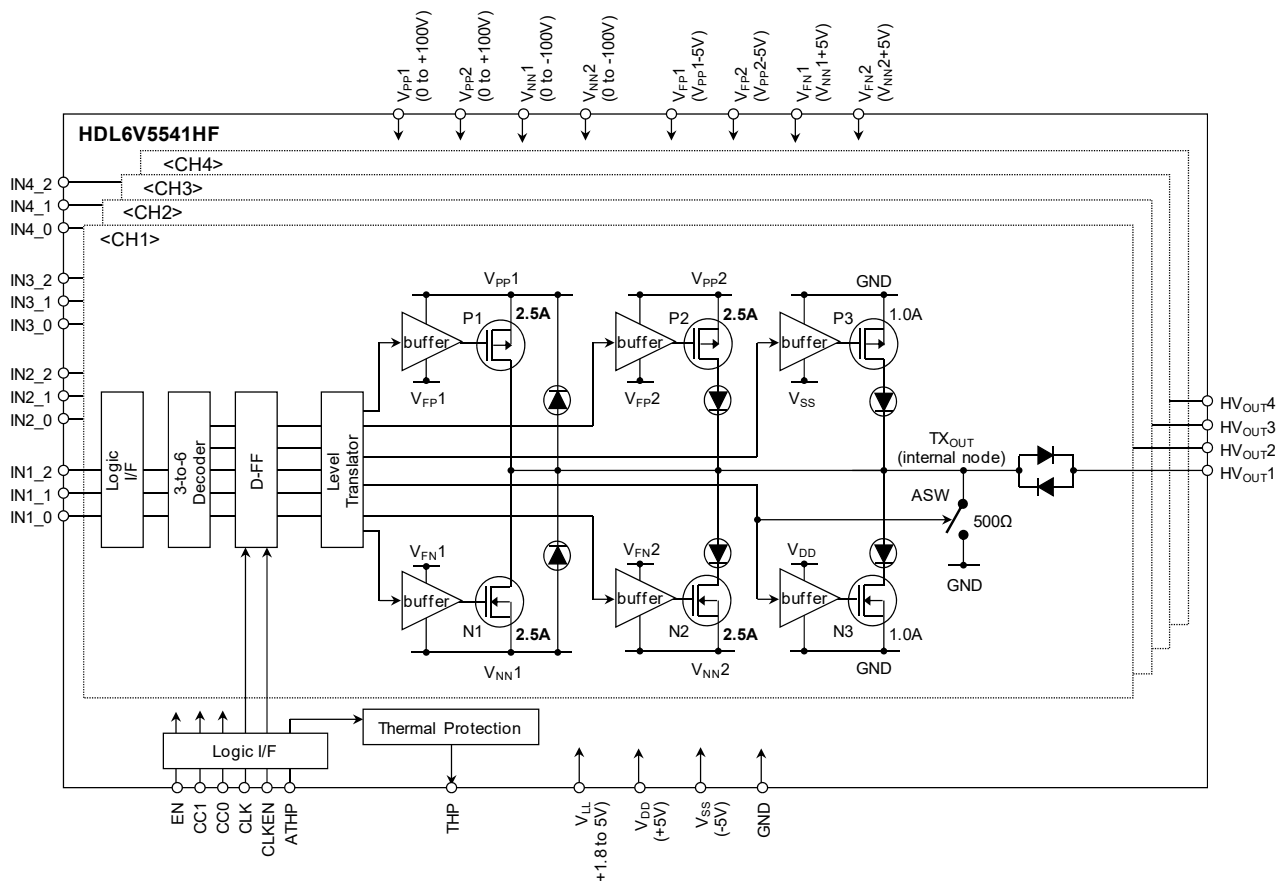


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V _{LL}	-0.4 to +7	V	
2	Positive supply voltage	V _{DD}	-0.4 to +7	V	
3	Negative supply voltage	V _{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	V _{PP1} , V _{PP2}	-0.5 to +105	V	
5	Negative high-voltage supplies	V _{NN1} , V _{NN2}	-105 to +0.5	V	
6	Positive high-voltage difference	(V _{PP1} -V _{PP2})	-0.5 to +105	V	INx_[2:0]='001'
			-105 to +105	V	Other than above
7	Negative high-voltage difference	(V _{NN1} -V _{NN2})	-105 to +0.5	V	INx_[2:0]='101'
			-105 to +105	V	Other than above
8	High-voltage outputs (x=1~4)	HV _{OUTX}	-105 to +105	V	
9	Gate drive floating voltages	(V _{PP1} - V _{FP1}), (V _{PP2} - V _{FP2}), (V _{FN1} - V _{NN1}), (V _{FN2} - V _{NN2})	-0.4 to +7	V	
10	THP (Thermal Protection) output	THP	-0.4 to +7	V	
11	All Logic input voltages (x=1~4)	INx_[2:0], EN, CLK, CLKEN, CC1, CC0, ATHP	-0.4 to +7	V	
12	Operating junction temperature	T _{Jop}	-20 to +150	°C	
13	Storage temperature	T _{STG}	-55 to +150	°C	
14	Maximum power dissipation	P _{Dmax}	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Temperature, Logic Inputs, and Power sequencing

2.1 Operating Supply Voltages and Temperature

Table 2 Operating Supply Voltages and Temperature

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V _{LL}	2.4	2.5 to 5	V _{DD}	V	CLK mode (CLK≤80MHz)
			2.6	2.7 to 5	V _{DD}	V	CLK mode (CLK≤100MHz)
			1.7	1.8 to 5	V _{DD}	V	TP mode (f _{OUT} ≤20MHz)
			2.4	2.5 to 5	V _{DD}	V	TP mode (f _{OUT} ≥20MHz)
2	Positive supply voltage	V _{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V _{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	V _{PP1} , V _{PP2}	0	-	100	V	
5	Negative high-voltage supplies	V _{NN1} , V _{NN2}	-100	-	0	V	
6	Positive high-voltage difference	(V _{PP1} -V _{PP2})	0	-	100	V	
7	Negative high-voltage difference	(V _{NN1} -V _{NN2})	-100	-	0	V	

Table 2 Operating Supply Voltages and Temperature (continued)

No	Items	Symbol	Min	Typ	Max	Units	Condition
8	P1 gate drive floating voltage	V _{FP1}	V _{PP1} -5.25	V _{PP1} -5	V _{PP1} -4.75	V	
9	P2 gate drive floating voltage	V _{FP2}	V _{PP2} -5.25	V _{PP2} -5	V _{PP2} -4.75	V	
10	N1 gate drive floating voltage	V _{FN1}	V _{NN1} +4.75	V _{NN1} +5	V _{NN1} +5.25	V	
11	N2 gate drive floating voltage	V _{FN2}	V _{NN2} +4.75	V _{NN2} +5	V _{NN2} +5.25	V	
12	IC substrate voltage *	V _{SUB}	-	0	-	V	
13	V _{PPX} , V _{NNX} slew rate (x=1,2)	SR _{MAX}	-	-	25	V/ms	
14	Operating Free-air Temperature	T _A	0	25	75	°C	

NOTE: * The package exposed pad internally connected to the IC substrate must be soldered to the ground.

2.2 Logic Inputs

There are two modes, transparent(TP) and clock(CLK) mode, to deal with the logic inputs IN_x_[2:0] (x=1~4).

TP mode:

Set CLKEN=1, CLK=0. IN_x_[2:0] are decoded, level-translated, then sent to high-voltage output stage. See table 3 for all the logic inputs.

CLK mode:

Set CLKEN=0. IN_x_[2:0] are decoded, clocked, level-translated, then sent to high-voltage output stage. See table 3 for all the logic inputs.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level logic input voltage	V _{IH}	0.8V _{LL}	-	V _{LL}	V	
2	Low-level logic input voltage	V _{IL}	0	-	0.2V _{LL}	V	
3	Logic input capacitance	C _{IN}	-	2	-	pF	
4	Logic input high current *1	I _{IH}	-10	-	10	μA	
5	Logic input low current *2	I _{IL}	-10	-	10	μA	
6	Logic input pulse width	t _{pw}	10	-	-	ns	
7	Input rise/fall time	t _r , t _f	-	-	2.0	ns	10% to 90% CLK, IN _x _[2:0] CLK mode, CLK≤100MHz
8	Input clock frequency	f _{CLK}	-	-	100	MHz	CLK mode, CLK
9	Duty cycle	D	40	50	60	%	D=τ/T, See Fig.2
10	Data setup time	t _{su}	0.8	-	-	ns	CLK mode IN _x _[2:0], See Fig.2
11	Data hold time	t _{hld}	2.8	-	-	ns	

NOTE:

*1) ATHP has 50μA leak at V_{LL}=2.5V due to 50kΩ internal pull-down resistor.

*2) EN, CC[1:0], and CLKEN have 50μA leak at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

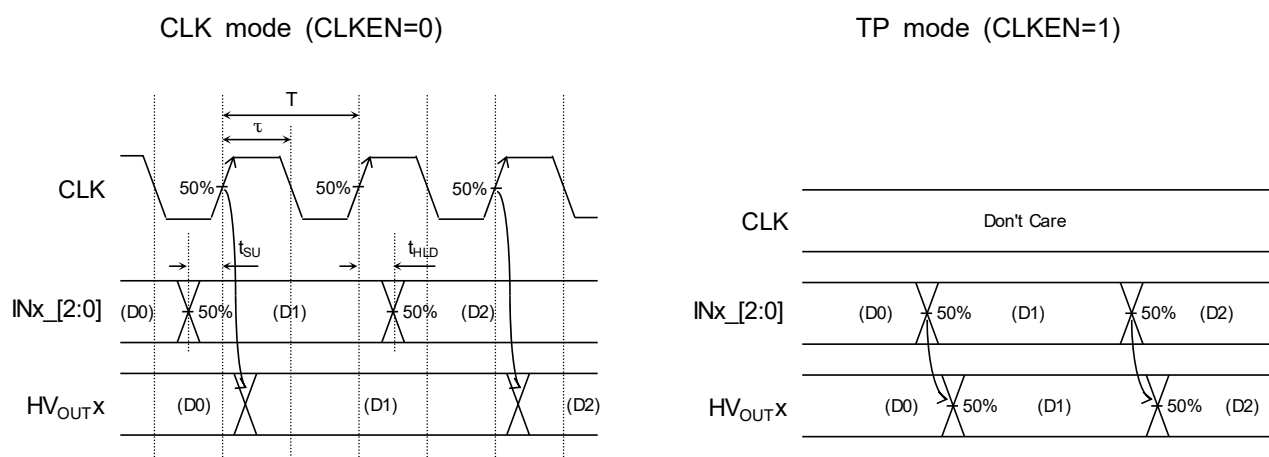


Fig.2 Setup/Hold Time

2.3 Power Supply Sequencing

Table 4 Power Supply Sequencing

Power-Up Sequence

1	V_{LL}
2	V_{DD} , V_{SS}
3	Set EN=1 (HV_{OUTX} =HiZ)
4	(V_{PP1} - V_{FP1}), (V_{PP2} - V_{FP2}), (V_{FN1} - V_{NN1}), (V_{FN2} - V_{NN2})
5	V_{PP1} , V_{PP2} , V_{NN1} , V_{NN2}
6	Logic control signals

Power-Down Sequence

1	Set EN=1 (HV_{OUTX} =HiZ)
2	V_{PP1} , V_{PP2} , V_{NN1} , V_{NN2}
3	(V_{PP1} - V_{FP1}), (V_{PP2} - V_{FP2}), (V_{FN1} - V_{NN1}), (V_{FN2} - V_{NN2})
4	V_{DD} , V_{SS}
5	V_{LL}

High-voltage Change Sequence during operation

1	Set EN=1 (HV_{OUTX} =HiZ)
2	Change V_{PP1} , V_{PP2} , V_{NN1} , V_{NN2}
3	Logic control signals

NOTE: It is indispensable to avoid the occurrence of the excessive voltage beyond the maximum rating in applying and cutting of the power supplies.

3. Typical Application Circuit

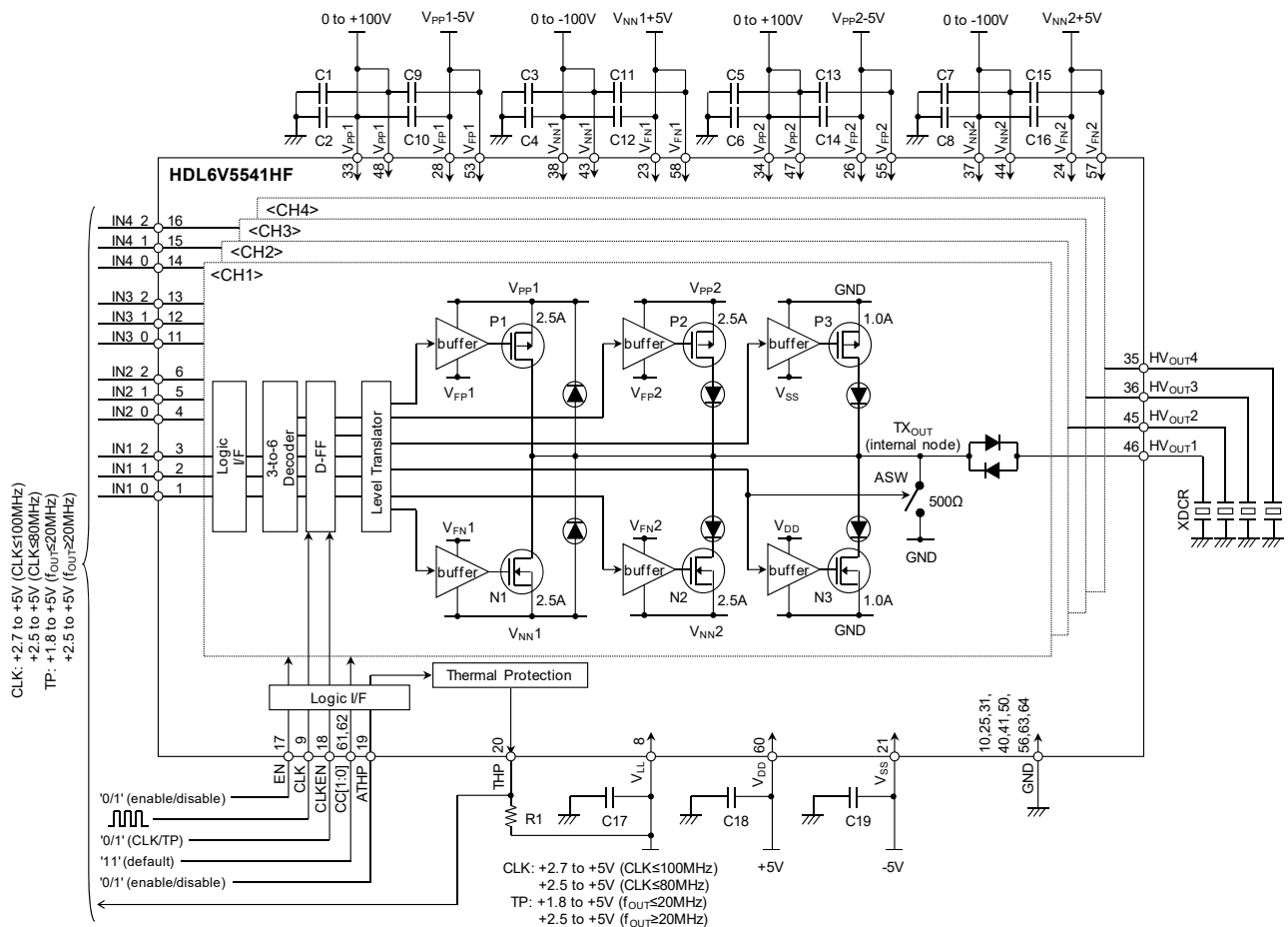


Fig. 3 Typical Application Circuit

NOTE:

1. High-voltage power supply pins, V_{PPX}/V_{NNX} ($x=1,2$), can draw fast transient currents up to $\pm 2.5A$. Therefore, ceramic capacitors of $\geq 200V$ $0.1\mu F$ to $1\mu F$ (C1~8) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of $\geq 16V$ $0.1\mu F$ to $1\mu F$ (C9~19) also should be connected between high-voltage power supply pins and corresponding floating voltage pins, V_{FPX}/V_{FNX} , and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.

4. Electrical Characteristics

4.1 Operating Supply Currents

Table 5 Operating Supply Currents

$V_{LL}=2.5V$, $V_{DD}=5V$, $V_{SS}=-5V$, $V_{FPX}=V_{PPX}-5V$, $V_{FNX}=V_{NNX}+5V$, $T_A=25^{\circ}C$, $CLK=100MHz/0(CLKEN=0/1)$, $ATHP=0$, HV_{OUT} load=220pF//200 Ω , unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	V_{LL} current	TP mode	I_{LLQD}	-	0	-	μA	Quiescent current-1 EN=1(Disable) INx_[2:0]='000' Current mode 4 (CC[1:0]='11') $V_{PP1}/V_{NN1}=+/-100V$ $V_{PP2}/V_{NN2}=+/-100V$
		CLK mode		-	0.7	-	mA	
2	V_{DD} current	TP mode	I_{DDQD}	-	0.7	-	mA	
		CLK mode		-	12	-	mA	
3	V_{SS} current		I_{SSQD}	-	0.10	-	mA	
4	V_{PP1} current		I_{PP1QD}	-	0	-	μA	
5	V_{NN1} current		I_{NN1QD}	-	0	-	μA	
6	V_{PP2} current		I_{PP2QD}	-	0.13	-	mA	
7	V_{NN2} current		I_{NN2QD}	-	0.10	-	mA	
8	V_{FP1} current		I_{FP1QD}	-	0	-	μA	
9	V_{FP2} current		I_{FP2QD}	-	0.07	-	mA	
10	V_{FN1} current		I_{FN1QD}	-	0	-	μA	
11	V_{FN2} current		I_{FN2QD}	-	0.04	-	mA	
12	V_{LL} current	TP mode	I_{LLQE}	-	0.06	-	mA	Quiescent current-2 EN=0(Enable) INx_[2:0]='000' Current mode 4 (CC[1:0]='11') $V_{PP1}/V_{NN1}=+/-100V$ $V_{PP2}/V_{NN2}=+/-100V$
		CLK mode		-	0.75	-	mA	
13	V_{DD} current	TP mode	I_{DDQE}	-	0.7	-	mA	
		CLK mode		-	12	-	mA	
14	V_{SS} current		I_{SSQE}	-	0.10	-	mA	
15	V_{PP1} current		I_{PP1QE}	-	0	-	μA	
16	V_{NN1} current		I_{NN1QE}	-	0	-	μA	
17	V_{PP2} current		I_{PP2QE}	-	0.13	-	mA	
18	V_{NN2} current		I_{NN2QE}	-	0.10	-	mA	
19	V_{FP1} current		I_{FP1QE}	-	0	-	μA	
20	V_{FP2} current		I_{FP2QE}	-	0.07	-	mA	
21	V_{FN1} current		I_{FN1QE}	-	0	-	μA	
22	V_{FN2} current		I_{FN2QE}	-	0.04	-	mA	

Table 5 Operating Supply Currents (continued)

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
23	V _{LL} current	TP mode	I _{LLPW}	-	0.06	-	mA	PW Operating current EN=0 Current mode 4 (CC[1:0]='11') 4-channel active Bipolar 3-level 2-cycle f=5MHz, PRT=200μs V _{PP1} /V _{NN1} =+/-60V V _{PP2} /V _{NN2} =+/-60V
		CLK mode		-	0.75	-	mA	
24	V _{DD} current	TP mode	I _{DDPW}	-	2.5	-	mA	
		CLK mode		-	14	-	mA	
25	V _{SS} current		I _{SSPW}	-	2.1	-	mA	
26	V _{PP1} current		I _{PP1PW}	-	2.2	-	mA	
27	V _{NN1} current		I _{NN1PW}	-	2.5	-	mA	
28	V _{PP2} current		I _{PP2PW}	-	0.13	-	mA	
29	V _{NN2} current		I _{NN2PW}	-	0.10	-	mA	
30	V _{FP1} current		I _{FP1PW}	-	0.08	-	mA	
31	V _{FP2} current		I _{FP2PW}	-	0.07	-	mA	
32	V _{FN1} current		I _{FN1PW}	-	0.05	-	mA	
33	V _{FN2} current		I _{FN2PW}	-	0.04	-	mA	
34	V _{LL} current	TP mode	I _{LLCW4}	-	0.25	-	mA	CW Operating current-1 EN=0 Current mode 4 (CC[1:0]='11') 4-channel active Bipolar 3-level Continuous f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		CLK mode		-	1.3	-	mA	
35	V _{DD} current	TP mode	I _{DDCW4}	-	7	-	mA	
		CLK mode		-	19	-	mA	
36	V _{SS} current		I _{SSCW4}	-	4.8	-	mA	
37	V _{PP1} current		I _{PP1CW4}	-	0	-	μA	
38	V _{NN1} current		I _{NN1CW4}	-	0	-	μA	
39	V _{PP2} current		I _{PP2CW4}	-	170	-	mA	
40	V _{NN2} current		I _{NN2CW4}	-	158	-	mA	
41	V _{FP1} current		I _{FP1CW4}	-	0	-	μA	
42	V _{FP2} current		I _{FP2CW4}	-	30	-	mA	
43	V _{FN1} current		I _{FN1CW4}	-	0	-	μA	
44	V _{FN2} current		I _{FN2CW4}	-	18	-	mA	
45	V _{LL} current	TP mode	I _{LLCW3}	-	0.25	-	mA	CW Operating current-2 EN=0 Current mode 3 (CC[1:0]='10') 4-channel active Bipolar 3-level Continuous f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		CLK mode		-	1.3	-	mA	
46	V _{DD} current	TP mode	I _{DDCW3}	-	7.2	-	mA	
		CLK mode		-	19	-	mA	
47	V _{SS} current		I _{SSCW3}	-	5.7	-	mA	
48	V _{PP1} current		I _{PP1CW3}	-	0	-	μA	
49	V _{NN1} current		I _{NN1CW3}	-	0	-	μA	
50	V _{PP2} current		I _{PP2CW3}	-	150	-	mA	
51	V _{NN2} current		I _{NN2CW3}	-	143	-	mA	
52	V _{FP1} current		I _{FP1CW3}	-	0	-	μA	
53	V _{FP2} current		I _{FP2CW3}	-	22	-	mA	
54	V _{FN1} current		I _{FN1CW3}	-	0	-	μA	
55	V _{FN2} current		I _{FN2CW3}	-	14	-	mA	

Table 5 Operating Supply Currents (continued)

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
56	V _{LL} current	TP mode	I _{LLCW2}	-	0.26	-	mA	CW Operating current-3 EN=0 Current mode 2 (CC[1:0]='01') 4-channel active Bipolar 3-level Continuous f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		CLK mode		-	1.3	-	mA	
57	V _{DD} current	TP mode	I _{DDCW2}	-	7.2	-	mA	
		CLK mode		-	19	-	mA	
58	V _{SS} current		I _{SSCW2}	-	4.7	-	mA	
59	V _{PP1} current		I _{PP1CW2}	-	0	-	μ A	
60	V _{NN1} current		I _{NN1CW2}	-	0	-	μ A	
61	V _{PP2} current		I _{PP2CW2}	-	133	-	mA	
62	V _{NN2} current		I _{NN2CW2}	-	130	-	mA	
63	V _{FP1} current		I _{FP1CW2}	-	0	-	μ A	
64	V _{FP2} current		I _{FP2CW2}	-	15	-	mA	
65	V _{FN1} current		I _{FN1CW2}	-	0	-	μ A	
66	V _{FN2} current		I _{FN2CW2}	-	10	-	mA	
67	V _{LL} current	TP mode	I _{LLCW1}	-	0.31	-	mA	CW Operating current-4 EN=0 Current mode 1 (CC[1:0]='00') 4-channel active Bipolar 3-level Continuous f=5MHz V _{PP1} /V _{NN1} =+/-5V V _{PP2} /V _{NN2} =+/-5V
		CLK mode		-	1.4	-	mA	
68	V _{DD} current	TP mode	I _{DDCW1}	-	7.2	-	mA	
		CLK mode		-	19	-	mA	
69	V _{SS} current		I _{SSCW1}	-	4.7	-	mA	
70	V _{PP1} current		I _{PP1CW1}	-	0	-	μ A	
71	V _{NN1} current		I _{NN1CW1}	-	0	-	μ A	
72	V _{PP2} current		I _{PP2CW1}	-	111	-	mA	
73	V _{NN2} current		I _{NN2CW1}	-	111	-	mA	
74	V _{FP1} current		I _{FP1CW1}	-	0	-	μ A	
75	V _{FP2} current		I _{FP2CW1}	-	7.9	-	mA	
76	V _{FN1} current		I _{FN1CW1}	-	0	-	μ A	
77	V _{FN2} current		I _{FN2CW1}	-	5.3	-	mA	

4.2 Static Characteristics

Table 6 Static Characteristics

$V_{LL}=2.5V$, $V_{DD}=5V$, $V_{SS}=-5V$, $V_{FPX}=V_{PPX}-5V$, $V_{FNX}=V_{NNX}+5V$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output voltage range	HV_{OUTX}	-100	-	100	V	
2	High-side output peak current	I_{OH}	-	2.5	-	A	P1 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$
			-	2.5	-	A	P2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ Current mode 4 (CC[1:0]='11')
			-	1.88	-	A	P2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ Current mode 3 (CC[1:0]='10')
			-	1.25	-	A	P2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ Current mode 2 (CC[1:0]='01')
			-	0.63	-	A	P2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ Current mode 1 (CC[1:0]='00')
3	High-side GND clamp peak current	I_{OHCL}	-	1.0	-	A	N3 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$
4	Low-side output peak current	I_{OL}	-	2.5	-	A	N1 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$
			-	2.5	-	A	N2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ Current mode 4 (CC[1:0]='11')
			-	1.88	-	A	N2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ Current mode 3 (CC[1:0]='10')
			-	1.25	-	A	N2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ Current mode 2 (CC[1:0]='01')
			-	0.63	-	A	N2 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$ Current mode 1 (CC[1:0]='00')
5	Low-side GND clamp peak current	I_{OLCL}	-	1.0	-	A	P3 active, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$
6	High-side output on-resistance	R_{ONH}	-	9	-	Ω	P1 active, $I_{OH}=100mA$
			-	11	-	Ω	P2 active, $I_{OH}=100mA$ Current mode 4 (CC[1:0]='11')
			-	13	-	Ω	P2 active, $I_{OH}=100mA$ Current mode 3 (CC[1:0]='10')
			-	15	-	Ω	P2 active, $I_{OH}=100mA$ Current mode 2 (CC[1:0]='01')
			-	23	-	Ω	P2 active, $I_{OH}=100mA$ Current mode 1 (CC[1:0]='00')
7	High-side GND clamp on-resistance	R_{ONHCL}	-	17	-	Ω	N3 active, $I_{OHCL}=100mA$
8	Low-side output on-resistance	R_{ONL}	-	9	-	Ω	N1 active, $I_{OL}=100mA$
			-	11	-	Ω	N2 active, $I_{OL}=100mA$ Current mode 4 (CC[1:0]='11')
			-	13	-	Ω	N2 active, $I_{OL}=100mA$ Current mode 3 (CC[1:0]='10')
			-	15	-	Ω	N2 active, $I_{OL}=100mA$ Current mode 2 (CC[1:0]='01')
			-	23	-	Ω	N2 active, $I_{OL}=100mA$ Current mode 1 (CC[1:0]='00')
9	Low-side GND clamp on-resistance	R_{ONLCL}	-	17	-	Ω	P3 active, $I_{OLCL}=100mA$
10	Output off-capacitance	CH_{VOFF}	-	10	-	pF	$TX_{OUTX}=HiZ$

4.3 Dynamic Characteristics

Table 7 Dynamic Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $V_{FPX}=V_{PPX}-5V$, $V_{FNX}=V_{NNX}+5V$, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$, $T_A=25^{\circ}C$, $CC[1:0]='11'$, $EN=0$, $ATHP=0$, $CLK=100MHz/0$ ($CLKEN=0/1$), HV_{OUT} load= $220pF//200\Omega$, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions							
				Min	Typ	Max									
1	Output frequency		f _{OUT}	-	20	-	MHz	Bipolar, TP mode							
2	Output slew rate	P1/N1 drive	SR _{rP-P} , SR _{fP-P}	15	-	-	V/ns	50Ω load	V _{PP1} /V _{NN1} =±30V V _{PP2} /V _{NN2} =±30V Bipolar, 1-cyc f _{OUT} =20MHz See Fig.4						
				4.5	-	-		220pF//200Ω load							
		P2/N2 drive		12	-	-		50Ω load							
				3.3	-	-		220pF//200Ω load							
		P1/N1 drive	SR _{rO-P} , SR _{fO-P}	6	-	-		50Ω load							
				2	-	-		220pF//200Ω load							
		P2/N2 drive		6	-	-		50Ω load							
				2	-	-		220pF//200Ω load							
3	Output rise time	P1/N1 drive	t _r	-	2	-	ns	50Ω load	See Fig.4						
				-	6	-		220pF//200Ω load							
		P2/N2 drive		-	2	-		50Ω load							
				-	6	-		220pF//200Ω load							
4	Output fall time	P1/N1 drive	t _f	-	2	-	ns	50Ω load		See Fig.4					
				-	6	-		220pF//200Ω load							
		P2/N2 drive		-	2	-		50Ω load							
				-	6	-		220pF//200Ω load							
5	Output rise propagation delay	TP mode	t _{dr}	-	56	-	ns	V _{PP1} /V _{NN1} =±30V V _{PP2} /V _{NN2} =±30V Bipolar, 1-cyc f _{OUT} =20MHz See Fig.4							
		CLK mode		-	61	-	ns								
6	Output fall propagation delay	TP mode	t _{df}	-	56	-	ns				See Fig.4				
		CLK mode		-	61	-	ns								
7	Output rise propagation delay clamp	TP mode	t _{drCL}	-	56	-	ns			See Fig.4					
		CLK mode		-	61	-	ns								
8	Output fall propagation delay clamp	TP mode	t _{dfCL}	-	56	-	ns						See Fig.4		
		CLK mode		-	61	-	ns								
9	Propagation delay matching	Δt _d	-	±1	±3	ns	Bipolar, 2-cyc, f _{OUT} =5MHz See Fig.5								
10	Second harmonic distortion	HD2	-	-40	-	dBc									
11	Pulse cancellation	HDPC	-	-40	-	dBc									
		HDPC2	-	-40	-	dBc									
12	RMS output jitter		t _j	-	10	-	ps	Bipolar CW, f _{OUT} =5MHz V _{PP1} /V _{NN1} =V _{PP2} /V _{NN2} =+/-5V							
13	Output enable time		t _{EN}	-	61	-	ns	See Fig.6							
14	Output disable time		t _{DS}	-	61	-	ns								
15	Clock mode enable time		t _{CLKEN}	-	61	-	ns								
16	Clock mode disable time		t _{CLKDS}	-	61	-	ns								

4.4 Integrated Peripheral Circuits Characteristics

Analog Switch

Table 8 Analog Switch Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	ASW on-resistance	R _{ONASW}	-	500	-	Ω	

HV Blocking Diode

Table 9 Output HV Blocking Diode Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V _{FDHV}	-	1.0	-	V	I _F =100mA
2	Reverse voltage	V _{RDHV}	200	-	-	V	I _R =1μA

LV Noise-cut Diode

Table 10 Output LV Noise-cut Diode Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V _{FDNC}	-	0.85	-	V	I _F =100mA

Thermal Protection

Table 11 Thermal Protection Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V _{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I _{THP}	-	1.0	-	mA	
3	THP output low voltage	V _{OLTHP}	-	-	1.0	V	THP active, V _{LL} =3.3V, I _{THP} =1mA
4	THP temperature threshold	T _{THP}	90	110	130	°C	
5	THP reset hysteresis	T _{HYSTHP}	-	10	-	°C	

5. Switching Time Diagram

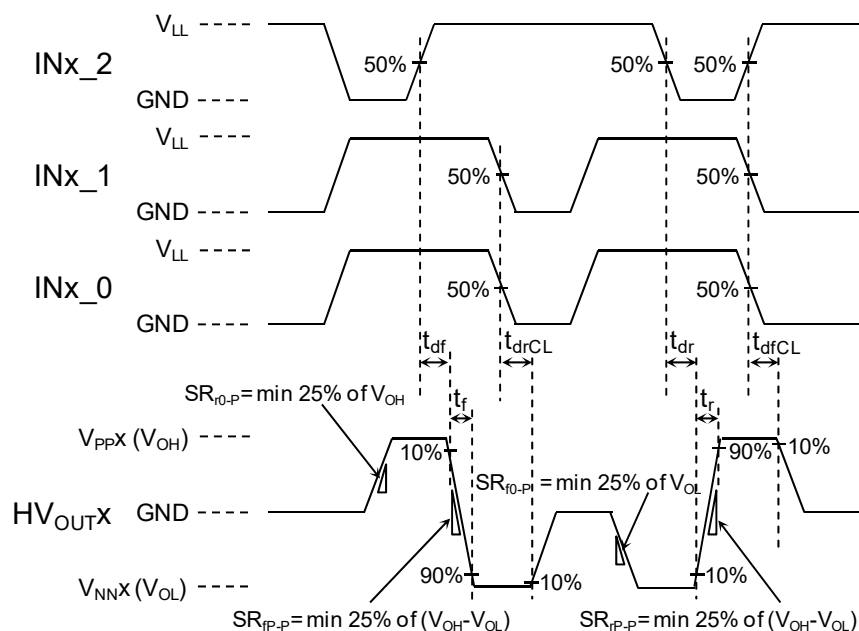
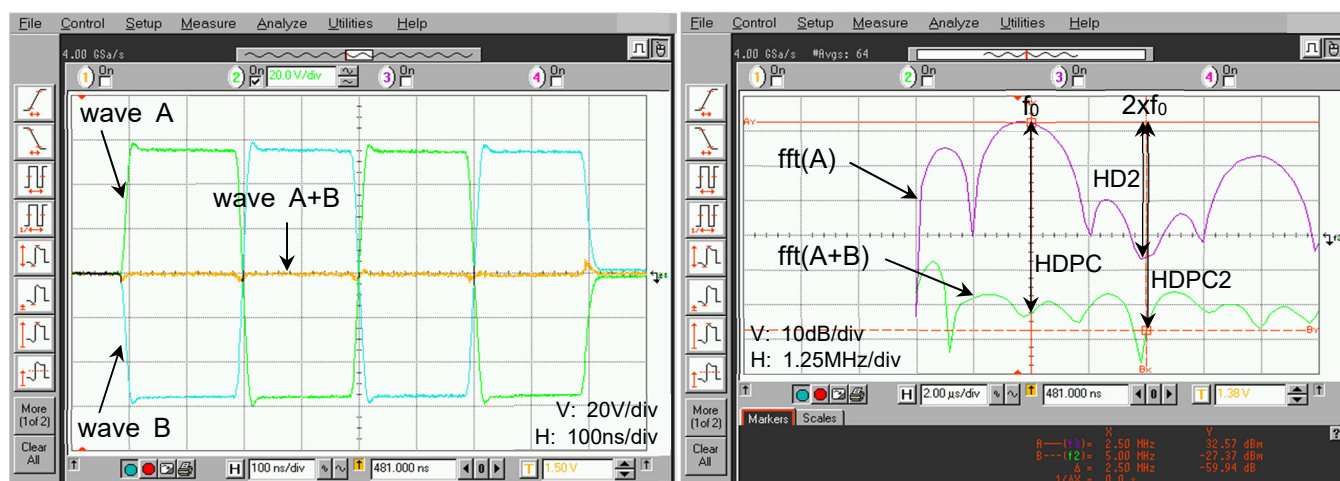


Fig. 4 Propagation delay and Output rise/fall time



Example waveforms: $V_{PP}/V_{NN} = \pm 60V$, $f_0 = 2.5MHz$, 2-cycle, HV_{OUT} load = 220pF//200 Ω

Fig.5 2nd harmonic distortion and Pulse cancellation

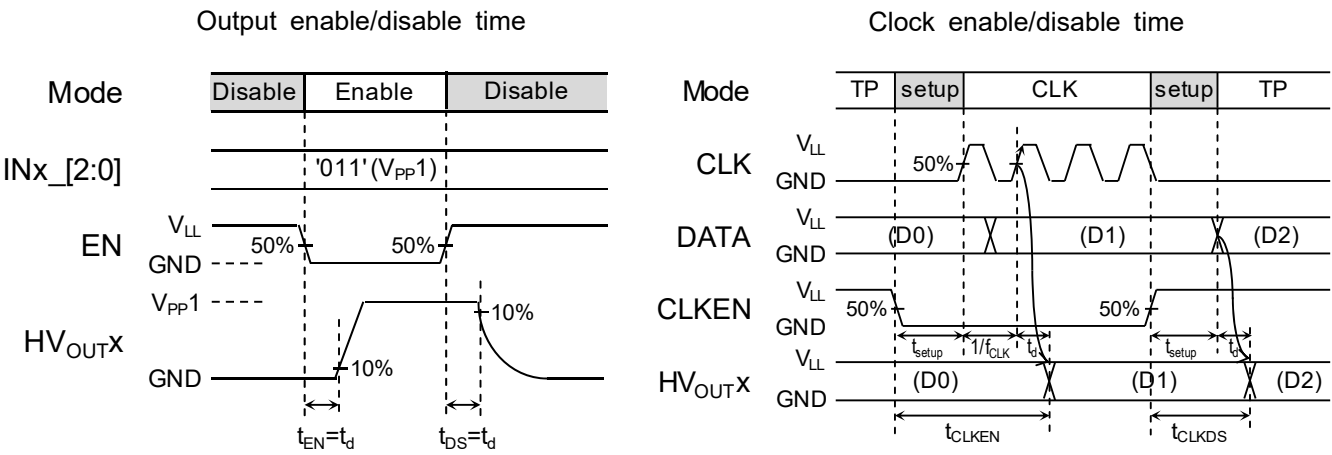


Fig.6 Output enable/disable and Clock enable/disable time

6. Truth Table and Current Mode Control

6.1 Truth Table

Table 12 Truth table

Logic Inputs				Internal MOSFET state							Output state
EN	INx_2	INx_1	INx_0	P1	N1	P2	N2	P3	N3	ASW	TX _{OUTX} (internal node)
				+HV1	-HV1	+HV2	-HV2	GND	GND	GND	
0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ
0	0	0	1	OFF	OFF	ON	OFF	OFF	OFF	OFF	+HV2
0	0	1	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ
0	0	1	1	ON	OFF	OFF	OFF	OFF	OFF	OFF	+HV1
0	1	0	0	OFF	OFF	OFF	OFF	ON	ON	ON	GND
0	1	0	1	OFF	OFF	OFF	ON	OFF	OFF	OFF	-HV2
0	1	1	0	OFF	OFF	OFF	OFF	ON	ON	ON	GND
0	1	1	1	OFF	ON	OFF	OFF	OFF	OFF	OFF	-HV1
1	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ

NOTE:

- $V_{PP1}/V_{NN1} = \pm HV1$, $V_{PP2}/V_{NN2} = \pm HV2$
- x=1~4

6.2 Current Mode Control

Table 13 P2/N2 Drive current mode control

Current Mode	CC1	CC0	I _{out} [A]	
			P2	N2
1	0	0	0.63	0.63
2	0	1	1.25	1.25
3	1	0	1.88	1.88
4	1	1	2.5	2.5

NOTE:

Recommended mode is as follows:

- Current mode 3 or 4 for high-amplitude short-cycle pulse waveforms, or for driving heavy load
- Current mode 1 or 2 for low-amplitude long pulse train waveforms (e.g. CW), or for driving light load

7. Pin Configuration

Table 14 Pin Configuration

Pin#	Pin Name	I/O	Function
1	IN1_0	I	Input logic control of the least significant bit of channel 1, HV2 control
2	IN1_1	I	Input logic control of 2nd significant bit of channel 1, HV1 control
3	IN1_2	I	Input logic control of the most significant bit of channel 1, polarity control
4	IN2_0	I	Input logic control of the least significant bit of channel 2, HV2 control
5	IN2_1	I	Input logic control of 2nd significant bit of channel 2, HV1 control
6	IN2_2	I	Input logic control of the most significant bit of channel 2, polarity control
7	NC	-	No connection
8	VLL	-	Positive voltage supply of low voltage interface (+3.3V)
9	CLK	I	Clock Input (100MHz)
10	GND	-	Drive power ground (0V)
11	IN3_0	I	Input logic control of the least significant bit of channel 3, HV2 control
12	IN3_1	I	Input logic control of 2nd significant bit of channel 3, HV1 control
13	IN3_2	I	Input logic control of the most significant bit of channel 3, polarity control
14	IN4_0	I	Input logic control of the least significant bit of channel 4, HV2 control
15	IN4_1	I	Input logic control of 2nd significant bit of channel 4, HV1 control
16	IN4_2	I	Input logic control of the most significant bit of channel 4, polarity control
17	EN	I	Control of drive output enable, Hi=off, Low=on (50k Ω internal pull-up resistor)
18	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50k Ω internal pull-up resistor)
19	ATHP	I	Control of active THP enable, Hi=disable, Low=enable (50k Ω internal pull-down resistor)
20	THP	O	Thermal protection output, open N-MOS drain
21	VSS	-	Negative low voltage power supply (-5V)
22	NC	-	No connection
23	VFN1	-	N-MOS (N1) floating gate drive power supply (VNN1+5V)
24	VFN2	-	N-MOS (N2) floating gate drive power supply (VNN2+5V)
25	GND	-	Drive power ground (0V)
26	VFP2	-	P-MOS (P2) floating gate drive power supply (VPP2-5V)
27	NC	-	No connection
28	VFP1	-	P-MOS (P1) floating gate drive power supply (VPP1-5V)
29	NC	-	No connection
30	NC	-	No connection
31	GND	-	Drive power ground (0V)
32	NC	-	No connection

Table 14 Pin Configuration (continued)

Pin#	Pin Name	I/O	Function
33	VPP1	-	Positive high voltage power supply 1 for channel 3,4 (0 to +100V)
34	VPP2	-	Positive high voltage power supply 2 for channel 3,4 (0 to +100V, VPP2<VPP1)
35	HVOUT4	O	Output high voltage for channel 4
36	HVOUT3	O	Output high voltage for channel 3
37	VNN2	-	Negative high voltage power supply 2 for channel 3,4 (0 to -100V, VNN2>VNN1)
38	VNN1	-	Negative high voltage power supply 1 for channel 3,4 (0 to -100V)
39	NC	-	No connection
40	GND	-	Drive power ground (0V)
41	GND	-	Drive power ground (0V)
42	NC	-	No connection
43	VNN1	-	Negative high voltage power supply 1 for channel 1,2 (0 to -100V)
44	VNN2	-	Negative high voltage power supply 2 for channel 1,2 (0 to -100V, VNN2>VNN1)
45	HVOUT2	O	Output high voltage for channel 2
46	HVOUT1	O	Output high voltage for channel 1
47	VPP2	-	Positive high voltage power supply 2 for channel 1,2 (0 to +100V)
48	VPP1	-	Positive high voltage power supply 1 for channel 1,2 (0 to +100V)
49	NC	-	No connection
50	GND	-	Drive power ground (0V)
51	NC	-	No connection
52	NC	-	No connection
53	VFP1	-	P-MOS (P1) floating gate drive power supply (VPP1-5V)
54	NC	-	No connection
55	VFP2	-	P-MOS (P2) floating gate drive power supply (VPP2-5V)
56	GND	-	Drive power ground (0V)
57	VFN2	-	N-MOS (N2) floating gate drive power supply (VNN2+5V)
58	VFN1	-	N-MOS (N1) floating gate drive power supply (VNN1+5V)
59	NC	-	No connection
60	VDD	-	Positive low voltage power supply (+5V)
61	CC0	I	Control of drive current mode 0 (50kΩ internal pull-up resistor)
62	CC1	I	Control of drive current mode 1 (50kΩ internal pull-up resistor)
63	GND	-	Drive power ground (0V)
64	GND	-	Drive power ground (0V)

TOP VIEW

Unit: mm

9.20 ±0.10
9.00 ±0.05
4-C0.5
A
B
Index
6.4
1
0.50
0.75
0.50
0.75

SIDE VIEW

S
0.90 ±0.05
0.02 TYP
0.005 MIN 0.04 MAX
0.22 ±0.03
0.45 ±0.10
0.05 S

BOTTOM VIEW

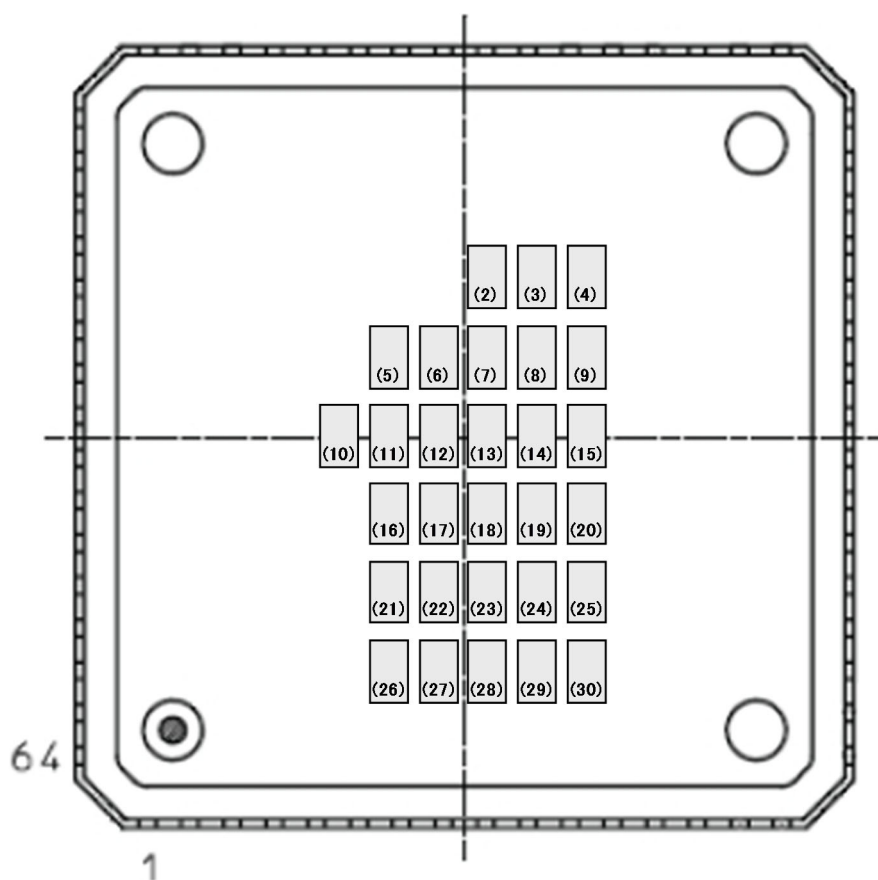
1
6.4
7.50
C0.30
45°
4-0.22 ±0.05
4-0.34 ±0.05
7.50
0.22 ±0.05
0.05 M S AB

OUTER LEAD (detail)

Exposed pad

Note:
Exposed pad is electrically connected to chip ground. Attaching the pad to a ground plane ensures reliable operation of the device, and also helps reduce the junction temperature of the device that may be beneficial in high temperature environments.

9. Package Marking



No.	Code
(2)	Year sealed : the last one digit of the year
(3)	Month sealed : A~M (exc "I") in the order of Jan. to Dec.
(4)	Week sealed : 1~5
(5)~(15)	HDL6V5541HF (product name)
(16)~(25)	Quality control code
(26)~(30)	Country of origin

Fig.8 Package Marking

10. Transport Media, Quantity

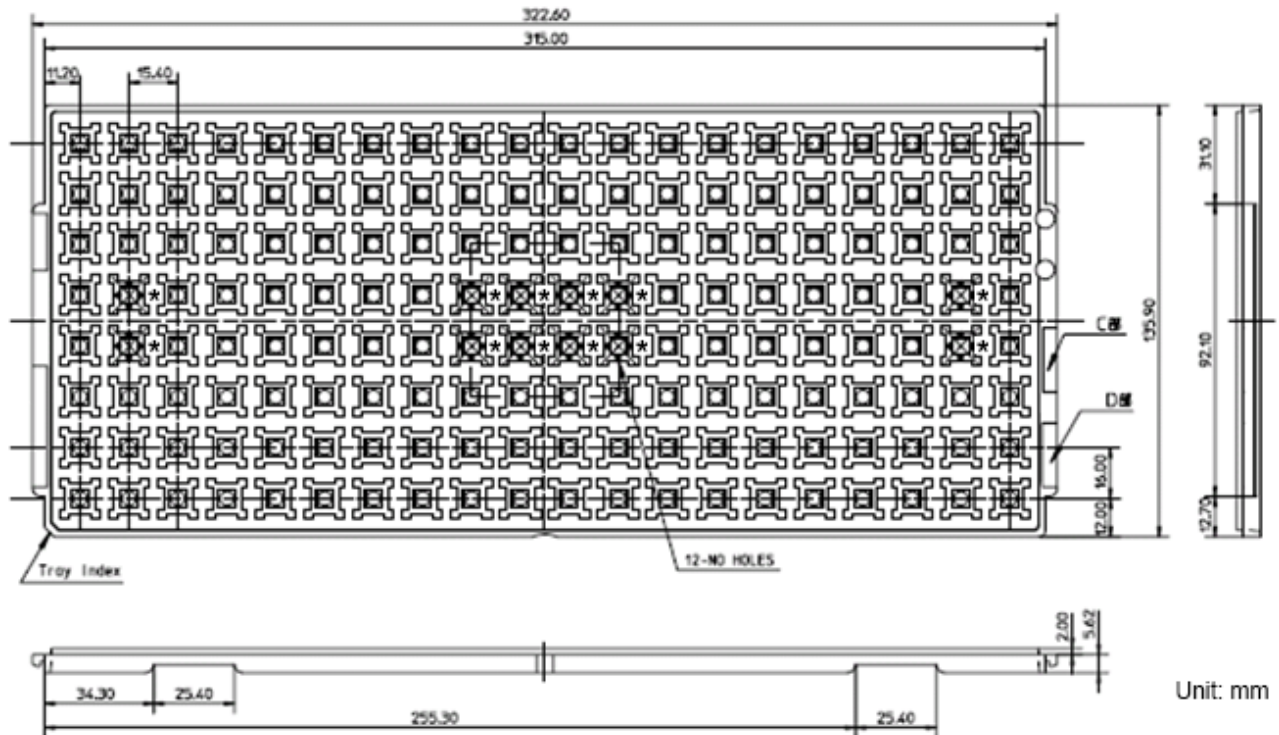


Fig.9 IC Tray Outline

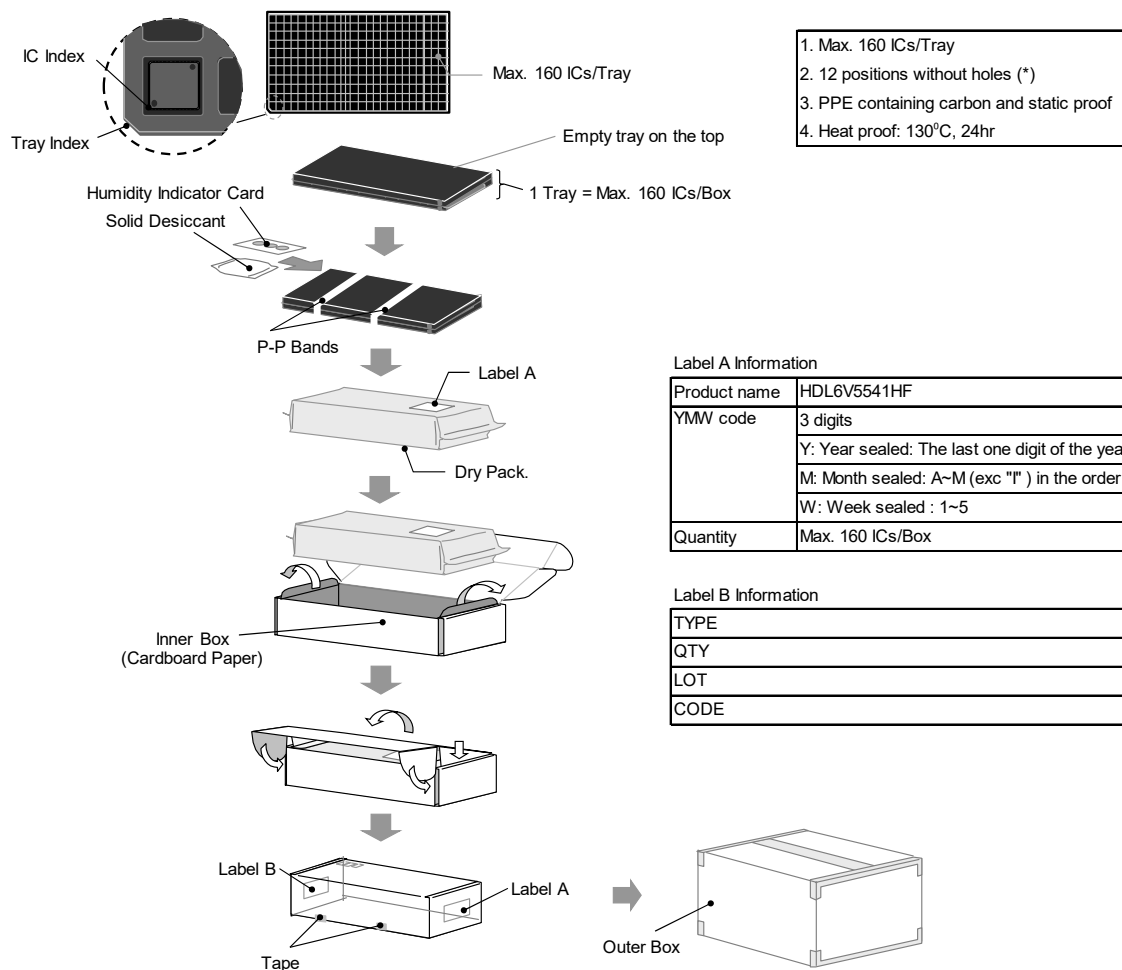


Fig.10 Transport Media, Quantity

11. Mounting, Storage

11.1 Mounting Pad Design Example

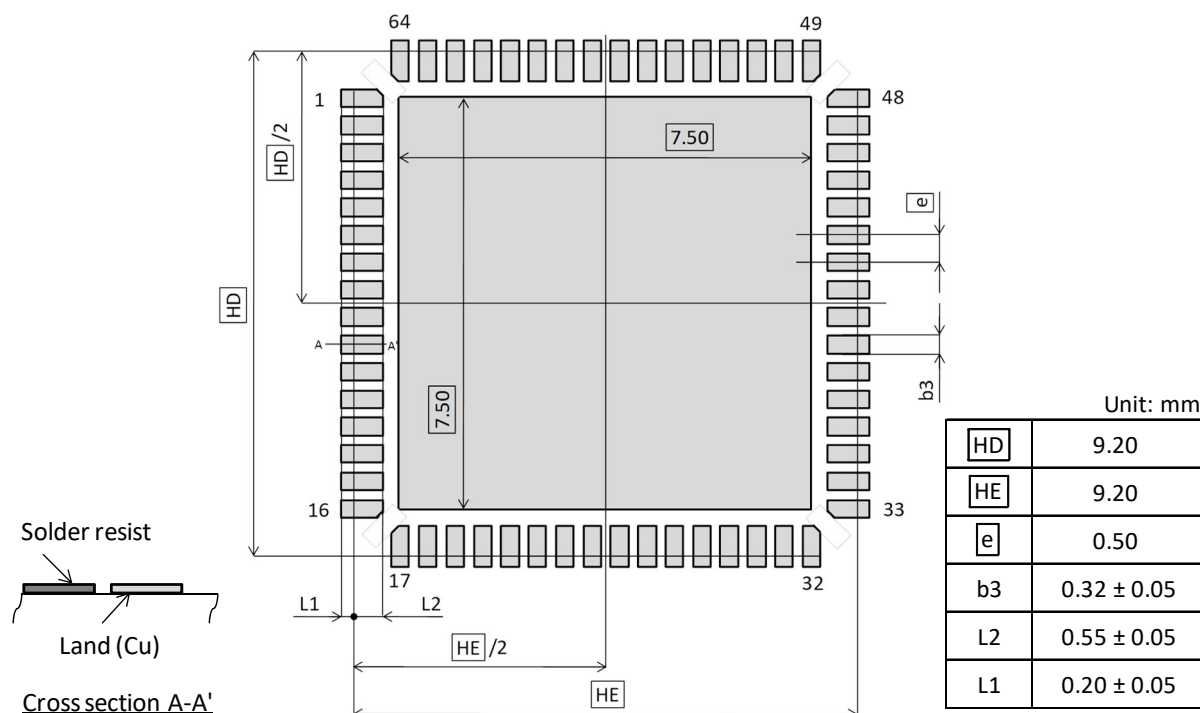


Fig.11 Mounting Pad Design Example

11.2 Storage Conditions

11.2.1 The storage location should be kept at 5 to 35 °C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

11.2.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125 °C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

11.3 Reflow Conditions

Typical full heating methods such as Infrared (IR), Hot air, and N2 reflow process are applicable. IR/Air reflow heating conditions are shown below.

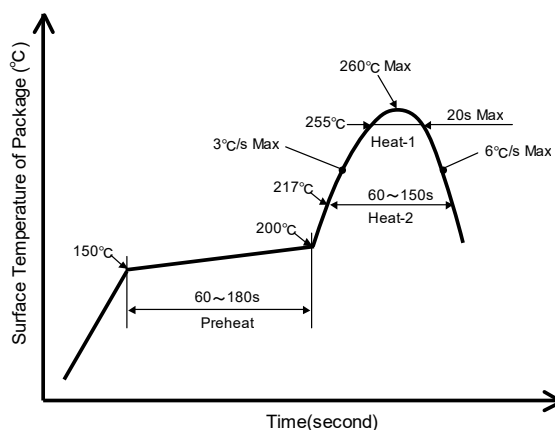


Fig.12 IR/Air Reflow Heating Conditions

12. Inspection

Hundred percent inspections shall be conducted on electrical characteristics.

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 - 14.1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.
 - 14.1.2 Those who touch products such as work platform, machine, measurement/test equipment should be grounded.
 - 14.1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.
 - 14.1.4 Prevent friction with other materials made with high polymer.
 - 14.1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
 - 14.1.6 Avoid dealing with or storing products in an extremely arid environment.
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