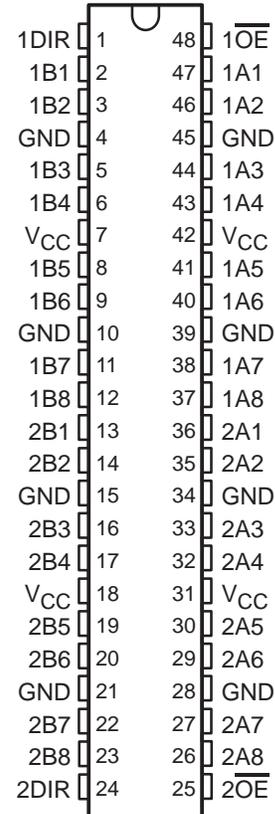


# SN54ABT16245A, SN74ABT16245A 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-IIB*™ BiCMOS Design Significantly Reduces Power Dissipation
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Thin Very Small-Outline (DGV), Shrink Small-Outline (DL), and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic (WD) Flat Package Using 25-mil Center-to-Center Spacings

SN54ABT16245A . . . WD PACKAGE  
SN74ABT16245A . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16245A devices are 16-bit noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16245A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16245A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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 **TEXAS  
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54ABT16245A, SN74ABT16245A

## 16-BIT BUS TRANSCEIVERS

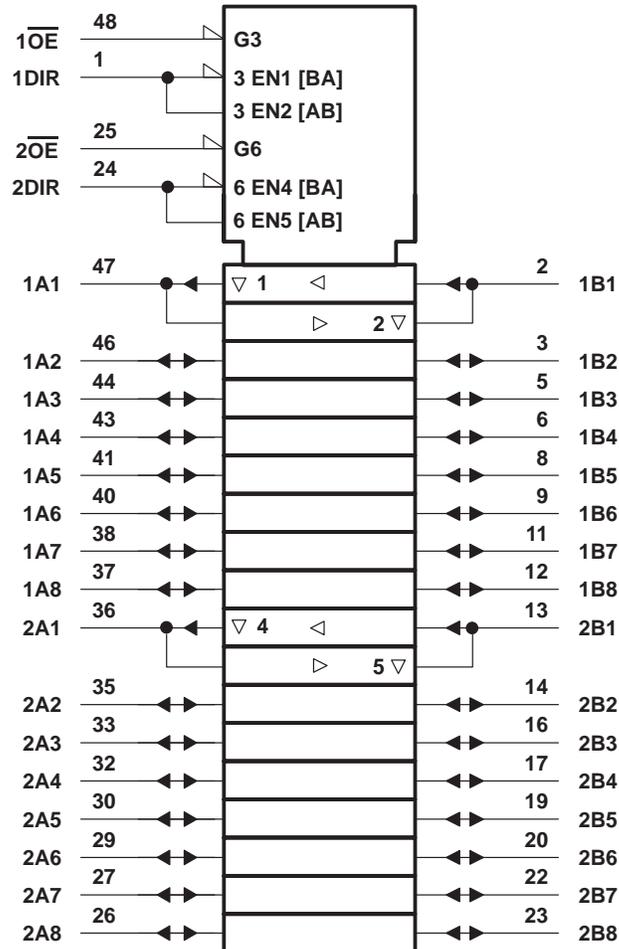
### WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†

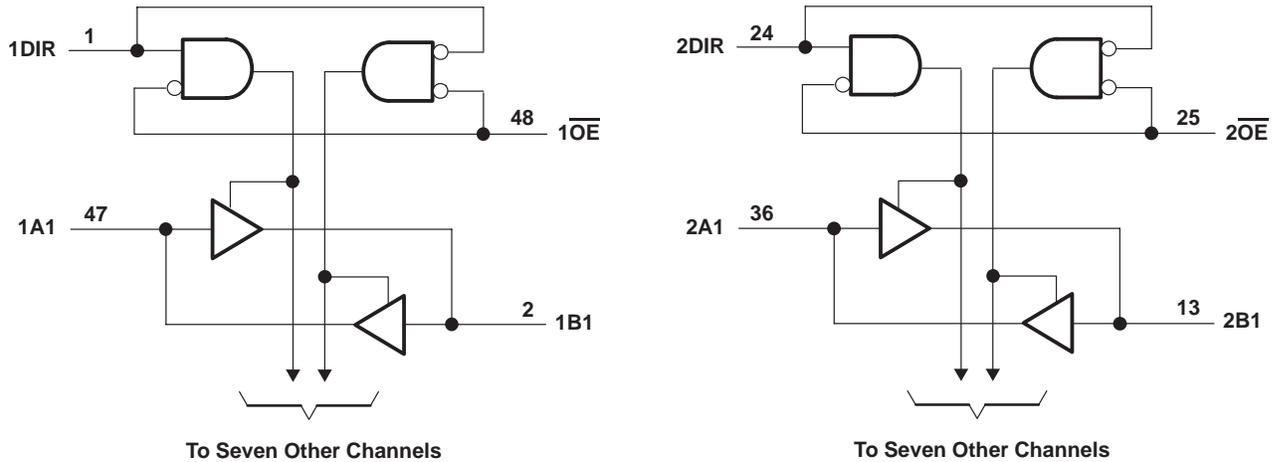


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ABT16245A, SN74ABT16245A 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16245A .....	96 mA
SN74ABT16245A .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	89°C/W
DGV package .....	93°C/W
DL package .....	94°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

		SN54ABT16245A		SN74ABT16245A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu$ s/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54ABT16245A, SN74ABT16245A

## 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

SCBS300E – MARCH 1994 – REVISED MARCH 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16245A		SN74ABT16245A		UNIT		
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5		2.5		2.5		V		
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3		3		3				
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA		2		2					
I <sub>OH</sub> = -32 mA			2*				2				
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA				0.55			V		
		I <sub>OL</sub> = 64 mA				0.55*		0.55			
V <sub>hys</sub>			100						mV		
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA	
	A or B ports	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±20*		±100		±20		
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$				±50**		±50**		±50	μA	
I <sub>OZPD</sub>	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$				±50**		±50**		±50	μA	
I <sub>OZH</sub> ‡	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V				10§		10		10§	μA	
I <sub>OZL</sub> ‡	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V				-10§		-10		-10§	μA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V				±100				±100	μA	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μA	
I <sub>O</sub> ¶	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA	
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI <sub>CC</sub> #	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Outputs enabled			2		1.5		2	mA
			Outputs disabled			0.05		1		0.05	
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5		1.5		1.5		
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			3					pF	
C <sub>O</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			6					pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ This limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54ABT16245A, SN74ABT16245A**  
**16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS300E – MARCH 1994 – REVISED MARCH 1999

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16245A					UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX		
			MIN	TYP	MAX				
$t_{PLH}$	A or B	B or A	0.5	2.2	3.4	0.5	4	ns	
$t_{PHL}$			0.5	2.3	3.8	0.5	4.6		
$t_{PZH}$	$\overline{OE}$	B or A	0.8	3.6	5.2	0.8	5.5	ns	
$t_{PZL}$			0.9	3.7	6.1	0.1	7.3		
$t_{PHZ}$	$\overline{OE}$	B or A	1.3	4.4	5.8	1.3	6.3	ns	
$t_{PLZ}$			1.4	3.3	4.7	1.4	5.3		

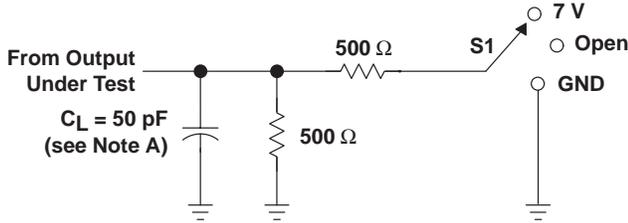
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16245A					UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX		
			MIN	TYP	MAX				
$t_{PLH}$	A or B	B or A	1	2.2	3.4	1	3.9	ns	
$t_{PHL}$			1	2.3	3.7	1	4.2		
$t_{PZH}$	$\overline{OE}$	B or A	1	3.6	5.2	1	6.3	ns	
$t_{PZL}$			1	3.7	5.4	1	6.4		
$t_{PHZ}$	$\overline{OE}$	B or A	2	4.4	5.8	2	6.3	ns	
$t_{PLZ}$			1.5	3.3	4.7	1.5	5.2		

**SN54ABT16245A, SN74ABT16245A**  
**16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

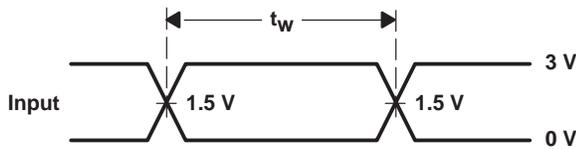
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**PARAMETER MEASUREMENT INFORMATION**

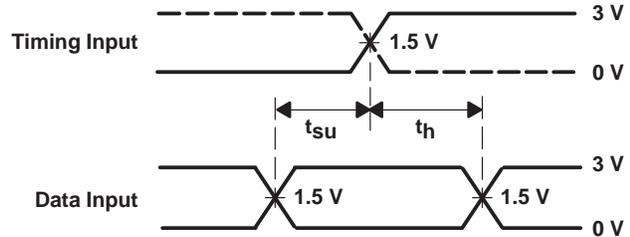


**LOAD CIRCUIT**

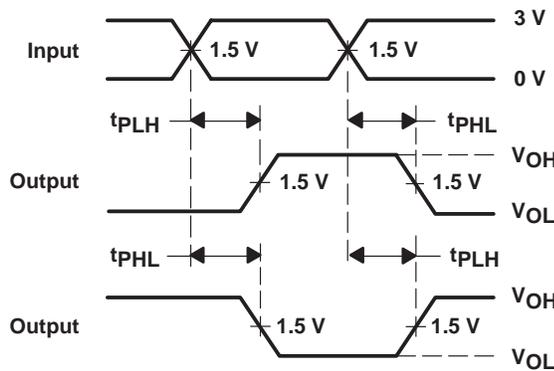
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



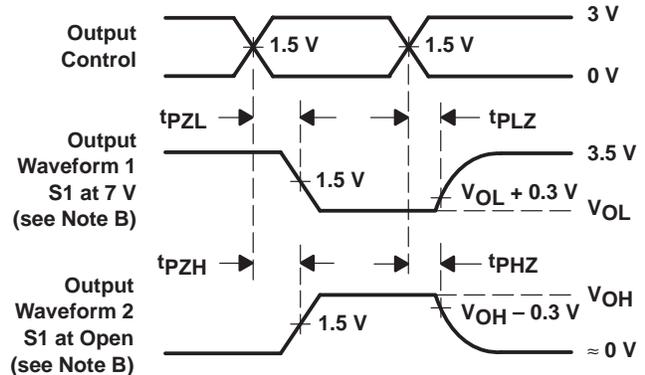
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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