National Semiconductor

93L10/93L16
BCD Decade Counter/4-Bit Binary Counter

General Description

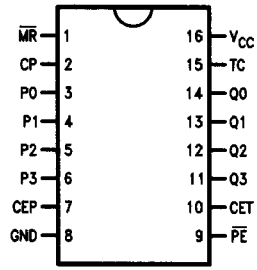
The 93L10 is a high speed synchronous BCD decade counter and the 93L16 is a high speed synchronous 4-bit binary counter. They are synchronously presettable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several states of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

Features

- Synchronous counting and parallel entry
- Decoded terminal count
- Built-in Carry Circuitry
- Easy interfacing with DTL, LPDTL, and TTL families

Connection Diagram

Dual-In-Line Package



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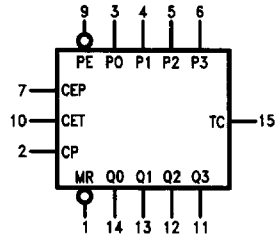
Order Number 93L10DMQB, 93L10FMQB, 93L16DMQB or 93L16FMQB
See NS Package Number J16A or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0–Q3	Flip-Flop Outputs
TC	Terminal Count Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
MIL	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L10/93L16 (MIL)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW P_n to CP	75 75			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW P_n to CP	10 10			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW $\overline{PE}$ to CP	(Note 2) 53			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW $\overline{PE}$ to CP	7.0 (Note 2)			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW CEP or CET to CP	26 (Note 1)			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW CEP or CET to CP	(Note 1) 10			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width	25 25			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW	65			ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	30			ns

Note 1: The Setup Time "$t_s(L)$" and Hold Time "$t_h(H)$" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH-to-LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.

Note 2: The Setup Time "$t_s(H)$" and Hold Time "$t_h(L)$" between the Parallel Enable ($\overline{PE}$) and Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{PE}$ must occur only while the Clock is HIGH for conventional operation.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			CET, CP, PE			40	
			P_n			13.3	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−400	μA
			CET, CP, PE			−800	
			P_n			−267	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max				27.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	13		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q		32 39	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		66 30	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		35 30	ns
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		72	ns

Functional Description

The 93L10 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it increments to state 0 (LLLL). The 93L16 counts modulo-16 in binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Four control inputs—Master Reset ($\overline{MR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 93L10 and 93L16 contain masterslave flip-flops which are "next-state catching" because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, nor the parallel entry mode is momentarily enabled while CP is LOW.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters—fully decoded in both types). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in *Figures a* and *b*. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

MULTISTAGE COUNTING

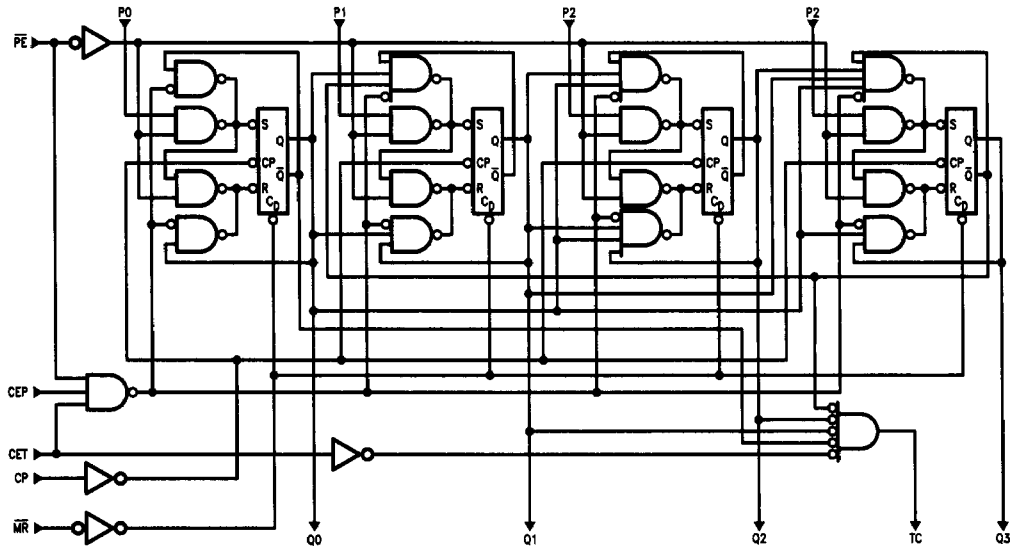
The '10/'16 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in *Figures a* and *b*.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The '10/'16 internally decodes the terminal count condition and "ANDs" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, *Figure a*. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in *Figure b* permits multistage counting, limited by the fan-out of the terminal count. The CEP input of the '10/'16 is internally "ANDed" with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.

Logic Diagrams

93L10



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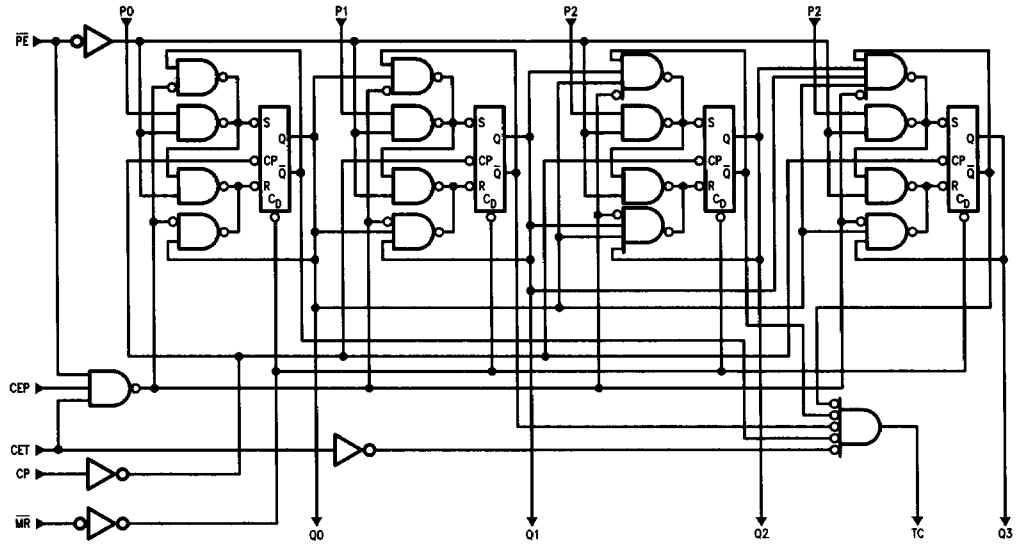
93L16



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Mode Select Table

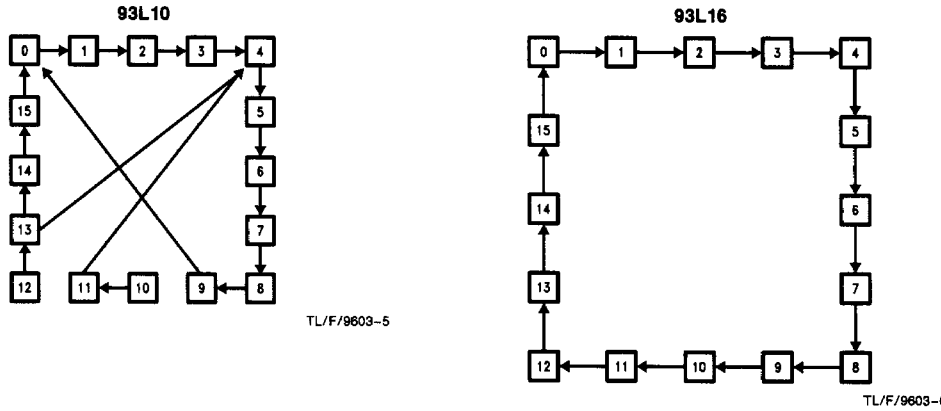
Inputs					Response
$\overline{MR}$	$\overline{PE}$	CEP	CET	CP	
L	X	X	X	X	Clear; All Outputs LOW
H	L	X	X	↗	Parallel Load; $P_n \rightarrow Q_n$
H	H	L	X	X	Hold
H	H	X	L	X	Hold; TC = LOW
H	H	H	H	↗	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Equations

Count Enable = MR • PE • CEP • CET
Terminal Count = CET • Q0 • Q1 • Q2 • Q3 ('16)
Terminal Count = CET • Q0 • $\overline{Q1}$ • $\overline{Q2}$ • Q3 ('10)

State Diagrams



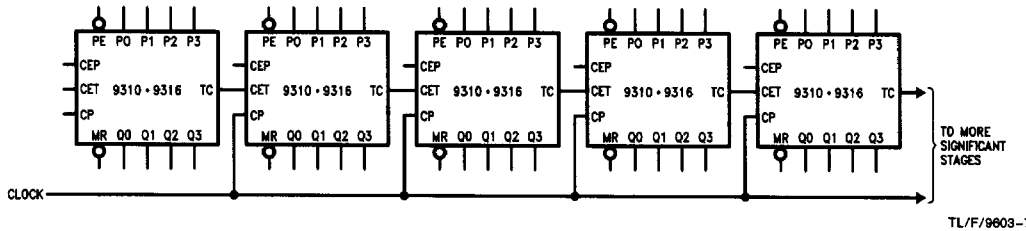


FIGURE a. Synchronous Multistage Counting Scheme (Slow)

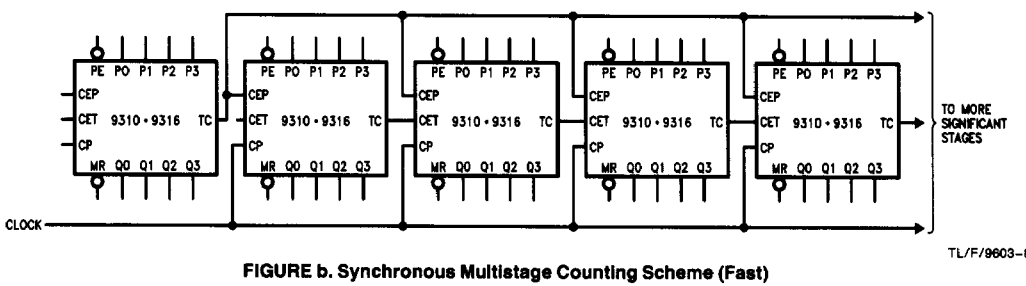


FIGURE b. Synchronous Multistage Counting Scheme (Fast)

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