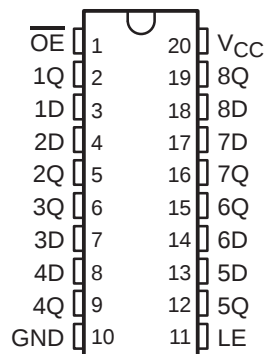


SN54ABT373, SN74ABT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS155D – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-IITM* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (N) and Ceramic (J) DIPs

SN54ABT373 . . . J OR W PACKAGE
SN74ABT373 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description

The eight latches of the 'ABT373 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

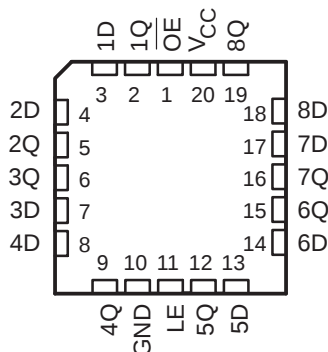
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT373 is characterized for operation from -40°C to 85°C .

SN54ABT373 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z



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**TEXAS
INSTRUMENTS**

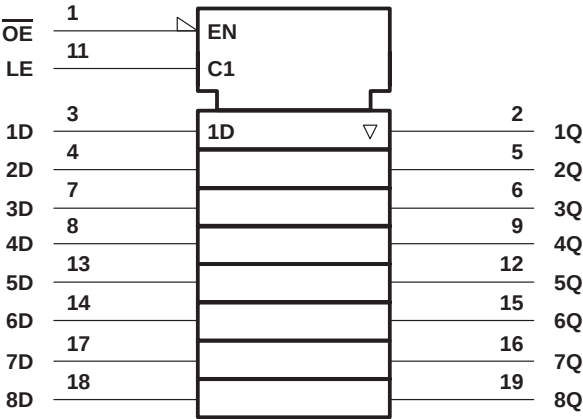
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SN54ABT373, SN74ABT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

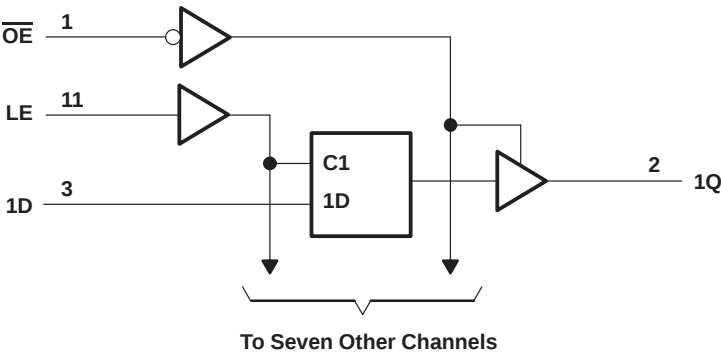
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT373	96 mA
SN74ABT373	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

SN54ABT373, SN74ABT373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

		SN54ABT373		SN74ABT373		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		–24		–32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT373		SN74ABT373		UNIT
		MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = –3 mA	3			3		3		
	V _{CC} = 4.5 V			2	2				
				2*			2		
V _{OL}	V _{CC} = 4.5 V			0.55	0.55				V
				0.55*			0.55		
V _{hys}			100						mV
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			10 [‡]		10 [‡]		10 [‡]	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			–10 [‡]		–10 [‡]		–10 [‡]	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high		50	50		50		μA
I _O [§]	V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1	250		250		μA
		Outputs low		24	30		30		mA
		Outputs disabled		0.5	250		250		μA
ΔI _{CC} [¶]	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5	1.5		1.5		mA
C _i	V _I = 2.5 V or 0.5 V			3					pF
C _O	V _O = 2.5 V or 0.5 V			6					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

[†] All typical values are at V_{CC} = 5 V.

[‡] This data sheet limit may vary among suppliers.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT373		UNIT		
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX
			MIN	MAX			
t _W	Pulse duration, LE high		3.3	3.3	ns		
t _{SU}	Setup time, data before LE↓	High	2.2	2.5	ns		
		Low	2.2	2.5			
t _H	Hold time, data after LE↓	High or low	2.2	2.5	ns		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT373		UNIT		
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX
			MIN	MAX			
t _w	Pulse duration, LE high		3.3	3.3	ns		
t _{su}	Setup time, data before LE↓	High	1.9	1.9	ns		
		Low	1.5	1.5			
t _h	Hold time, data after LE↓	High or low	1	1	ns		

SN54ABT373, SN74ABT373
OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT373					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	D	Q	1.9	3.9	5.4	1.3	6.8	ns
t _{PHL}			2.2	4.2	5.7	2	7	
t _{PLH}	LE	Q	2.2	4.6	6.1	1.8	7.7	ns
t _{PHL}			3.2	5.2	6.7	2.5	7.7	
t _{PZH}	$\overline{OE}$	Q	1.2	3.2	5.5	1	6.2	ns
t _{PZL}			2	4.7	6.2	1.5	7.2	
t _{PHZ}	$\overline{OE}$	Q	2.5	4.9	6.4	2.4	8	ns
t _{PLZ}			2	4.5	6	2	7	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT373					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t _{PLH}	D	Q	1.9	3.9	5.4	1.9	5.9	ns
t _{PHL}			2.2	4.2	5.7	2.2	6.2	
t _{PLH}	LE	Q	2.2	4.6	6.1	2.2	6.6	ns
t _{PHL}			3.2	5.2	6.7	3.2	7.2	
t _{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	1.2	5.2	ns
t _{PZL}			2.7	4.7	6.2	2.7	6.7	
t _{PHZ}	$\overline{OE}$	Q	2.5	4.9	6.4	2.5	6.9	ns
t _{PLZ}			2	4.5	6	2	6.5	

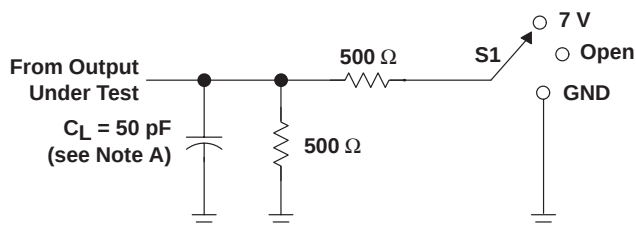
SN54ABT373, SN74ABT373

OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

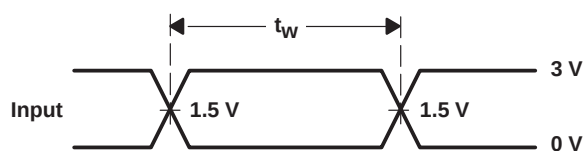
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PARAMETER MEASUREMENT INFORMATION

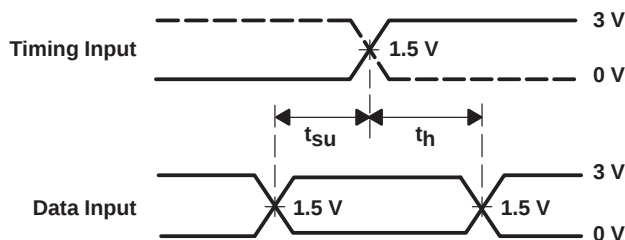


LOAD CIRCUIT

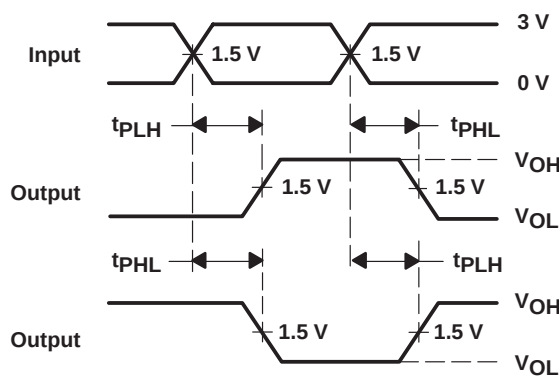
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



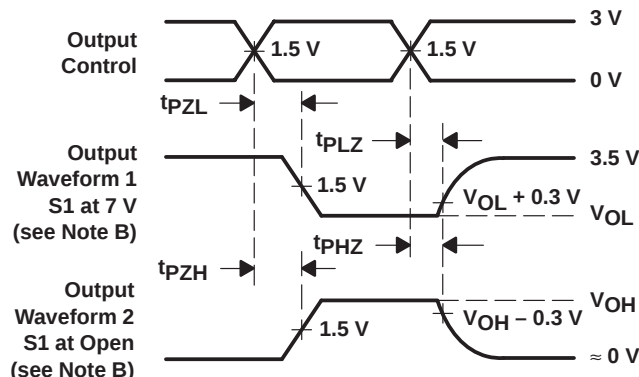
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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