



# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## General Description

The MAX190/MAX191 are monolithic, CMOS, 12-bit analog-to-digital converters (ADCs) featuring differential inputs, track/hold (T/H), internal voltage reference, internal or external clock, and parallel or serial  $\mu$ P interface. Both devices have a 7.5 $\mu$ s conversion time. The MAX190 has a 5 $\mu$ s acquisition time and sampling rate of 76k samples per second (ksps), while the MAX191 has a 2 $\mu$ s acquisition time and is guaranteed at 100ksps.

Decoupling capacitors are the only external components needed for the power supply and reference. These ADCs operate with either an external reference, or an internal reference that features an adjustment input for trimming system gain errors.

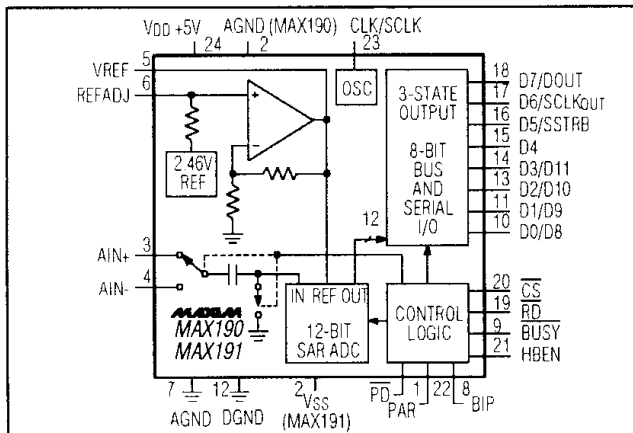
Both the MAX190 and MAX191 operate from a single +5V supply. The MAX191 also operates from dual  $\pm$ 5V supplies, allowing ground-referenced bipolar input signals. Both devices feature a logic power-down input, which reduces the 3mA  $V_{DD}$  supply current to 50 $\mu$ A max, including the internal-reference current.

The MAX190/MAX191 provide three interface modes: two 8-bit parallel modes, and a serial interface mode that is compatible with SPI, QSPI and Microwire™ serial-interface standards.

## Applications

Battery-Powered Data Logging  
PC Pen Digitizers  
High-Accuracy Process Control  
Electromechanical Systems  
Data-Acquisition Boards for PCs  
Automatic Testing Systems  
Telecommunications  
Digital-Signal Processing (DSP)

## Functional Diagram



™ Microwire is a registered trademark of National Semiconductor.

## Features

- ◆ 12-Bit Resolution, 1/2LSB Linearity
- ◆ +5V or  $\pm$ 5V Operation (MAX191)
- ◆ Built-In Track/Hold
- ◆ Internal Reference with Adjustment Capability
- ◆ Low Power: 3mA Operating Mode  
20 $\mu$ A Power-Down Mode
- ◆ 100ksps Tested Sampling Rate (MAX191)
- ◆ Serial and 8-Bit Parallel  $\mu$ P Interface
- ◆ 24-Pin Narrow DIP and Wide SO Packages

## Ordering Information

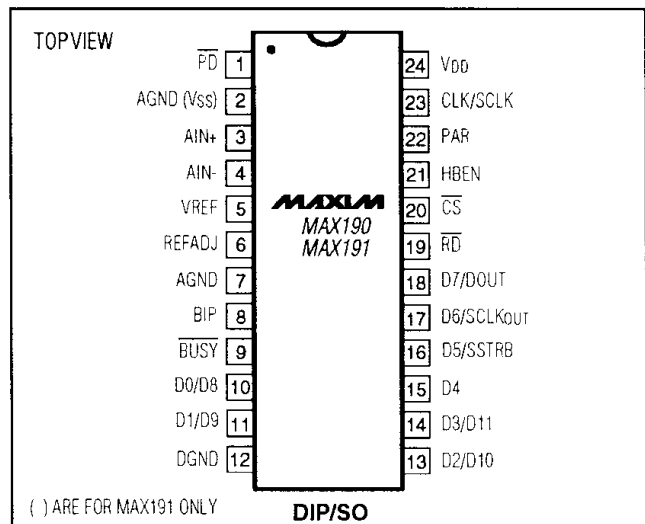
| PART       | TEMP. RANGE     | PIN-PACKAGE           | ERROR (LSBs) |
|------------|-----------------|-----------------------|--------------|
| MAX190ACNG | 0°C to +70°C    | 24 Narrow Plastic DIP | $\pm 1/2$    |
| MAX190BCNG | 0°C to +70°C    | 24 Narrow Plastic DIP | $\pm 1$      |
| MAX190ACWG | 0°C to +70°C    | 24 Wide SO            | $\pm 1/2$    |
| MAX190BCWG | 0°C to +70°C    | 24 Wide SO            | $\pm 1$      |
| MAX190BC/D | 0°C to +70°C    | Dice*                 | $\pm 1$      |
| MAX190AENG | -40°C to +85°C  | 24 Narrow Plastic DIP | $\pm 1/2$    |
| MAX190BENG | -40°C to +85°C  | 24 Narrow Plastic DIP | $\pm 1$      |
| MAX190AEWG | -40°C to +85°C  | 24 Wide SO            | $\pm 1/2$    |
| MAX190BEWG | -40°C to +85°C  | 24 Wide SO            | $\pm 1$      |
| MAX190AMRG | -55°C to +125°C | 24 Narrow CERPDP**    | $\pm 1/2$    |
| MAX190BMRG | -55°C to +125°C | 24 Narrow CERPDP**    | $\pm 1$      |

Ordering Information continued on last page.

\* Dice are specified at  $T_A = +25^\circ\text{C}$ , DC parameters only.

\*\*Contact factory for availability and processing to MIL-STD-883.

## Pin Configuration



MAX190/MAX191

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## ABSOLUTE MAXIMUM RATINGS

|                                                       |                                   |
|-------------------------------------------------------|-----------------------------------|
| V <sub>DD</sub> to DGND                               | -0.3V to +7V                      |
| V <sub>SS</sub> to AGND (MAX191)                      | -7V to +0.3V                      |
| V <sub>DD</sub> to V <sub>SS</sub> (MAX191)           | 12V                               |
| AGND, VREF, REFADJ to DGND                            | -0.3V to (V <sub>DD</sub> + 0.3V) |
| AIN+, AIN-, PD to V <sub>SS</sub> (MAX191)            | -0.3V to (V <sub>DD</sub> + 0.3V) |
| AIN+, AIN-, PD to AGND (MAX190)                       | -0.3V to (V <sub>DD</sub> + 0.3V) |
| CS, RD, CLK, BIP, HBEN, PAR, to DGND                  | -0.3V to (V <sub>DD</sub> + 0.3V) |
| BUSY, D0-D7 to DGND                                   | -0.3V to (V <sub>DD</sub> + 0.3V) |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                                   |
| Narrow Plastic DIP (derate 13.33mW/°C above +70°C)    | 1067mW                            |
| Wide SO (derate 11.76mW/°C above +70°C)               | 941mW                             |
| Narrow CERDIP (derate 12.50mW/°C above +70°C)         | 1000mW                            |

Operating Temperature Ranges:

|                                      |                 |
|--------------------------------------|-----------------|
| MAX19__C__                           | 0°C to +70°C    |
| MAX19__E__                           | -40°C to +85°C  |
| MAX19__M__                           | -55°C to +125°C |
| Storage Temperature Range            | -65°C to +160°C |
| Lead Temperature (soldering, 10 sec) | +300°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 5V ±5%, V<sub>SS</sub> = 0V or -5V ±5% (MAX191 only), f<sub>CLK</sub> = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = GND, slow-memory mode, internal-reference mode, external-reference compensation mode, synchronous operation, Figure 6, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Note 1)

| PARAMETER                                                                                                                     | SYMBOL            | CONDITIONS                                | MIN  | TYP  | MAX   | UNITS  |
|-------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------------------------------------|------|------|-------|--------|
| <b>DC ACCURACY</b> (Note 2)                                                                                                   |                   |                                           |      |      |       |        |
| Resolution                                                                                                                    |                   |                                           | 12   |      |       | Bits   |
| Integral Nonlinearity                                                                                                         | INL               | MAX19_A                                   |      |      | ±1/2  | LSB    |
|                                                                                                                               |                   | MAX19_B                                   |      |      | ±1    |        |
| Differential Nonlinearity                                                                                                     | DNL               | No missing codes over temperature         |      |      | ±1    | LSB    |
| Offset Error                                                                                                                  |                   | MAX19_A                                   |      |      | ±1    | LSB    |
|                                                                                                                               |                   | MAX19_B                                   |      |      | ±2    |        |
| Gain-Error (Note 3)                                                                                                           |                   | MAX19_A                                   |      |      | ±2    | LSB    |
|                                                                                                                               |                   | MAX19_B                                   |      |      | ±3    |        |
| Gain-Error Tempco (Note 4)                                                                                                    |                   | Excludes internal-reference drift         |      | ±0.2 |       | ppm/°C |
| <b>DYNAMIC ACCURACY</b> (sample rate = 76kHz for the MAX190, and 100kHz for the MAX191, V <sub>IN</sub> = 4V <sub>p-p</sub> ) |                   |                                           |      |      |       |        |
| Signal-to-Noise plus Distortion Ratio                                                                                         | SINAD             | 1kHz input signal, T <sub>A</sub> = +25°C | 70   |      |       | dB     |
| Total Harmonic Distortion (up to the 5th Harmonic)                                                                            | THD               | 1kHz input signal, T <sub>A</sub> = +25°C |      |      | -80   | dB     |
| Spurious-Free Dynamic Range                                                                                                   | SFDR              | 1kHz input signal, T <sub>A</sub> = +25°C | 80   |      |       | dB     |
| <b>CONVERSION RATE</b>                                                                                                        |                   |                                           |      |      |       |        |
| Conversion Time (Note 5)                                                                                                      | t <sub>CONV</sub> | MAX190, synchronous CLK (12 to 12.5 CLKs) | 7.50 |      | 7.81  | μs     |
|                                                                                                                               |                   | MAX191, synchronous CLK (12 to 13 CLKs)   | 7.50 |      | 8.125 |        |
|                                                                                                                               |                   | MAX190/MAX191, internal CLK, CL = 120pF   | 6    | 12   | 18    |        |
| Track/Hold Acquisition Time                                                                                                   |                   | MAX190                                    |      |      | 5     | μs     |
|                                                                                                                               |                   | MAX191                                    |      |      | 2     |        |
| Aperture Delay                                                                                                                |                   |                                           |      | 25   |       | ns     |
| Aperture Jitter                                                                                                               |                   |                                           |      | 50   |       | ps     |
| External Clock Frequency Range (Note 6)                                                                                       | f <sub>CLK</sub>  |                                           | 0.1  |      | 1.6   | MHz    |

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

MAX190/MAX191

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = 5V ±5%, V<sub>SS</sub> = 0V or -5V ±5% (MAX191 only), f<sub>CLK</sub> = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = GND, slow-memory mode, internal-reference mode, external-reference compensation mode, synchronous operation, Figure 6, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Note 1)

| PARAMETER                                     | SYMBOL           | CONDITIONS                                                                                                        | MIN             | TYP   | MAX             | UNITS  |
|-----------------------------------------------|------------------|-------------------------------------------------------------------------------------------------------------------|-----------------|-------|-----------------|--------|
| <b>ANALOG INPUT</b>                           |                  |                                                                                                                   |                 |       |                 |        |
| Input Voltage Range (Note 7)                  |                  | MAX190                                                                                                            | 0               |       | V <sub>DD</sub> | V      |
|                                               |                  | MAX191                                                                                                            | V <sub>SS</sub> |       | V <sub>DD</sub> |        |
| Input Leakage Current                         |                  | V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub> (MAX191),<br>V <sub>IN</sub> = 0 to V <sub>DD</sub> (MAX190) |                 |       | ±10             | μA     |
| Input Capacitance (Note 6)                    |                  |                                                                                                                   |                 | 45    | 80              | pF     |
| Small-Signal Bandwidth                        |                  |                                                                                                                   |                 | 2     |                 | MHz    |
| <b>INTERNAL REFERENCE</b>                     |                  |                                                                                                                   |                 |       |                 |        |
| VREF Output Voltage                           |                  | T <sub>A</sub> = +25°C                                                                                            | 4.076           | 4.096 | 4.116           | V      |
| VREF Output TC (Note 8)                       |                  | MAX19_C                                                                                                           |                 |       | 50              | ppm/°C |
|                                               |                  | MAX19_E                                                                                                           |                 |       | 60              |        |
|                                               |                  | MAX19_M                                                                                                           |                 |       | 80              |        |
| Output Current Capability (Note 9)            |                  | T <sub>A</sub> = +25°C                                                                                            |                 |       | 2               | mA     |
| Load Regulation                               |                  | T <sub>A</sub> = +25°C, I <sub>OUT</sub> = 0mA to 2mA                                                             |                 |       | 4               | mV     |
| Output Short-Circuit Current                  |                  |                                                                                                                   |                 | 18    |                 | mA     |
| Capacitive Load Required                      |                  | External-reference compensation mode                                                                              | 4.7             |       |                 | μF     |
| Power-Supply Rejection                        |                  | V <sub>DD</sub> = ±5%, V <sub>SS</sub> = ±5% (MAX191)                                                             |                 | ±300  |                 | μV     |
| REFADJ Input Adjustment Range (Note 10)       |                  |                                                                                                                   | -60             |       | 30              | mV     |
| REFADJ Disable Threshold                      |                  |                                                                                                                   | 4.5             |       |                 | V      |
| REFADJ Output Voltage                         |                  |                                                                                                                   |                 | 2.4   |                 | V      |
| REFADJ Input Current                          |                  | REFADJ = 5V                                                                                                       |                 |       | 60              | μA     |
| <b>REFERENCE INPUT</b>                        |                  |                                                                                                                   |                 |       |                 |        |
| Input Voltage Range                           |                  | External-reference mode                                                                                           | 2.5             |       | 5               | V      |
| Input Current                                 |                  | External reference = 5V                                                                                           |                 |       | 1               | mA     |
| Input Resistance                              |                  | External-reference mode                                                                                           | 5               | 10    |                 | kΩ     |
| <b>LOGIC INPUTS</b>                           |                  |                                                                                                                   |                 |       |                 |        |
| Input Low Voltage                             | V <sub>IL</sub>  | CS, RD, CLK, HBEN, PAR, BIP                                                                                       |                 |       | 0.8             | V      |
| Input High Voltage                            | V <sub>IH</sub>  | CS, RD, CLK, HBEN, PAR, BIP                                                                                       | 2.4             |       |                 | V      |
| Input Current                                 | I <sub>IN</sub>  | V <sub>IN</sub> = 0V to V <sub>DD</sub>                                                                           |                 |       | ±10             | μA     |
| Input Current CLK                             | I <sub>IN</sub>  | PD = high/float                                                                                                   |                 |       | ±200            | μA     |
|                                               |                  | PD = low                                                                                                          |                 | ±0.1  |                 |        |
| Input Capacitance (Note 6)                    | C <sub>IN</sub>  |                                                                                                                   |                 |       | 10              | pF     |
| PD Input Low Voltage                          | V <sub>IL</sub>  |                                                                                                                   |                 |       | 0.5             | V      |
| PD Input High Voltage                         | V <sub>IH</sub>  |                                                                                                                   | 4.5             |       |                 | V      |
| PD Input Current                              | I <sub>IN</sub>  | PD = 0V to V <sub>DD</sub> (Note 11)                                                                              |                 |       | ±20             | μA     |
| PD External Leakage for Float State (Note 12) |                  | Maximum current allowed for "floating state"                                                                      |                 |       | ±100            | nA     |
| PD Floating State Voltage                     | V <sub>FLT</sub> | External-reference compensation mode                                                                              |                 | 2.8   |                 | V      |

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = 5V ±5%, V<sub>SS</sub> = 0V or -5V ±5% (MAX191 only), f<sub>CLK</sub> = 1.6MHz, 50% duty cycle, AIN- = AGND, BIP = GND, slow-memory mode, internal-reference mode, external-reference compensation mode, synchronous operation, Figure 6, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Note 1)

| PARAMETER                                         | SYMBOL           | CONDITIONS                                                                                                             |                 | MIN   | TYP | MAX  | UNITS |
|---------------------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------|-----------------|-------|-----|------|-------|
| LOGIC OUTPUTS                                     |                  |                                                                                                                        |                 |       |     |      |       |
| Output Low Voltage                                | V <sub>OL</sub>  | I <sub>OUT</sub> = 1.6mA                                                                                               |                 |       |     | 0.4  | V     |
| Output High Voltage                               | V <sub>OH</sub>  | I <sub>OUT</sub> = -200μA                                                                                              |                 | 4.0   |     |      | V     |
| Three-State Leakage Current                       | I <sub>L</sub>   | D0/D8-D7/DOUT                                                                                                          |                 |       |     | ±10  | μA    |
| Three-State Output Capacitance (Note 6)           | C <sub>OUT</sub> |                                                                                                                        |                 |       |     | 15   | pF    |
| POWER REQUIREMENTS                                |                  |                                                                                                                        |                 |       |     |      |       |
| Positive Supply Voltage                           | V <sub>DD</sub>  |                                                                                                                        |                 | 4.75  |     | 5.25 | V     |
| Negative Supply Voltage (MAX191 only)             | V <sub>SS</sub>  | MAX191                                                                                                                 |                 | -5.25 |     | 0    | V     |
| Positive Supply Current                           | I <sub>DD</sub>  | CS = RD = V <sub>DD</sub> , AIN = 5V, D0/D8-D7/DOUT = 0V or V <sub>DD</sub> , HBEN = PAR = BIP = 0V or V <sub>DD</sub> | PD = high/float |       | 3   | 5    | mA    |
|                                                   |                  |                                                                                                                        | PD = low        |       | 20  | 50   | μA    |
| Negative Supply Current (MAX191 only)             | I <sub>SS</sub>  |                                                                                                                        | PD = high/float |       | 20  | 100  | μA    |
|                                                   |                  |                                                                                                                        | PD = low        |       | 1   | 20   | μA    |
| Positive Supply Rejection (Note 13)               |                  | FS change, V <sub>DD</sub> = 5V ±5%                                                                                    |                 |       |     | ±1/2 | LSB   |
| Negative Supply Rejection (MAX191 only) (Note 13) |                  | FS change, V <sub>SS</sub> = -5V ±5%                                                                                   |                 |       |     | ±1/2 | LSB   |

## TIMING CHARACTERISTICS (see Figures 6-10)

(V<sub>DD</sub> = 5V ±5%, V<sub>SS</sub> = 0V or -5V ±5% (MAX191 only), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Note 14)

| PARAMETER                              | SYMBOL          | CONDITIONS    | T <sub>A</sub> = +25°C |     |     | MAX19_C/E |     |     | MAX19_M |     |     | UNITS |
|----------------------------------------|-----------------|---------------|------------------------|-----|-----|-----------|-----|-----|---------|-----|-----|-------|
|                                        |                 |               | MIN                    | TYP | MAX | MIN       | TYP | MAX | MIN     | TYP | MAX |       |
| CS to RD Setup Time                    | t <sub>1</sub>  |               | 0                      |     |     | 0         |     |     | 0       |     |     | ns    |
| RD to BUSY Delay                       | t <sub>2</sub>  | CL = 50pF     |                        |     | 120 |           |     | 140 |         |     | 160 | ns    |
| Data Access Time (Note 15)             | t <sub>3</sub>  | CL = 100pF    |                        |     | 120 |           |     | 140 |         |     | 160 | ns    |
| RD Pulse Width                         | t <sub>4</sub>  |               | 150                    |     |     | 150       |     |     | 150     |     |     | ns    |
| CS to RD Hold Time                     | t <sub>5</sub>  |               | 0                      |     |     | 0         |     |     | 0       |     |     | ns    |
| Data Setup Time After BUSY (Note 15)   | t <sub>6</sub>  |               |                        |     | 80  |           |     | 100 |         |     | 120 | ns    |
| Bus Relinquish Time (Note 16)          | t <sub>7</sub>  |               |                        |     | 100 |           |     | 110 |         |     | 120 | ns    |
| HBEN to RD Setup Time                  | t <sub>8</sub>  |               | 80                     |     |     | 100       |     |     | 120     |     |     | ns    |
| HBEN to RD Hold Time                   | t <sub>9</sub>  |               | 0                      |     |     | 0         |     |     | 0       |     |     | ns    |
| Delay Between Read Operations (Note 6) | t <sub>10</sub> |               | 200                    |     |     | 200       |     |     | 200     |     |     | ns    |
| Delay Between Conversions              | t <sub>11</sub> | MAX190        | 5                      |     |     | 5         |     |     | 5       |     |     | μs    |
|                                        |                 | MAX191        | 2                      |     |     | 2         |     |     | 2       |     |     |       |
| Aperture Delay                         | t <sub>12</sub> | Jitter < 50ps |                        | 25  |     |           |     |     |         |     |     | ns    |
| CLK to BUSY Delay (Note 6)             | t <sub>13</sub> |               |                        |     | 200 |           |     | 230 |         |     | 260 | ns    |

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## TIMING CHARACTERISTICS (see Figures 6-10) (continued)

(V<sub>DD</sub> = 5V ±5%, V<sub>SS</sub> = 0V or -5V ±5% (MAX191 only). T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Note 14)

| PARAMETER                                   | SYMBOL          | CONDITIONS | T <sub>A</sub> = +25°C |     |     | MAX19_C/E |     |     | MAX19_M |     |     | UNITS |
|---------------------------------------------|-----------------|------------|------------------------|-----|-----|-----------|-----|-----|---------|-----|-----|-------|
|                                             |                 |            | MIN                    | TYP | MAX | MIN       | TYP | MAX | MIN     | TYP | MAX |       |
| SCLK <sub>OUT</sub> to SSTRB Rise Delay     | t <sub>14</sub> |            |                        |     | 100 |           |     | 130 |         |     | 150 | ns    |
| SCLK <sub>OUT</sub> to SSTRB Fall Delay     | t <sub>15</sub> |            |                        |     | 100 |           |     | 130 |         |     | 150 | ns    |
| CS or RD Hold Time                          | t <sub>16</sub> | MAX190     | 5                      |     |     | 5         |     |     | 5       |     |     | ns    |
|                                             |                 | MAX191     | 10                     |     |     | 10        |     |     | 10      |     |     |       |
| CS or RD Delay (MAX190 only)                | t <sub>17</sub> |            |                        |     | 50  |           |     | 50  |         |     | 50  | ns    |
| CS or RD Setup Time (MAX191 only)           | t <sub>17</sub> |            | 150                    |     |     | 150       |     |     | 150     |     |     | ns    |
| CS to Data Access Serial Mode (MAX190 only) | t <sub>18</sub> |            |                        |     | 180 |           |     | 230 |         |     | 250 | ns    |
| CS to DOUT Three-State                      | t <sub>19</sub> |            |                        |     | 100 |           |     | 110 |         |     | 120 | ns    |
| SCLK to SCLK <sub>OUT</sub> Delay           | t <sub>20</sub> |            |                        |     | 160 |           |     | 180 |         |     | 200 | ns    |
| SCLK <sub>OUT</sub> to DOUT Delay           | t <sub>21</sub> |            |                        |     | 100 |           |     | 130 |         |     | 150 | ns    |
| SCLK to DOUT Delay                          | t <sub>22</sub> |            |                        |     | 240 |           |     | 260 |         |     | 280 | ns    |
| SCLK to SSTRB Delay                         | t <sub>23</sub> |            |                        |     | 260 |           |     | 310 |         |     | 350 | ns    |

**Note 1:** Performance at power-supply tolerance limits guaranteed by power-supply rejection test.

**Note 2:** V<sub>DD</sub> = 5V, V<sub>SS</sub> = 0V (MAX191), FS = VREF.

**Note 3:** FS = VREF, offset nulled, ideal last-code transition = FS - 3/2 LSB.

**Note 4:** Gain-Error Tempco = ΔGE/ΔT, where ΔGE is the gain-error change from T<sub>A</sub> = +25°C to T<sub>MIN</sub> or T<sub>MAX</sub>.

**Note 5:** Conversion time defined as the number of clock cycles times the clock period, clock has a 50% duty cycle.

**Note 6:** Guaranteed by design, not production tested.

**Note 7:** AIN<sub>+</sub>, AIN<sub>-</sub> must not exceed supplies for specified accuracy.

**Note 8:** VREF TC = ΔVREF/ΔT, where ΔVREF is reference-voltage change from T<sub>A</sub> = +25°C to T<sub>MIN</sub> or T<sub>MAX</sub>.

**Note 9:** Output current should not change during conversion. This current is in addition to the current required by the internal DAC.

**Note 10:** REFADJ adjustment range is defined as the allowed voltage excursion on REFADJ relative to its unadjusted value of 2.4V. This will typically result in a 1.7 times larger change in the REF output (Figure 12a).

**Note 11:** This current is included in the PD supply current specification.

**Note 12:** Floating the PD pin guarantees external compensation mode.

**Note 13:** VREF = 4.096V, external reference

**Note 14:** All input control signals are specified with t<sub>r</sub> = t<sub>f</sub> = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.

**Note 15:** t<sub>3</sub> and t<sub>6</sub> are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

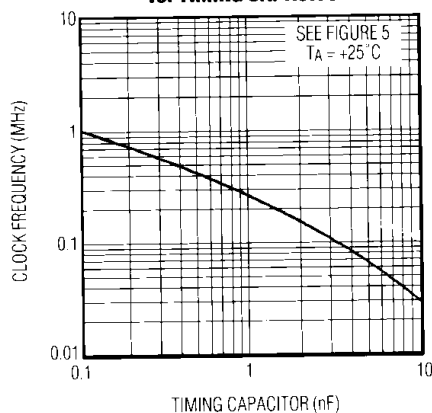
**Note 16:** t<sub>7</sub> is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

MAX190/MAX191

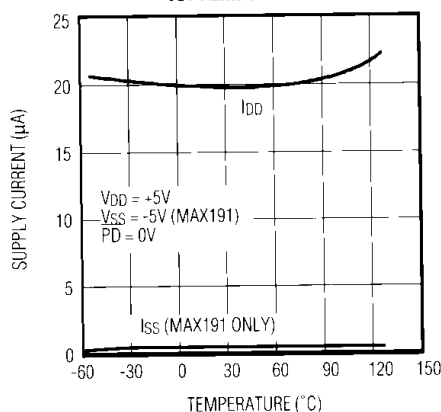
# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## Typical Operating Characteristics

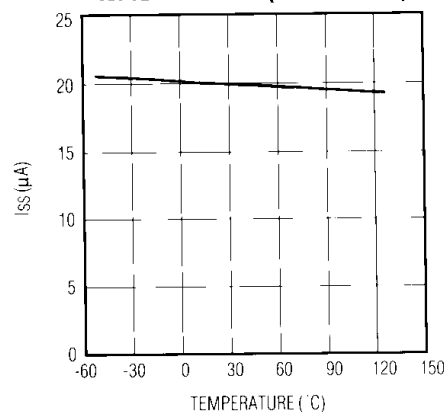
**CLOCK FREQUENCY  
vs. TIMING CAPACITOR**



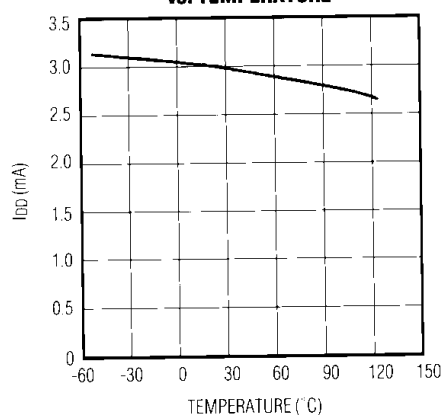
**POWER-DOWN SUPPLY CURRENT  
vs. TEMPERATURE**



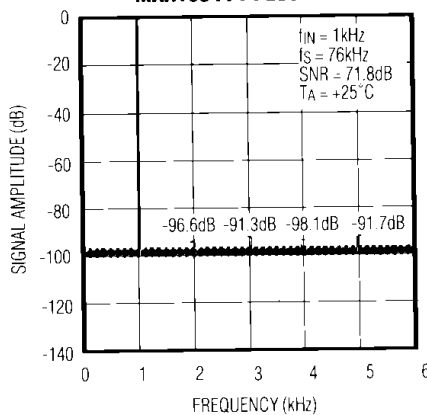
**NEGATIVE SUPPLY CURRENT  
vs. TEMPERATURE (MAX191 ONLY)**



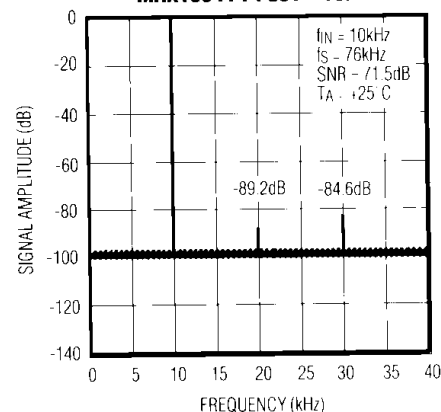
**POSITIVE SUPPLY CURRENT  
vs. TEMPERATURE**



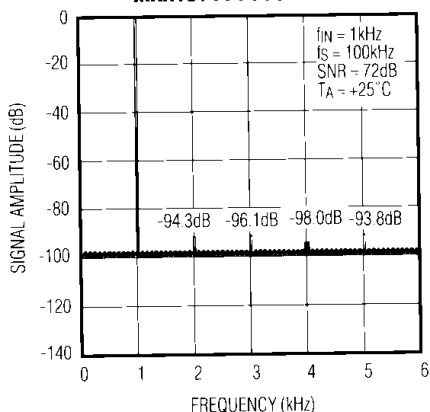
**MAX190 FFT PLOT – 1kHz**



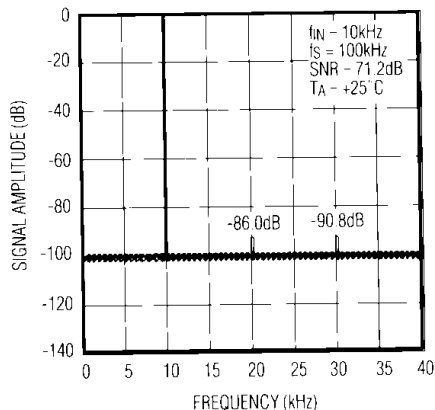
**MAX190 FFT PLOT – 10kHz**



**MAX191 FFT PLOT – 1kHz**



**MAX191 FFT PLOT – 10kHz**



# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## Pin Description

MAX190/MAX191

| PIN    |        | NAME                   | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------|--------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX190 | MAX191 |                        |                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 1      | 1      | $\overline{\text{PD}}$ | Power-Down Input. A logic low at $\overline{\text{PD}}$ deactivates the ADC - only the bandgap reference is active. A logic high selects normal operation, internal-reference compensation mode. An open-circuit condition selects normal operation, external-reference compensation mode.                                                                                                                        |
| 2      |        | AGND                   | Analog Ground. Connect both AGND pins to ground.                                                                                                                                                                                                                                                                                                                                                                  |
|        | 2      | V <sub>SS</sub>        | Negative Supply Input, 0V to -5.25V                                                                                                                                                                                                                                                                                                                                                                               |
| 3      | 3      | A <sub>IN</sub> +      | Sampled Analog Input                                                                                                                                                                                                                                                                                                                                                                                              |
| 4      | 4      | A <sub>IN</sub> -      | Analog Input Return. Pseudo-differential (see <i>Gain and Offset Adjustment</i> section).                                                                                                                                                                                                                                                                                                                         |
| 5      | 5      | VREF                   | Reference-Buffer Output for Internal Reference. Input for external reference when REFADJ is connected to V <sub>DD</sub> .                                                                                                                                                                                                                                                                                        |
| 6      | 6      | REFADJ                 | Reference Adjust                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7      | 7      | AGND                   | Analog Ground                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8      | 8      | BIP                    | BIP = low selects unipolar mode,<br>BIP = high selects bipolar mode (see <i>Gain and Offset Adjustment</i> section)                                                                                                                                                                                                                                                                                               |
| 9      | 9      | BUSY                   | BUSY Output is low during a conversion.                                                                                                                                                                                                                                                                                                                                                                           |
| 10     | 10     | D0/D8                  | Three-State Data Outputs: LSB = D0                                                                                                                                                                                                                                                                                                                                                                                |
| 11     | 11     | D1/D9                  | Three-State Data Outputs                                                                                                                                                                                                                                                                                                                                                                                          |
| 12     | 12     | DGND                   | Digital Ground                                                                                                                                                                                                                                                                                                                                                                                                    |
| 13     | 13     | D2/D10                 | Three-State Data Outputs                                                                                                                                                                                                                                                                                                                                                                                          |
| 14     | 14     | D3/D11                 | Three-State Data Outputs: MSB = D11                                                                                                                                                                                                                                                                                                                                                                               |
| 15     | 15     | D4                     | Three-State Data Output                                                                                                                                                                                                                                                                                                                                                                                           |
| 16     | 16     | D5/SSTRB               | Three-State Data Output/Serial Strobe Output in serial mode                                                                                                                                                                                                                                                                                                                                                       |
| 17     | 17     | D6/SCLK <sub>OUT</sub> | Three-State Data Output/Serial Clock Output in serial mode                                                                                                                                                                                                                                                                                                                                                        |
| 18     | 18     | D7/DOUT                | Three-State Data Output/Data Output in serial mode                                                                                                                                                                                                                                                                                                                                                                |
| 19     | 19     | $\overline{\text{RD}}$ | Read Input. In parallel mode, a low signal starts a conversion when CS and HBEN are low (memory mode). $\overline{\text{RD}}$ also enables the outputs when CS is low. In serial mode, $\overline{\text{RD}}$ = low enables SCLK <sub>OUT</sub> and SSTRB when CS is low. $\overline{\text{RD}}$ = high forces SCLK <sub>OUT</sub> and SSTRB into a high-impedance state.                                         |
| 20     | 20     | $\overline{\text{CS}}$ | Chip-Select Input. Must be low for the ADC to recognize $\overline{\text{RD}}$ and HBEN inputs in parallel mode. The falling edge of CS starts a conversion in serial mode. CS = high in serial mode forces SCLK <sub>OUT</sub> , SSTRB, and DOUT into a high-impedance state.                                                                                                                                    |
| 21     | 21     | HBEN                   | High-Byte Enable Input. In parallel mode, HBEN = high multiplexes the 4 MSBs of the conversion result into the lower bit outputs. HBEN = high also disables conversion starts. HBEN = low places the 8 LSBs onto the data bus. In serial mode, HBEN = low enables SCLK <sub>OUT</sub> to operate during the conversion only, HBEN = high enables SCLK <sub>OUT</sub> to operate continuously, provided CS is low. |
| 22     | 22     | PAR                    | Sets the output mode. PAR = high selects parallel output mode. PAR = low selects serial output mode.                                                                                                                                                                                                                                                                                                              |
| 23     | 23     | CLK/SCLK               | Clock Input/Serial Clock Input in serial mode. An external TTL-/CMOS-compatible clock may be applied to this pin, or a capacitor (120pF nominal) may be connected between CLK and DGND to operate the internal oscillator.                                                                                                                                                                                        |
| 24     | 24     | V <sub>DD</sub>        | Positive Supply, +5V $\pm$ 5%                                                                                                                                                                                                                                                                                                                                                                                     |

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

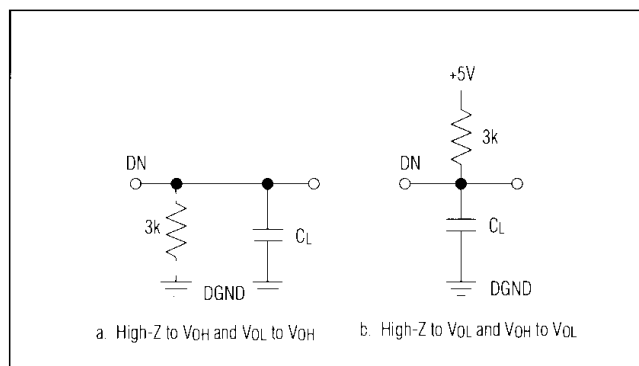


Figure 1. Load Circuits for Access Time

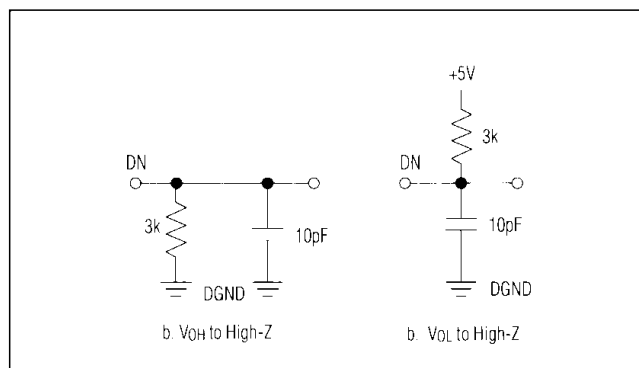


Figure 2. Load Circuits for Bus-Relinquish Time

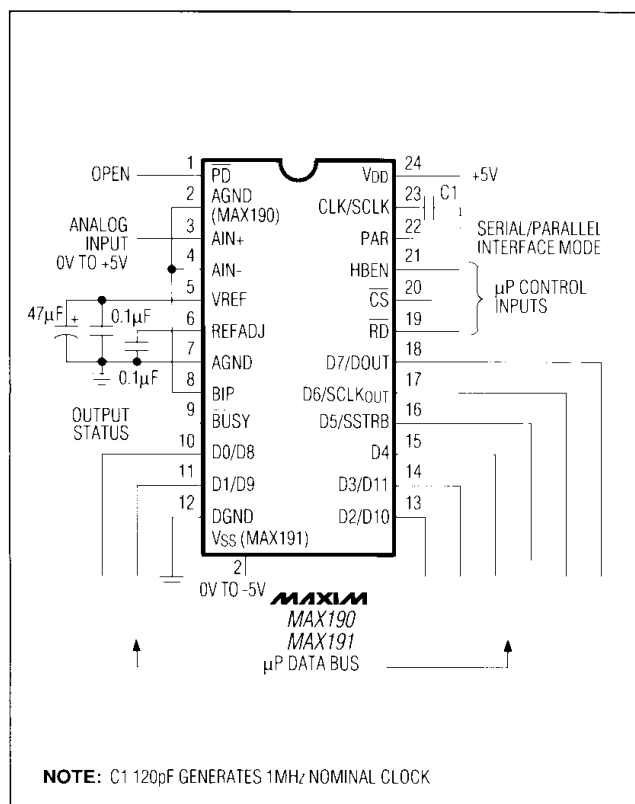


Figure 3. MAX190/MAX191 Operational Diagram

## Detailed Description

The MAX190/MAX191 use successive approximation and input track/hold (T/H) circuitry to convert an analog input signal to a 12-bit digital output. Flexible control logic provides easy interface to microprocessors ( $\mu$ Ps), so most applications require only the addition of passive components. No external hold capacitor is required for the T/H. Figure 3 shows the MAX190/MAX191 in their simplest operational configuration. The MAX190 generates a conversion in 12.5 $\mu$ s, including the T/H acquisition time, and converts input signals in the range of 0V to VREF+. The MAX191 also converts input signals from -VREF/2 to +VREF/2 in 9.5 $\mu$ s, including the T/H acquisition time. The VREF input accepts reference voltages from 2.5V to 5V (see the *Gain and Offset Adjustment* section).

### Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the *Equivalent Input Circuit* (Figure 4). A capacitor switching between the AIN+ and AIN- inputs acquires the signal at the ADC's analog input. At the end of the conversion, the capacitor reconnects to AIN+ and charges to the input signal. An external input buffer is

usually not needed for low-bandwidth input signals (<100Hz) because the ADC disconnects from the input during the conversion. In unbuffered applications, an input filter capacitor reduces conversion noise, but also may limit input bandwidth.

When converting a single-ended input signal, AIN- should be connected to AGND. If a differential signal is connected, consider that the configuration is pseudo differential – only the signal side to the input channel is held by the T/H. The return side (AIN-) must remain stable within  $\pm 0.5$ LSB ( $\pm 0.1$ LSB for best results) with respect to AGND during a conversion. Accomplish this by connecting a 0.1 $\mu$ F capacitor from AIN- to AGND.

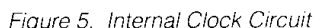
### Analog Input – Track/Hold

The T/H enters its tracking mode when the ADC is deselected ( $\overline{CS}$  pin is held high and  $\overline{BUSY}$  pin is high). Hold mode starts approximately 25ns after a conversion is initiated. The variation in this delay from one conversion to the next (aperture jitter) is about 50ps. Figures 6-10 detail the T/H and interface timing for the various interface modes.

**MAX190/MAX197**



Internal protection diodes, which clamp the analog input to  $V_{DD}$  and GND, allow AIN+ to swing from  $-0.3V$  to  $(V_{DD} + 0.3V)$  on the MAX190 and  $(V_{SS} - 0.3V)$  to  $(V_{DD} + 0.3V)$  on the MAX191 with no risk of damage to the ADC. However, for accurate conversions near full scale, AIN+ should not exceed the power supplies ( $V_{DD}$  and GND for



Alternatively, an external clock (between 100kHz and 1.6MHz) can be applied to CLK. When using an external clock source, acceptable clock duty cycles are between 45% and 55%.

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## Clock and Control Synchronization

For best analog performance on the MAX190/MAX191, the clock should be synchronized to the conversion start signals ( $\overline{CS}$  and  $\overline{RD}$ ) as shown in Figure 6. At least 100ns should separate the start of a conversion from the nearest clock edge. This ensures that CLK transitions are not coupled to the analog input and sampled by the T/H. The magnitude of this feedthrough can be a few millivolts. When the clock and conversion start signals are synchronized, small end-point errors (offset and full-scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be avoided by ensuring that the start of a conversion ( $\overline{RD}$  or  $\overline{CS}$  falling edge) does not occur within 100ns of a clock transition (Figure 6).

## MAX190 Asynchronous Mode

When using the MAX190 in asynchronous mode, where CLK and conversion start signals ( $\overline{CS}$  and  $\overline{RD}$ ) are not synchronous, full-accuracy specification performances are realized with a 0.8MHz clock; this ensures a full 625ns for the most significant bit (MSB) decision. In asynchronous mode, with clock frequencies greater than 0.8MHz, less than 625ns MSB decision times can occur. This shortened decision time can result in linearity errors at mid-scale. Linearity errors can appear in the synchronous mode when the  $\overline{CS}$  and  $\overline{RD}$  to CLK hold ( $t_{16}$ ) and setup ( $t_{17}$ ) times are violated (Figure 6a). Frequency components caused by clock and conversion start-signal overlap can increase the apparent input noise.

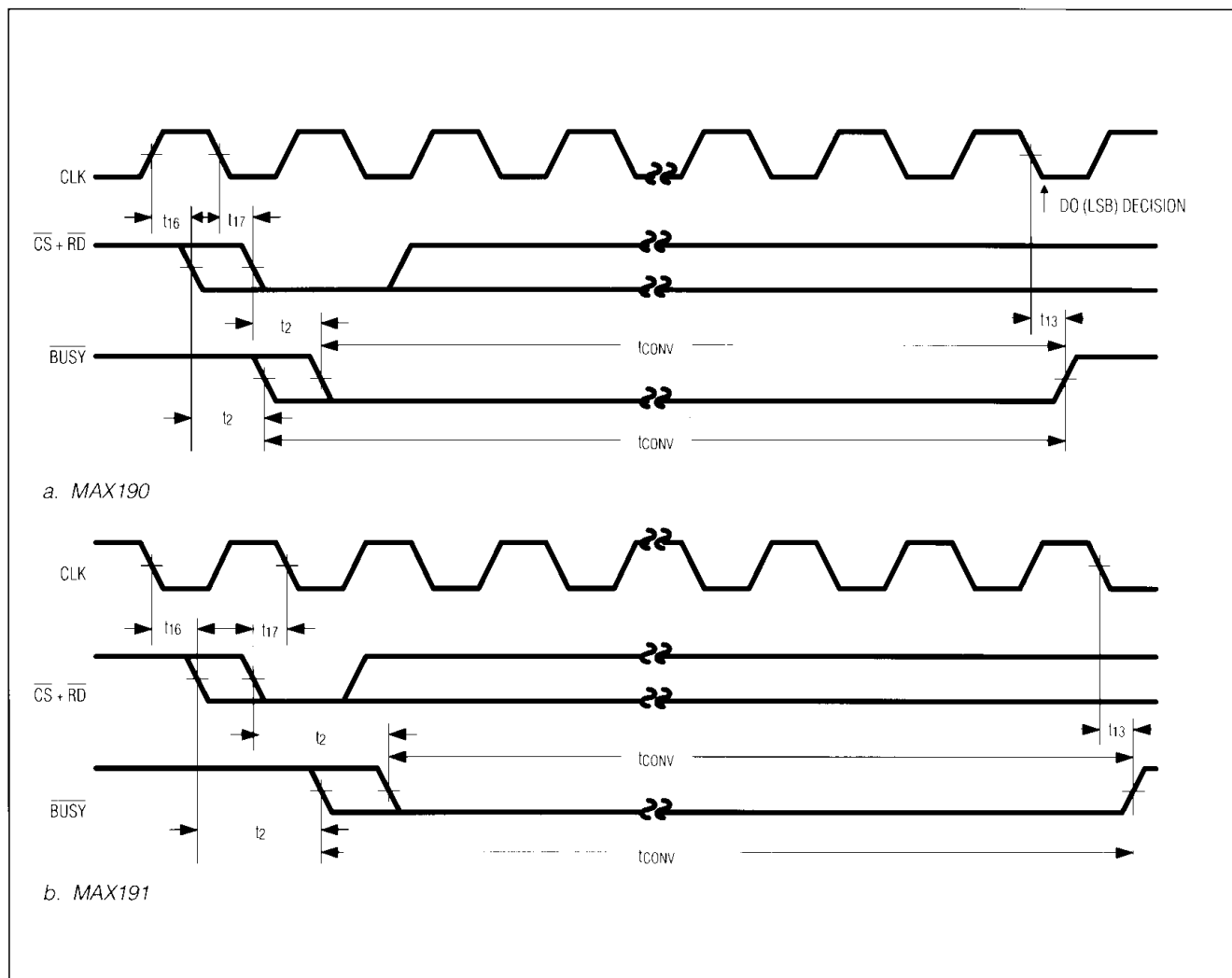


Figure 6.  $\overline{CS}$ ,  $\overline{RD}$ , and CLK Synchronous Operation

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## MAX191 Asynchronous Mode

The above precautions for the MAX190 are not necessary on the MAX191, since conversion always begins on the falling edge of the clock.

## Parallel Digital-Interface Mode

### Output-Data Format

The data output from the MAX190/MAX191 is straight binary in the unipolar mode. In the bipolar mode, the MSB is inverted (see Figure 22). The 12 data bits can be output either in two 8-bit bytes or as a serial output. The data-bus output format is shown in Table 1.

A 2-byte read uses outputs D7-D0. Byte selection is controlled by HBEN. When HBEN is low, the lower 8 bits appear at the data outputs. When HBEN is high, the upper 4 bits appear at D0-D3 with the leading 4 bits low in locations D4-D7.

### Timing and Control

Conversion-start and data-read operations are controlled by the HBEN,  $\overline{CS}$ , and  $\overline{RD}$  digital inputs. A logic low is required on all three inputs to start a conversion, and once the conversion is in progress it cannot be restarted.  $\overline{BUSY}$  remains low during the entire conversion cycle.

The timing diagrams of Figures 7-10 outline two parallel-interface modes and one serial mode.

### Slow-Memory Mode

In slow-memory mode, the device appears to the  $\mu P$  as a slow peripheral or memory. Conversion is initiated with a read instruction (see Figure 7 and Table 2). Set the  $\overline{PAR}$  pin high for parallel interface mode. Beginning with HBEN low, taking  $\overline{CS}$  and  $\overline{RD}$  low starts the conversion. The analog input is sampled on the falling edge of  $\overline{RD}$ .  $\overline{BUSY}$  remains low while the conversion is in progress. The previous conversion result appears at the digital outputs until the end of conversion, when  $\overline{BUSY}$  returns high. The output latches are then updated with the newest results of the 8 LSBs on D7-D0. A second read operation with HBEN high places the 4 MSBs, with 4 leading 0s, on data outputs D7-D0. The second read operation does not start a new conversion because HBEN is high.

### ROM Mode

As in slow-memory mode, D7-D0 are used for 2-byte reads. A conversion starts with a read instruction with HBEN and  $\overline{CS}$  low. The T/H samples the input on the falling edge of  $\overline{RD}$  (see Figure 8 and Table 3).  $\overline{PAR}$  is set high. At this point the data outputs contain the 8 LSBs from the previous conversion. Two more

read operations are needed to access the conversion result. The first occurs with HBEN high, where the 4 MSBs with 4 leading 0s are accessed. The second read, with HBEN low, outputs the 8 LSBs and also starts a new conversion.

Figure 9 and Table 4 show how to read output data within one conversion cycle without starting another conversion. Trigger the falling edge of a read on the rising edge of the first clock cycle after conversion end (when  $\overline{BUSY}$  goes high). As mentioned previously, two more read operations (after  $\overline{BUSY}$  goes high) are needed to access the conversion results. The only difference is that now the low byte can be read first. This happens by allowing the first read operation to occur with HBEN low, where the 8 LSBs are accessed. The second read, with HBEN high, accesses the 4 MSBs with 4 leading 0s.

## Serial-Interface Mode

The serial mode is compatible with Microwire, SPI and QSPI serial interfaces. In addition, a framing signal ( $\overline{SSTRB}$ ) is provided that allows the devices to interface with the TMS320 family of DSPs. Set  $\overline{PAR}$  low for serial mode. Conversion begins when  $\overline{CS}$  goes low, causing the T/H to sample the input (Figure 10). If the  $\overline{CS}$  falling edge occurs when  $\overline{SCLK}$  is low, a conversion begins immediately on the MAX190, otherwise the  $\overline{CS}$  signal is internally latched on the next falling edge of  $\overline{SCLK}$ , beginning the conversion. Conversion always begins on the next falling edge of  $\overline{SCLK}$  on the MAX191, regardless of where  $\overline{CS}$  occurs. The  $\overline{DOUT}$  line remains high-impedance until a conversion begins. During the MSB decision,  $\overline{DOUT}$  remains low (leading 0), while  $\overline{SSTRB}$  goes high to indicate that a data frame is beginning. The data is available at  $\overline{DOUT}$  on the rising edge of  $\overline{SCLK}$  ( $\overline{SCLK}_{OUT}$  when using an internal clock) and transitions on the falling edge.  $\overline{DOUT}$  remains low after all data bits have been shifted out, inserting trailing 0s in the data stream until  $\overline{CS}$  returns high. The  $\overline{SCLK}_{OUT}$  signal is synchronous with the internal or external clock.

For interface flexibility,  $\overline{DOUT}$ ,  $\overline{SCLK}_{OUT}$  and  $\overline{SSTRB}$  signals enter a high-impedance state when  $\overline{CS}$  is set high. When  $\overline{CS}$  is low,  $\overline{RD}$  controls the status of  $\overline{SCLK}_{OUT}$  and  $\overline{SSTRB}$  outputs. A logic low on  $\overline{RD}$  enables  $\overline{SCLK}_{OUT}$  and  $\overline{SSTRB}$ , while a logic low forces both outputs into a high impedance state. Also, with  $\overline{CS}$  low and HBEN high,  $\overline{SCLK}_{OUT}$  drives continuously, regardless of conversion status. This is useful with  $\mu P$ s that require a continuous serial clock. If  $\overline{CS}$  and HBEN are low,  $\overline{SCLK}_{OUT}$  is output only during the conversion cycle, while the converter internal clock runs continuously. This is useful for creating a simple serial-to-parallel interface without shift-register overflow (Figure 11).

# **Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down**

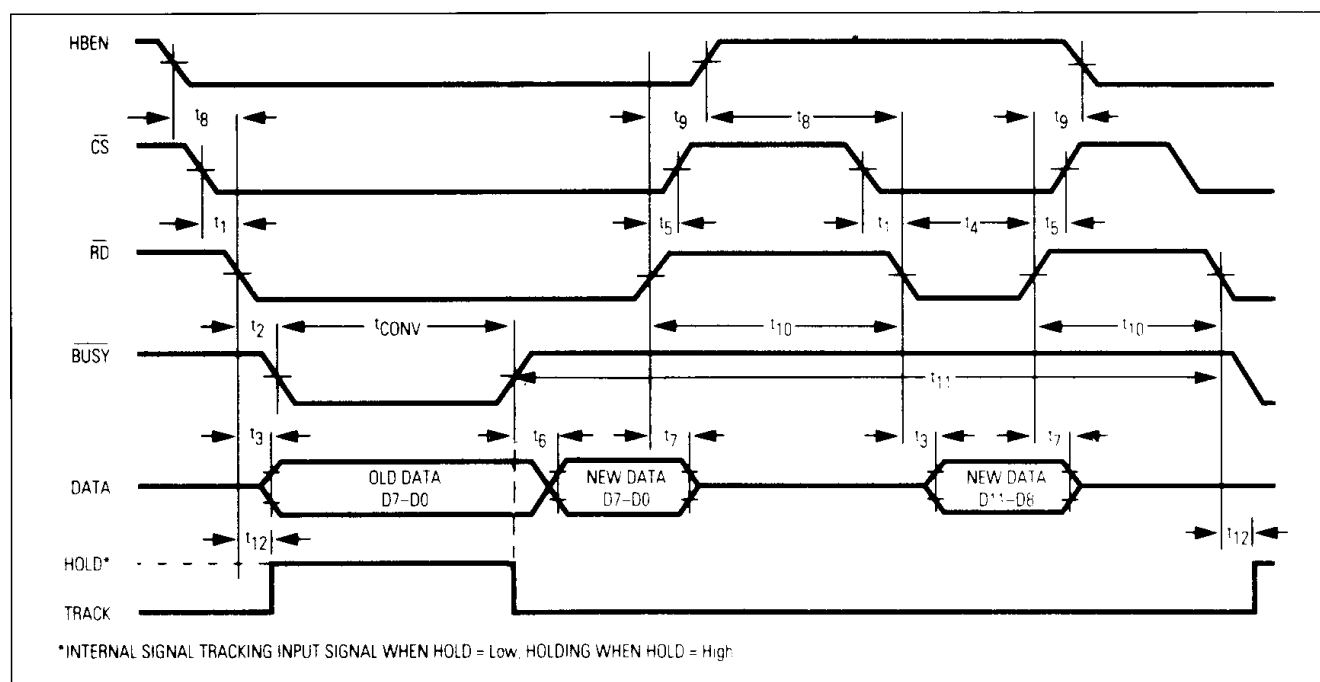


Figure 7. Slow-Memory Mode, 2-Byte Read Data-Bus Status

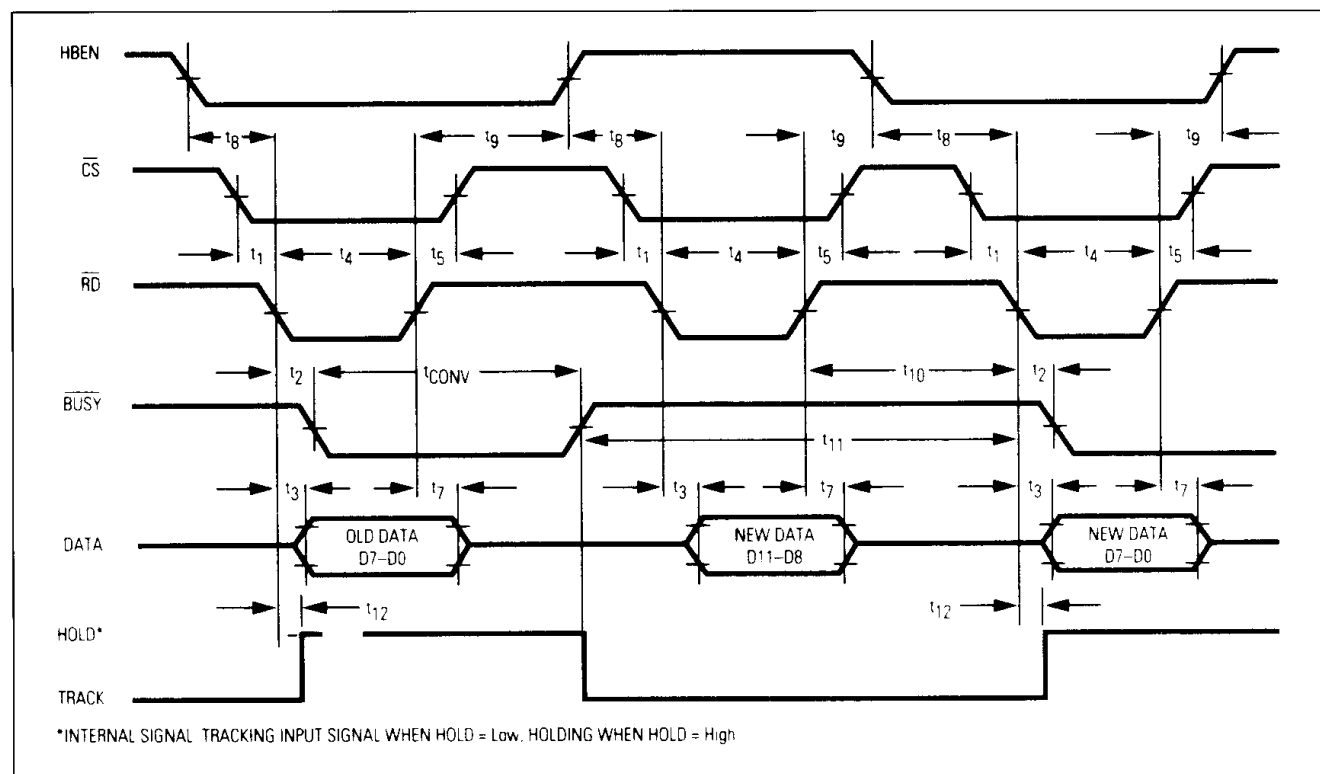


Figure 8. ROM Mode, 2-Byte Read Data-Bus Status

## Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

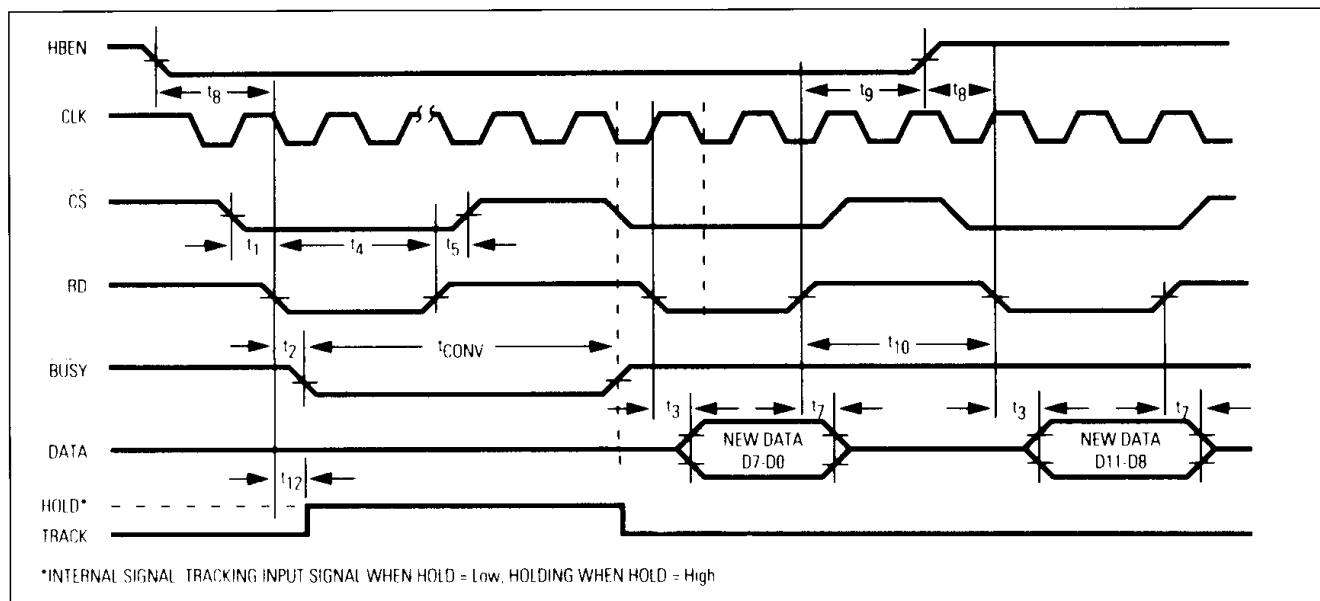


Figure 9. ROM Mode, 2-Byte Read within One Conversion Timing Diagram

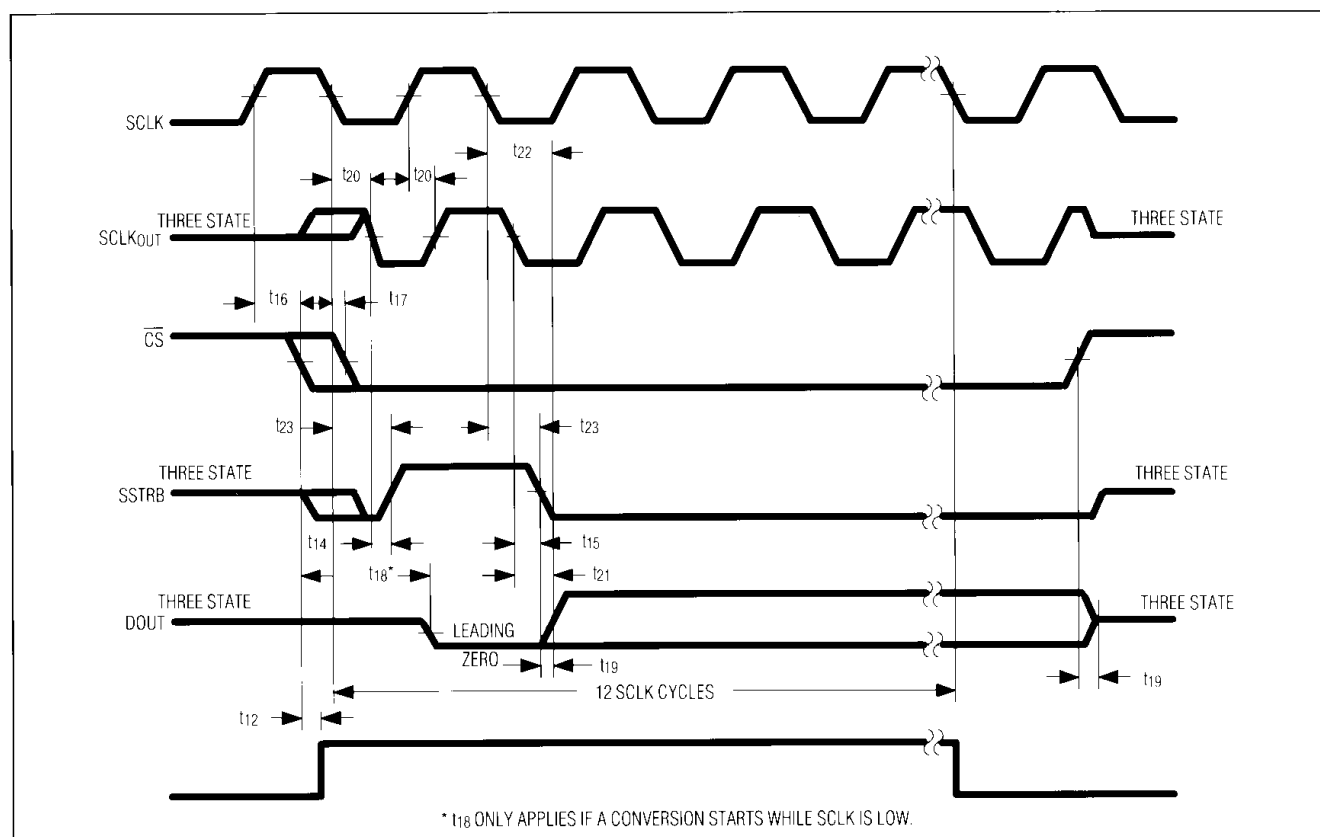


Figure 10a. MAX190 Serial-Interface Mode Timing Diagram ( $\overline{RD} = \text{low}$ )

# **Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down**

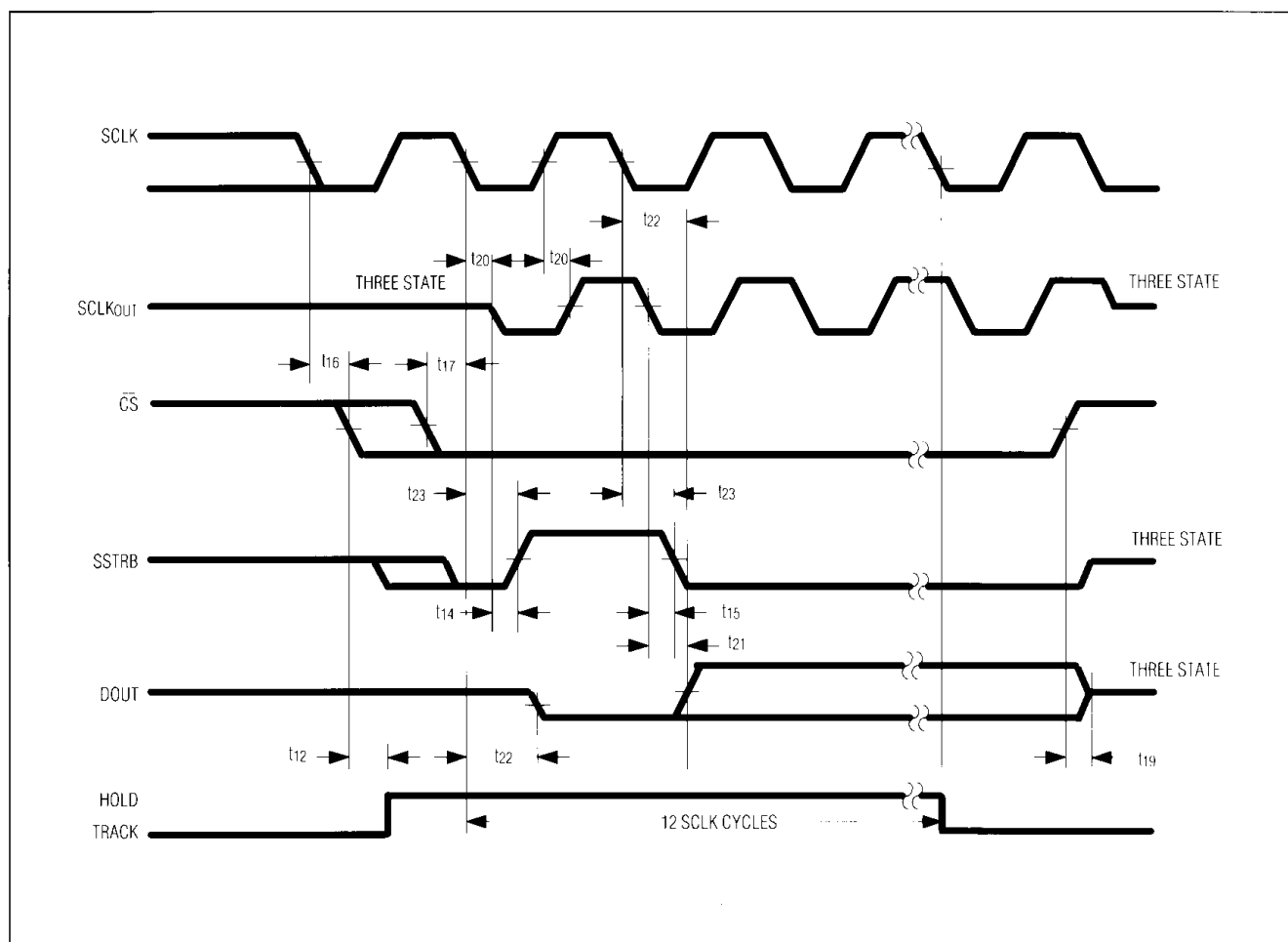


Figure 10b. MAX191 Serial-Interface Mode Timing Diagram ( $\overline{RD} = \text{low}$ )

## Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

**Table 1. Data-Bus Output,  $\overline{CS} = \overline{RD} = \text{Low}$**

| PIN NAME                                  | D7/DOUT | D6/SCLK <sub>OUT</sub> | D5/SSTRB         | D4  | D3/D11 | D2/D10 | D1/D9 | D0/D8 |
|-------------------------------------------|---------|------------------------|------------------|-----|--------|--------|-------|-------|
| HBEN = 0, PAR = 1,<br>PARALLEL MODE       | D7      | D6                     | D5               | D4  | D3     | D2     | D1    | D0    |
| HBEN = 1, PAR = 1,<br>PARALLEL MODE       | Low     | Low                    | Low              | Low | D11    | D10    | D9    | D8    |
| HBEN = X, PAR = 0,<br>SERIAL MODE, RD = 0 | DOUT    | SCLK <sub>OUT</sub>    | SSTRB            | Low | Low    | Low    | Low   | Low   |
| HBEN = X, PAR = 0,<br>SERIAL MODE, RD = 1 | DOUT    | Three-<br>Stated       | Three-<br>Stated | Low | Low    | Low    | Low   | Low   |

**Note:** D7/DOUT – D0/D8 are the ADC data output pins. DOUT = Three-state data output. Data output in serial mode.  
D11 – D0 are the 12-bit conversion results, D11 is the MSB. SCLK<sub>OUT</sub> = Three-state data output. Clock output in serial mode.  
SSTRB = Three state data output. Strobe output in serial mode.

**Table 2. Slow-Memory Mode, 2-Byte Read Data-Bus Status**

| PIN NAME               | D7/DOUT | D6/SCLK <sub>OUT</sub> | D5/SSTRB | D4  | D3/D11 | D2/D10 | D1/D9 | D0/D8 |
|------------------------|---------|------------------------|----------|-----|--------|--------|-------|-------|
| FIRST READ (New Data)  | D7      | D6                     | D5       | D4  | D3     | D2     | D1    | D0    |
| SECOND READ (New Data) | Low     | Low                    | Low      | Low | D11    | D10    | D9    | D8    |

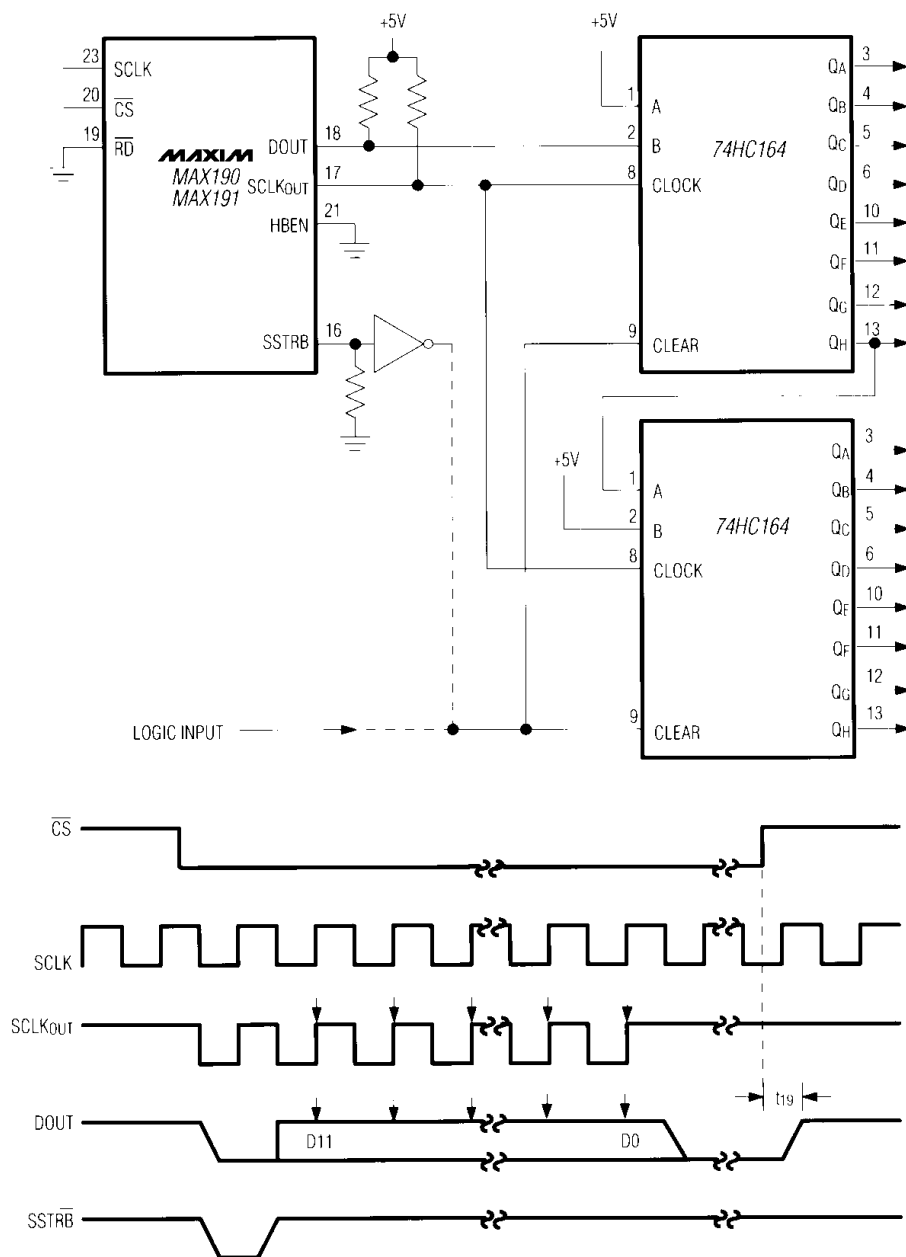
**Table 3. ROM Mode, 2-Byte Read Data-Bus Status**

| PIN NAME               | D7/DOUT | D6/SCLK <sub>OUT</sub> | D5/SSTRB | D4  | D3/D11 | D2/D10 | D1/D9 | D0/D8 |
|------------------------|---------|------------------------|----------|-----|--------|--------|-------|-------|
| FIRST READ (Old Data)  | D7      | D6                     | D5       | D4  | D3     | D2     | D1    | D0    |
| SECOND READ (New Data) | Low     | Low                    | Low      | Low | D11    | D10    | D9    | D8    |
| THIRD READ (New Data)  | D7      | D6                     | D5       | D4  | D3     | D2     | D1    | D0    |

**Table 4. ROM Mode, 2-Byte Read Data-Bus Status without Starting a Conversion Cycle**

| PIN NAME               | D7/DOUT | D6/SCLK <sub>OUT</sub> | D5/SSTRB | D4  | D3/D11 | D2/D10 | D1/D9 | D0/D8 |
|------------------------|---------|------------------------|----------|-----|--------|--------|-------|-------|
| FIRST READ (Old Data)  | D7      | D6                     | D5       | D4  | D3     | D2     | D1    | D0    |
| SECOND READ (New Data) | D7      | D6                     | D5       | D4  | D3     | D2     | D1    | D0    |
| THIRD READ (New Data)  | Low     | Low                    | Low      | Low | D11    | D10    | D9    | D8    |

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down



**NOTE:** USE SSTRB TO GATE PARALLEL DATA TRANSFER FROM SHIFT REGISTER, OR TO CLEAR SHIFT REGISTERS IF DESIRED.

Figure 11. Simple Serial-to-Parallel Interface

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## Maximum Clock Rate in Serial Mode

The maximum SCLK rate depends on the minimum set-up time required at the serial data input to the  $\mu$ P and the ADC's DOUT to SCLK delay ( $t_{22}$ ) (see Figure 12). The maximum  $f_{SCLK}$  is as follows:

$$f_{SCLK}(MAX) = (1/2) \times 1/(t_{su}(M) + t_{22})$$

where  $t_{su}(m)$  is the minimum data set-up time required at the serial data input to the  $\mu$ P. For example, Motorola's MC68HC11A8 data book specifies a 100ns minimum data setup time. Using the worst case for a military grade part of  $t_{22} = 280$ ns (see *Timing Characteristics*) and substituting in the above equation indicates a maximum SCLK frequency of 1.3MHz.

## Using the MAX190/MAX191 with SPI, QSPI and Microwire Serial Interfaces

Figure 13 shows interface connections to the MAX190/MAX191 for common serial-interface standards.

### SPI and Microwire (CPOL=0, CPHA=0)

The MAX190/MAX191 are compatible with SPI, QSPI and Microwire serial-interface standards. When using SPI or QSPI, two modes are available to interface with the MAX190/MAX191. You can set CPOL = 0 and CPHA = 0 (Figure 14a), or set CPOL = 1 and CPHA = 1 (Figure 14b). When using CPOL = 0 and CPHA = 0 with the MAX190, conversion begins and DOUT goes low, from three-state, immediately following the CS falling edge. Therefore, the delay from CS to the first falling edge of SCLK must be at least 625ns for the MSB decision and no more than 50 $\mu$ s to avoid excessive T/H droop. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. Data is available from DOUT on the rising edge of SCLK, and transitions on the falling edge. The first byte contains

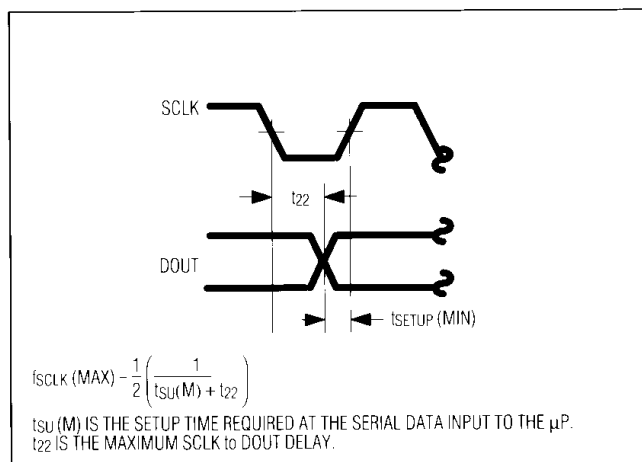


Figure 12.  $f_{SCLK}(MAX)$  is limited by the setup time required by the serial data input to the  $\mu$ P.

a leading 0 and seven MSBs. The second byte contains the remaining five LSBs and three trailing 0s.

When using the MAX191 in this mode, the conversion begins on the first falling edge of SCLK following  $\overline{CS}$  going low. The first byte contains the following, in this order: a reading unknown bit (DOUT will still be in three-state on the first bit), a 0, and six MSBs. The second byte contains the remaining six LSBs and two trailing 0s.

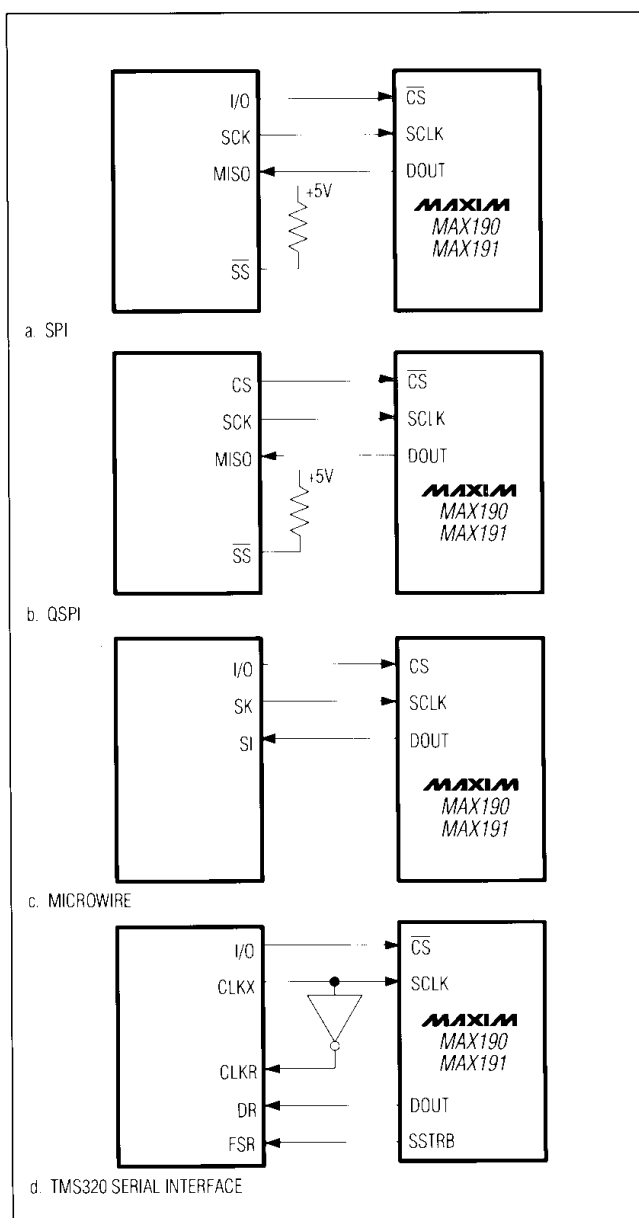


Figure 13. Common Serial-Interface Connections to the MAX190/MAX191

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## SPI (CPOL=1, CPHA=1)

Setting CPOL = 1 and CPHA = 1 starts the clock high during a read instruction. Both the MAX190 and MAX191 will shift out a leading 0 followed by the 12 data bits and three trailing 0s (Figure 14b).

## QSPI

Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles required to clock in the data. The MAX190/MAX191 require thirteen clock cycles from the  $\mu$ P to clock out the 12-bits of data with no trailing 0s in either of the allowable modes (Figure 15).

## TMS320 Serial Interface

Figure 13d shows the pin connections to interface the MAX190/MAX191 to the TMS320. Since the MAX190/MAX191 make data available on the rising edge of SCLK and the TMS320 shifts data in on the falling edge

of CLKR, use CLKX of the DSP to drive SCLK, and CLKX to drive the DSP's CLKR input. The inverter's propagation delay provides more data setup time at the DSP. For example, with no inverter delay, and using  $t_{22} = 280\text{ns}$  and  $f_{\text{SCLK}} = 1.6\text{MHz}$ , the available setup time before the SCLK transition is:

$$\text{setup time} = (1/2 \times f_{\text{SCLK}}) - t_{22} = (1/2 \times 1.6\text{E6}) - 280\text{ns} = 32\text{ns}$$

This still exceeds the minimum DR setup time before the CLKR goes low ( $t_{\text{su}}(\text{DR})$ ) of 13ns, however, a generic 74HC04 provides an additional 20ns setup time (see Figure 13d).

Figure 16 shows the DSP serial interface timing characteristics. The DSP begins clocking data in on the falling edge of CLKR after the falling edge of SSTRB. Following the data transfer, the DSP receive shift register (RSR) contains a 16-bit word consisting of the 12 data bits, MSB first, followed by four trailing 0s.

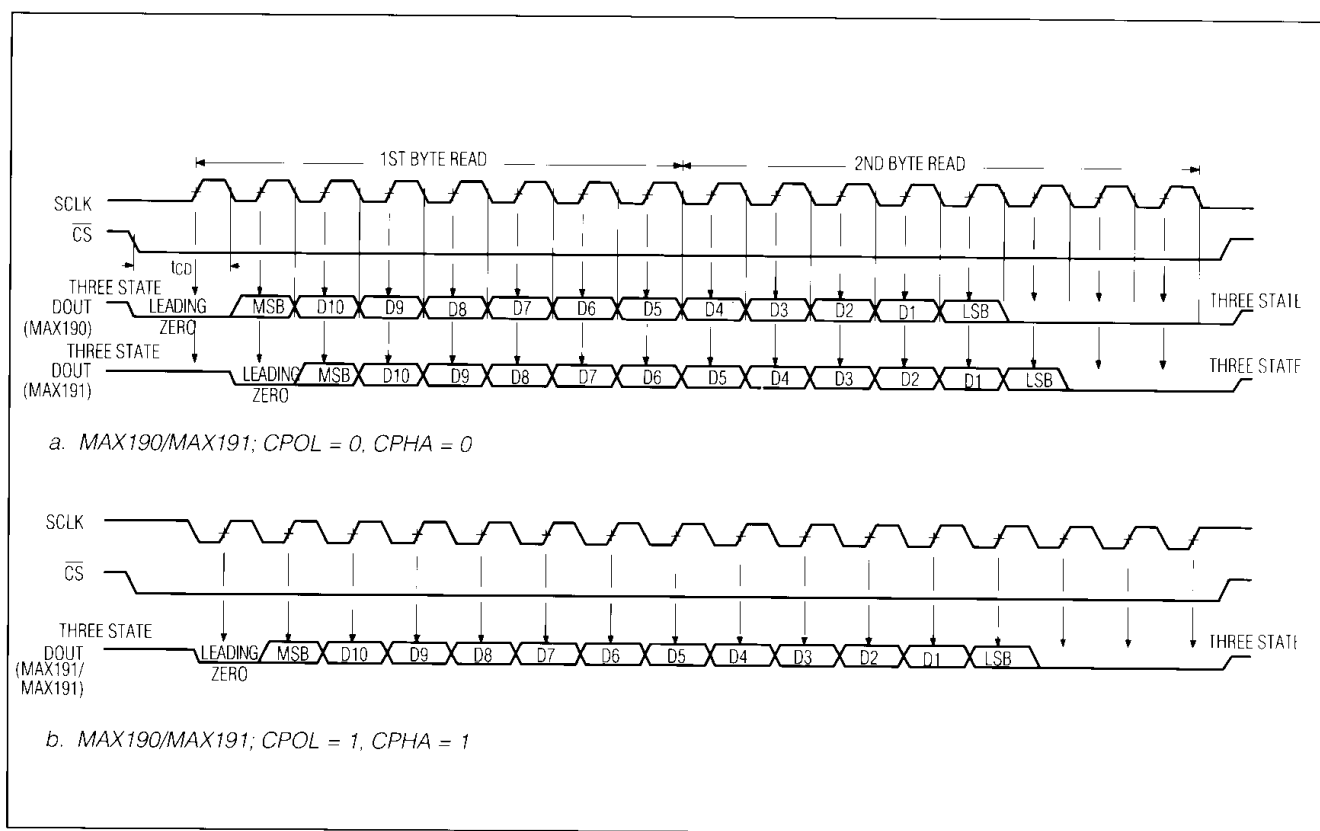


Figure 14. SPI/Microwire Serial-Interface Timing

# **Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down**

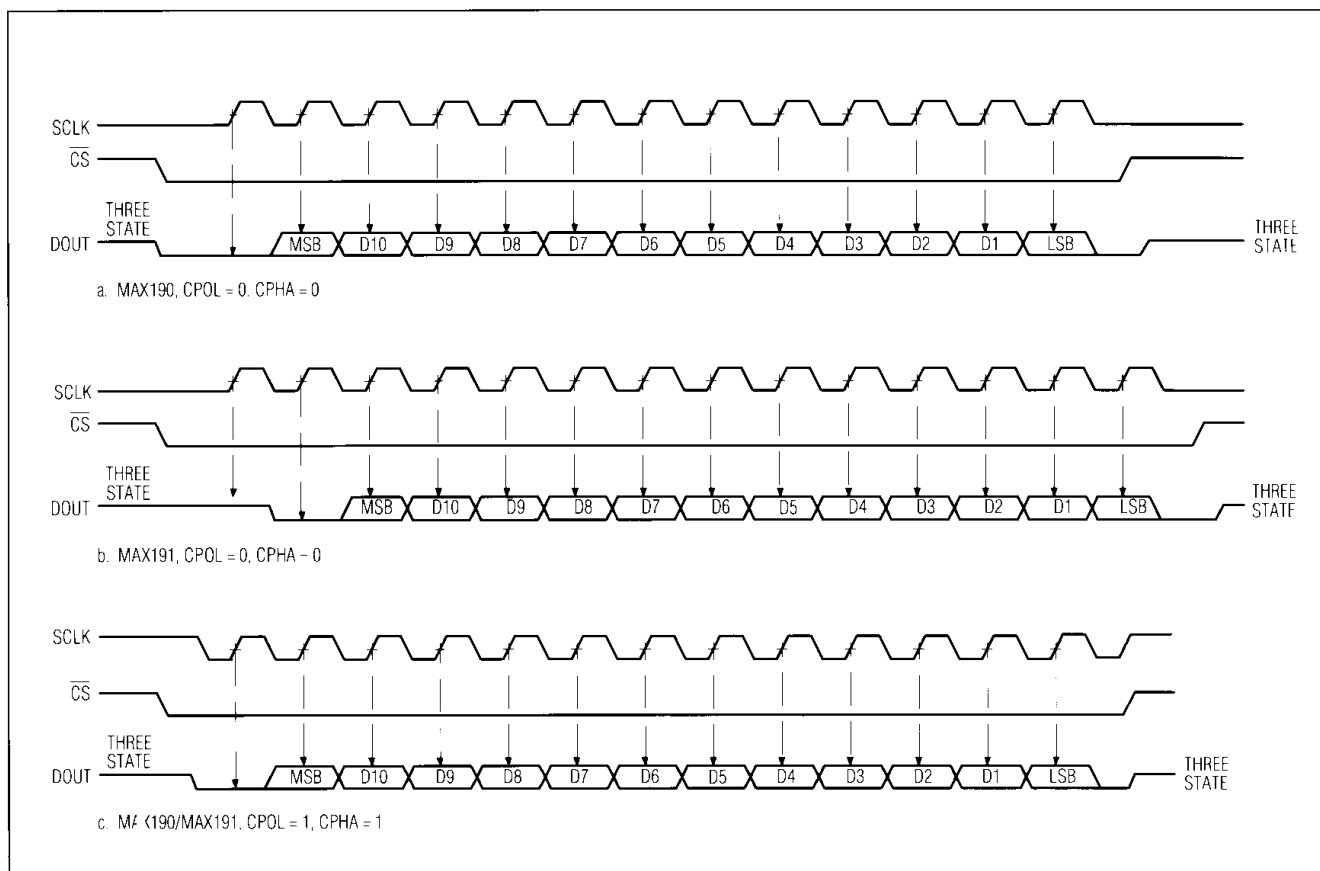


Figure 15. I<sup>2</sup>C Serial-Interface Timing

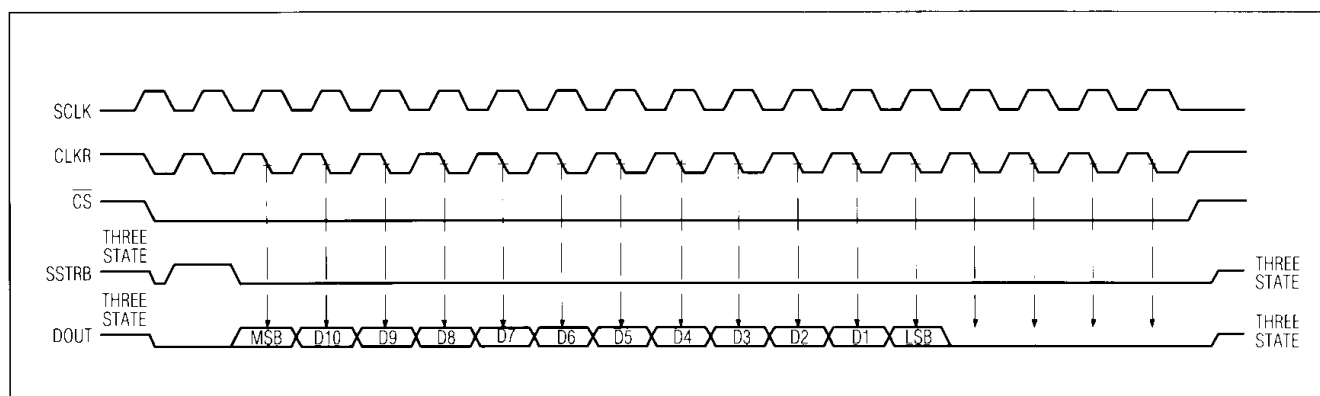


Figure 16. MAX190/MAX191 TMS320C Interface Timing

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## Applications Information

### Power-Down Mode/Initialization After Power-Up

In some battery-powered systems, it is desirable to power down or remove power from the ADC during inactive periods. To power down the MAX190/MAX191, drive  $\overline{\text{PD}}$  low. In this mode, all internal ADC circuitry is off except the reference, and the ADC consumes less than 50 $\mu\text{A}$  max (assuming all signals  $\overline{\text{CS}}$ ,  $\overline{\text{RD}}$ ,  $\text{CLK}$ , and  $\text{HBEN}$  are static and within 200mV of the supplies). To initialize the MAX190/MAX191 at power-up, perform a single conversion and disregard the data outputs. Figure 17 shows a practical way to drive the  $\overline{\text{PD}}$  pin. If you use internal reference compensation, drive  $\overline{\text{PD}}$  between  $\text{V}_{\text{DD}}$  and  $\text{DGND}$  with a  $\mu\text{P}$  I/O pin or other logic device (Figure 17a). For external-reference compensation mode, use the circuit in Figure 17b to drive  $\overline{\text{PD}}$  between  $\text{DGND}$  and the floating voltage of  $\overline{\text{PD}}$ . An alternative is to drive  $\overline{\text{PD}}$  with three-state logic or a switch, provided the off leakage does not exceed 100nA.

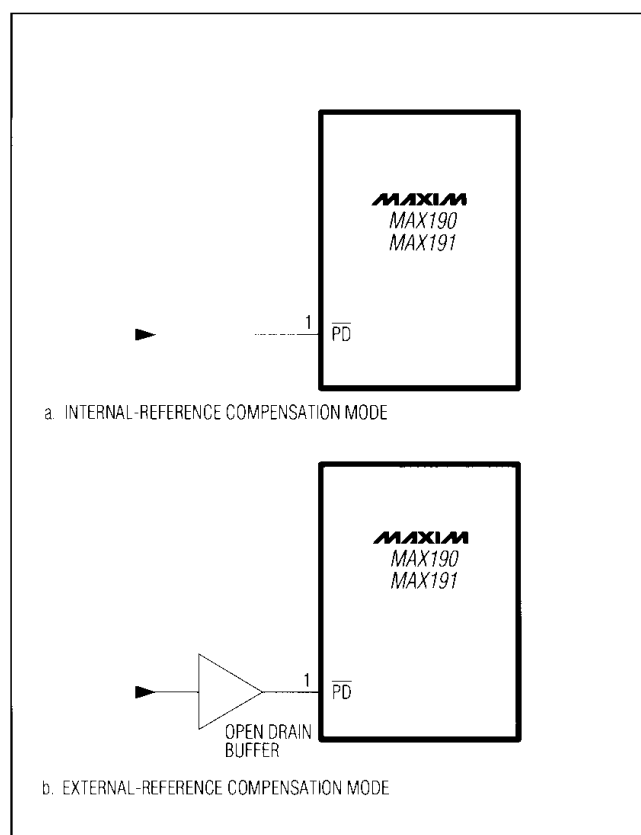


Figure 17. Drive Circuits for  $\overline{\text{PD}}$  pin

## Internal Reference

The internal 4.096V reference is available at  $\text{V}_{\text{REF}}$  and must be bypassed to  $\text{AGND}$  with a 4.7 $\mu\text{F}$  low-ESR capacitor (less than  $1/2\Omega$ ) in parallel with a 0.1 $\mu\text{F}$  capacitor, unless internal-reference compensation mode is used (see the *Internal Reference Compensation* section). This minimizes noise and maintains a low reference impedance at high frequencies. The reference output can be disabled by connecting  $\text{REFADJ}$  to  $\text{V}_{\text{DD}}$  when using an external reference.

## Reference-Compensation Modes

In the MAX190/MAX191, power-down performance can be optimized for a given conversion rate by selecting either internal or external reference compensation.

## Internal Compensation

The connection for internal compensation is shown in Figure 18a. In this mode, the reference stabilizes quickly enough so that a conversion typically starts within 35 $\mu\text{s}$  after the ADC is reactivated ( $\overline{\text{PD}}$  pulled high). In this compensation mode, the reference buffer requires longer recovery time from SAR transients, therefore requiring a slower clock (and conversion time). With internal reference compensation, the typical conversion time rises to 25 $\mu\text{s}$  (Figure 18b). Figure 18c illustrates the typical average supply current vs. conversion rate, which can be achieved using power-down between conversions.

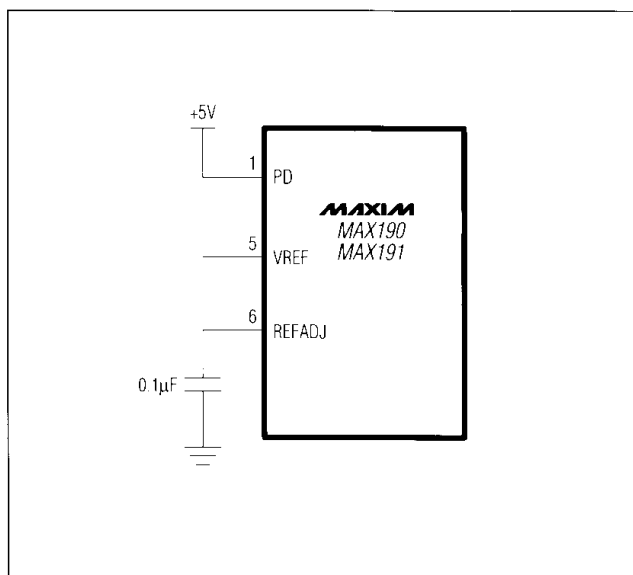


Figure 18a. Internal-Compensation Mode Circuit

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

MAX190/MAX191

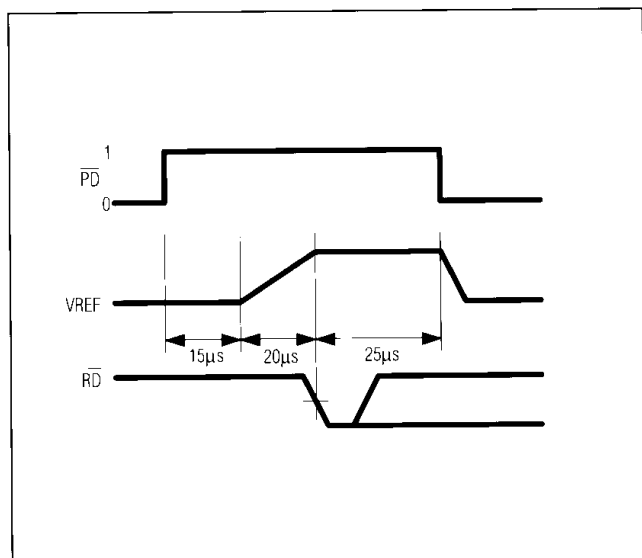


Figure 18b. Low Average-Power Mode Operation (Internal Compensation)

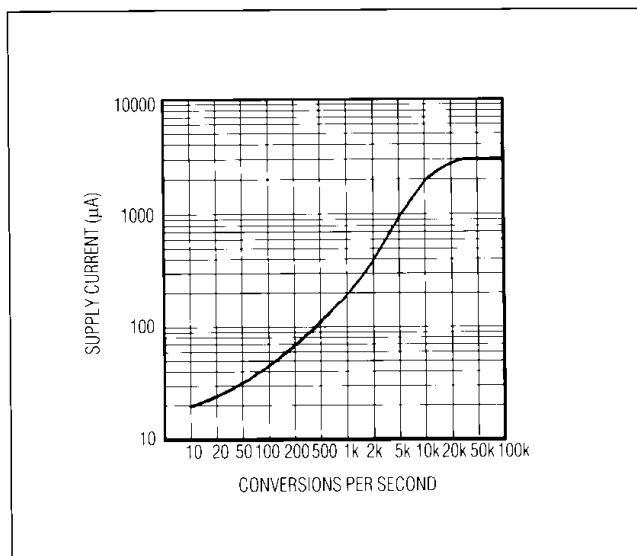


Figure 18c. Average Supply Current vs. Conversion Rate. Powering Down Between Conversions

## External Compensation

Figure 19a shows the connection for external compensation with reference adjustment. In this mode, an external 4.7μF capacitor compensates the reference output amplifier, allowing for maximum conversion speed and lowest conversion noise. However, when reactivating the ADC after power-down, the reference takes typically 2ms to fully charge the 4.7μF capacitor, so more time is required before a conversion can start (Figure 19b). Thus, the average current consumed in power-up/power-down operations is higher in external compensation mode than in internal compensation mode.

## Gain and Offset Adjustment

Figure 20 depicts the nominal, unipolar input/output (I/O) transfer function of the MAX190/MAX191, and Figure 22 shows the bipolar I/O transfer function for the MAX191. Code transitions occur halfway between successive integer LSB values. Note that 1LSB = 1.00mV (4.096V/4096) for unipolar operation and 1LSB = 1.00mV ((4.096V/2 - -4.096V/2)/4096) for bipolar operation.

Figures 19a and 21a show how to adjust the ADC gain in applications that require full-scale range adjustment. The connection shown in Figure 21a provides ±0.5% for ±20LSBs of adjustment range and is recommended for applications that use an external reference. On the other

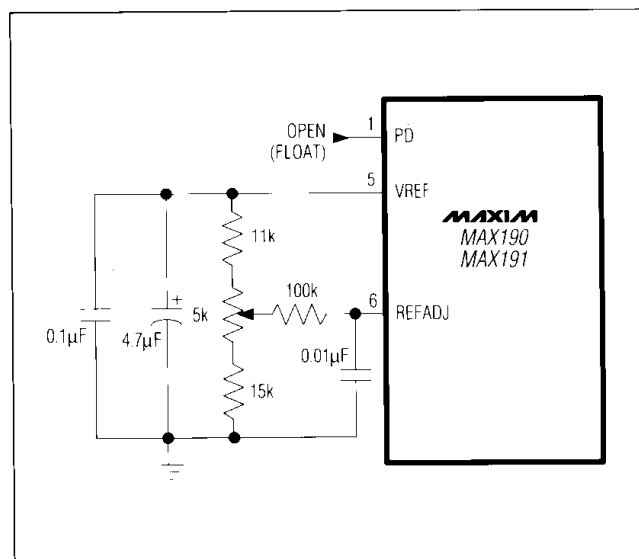


Figure 19a. External-Compensation Mode with Internal Reference Adjustment Circuit

hand, Figure 19a is recommended for applications that use the internal reference, because it uses fewer external components.

## Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

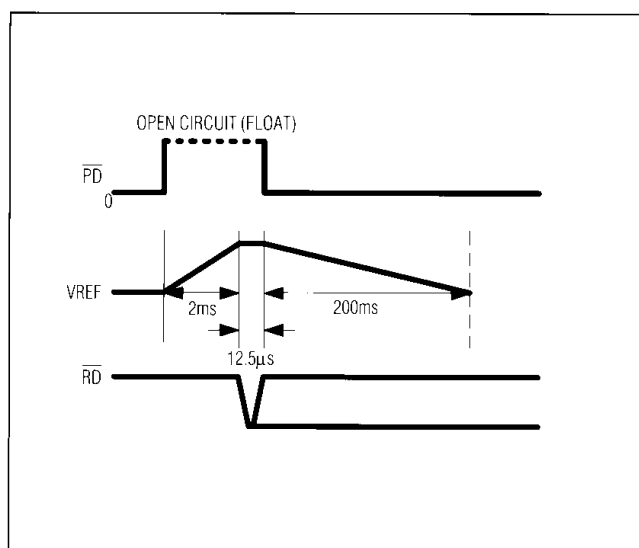


Figure 19b. Low Average-Power Mode Operation (External Compensation)

If both offset and full scale need adjustment, the circuit in Figure 21b is recommended. For single-supply ADCs, it is virtually impossible to null system negative offset errors. However, the MAX190/MAX191 input configuration is pseudo-differential – only the difference in voltage between AIN+ and AIN- will be converted into its digital representation. By applying a small positive voltage to AIN-, the 0 input voltage at AIN+ can be adjusted to above or below AIN- voltage, thus nulling positive or negative system offset errors. R9 and R10 can be removed for applications that require only positive system errors to be nulled. To trim the offset error of the MAX190/MAX191, apply 1/2LSB to the analog input and adjust R6 so the digital output code changes between 000 000 000 and 000 000 001. To adjust full scale, apply FS - 1½LSBs and adjust R2 until the output code changes between 1111 1111 1110 and 111 111 111 111. Because interaction occurs between adjustments, offset should be adjusted before gain. For an input gain of two, remove R7 and R8.

The MAX190 accepts input voltages between AGND and  $V_{DD}$ ; input signals below ground cannot be converted. The full-scale range of the MAX190 is from 0V to VREF. The MAX190 can be configured for bipolar operation on its pseudo-differential input. Instead of using AIN- as an analog input return, AIN- can be set to a different **positive** potential voltage above ground (BIP pin is set high). The sampled analog input (AIN+) can swing to any positive voltage above and below AIN-, and the ADC performs bipolar conversions with respect to AIN-. The MAX191 accepts input voltages from

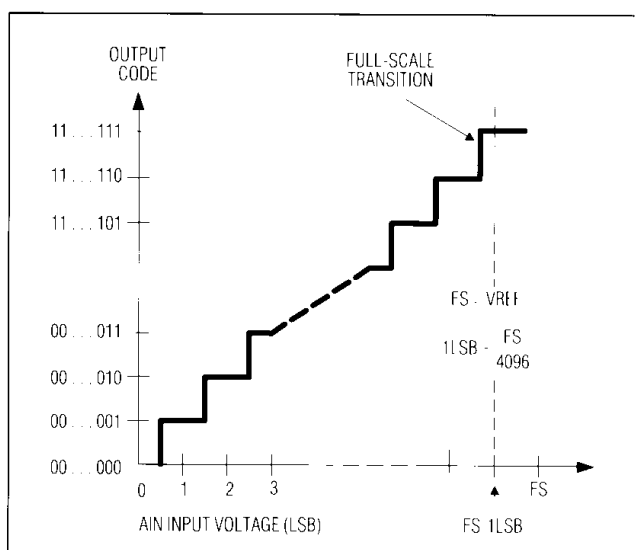


Figure 20. MAX190/MAX191 Unipolar Transfer Function

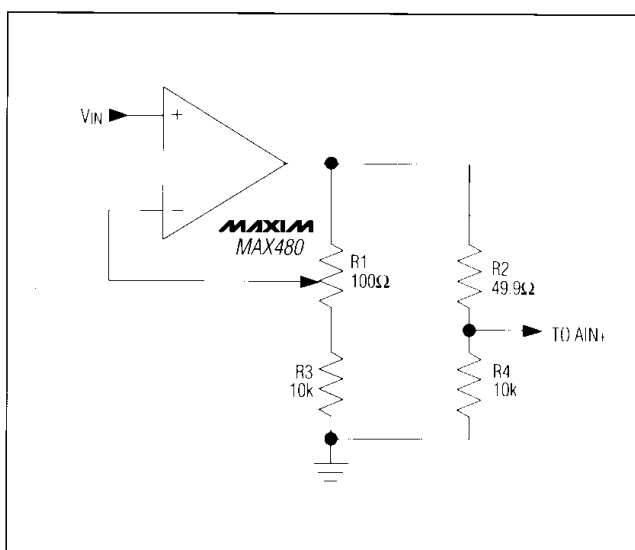


Figure 21a. Trim Circuit for Gain ( $\pm 0.5\%$ )

AGND to  $V_{DD}$  while operating from a single supply and  $V_{SS}$  to  $V_{DD}$  when operating from dual supplies. Figure 22 shows the bipolar input transfer function with AIN- connected to midscale for single-supply operation and connected to GND for MAX191 operating from dual supplies. When operating from a single supply, the MAX191 has the same full-scale range as the MAX190; when operating from dual supplies, the MAX191 full-scale range is from  $-V_{REF}/2$  to  $+V_{REF}/2$ .

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

MAX190/MAX191

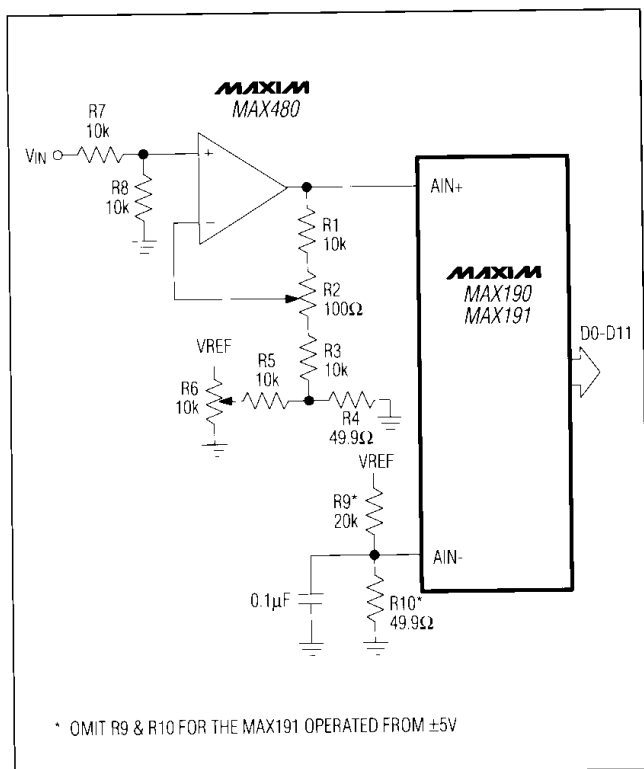


Figure 21b. Offset ( $\pm 10\text{mV}$ ) and Gain ( $\pm 1\%$ ) Trim Circuit

## Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, crosstalk from the data pins to the ADC comparator may generate errors. Slow-memory mode avoids this problem by placing the  $\mu\text{P}$  in a wait state during the conversion. In ROM mode, if the data bus is active during the conversion, it should be isolated from the ADC using three-state drivers.

The ADC generates considerable digital noise in ROM mode when RD or CS go high and the output data drivers are disabled after a conversion has started. This noise can cause large errors if it occurs when the SAR latches a comparator decision. To avoid this problem, RD and CS should be active for less than one clock cycle. If this is not possible, RD or CS should go high at the rising edge of CLK, since the comparator output is always latched on falling edges of CLK.

## Layout, Grounding, Bypassing

Use printed circuit boards for best system performance. Wire-wrap boards are not recommended. Board layout should ensure that digital- and analog-signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

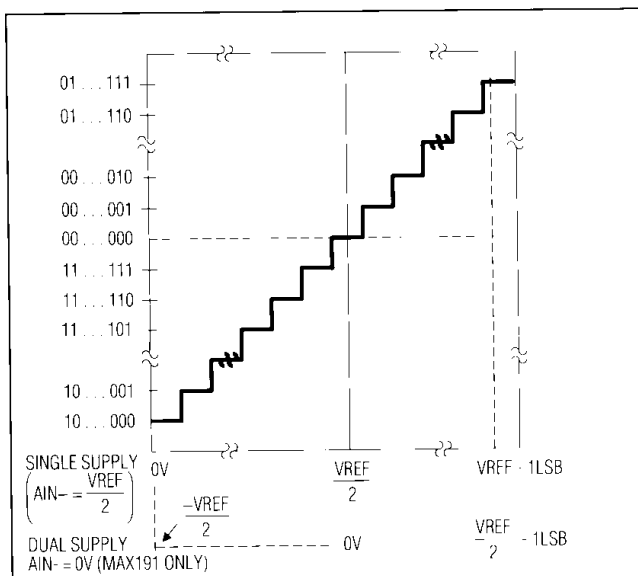


Figure 22. MAX190/MAX191 Bipolar Transfer Function

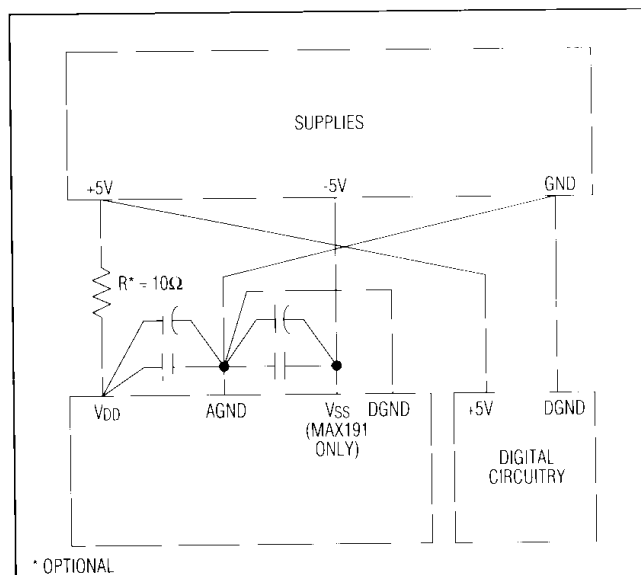


Figure 23. Power-Supply Grounding Connection

Figure 23 shows the recommended system ground connections. Established a single-point analog ground ("star" ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to it. No other digital-system ground should be connected to this single-point analog ground. The ground return to the power supply for this star ground should be low impedance and as short as possible for noise-free operation.

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

High-frequency noise in the  $V_{DD}$  power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.01 $\mu$ F and 10 $\mu$ F bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10 $\Omega$  resistor can be connected as a lowpass filter to filter out supply noise (Figure 23).

## Dynamic Performance

High-speed sampling capability and throughput (MAX190 = 76kHz, MAX191 = 100kHz) make the MAX190/MAX191 ideal for wideband-signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm, which determines its spectral content. Conversion errors are then seen as spectral elements outside the fundamental input frequency. FFT plots for both the MAX190 and MAX191 are shown in the *Typical Operating Characteristics*.

ADCs have traditionally been evaluated by specifications such as Zero and Full-Scale Error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

## Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals, except signal harmonics. Signal-to-Noise + Distortion ratio (SINAD) is the same as the SNR, but includes signal harmonics.

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution:  $SNR = (6.02n + 1.76)$  dB, where  $n$  is the number of bits of resolution. 74dB is the SNR of a perfect 12-bit ADC.

By transposing the equation that converts resolution to SNR we can compute the effective resolution or the "effective number of bits" the ADC provides from the measured SNR:

$$n = (SNR - 1.76)/6.02$$

## Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20\text{Log} \left[ \sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + \dots + V_n^2)} / V_1 \right]$$

where  $V_1$  is the fundamental RMS amplitude and  $V_2$  to  $V_n$  are the amplitudes of the 2nd through  $n$ th harmonics.

## Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency. But if the ADC is exceptionally linear, it can occur at a random peak in the ADC's noise floor.

## Opto-Isolated A/D Interface

Many industrial applications require isolation to prevent excessive current flow where ground disparities exist between the ADC and the rest of the system. In Figure 24, a MAX250 and four 6N136 optocouplers create an isolation barrier between the MAX190/MAX191 and  $\mu$ P.

The 6N136 optocouplers limit the maximum data rate to 90kbps. This requires a slower clock, and therefore a longer conversion time.

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

MAX190/MAX191

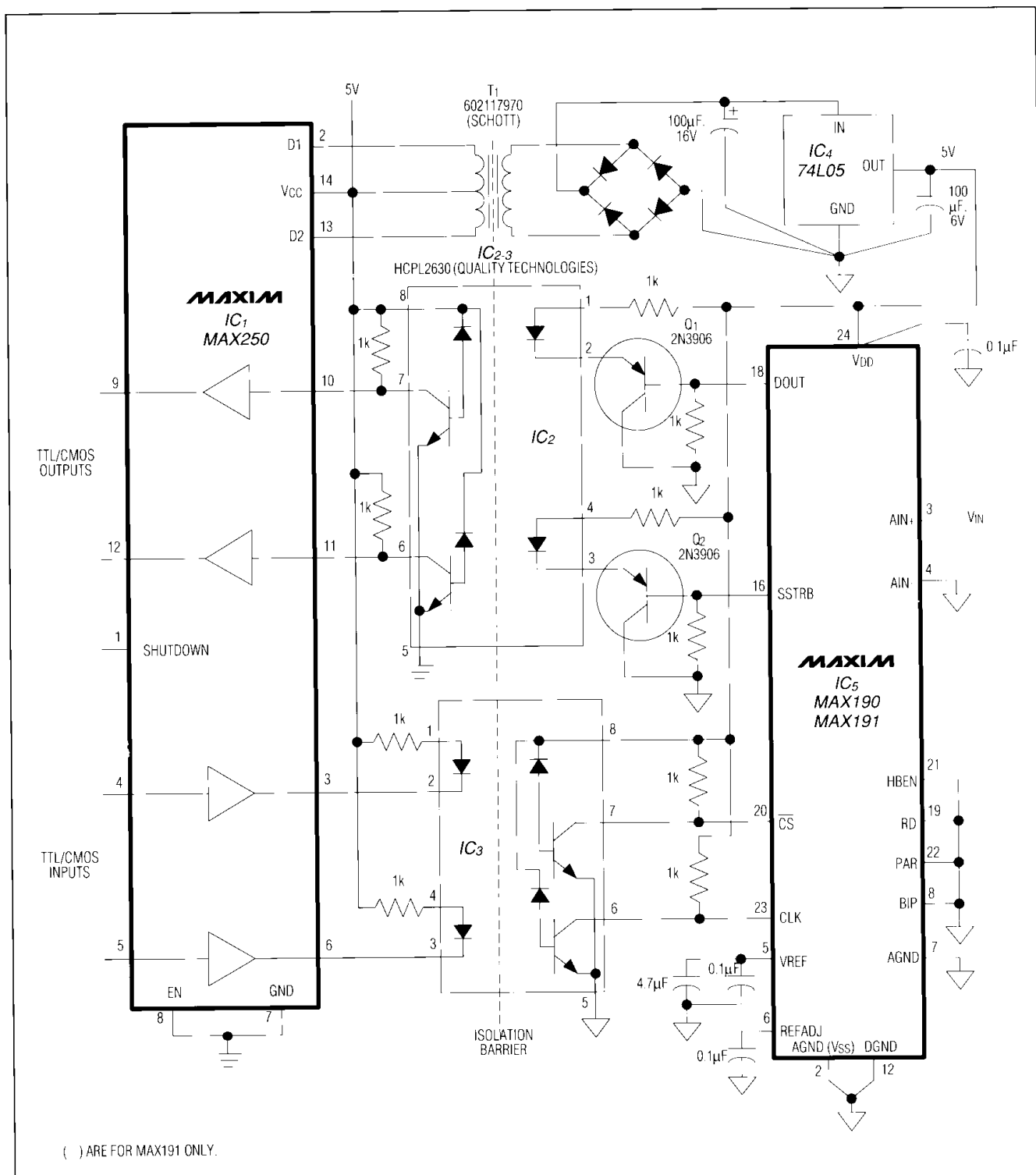


Figure 24. Isolated Data-Acquisition Circuit

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

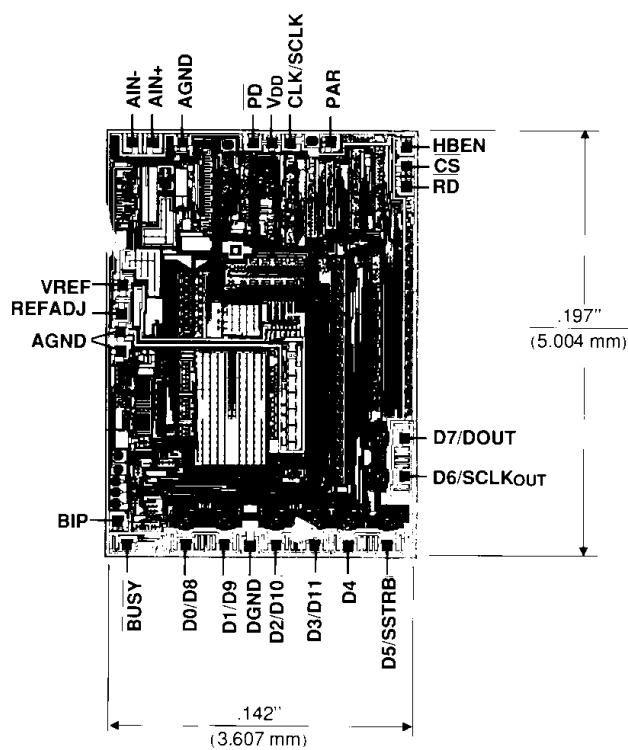
## Ordering Information (continued)

| PART       | TEMP. RANGE     | PIN-PACKAGE           | ERROR (LSBs) |
|------------|-----------------|-----------------------|--------------|
| MAX191ACNG | 0°C to +70°C    | 24 Narrow Plastic DIP | ±1/2         |
| MAX191BCNG | 0°C to +70°C    | 24 Narrow Plastic DIP | ±1           |
| MAX191ACWG | 0°C to +70°C    | 24 Wide SO            | ±1/2         |
| MAX191BCWG | 0°C to +70°C    | 24 Wide SO            | ±1           |
| MAX191BC/D | 0°C to +70°C    | Dice*                 | ±1           |
| MAX191AENG | -40°C to +85°C  | 24 Narrow Plastic DIP | ±1/2         |
| MAX191BENG | -40°C to +85°C  | 24 Narrow Plastic DIP | ±1           |
| MAX191AEWG | -40°C to +85°C  | 24 Wide SO            | ±1/2         |
| MAX191BEWG | -40°C to +85°C  | 24 Wide SO            | ±1           |
| MAX191AMRG | -55°C to +125°C | 24 Narrow CERDIP**    | ±1/2         |
| MAX191BMRG | -55°C to +125°C | 24 Narrow CERDIP**    | ±1           |

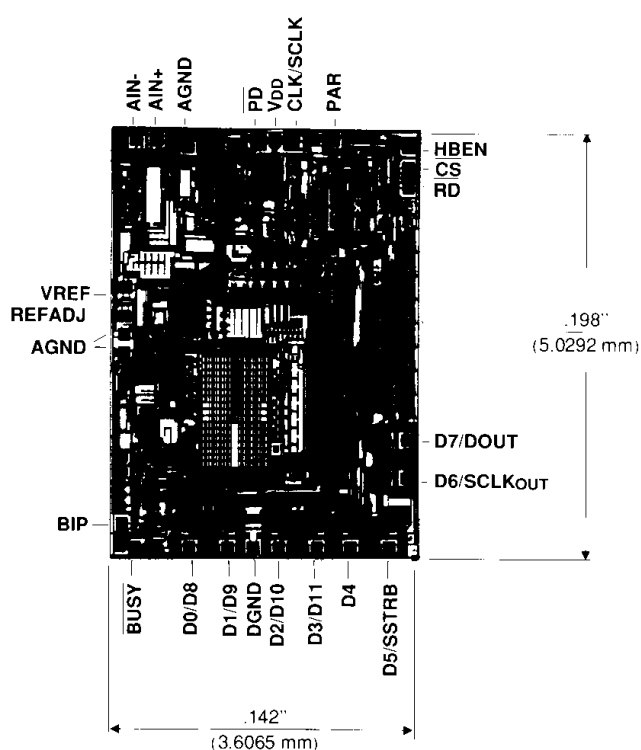
\* Dice are specified at  $T_A = +25^\circ\text{C}$ , DC parameters only.

\*\*Contact factory for availability and processing to MIL-STD-883.

## Chip Topographies



MAX190

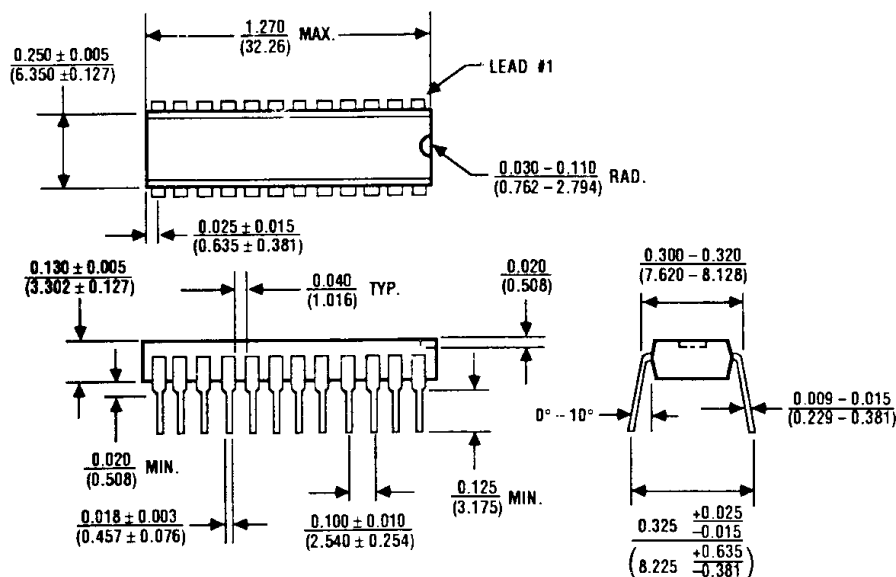


MAX191

# Low-Power, 12-Bit Sampling ADCs with Internal Reference and Power-Down

## Package Information

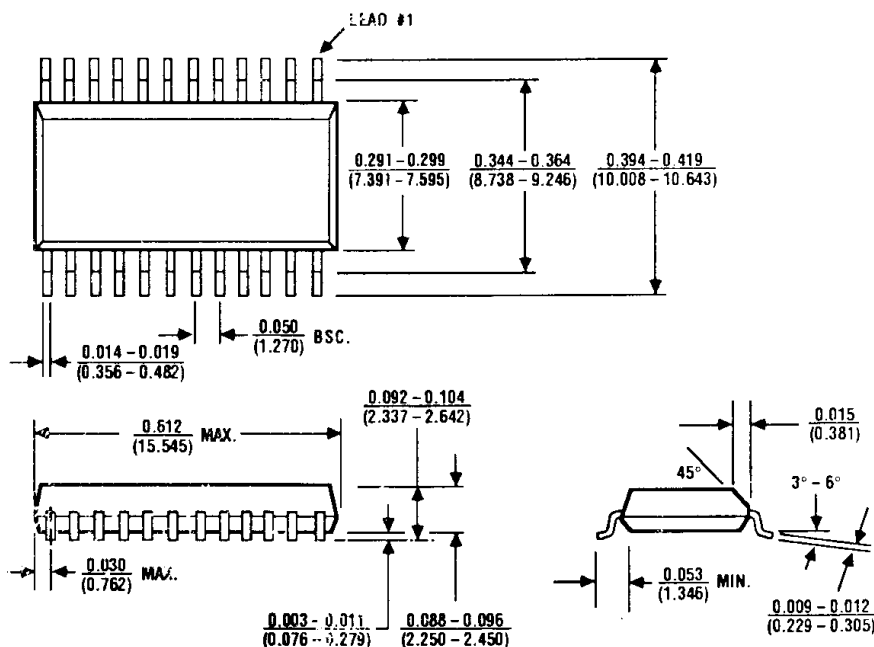
MAX190/MAX191



### 24 Lead Plastic Narrow DIP

$$\theta_{JA} = 120^{\circ}\text{C/W}$$

$$\theta_{JC} = 60^{\circ}\text{C/W}$$



### 24 Lead Small Outline, Wide

$$\theta_{JA} = 85^{\circ}\text{C/W}$$

$$\theta_{JC} = 45^{\circ}\text{C/W}$$

# MAX190/MAX191

Figure 1 shows the mechanical drawing of the MAX120 package. The top view is a rectangle with dimensions 0.750 inches (19.05 mm) by 0.300 inches (7.62 mm). The side view shows a package with a height of 0.15 inches (3.81 mm) and a pin pitch of 0.05 inches (1.27 mm). The bottom view shows the pin locations. The drawing is labeled with dimensions in inches and millimeters.

| Symbol | Value | Unit | Value | Unit |
|--------|-------|------|-------|------|
| A      | 0.150 | in   | 3.81  | mm   |
| B      | 0.750 | in   | 19.05 | mm   |
| C      | 0.300 | in   | 7.62  | mm   |
| D      | 0.050 | in   | 1.27  | mm   |
| E      | 0.050 | in   | 1.27  | mm   |
| F      | 0.050 | in   | 1.27  | mm   |
| G      | 0.050 | in   | 1.27  | mm   |
| H      | 0.050 | in   | 1.27  | mm   |
| I      | 0.050 | in   | 1.27  | mm   |
| J      | 0.050 | in   | 1.27  | mm   |
| K      | 0.050 | in   | 1.27  | mm   |
| L      | 0.050 | in   | 1.27  | mm   |
| M      | 0.050 | in   | 1.27  | mm   |
| N      | 0.050 | in   | 1.27  | mm   |
| O      | 0.050 | in   | 1.27  | mm   |
| P      | 0.050 | in   | 1.27  | mm   |
| Q      | 0.050 | in   | 1.27  | mm   |
| R      | 0.050 | in   | 1.27  | mm   |
| S      | 0.050 | in   | 1.27  | mm   |
| T      | 0.050 | in   | 1.27  | mm   |
| U      | 0.050 | in   | 1.27  | mm   |
| V      | 0.050 | in   | 1.27  | mm   |
| W      | 0.050 | in   | 1.27  | mm   |
| X      | 0.050 | in   | 1.27  | mm   |
| Y      | 0.050 | in   | 1.27  | mm   |
| Z      | 0.050 | in   | 1.27  | mm   |

28 **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 (408) 737-7600**