

Surge and Over-Voltage Protection Switch for VBUS

FPF2280

Description

The FPF2280 features a low- R_{ON} internal FET and an operating range of 2.5 V_{DC} to 5.5 V_{DC} (absolute maximum of 29 V_{DC}). An internal clamp is capable of shunting surge voltages > 100 V, protecting downstream components and enhancing system robustness. The FPF2280 features over-voltage protection that powers down the internal FET if the input voltage exceeds the OVP threshold. The OVP threshold is adjustable with optional external resistors. Over-temperature protection also powers down the device at 130°C (typical). Exceptionally low off-state current (< 1 μ A maximum) facilitates compliance with standby power requirements.

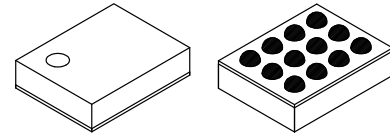
The FPF2280 is available in a fully “green” compliant 1.3 mm $\times$ 1.8 mm Wafer-Level Chip-Scale Package (WLCSP) with backside laminate.

Features

- Surge Protection
 - ◆ IEC 61000-4-5: > 100 V
- Over-Voltage Protection (OVP)
- Over-Temperature Protection (OTP)
- ESD Protection
 - ◆ Human Body Model (HBM): > 3.5 kV
 - ◆ Charged Device Model (CDM): > 2 kV
 - ◆ IEC 61000-4-2 Air Discharge: > 15 kV
 - ◆ IEC 61000-4-2 Contact Discharge: > 8 kV
- This is a Pb-Free Device

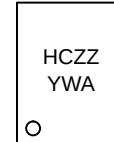
Typical Applications

- Mobile Handsets and Tablets
- Portable Media Players
- MP3 Players



WLCSP12 1.288x1.828x0.586
CASE 567QX

MARKING DIAGRAM



- | | |
|----|------------------------|
| HC | = Specific Device Code |
| ZZ | = Assembly Lot Code |
| Y | = Year |
| W | = Work Week |
| A | = Assembly Location |

ORDERING INFORMATION

Part Number	Top Marking	Operating Temperature Range	Package	Shipping [†]
FPF2280BUCX-F130	HC	-40°C to +105°C	WLCSP12 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FPF2280

Block Diagram

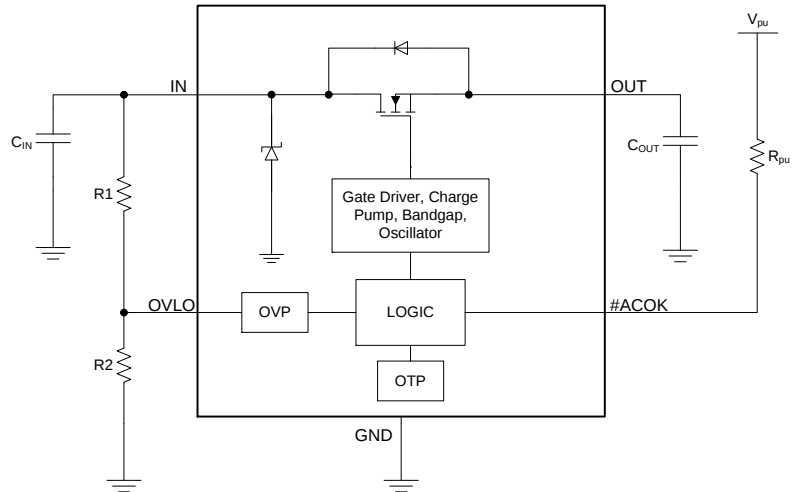


Figure 1. Functional Block Diagram

Pin Configuration

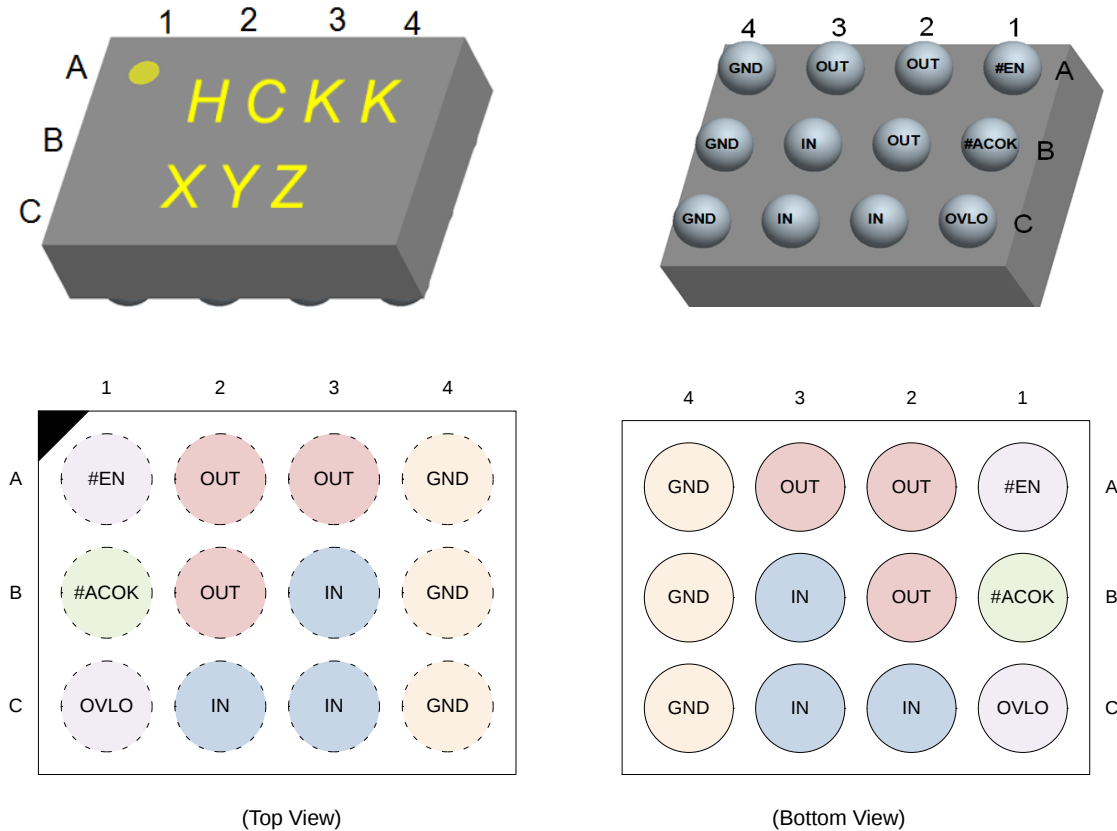


Figure 2. Pin Configuration

PIN DEFINITIONS

Name	Bump	Type	Description		
IN	B3, C2, C3	Input/Supply	Switch Input and Device Supply		
OUT	A2, A3, B2	Output	Switch Output to Load		
#ACOK	B1	Output (Open Drain)		1	V _{IN} < V _{IN_min} or V _{IN} ≥ V _{OVLO}
				0	Voltage Stable
#EN	A1	Input	Device Enable (Active LOW)		
OVLO	C1	Input	Over–Voltage Lockout Adjustment Pin		
GND	A4, B4, C4	Supply	Device Ground		

Over-Voltage Lockout (OVLO) Calculation

OVLO can be set externally and override default OVP. By connecting an external resistor-driver to the OVLO pin. Equation (1) can produce the desired trip voltage and resistor values.

$$V_{IN_OVLO} = V_{OVLO_TH} \times [1 + R1/R2] \quad (\text{eq. 1})$$

Recommended minimum $R1 = 1 \text{ M}\Omega$

On-The-Go (OTG) Functionality

During OTG operation, the FPF2280 is initially disabled and the power FET's bulk diode is forward biased. The bulk

diode represents $\sim 0.7 \text{ V}$ drop across the device, which remains until the V_{IN} voltage increases past 2.5 V , when the device is fully enabled. While the device is disabled and the body diode is forward biased, the max DC current through the diode is 1.8 A . This current is limited by the thermal performance of the device ($0.7 \text{ V} \times 1.8 \text{ A} = 1.36 \text{ W}$). This current should be transient; the #EN pin must be pulled LOW to ensure the device fully enables. The transient should not exceed the RC time constant of the C_{IN} and C_{OUT} capacitors. At the system level, over-voltage and current protection should be provided outside the FPF2280.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V _{IN}	V _{IN} to GND & V _{IN} to V _{OUT} = GND or Float		-0.3	29.0	V
V _{OUT}	V _{OUT} to GND		-0.3	V _{IN} + 0.3	V
V _{OVLO}	OVLO to GND		-0.3	24.0	V
V _{#EN_ACOK}	Maximum DC Voltage Allowed on #EN or ACOK Pin			6	V
I _{IN}	Switch I/O Current (Continuous)			4.5	A
t _{PD}	Total Power Dissipation at T _A = 25°C			1.48	W
T _{STG}	Storage Temperature Range		-65	150	°C
T _J	Maximum Junction Temperature			150	°C
T _L	Lead Temperature (Soldering, 10 Seconds)			260	°C
Θ _{JA}	Thermal Resistance, Junction-to-Ambient ⁽¹⁾ (1-in. ² Pad of 2-oz. Copper)			84.1	°C/W
ESD	IEC 61000-4-2 System ESD	Air Gap	15.0		kV
		Contact	8.0		
	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	3.5		
	Charged Device Model, JESD22-C101	All Pins	2.0		
Surge	IEC 61000-4-5, Surge Protection	V _{IN}	100		V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured using 2S2P JEDEC std. PCB

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	Supply Voltage	2.5	20.0	V
T _A	Operating Temperature	-40	105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to 105°C unless otherwise indicated. Typical values are V_{IN} = 5.0 V, I_{IN} ≤ 3 A, C_{IN} = 0.1 μF and T_A = 25°C.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{IN_CLAMP}	Input Clamping Voltage	I _{IN} = 10 mA		35		V
I _Q	Input Quiescent Current	V _{IN} = 5 V, #EN = 0 V		58	100	μA
I _{IN_Q}	OVLO Supply Current	V _{OVLO} = 3 V, V _{IN} = 5 V, V _{OUT} = 0 V		63	100	μA
V _{IN_OVLO}	Internal Over-Voltage Trip Level	V _{IN} Rising, OVLO = GND	6.6	6.8	7.0	V
		V _{IN} Falling	6.2			V
V _{OVLO_TH}	OVLO Set Threshold	V _{IN} = 2.5 V to V _{OVLO}	1.12	1.20	1.24	V
V _{OVLO_RNG}	Adjustable OVLO Threshold Range	V _{IN} = 2.5 V to V _{OVLO}	4		20	V
V _{OVLO_SELECT}	External OVLO Select Threshold			0.30	0.28	V
R _{ON}	Resistance from V _{IN} to V _{OUT}	V _{IN} = 5 V, I _{OUT} = 1 A, T _A = 25°C		30	39	mΩ
C _{OUT}	OUT Load Capacitance ⁽²⁾	V _{IN} = 5 V			1000	μF
I _{OLVO}	OVLO Input Leakage Current	V _{OVLO} = V _{OVLO_TH}	-100		100	nA
T _{SDN}	Thermal Shutdown ⁽²⁾			130		°C
T _{SDN_HYS}	Thermal Shutdown Hysteresis ⁽²⁾			20		°C

Digital Signals

V _{OL}	#ACOK Output Low Voltage	V _{I/O} = 3.3 V, I _{SINK} = 1 mA			0.4	V
V _{IH_#EN}	Enable HIGH Voltage	V _{IN} = 2.5 V to V _{OVLO}	1.2			V
V _{IL_#EN}	Enable LOW Voltage	V _{IN} = 2.5 V to V _{OVLO}			0.5	V
I _{ACOK_LEAK}	#ACOK Leakage Current	V _{I/O} = 3.3 V, #ACOK Deasserted, #EN = 0 V	-0.5		0.5	μA
#EN_Leak	#EN Leakage Current	V _{IN} = 5.0 V, V _{OUT} = Float	-1.0		1.0	μA

Timing Characteristics

t _{DEB}	Debounce Time	Time from 2.5 V < V _{IN} < V _{IN_OVLO} to V _{OUT} = 0.1 × V _{IN}		15		ms
t _{START}	Soft-Start Time	Time from V _{IN} = V _{IN_min} to 0.2 × #ACOK, V _{I/O} = 1.8 V with 10 kΩ Pull-up Resistor		30		ms
t _{ON}	Switch Turn-On Time	V _{IN} = 5 V, R _L = 100 Ω, V _{OUT} from 0.1 × V _{IN} to 0.9 × V _{IN} , C _{LOAD} = 100 μF		2		ms
t _{OFF}	Switch Turn-Off Time ⁽²⁾	R _L = 100 Ω, C _L = 0 μF, V _{IN} > V _{OVLO} to V _{OUT} = 0.8 × V _{IN}		125		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Guaranteed by characterization and design.

Timing Diagrams

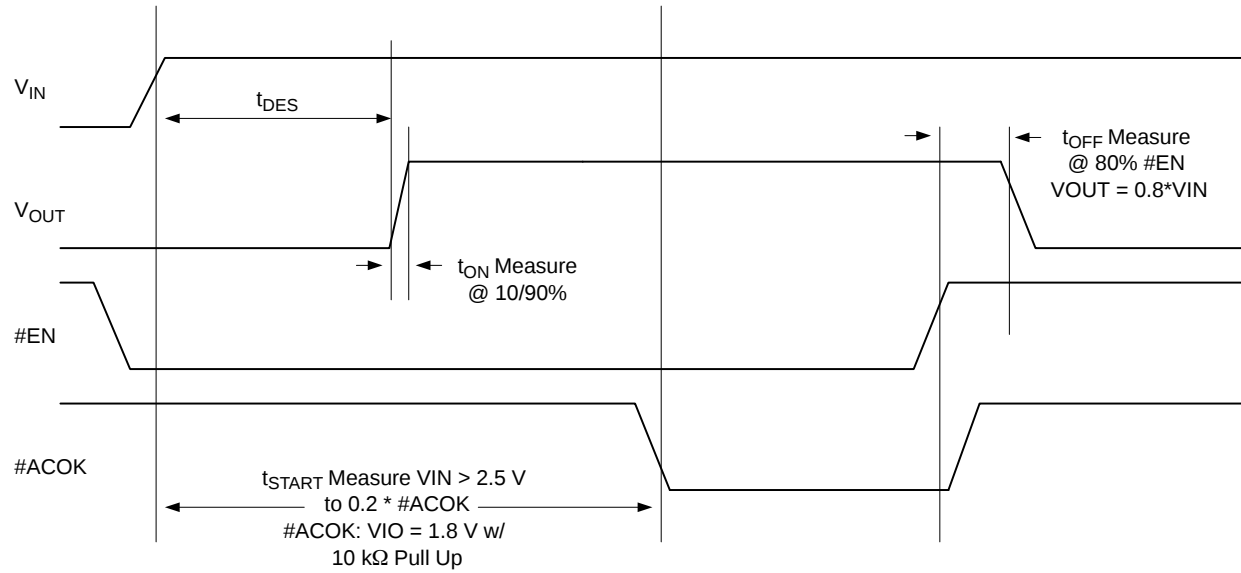


Figure 3. Timing for Power Up and Normal Operation

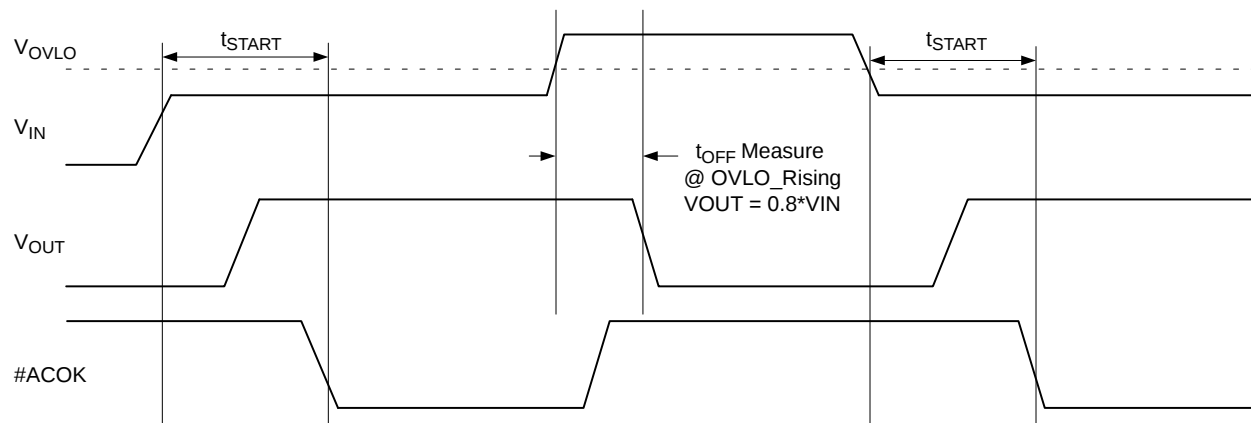


Figure 4. Timing for OVLO Trip

PRODUCT-SPECIFIC PACKAGE DIMENSIONS

D	E	X	Y
1288 $\mu\text{m} \pm 30\text{ }\mu\text{m}$	1828 $\mu\text{m} \pm 30\text{ }\mu\text{m}$	314 $\mu\text{m} \pm 18\text{ }\mu\text{m}$	244 $\mu\text{m} \pm 18\text{ }\mu\text{m}$

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