



### FEATURES

- 16-bit ADC family
- Dual simultaneous sampling
- Fully differential analog inputs
- Throughput conversion rate
  - 1 MSPS for AD4680
  - 500 kSPS for AD4681
- SNR (typical)
  - 92.5 dB,  $V_{REF} = 3.3$  V external
  - 100 dB with  $8\times$  OSR,  $RES = 1$
- On-chip oversampling function
- Resolution boost function
- INL (maximum) 1.5 LSBs
- 2.5 V internal reference at 10 ppm/°C
- High speed serial interface
- 40°C to +125°C operation
- 3 mm × 3 mm, 16-lead LFCSP
- Wide common-mode range
- Alert function

### APPLICATIONS

- Motor control position feedback
- Motor control current sense
- Sonar
- Power quality
- Data acquisition systems
- Erbium doped fiber amplifier (EDFA) applications
- Inphase (I) and quadrature (Q) demodulation

### GENERAL DESCRIPTION

The AD4680/AD4681 are 16-bit, pin-compatible, dual simultaneous sampling, high speed, low power, successive approximation register (SAR) analog-to-digital converters (ADCs) that operate from a 3.0 V to 3.6 V power supply and feature throughput rates of 1 MSPS for the AD4680 and 500 kSPS for the AD4681. The analog input type is differential, accepts a wide common-mode input voltage, and is sampled and converted on the falling edge of CS. Integrated on-chip oversampling blocks improve dynamic range and reduce noise at lower bandwidths. A buffered internal 2.5 V reference is included. Alternatively, an external reference up to 3.3 V can be used.

The conversion process and data acquisition use standard control inputs, allowing easy interfacing to microprocessors or digital signal processors (DSPs). The device is compatible with 1.8 V, 2.5 V, and 3.3 V interfaces using a separate logic supply. The AD4680/AD4681 are available in a 16-lead lead frame chip scale package (LFCSP) with operation specified from –40°C to +125°C.

### COMPANION PRODUCTS

**ADC Drivers:** [ADA4896-2](#), [ADA4940-2](#), [ADA4807-2](#), [LTC6227](#)  
**Voltage References:** [ADR4533](#), [ADR4525](#)  
**Low Dropout Regulators:** [ADP166](#), [ADP7104](#), [ADP7182](#)  
**Additional companion products on the [AD4680](#) and [AD4681](#) product pages**

Table 1. Related Products

| Input Type          | 16-Bit                 | 14-Bit                 | 12-Bit                 |
|---------------------|------------------------|------------------------|------------------------|
| Differential        | <a href="#">AD7380</a> | <a href="#">AD7381</a> |                        |
| Pseudo Differential | <a href="#">AD7383</a> | <a href="#">AD7384</a> |                        |
| Single-Ended        | <a href="#">AD7386</a> | <a href="#">AD7387</a> | <a href="#">AD7388</a> |

### FUNCTIONAL BLOCK DIAGRAM

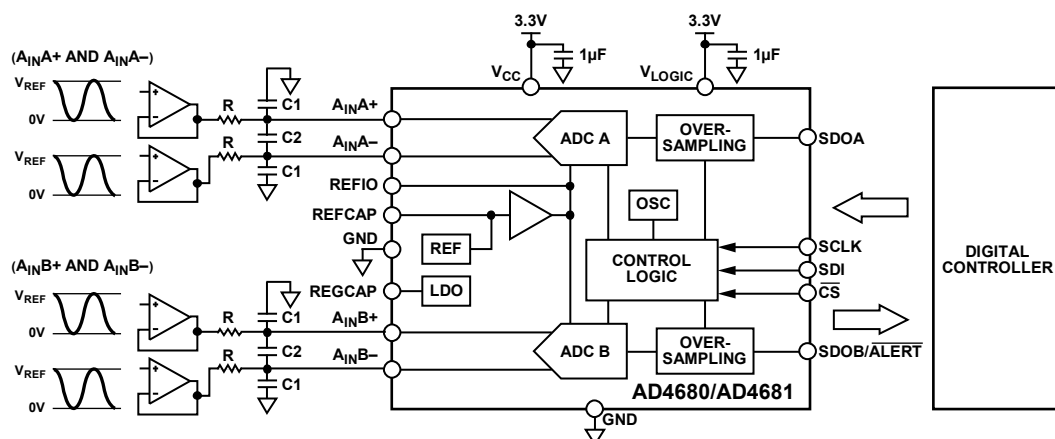


Figure 1.

23409-001

Rev. 0

### Document Feedback

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## REVISION HISTORY

10/2020—Revision 0: Initial Version

## SPECIFICATIONS

$V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $V_{LOGIC} = 1.65\text{ V}$  to  $3.6\text{ V}$ , reference voltage ( $V_{REF}$ ) =  $2.5\text{ V}$  internal, sampling frequency ( $f_{SAMPLE}$ ) =  $1\text{ MSPS}$  (AD4680) or  $500\text{ kSPS}$  (AD4681),  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , no oversampling enabled, unless otherwise noted. FS is full scale.

Table 2.

| Parameter                                       | Test Conditions/Comments                                                           | Min        | Typ                    | Max             | Unit                         |
|-------------------------------------------------|------------------------------------------------------------------------------------|------------|------------------------|-----------------|------------------------------|
| RESOLUTION                                      |                                                                                    | 16         |                        |                 | Bits                         |
| THROUGHPUT                                      |                                                                                    |            |                        |                 |                              |
| AD4680                                          |                                                                                    |            |                        | 1               | MSPS                         |
| AD4681                                          |                                                                                    |            |                        | 500             | kSPS                         |
| DC ACCURACY                                     |                                                                                    |            |                        |                 |                              |
| No Missing Codes                                |                                                                                    | 16         |                        |                 | Bits                         |
| Differential Nonlinearity (DNL) Error           |                                                                                    | -1.0       | $\pm 0.7$              | +1.0            | LSB                          |
| Integral Nonlinearity (INL) Error               |                                                                                    | -1.5       | $\pm 0.7$              | +1.5            | LSB                          |
| Gain Error                                      |                                                                                    | -0.015     | $\pm 0.002$            | +0.015          | % FS                         |
| Gain Error Temperature Drift                    |                                                                                    | -11        | $\pm 1$                | +11             | ppm/ $^\circ\text{C}$        |
| Gain Error Match                                |                                                                                    | -0.01      | $\pm 0.002$            | +0.01           | % FS                         |
| Offset Error                                    | At $25^\circ\text{C}$ , $V_{CC} = 3.3\text{ V}$                                    | -0.2       | $\pm 0.01$             | +0.2            | mV                           |
|                                                 |                                                                                    | -0.5       |                        | +0.5            | mV                           |
| Zero Error Drift                                |                                                                                    | -2         | $\pm 0.5$              | +2              | $\mu\text{V}/^\circ\text{C}$ |
| Zero Error Matching                             |                                                                                    | -0.5       | $\pm 0.1$              | +0.5            | mV                           |
| AC ACCURACY                                     |                                                                                    |            |                        |                 |                              |
| Dynamic Range                                   | Input frequency ( $f_{IN}$ ) = $1\text{ kHz}$<br>$V_{REF} = 3.3\text{ V}$ external |            | 93.3                   |                 | dB                           |
|                                                 |                                                                                    |            | 91.8                   |                 | dB                           |
| Oversampled Dynamic Range                       | Oversampling ratio (OSR) = $4\times$                                               |            | 95.2                   |                 | dB                           |
| Signal-to-Noise Ratio (SNR)                     | $V_{REF} = 3.3\text{ V}$ external                                                  | 91         | 92.5                   |                 | dB                           |
|                                                 |                                                                                    | 89.5       | 91                     |                 | dB                           |
|                                                 | OSR = $8\times$ , RES = 1, $V_{REF} = 3.3\text{ V}$ external                       |            | 100                    |                 | dB                           |
|                                                 | $f_{IN} = 100\text{ kHz}$                                                          |            | 89                     |                 | dB                           |
| Spurious-Free Dynamic Range (SFDR)              |                                                                                    |            | 112                    |                 | dB                           |
| Total Harmonic Distortion (THD)                 |                                                                                    |            | -113                   |                 | dB                           |
|                                                 | $f_{IN} = 100\text{ kHz}$                                                          |            | -104                   |                 | dB                           |
| Signal-to-Noise-and-Distortion (SINAD) Ratio    | $V_{REF} = 3.3\text{ V}$ external                                                  | 90         | 92.5                   |                 | dB                           |
|                                                 |                                                                                    | 89         | 91                     |                 | dB                           |
| Channel to Channel Isolation                    |                                                                                    |            | -110                   |                 | dB                           |
| ANALOG INPUT                                    |                                                                                    |            |                        |                 |                              |
| Voltage Range                                   | $(A_{INX+}) - (A_{INX-})$                                                          | $-V_{REF}$ |                        | $+V_{REF}$      | V                            |
| Absolute Input Voltage                          | $A_{INX+}$ , $A_{INX-}$                                                            | -0.1       |                        | $V_{REF} + 0.1$ | V                            |
| Common-Mode Input Range                         | $A_{INX+}$ , $A_{INX-}$                                                            |            | 0.2 to $V_{REF} - 0.2$ |                 | V                            |
| Analog Input Common-Mode Rejection Ratio (CMRR) | $f_{IN} = 500\text{ kHz}$                                                          |            | -75                    |                 | dB                           |
| DC Leakage Current                              |                                                                                    |            | 0.1                    | 1               | $\mu\text{A}$                |
| Input Capacitance                               | When in track mode                                                                 |            | 18                     |                 | pF                           |
|                                                 | When in hold mode                                                                  |            | 5                      |                 | pF                           |
| SAMPLING DYNAMICS                               |                                                                                    |            |                        |                 |                              |
| Input Bandwidth                                 | At -0.1 dB                                                                         |            | 6                      |                 | MHz                          |
|                                                 | At -3 dB                                                                           |            | 25                     |                 | MHz                          |
| Aperture Delay                                  |                                                                                    |            | 2                      |                 | ns                           |
| Aperture Delay Match                            |                                                                                    |            | 26                     | 100             | ps                           |
| Aperture Jitter                                 |                                                                                    |            | 20                     |                 | ps                           |

| Parameter                                         | Test Conditions/Comments                    | Min                    | Typ             | Max                    | Unit   |
|---------------------------------------------------|---------------------------------------------|------------------------|-----------------|------------------------|--------|
| REFERENCE INPUT AND OUTPUT                        |                                             |                        |                 |                        |        |
| $V_{REF}$ Input Voltage Range                     | External reference                          | 2.49                   |                 | 3.4                    | V      |
| $V_{REF}$ Input Current                           | External reference                          |                        |                 |                        |        |
| AD4680                                            | 1 MSPS                                      |                        | 0.26            | 0.29                   | mA     |
| AD4681                                            | 500 kSPS                                    |                        | 0.23            | 0.26                   | mA     |
| $V_{REF}$ Output Voltage                          | At 25°C                                     | 2.498                  | 2.5             | 2.502                  | V      |
|                                                   | −40°C to +125°C                             | 2.495                  |                 | 2.505                  | V      |
| $V_{REF}$ Temperature Coefficient                 |                                             |                        | 1               | 10                     | ppm/°C |
| $V_{REF}$ Noise                                   |                                             |                        | 7               |                        | μV rms |
| DIGITAL INPUTS (SCLK, SDI, $\overline{CS}$ )      |                                             |                        |                 |                        |        |
| Logic Levels                                      |                                             |                        |                 |                        |        |
| Input Voltage                                     |                                             |                        |                 |                        |        |
| Low ( $V_{IL}$ )                                  |                                             |                        |                 | $0.2 \times V_{LOGIC}$ | V      |
| High ( $V_{IH}$ )                                 |                                             | $0.8 \times V_{LOGIC}$ |                 |                        | V      |
| Input Current                                     |                                             |                        |                 |                        |        |
| Low ( $I_{IL}$ )                                  |                                             | −1                     |                 | +1                     | μA     |
| High ( $I_{IH}$ )                                 |                                             | −1                     |                 | +1                     | μA     |
| DIGITAL OUTPUTS (SDOA, SDOB/ $\overline{ALERT}$ ) |                                             |                        |                 |                        |        |
| Output Coding                                     |                                             |                        | Twos complement |                        | Bits   |
| Output Low Voltage ( $V_{OL}$ )                   | Sink current ( $I_{SINK}$ ) = 300 μA        |                        |                 | 0.4                    | V      |
| Output High Voltage ( $V_{OH}$ )                  | Source current ( $I_{SOURCE}$ ) = −300 μA   | $V_{LOGIC} - 0.3$      |                 |                        | V      |
| Floating-State Leakage Current                    |                                             |                        |                 | ±1                     | μA     |
| Floating-State Output Capacitance                 |                                             |                        | 10              |                        | pF     |
| POWER SUPPLIES                                    |                                             |                        |                 |                        |        |
| $V_{CC}$                                          |                                             | 3.0                    | 3.3             | 3.6                    | V      |
|                                                   | External reference = 3.3 V                  | 3.2                    | 3.3             | 3.6                    | V      |
| $V_{LOGIC}$                                       |                                             | 1.65                   |                 | 3.6                    | V      |
| $V_{CC}$ Current ( $I_{VCC}$ )                    |                                             |                        |                 |                        |        |
| Normal Mode (Operational)                         | AD4680, 1 MSPS                              |                        | 7.28            | 8.4                    | mA     |
|                                                   | AD4681, 500 kSPS                            |                        | 4.76            | 5.6                    | mA     |
| Normal Mode (Static)                              |                                             |                        | 2.3             | 2.8                    | mA     |
| Shutdown Mode                                     |                                             |                        | 100             | 200                    | μA     |
| $V_{LOGIC}$ Current ( $I_{VLOGIC}$ )              | SDOA and SDOB/ $\overline{ALERT}$ at 0x1FFF |                        |                 |                        |        |
| Normal Mode (Operational)                         | AD4680, 1 MSPS                              |                        | 884             | 950                    | μA     |
|                                                   | AD4681, 500 kSPS                            |                        | 438             | 470                    | μA     |
| Normal Mode (Static)                              |                                             |                        | 10              | 200                    | nA     |
| Shutdown Mode                                     |                                             |                        | 10              | 200                    | nA     |
| POWER DISSIPATION                                 |                                             |                        |                 |                        |        |
| Total Power ( $P_{TOTAL}$ )                       | AD4680                                      |                        | 29.4            | 33.7                   | mW     |
|                                                   | AD4681                                      |                        | 18.7            | 21.9                   | mW     |
| $V_{CC}$ Power ( $P_{VCC}$ )                      |                                             |                        |                 |                        |        |
| Normal Mode                                       |                                             |                        |                 |                        |        |
| Operational                                       | AD4680, 1 MSPS                              |                        | 26.2            | 30.3                   | mW     |
|                                                   | AD4681, 500 kSPS                            |                        | 17.1            | 20.2                   | mW     |
| Static                                            |                                             |                        | 7               | 10                     | mW     |
| Shutdown Mode                                     |                                             |                        | 330             | 720                    | μW     |
| $V_{LOGIC}$ Power ( $P_{VLOGIC}$ )                |                                             |                        |                 |                        |        |
| Normal Mode                                       |                                             |                        |                 |                        |        |
| Operational                                       | AD4680, 1 MSPS                              |                        | 3.2             | 3.4                    | mW     |
|                                                   | AD4681, 500 kSPS                            |                        | 1.6             | 1.7                    | mW     |
| Static                                            |                                             |                        | 33              | 720                    | nW     |
| Shutdown Mode                                     |                                             |                        | 33              | 720                    | nW     |

## TIMING SPECIFICATIONS

$V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $V_{LOGIC} = 1.65\text{ V}$  to  $3.6\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  internal, and  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

Table 3.

| Parameter      | Min  | Typ | Max | Unit          | Description                                                                     |
|----------------|------|-----|-----|---------------|---------------------------------------------------------------------------------|
| $t_{CYC}$      |      |     |     |               | Time between conversions                                                        |
|                | 1    |     |     | $\mu\text{s}$ | AD4680                                                                          |
|                | 2    |     |     | $\mu\text{s}$ | AD4681                                                                          |
| $t_{SCLKED}$   | 190  |     |     | ns            | $\overline{CS}$ falling edge to first SCLK falling edge                         |
| $t_{SCLK}$     | 25   |     |     | ns            | SCLK period                                                                     |
| $t_{SCLKH}$    | 10   |     |     | ns            | SCLK high time                                                                  |
| $t_{SCLKL}$    | 10   |     |     | ns            | SCLK low time                                                                   |
| $t_{CSH}$      | 10   |     |     | ns            | $\overline{CS}$ pulse width                                                     |
| $t_{QUIET}$    |      |     |     |               | Interface quiet time prior to conversion                                        |
|                | 500  |     |     | ns            |                                                                                 |
|                | 1500 |     |     | ns            |                                                                                 |
| $t_{SDOEN}$    |      |     |     |               | $\overline{CS}$ low to SDOA and SDOB/ $\overline{ALERT}$ enabled                |
|                |      |     | 6   | ns            | $V_{LOGIC} \geq 2.25\text{ V}$                                                  |
|                |      |     | 8   | ns            | $1.65\text{ V} \leq V_{LOGIC} < 2.25\text{ V}$                                  |
| $t_{SDOH}$     | 2    |     |     | ns            | SCLK rising edge to SDOA and SDOB/ $\overline{ALERT}$ hold time                 |
| $t_{SDOS}$     |      |     |     |               | SCLK rising edge to SDOA and SDOB/ $\overline{ALERT}$ setup time                |
|                |      |     | 6   | ns            | $V_{LOGIC} \geq 2.25\text{ V}$                                                  |
|                |      |     | 8   | ns            | $1.65\text{ V} \leq V_{LOGIC} < 2.25\text{ V}$                                  |
| $t_{SDOT}$     |      |     | 45  | ns            | $\overline{CS}$ rising edge to SDOA and SDOB/ $\overline{ALERT}$ high impedance |
| $t_{SDIS}$     | 1    |     |     | ns            | SDI setup time prior to SCLK falling edge                                       |
| $t_{SDIH}$     | 1    |     |     | ns            | SDI hold time after SCLK falling edge                                           |
| $t_{SCLKCS}$   | 0    |     |     | ns            | SCLK rising edge to $\overline{CS}$ rising edge                                 |
| $t_{CONVERT}$  |      |     | 190 | ns            | Conversion time                                                                 |
| $t_{ACQUIRE}$  |      |     |     |               | Acquire time                                                                    |
|                | 810  |     |     | ns            | AD4680                                                                          |
|                | 1800 |     |     | ns            | AD4681                                                                          |
| $t_{RESET}$    |      |     |     |               | Valid time to start conversion after software reset (see Figure 37)             |
|                |      | 250 |     | ns            | Valid time to start conversion after soft reset                                 |
|                |      | 800 |     | ns            | Valid time to start conversion after hard reset                                 |
| $t_{POWERUP}$  |      |     |     |               | Supply active to conversion                                                     |
|                |      |     | 5   | ms            | First conversion allowed                                                        |
|                |      |     | 11  | ms            | Settled to within 1% with internal reference                                    |
|                |      |     | 5   | ms            | Settled to within 1% with external reference                                    |
| $t_{REGWRITE}$ |      |     | 5   | ms            | Supply active to register read write access allowed                             |
| $t_{STARTUP}$  |      |     |     |               | Exiting shutdown mode to conversion                                             |
|                |      |     | 11  | ms            | Settled to within 1% with internal reference                                    |
|                |      |     | 10  | $\mu\text{s}$ | Settled to within 1% with external reference                                    |
| $t_{ALERTS}$   |      |     | 200 | ns            | Time from $\overline{CS}$ to $\overline{ALERT}$ indication (see Figure 36)      |
| $t_{ALERTC}$   |      |     | 12  | ns            | Time from $\overline{CS}$ to $\overline{ALERT}$ clear (see Figure 36)           |

## Timing Diagrams

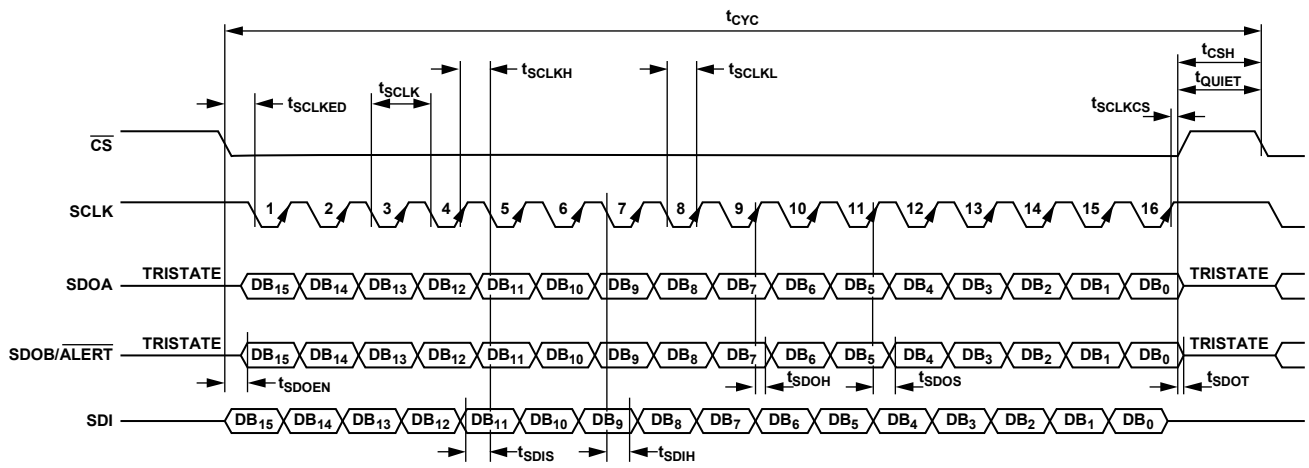


Figure 2. Serial Interface Timing Diagram

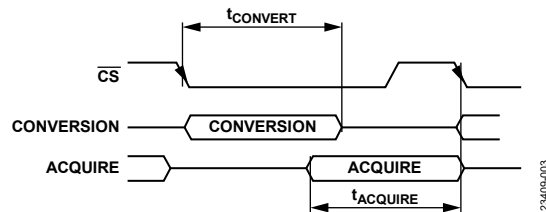


Figure 3. Internal Conversion Acquire Timing

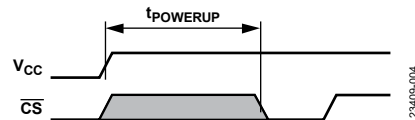


Figure 4. Power-Up Time to Conversion

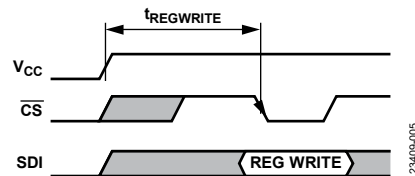


Figure 5. Power-Up Time to Register Read Write Access

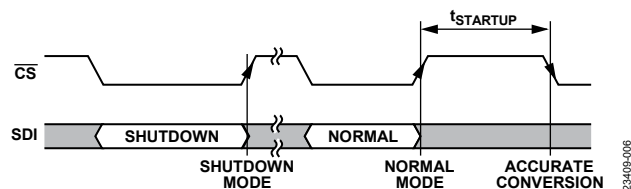


Figure 6. Shutdown Mode to Normal Mode Timing

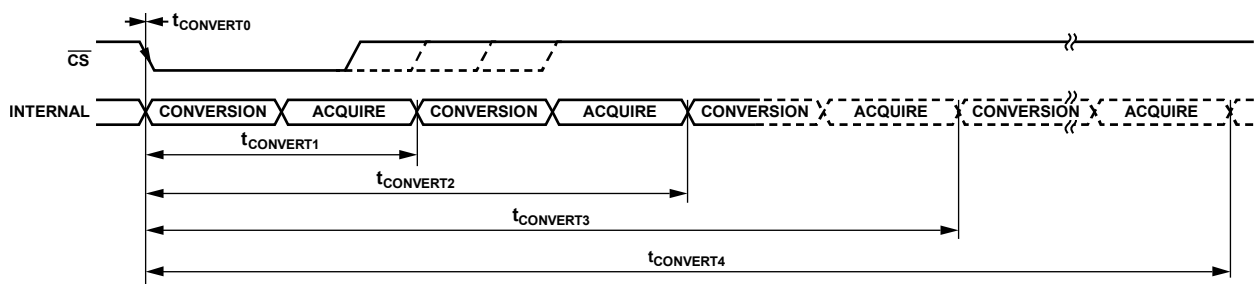


Figure 7. Conversion Timing During OS Normal Mode

## ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter                                       | Rating                                                                         |
|-------------------------------------------------|--------------------------------------------------------------------------------|
| $V_{CC}$ to Ground (GND)                        | −0.3 V to +4 V                                                                 |
| $V_{LOGIC}$ to GND                              | −0.3 V to +4 V                                                                 |
| Analog Input Voltage to GND                     | −0.3 V to $V_{REF} + 0.3 V$ , $V_{CC} + 0.3 V$ , or 4 V (whichever is smaller) |
| Digital Input Voltage to GND                    | −0.3 V to $V_{LOGIC} + 0.3 V$ , or 4 V (whichever is smaller)                  |
| Digital Output Voltage to GND                   | −0.3 V to $V_{LOGIC} + 0.3 V$ , or 4 V (whichever is smaller)                  |
| Reference Input and Output (REFIO) Input to GND | −0.3 V to $V_{CC} + 0.3 V$ , or 4 V (whichever is smaller)                     |
| Input Current to Any Pin Except Supplies        | ±10 mA                                                                         |
| Operating Temperature Range                     | −40°C to +125°C                                                                |
| Storage Temperature Range                       | −65°C to +150°C                                                                |
| Maximum Junction Temperature                    | 150°C                                                                          |
| Pb-Free Soldering Reflow Temperature            | 260°C                                                                          |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.  $\theta_{JC}$  is the junction to case thermal resistance.

Table 5. Thermal Resistance

| Package Type          | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|-----------------------|---------------|---------------|------|
| CP-16-45 <sup>1</sup> | 55.4          | 12.7          | °C/W |

<sup>1</sup> Test Condition 1: thermal impedance simulated values are based on JEDEC 2S2P thermal test board four thermal vias. See JEDEC JESD51.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charge device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

### ESD Ratings for AD4680/AD4681

Table 6. AD4680/AD4681, 16-Lead LFCSP

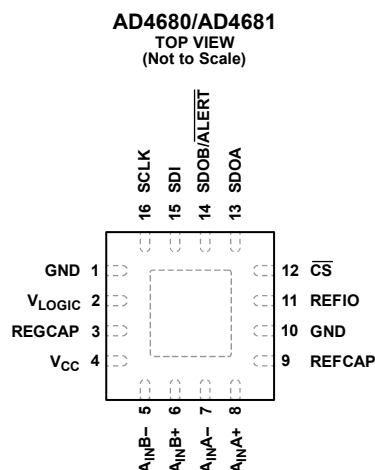
| ESD Model | Withstand Threshold (V) | Class |
|-----------|-------------------------|-------|
| HBM       | ±4000                   | 3A    |
| FICDM     | ±1250                   | C3    |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. EXPOSED PAD. FOR CORRECT OPERATION OF THE DEVICE, THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

23409-008

Figure 8. Pin Configuration

Table 7. Pin Function Descriptions

| Pin No. | Mnemonic                              | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|---------|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 10   | GND                                   | Ground Reference Point. This pin is the ground reference point for all circuitry on the device.                                                                                                                                                                                                                                                                                                  |
| 2       | V <sub>LOGIC</sub>                    | Logic Interface Supply Voltage, 1.65 V to 3.6 V. Decouple this pin to GND with a 1 $\mu$ F capacitor.                                                                                                                                                                                                                                                                                            |
| 3       | REGCAP                                | Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this pin to GND with a 1 $\mu$ F capacitor. The voltage at this pin is 1.9 V typical.                                                                                                                                                                                                                              |
| 4       | V <sub>CC</sub>                       | Power Supply Input Voltage, 3.0 V to 3.6 V. Decouple this pin to GND using a 1 $\mu$ F capacitor.                                                                                                                                                                                                                                                                                                |
| 5, 6    | A <sub>INB-</sub> , A <sub>INB+</sub> | Analog Inputs of ADC B. These analog inputs form a differential pair.                                                                                                                                                                                                                                                                                                                            |
| 7, 8    | A <sub>INA-</sub> , A <sub>INA+</sub> | Analog Inputs of ADC A. These analog inputs form a differential pair.                                                                                                                                                                                                                                                                                                                            |
| 9       | REFCAP                                | Decoupling Capacitor Pin for Band Gap Reference. Decouple this pin to GND with a 0.1 $\mu$ F capacitor. The voltage at this pin is 2.5 V typical.                                                                                                                                                                                                                                                |
| 11      | REFIO                                 | Reference Input and Output. The on-chip reference of 2.5 V is available as an output on this pin for external use if the device is configured accordingly. Alternatively, an external reference of 2.5 V to 3.3 V can be input to this pin. Decoupling is required on this pin for both the internal and external reference options. A 1 $\mu$ F capacitor must be applied from this pin to GND. |
| 12      | $\overline{\text{CS}}$                | Chip Select Input. Active low, logic input. This input provides the dual function of initiating conversions on the AD4680/AD4681 and framing the serial data transfer.                                                                                                                                                                                                                           |
| 13      | SDOA                                  | Serial Data Output A. This pin functions as a serial data output pin to access the ADC A or ADC B conversion results or data from any of the on-chip registers.                                                                                                                                                                                                                                  |
| 14      | SDOB/ $\overline{\text{ALERT}}$       | Serial Data Output B (SDOB). This pin functions as a serial data output to access the conversion results. Alert Indication Output ( $\overline{\text{ALERT}}$ ). This pin operates as an alert going low to indicate that a conversion result has exceeded a configured threshold. This pin can operate as a serial data output pin or alert indication output.                                  |
| 15      | SDI                                   | Serial Data Input. This input provides the data written to the on-chip control registers.                                                                                                                                                                                                                                                                                                        |
| 16      | SCLK                                  | Serial Clock Input. This serial clock input is for data transfers to and from the ADC.                                                                                                                                                                                                                                                                                                           |
|         | EPAD                                  | Exposed Pad. For correct operation of the device, the exposed pad must be connected to ground.                                                                                                                                                                                                                                                                                                   |

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{REF} = 2.5$  V internal,  $V_{CC} = 3.6$  V,  $V_{LOGIC} = 3.3$  V,  $f_{IN} = 1$  kHz, and  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

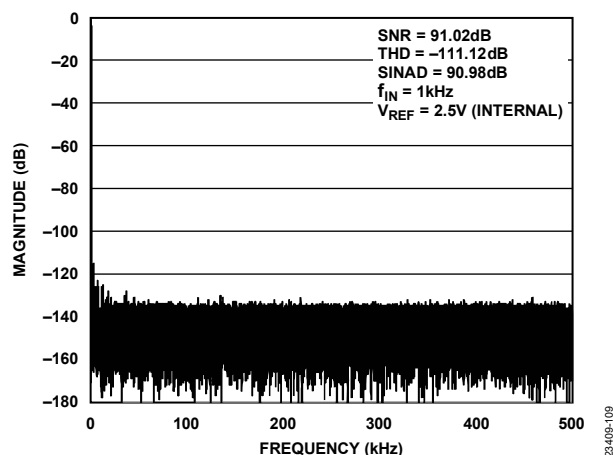


Figure 9. AD4680 Fast Fourier Transform (FFT),  $V_{REF} = 2.5$  V Internal

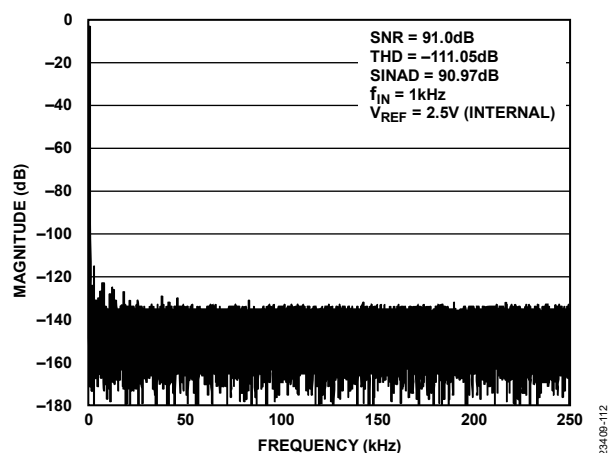


Figure 12. AD4681 FFT,  $V_{REF} = 2.5$  V Internal

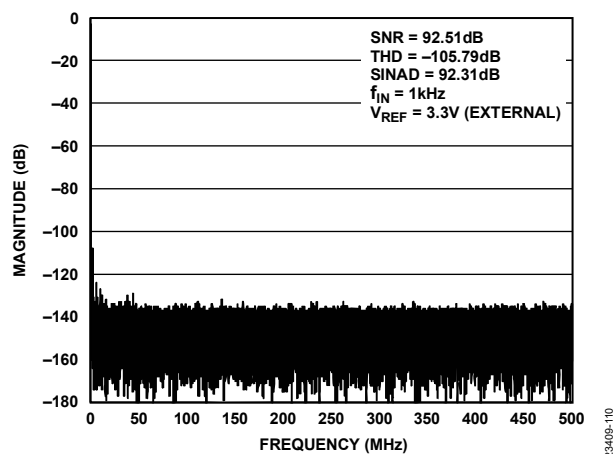


Figure 10. AD4680 FFT,  $V_{REF} = 3.3$  V External

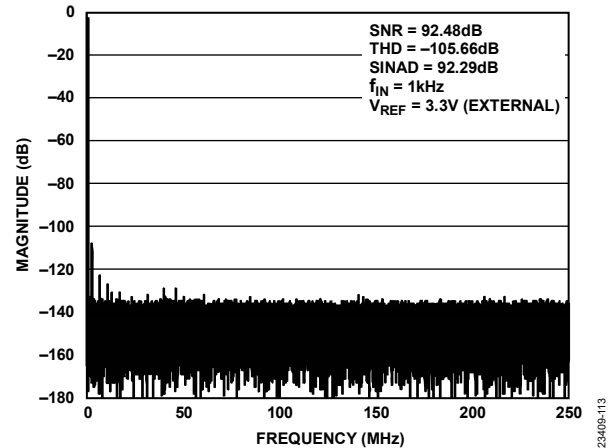


Figure 13. AD4681 FFT,  $V_{REF} = 3.3$  V External

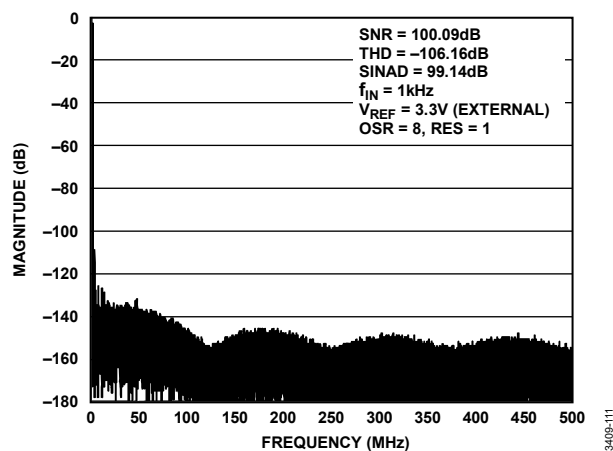


Figure 11. AD4680 FFT with Oversampling,  $V_{REF} = 3.3$  V External

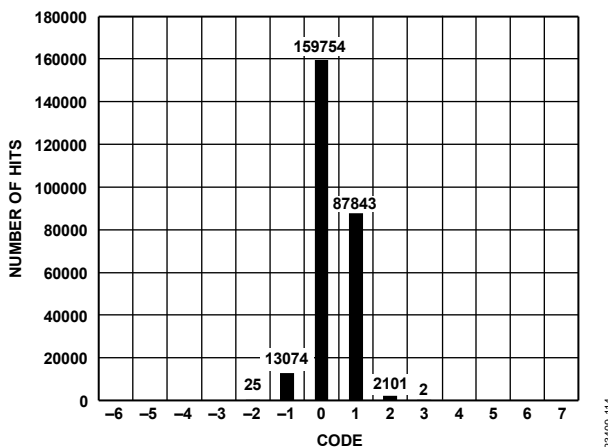


Figure 14. DC Histogram Codes at Code Center

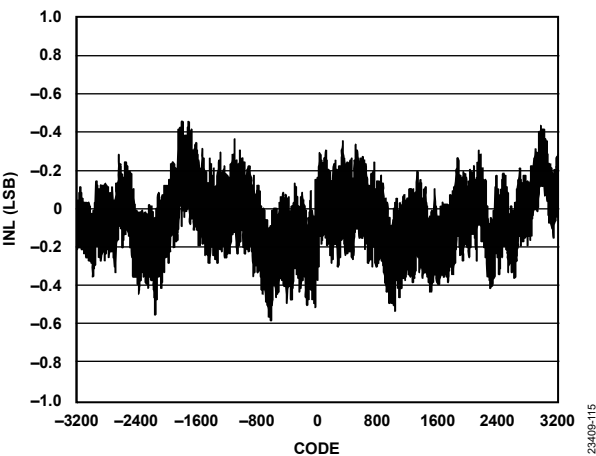


Figure 15. INL Error

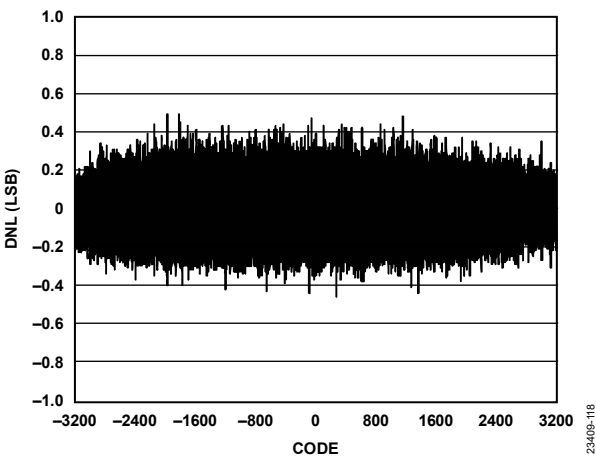


Figure 18. DNL Error

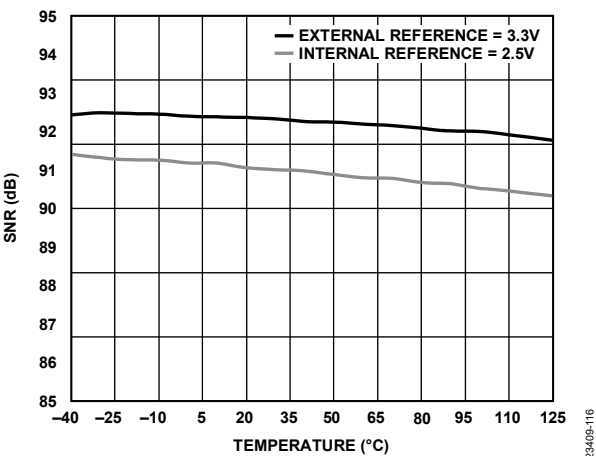


Figure 16. SNR vs. Temperature

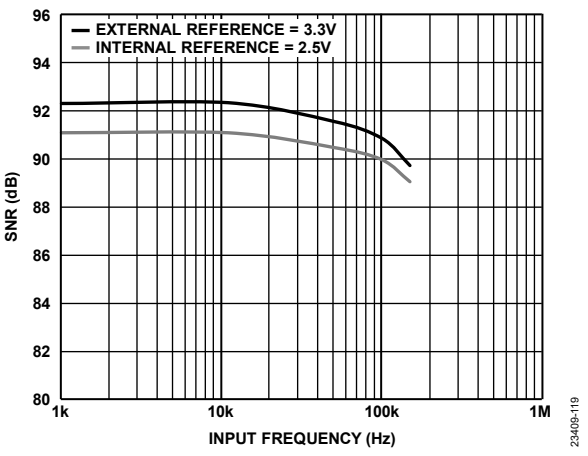


Figure 19. AD4680 SNR vs. Input Frequency

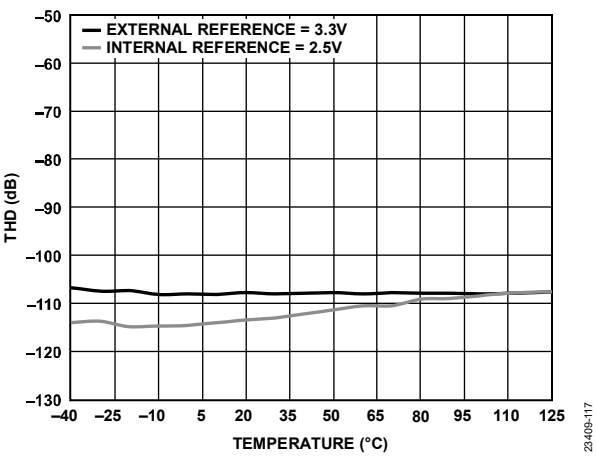


Figure 17. THD vs. Temperature

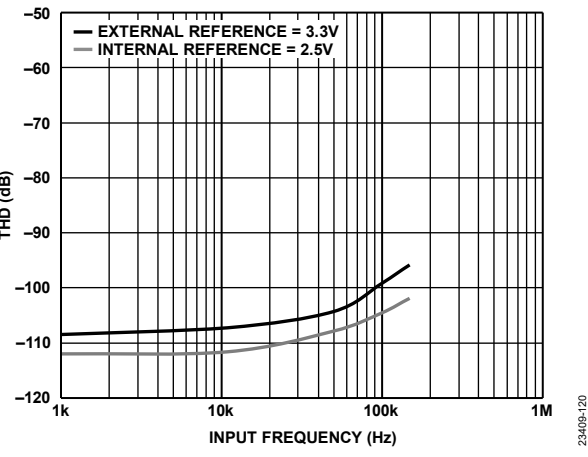


Figure 20. AD4680 THD vs. Input Frequency

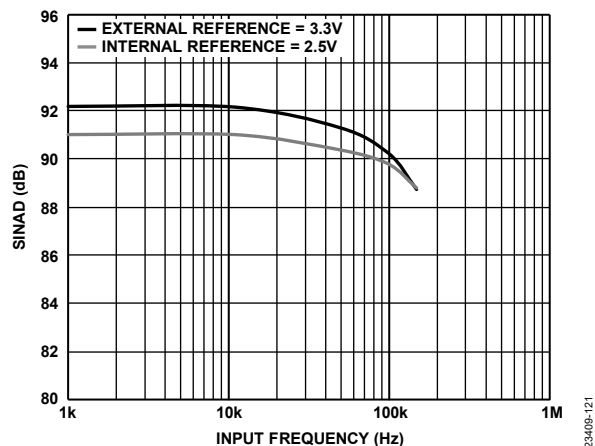


Figure 21. AD4680 SINAD vs. Input Frequency

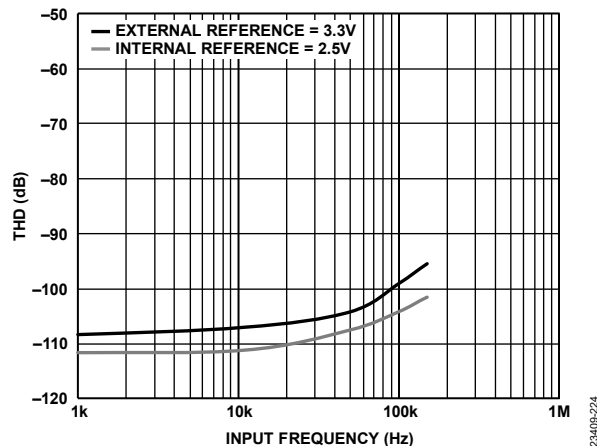


Figure 24. AD4681 THD vs. Input Frequency

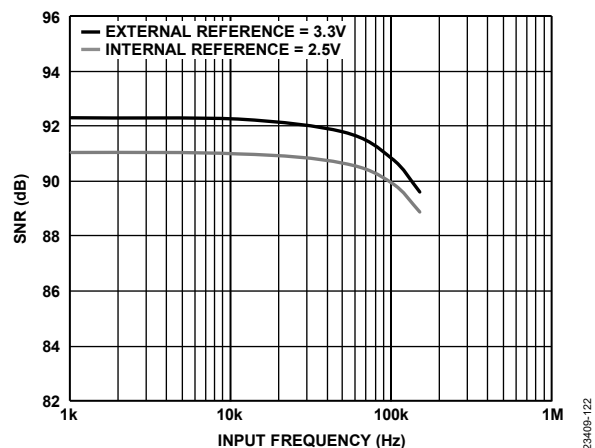


Figure 22. AD4681 SNR vs. Input Frequency

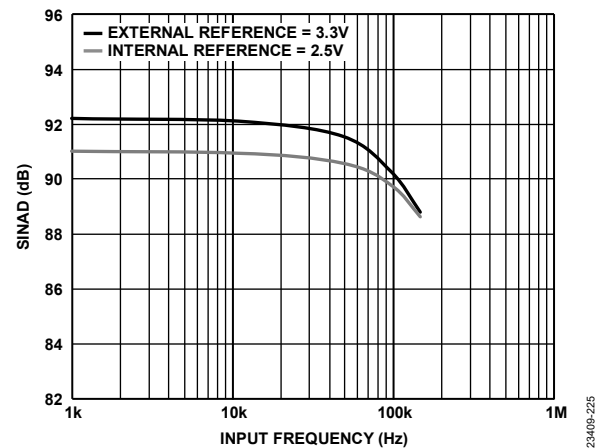


Figure 25. AD4681 SINAD vs. Input Frequency

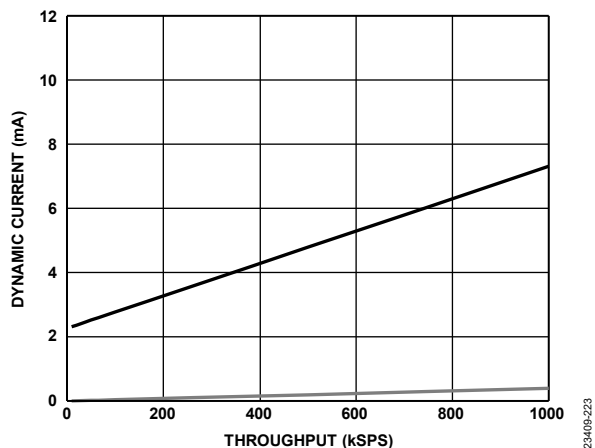


Figure 23. Dynamic Current vs. Throughput

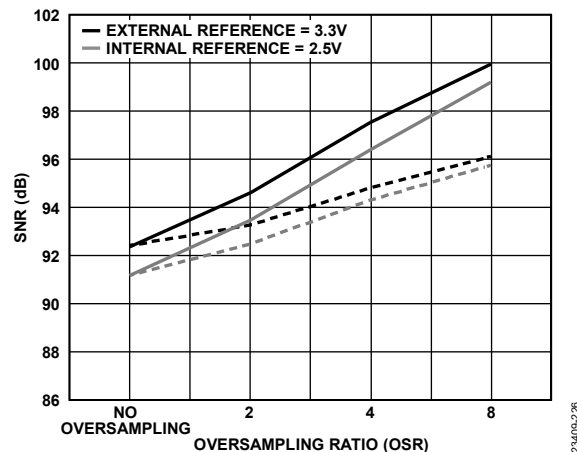


Figure 26. AD4680 SNR vs. Oversampling Ratio, Oversampling Mode

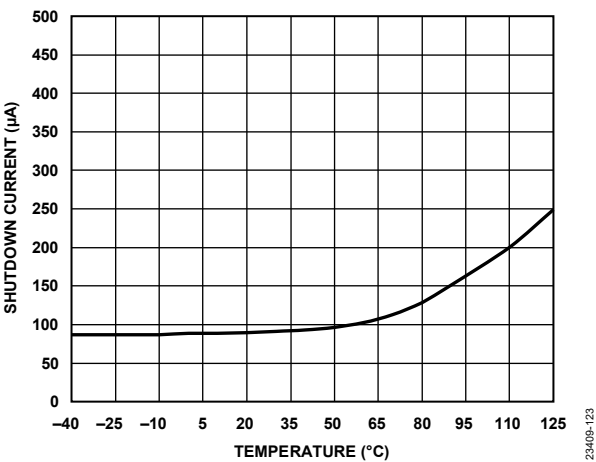


Figure 27. Shutdown Current vs. Temperature

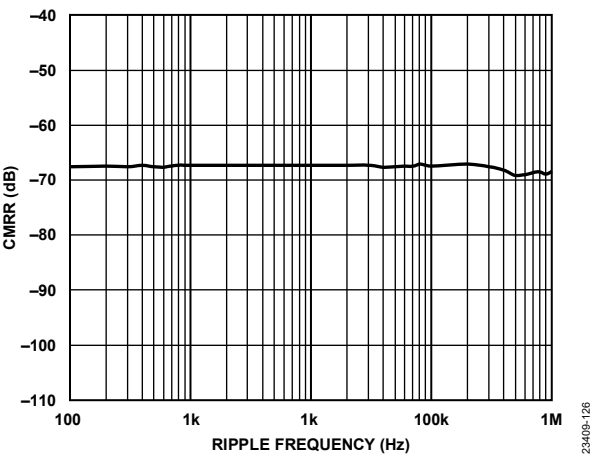


Figure 29. CMRR vs. Ripple Frequency

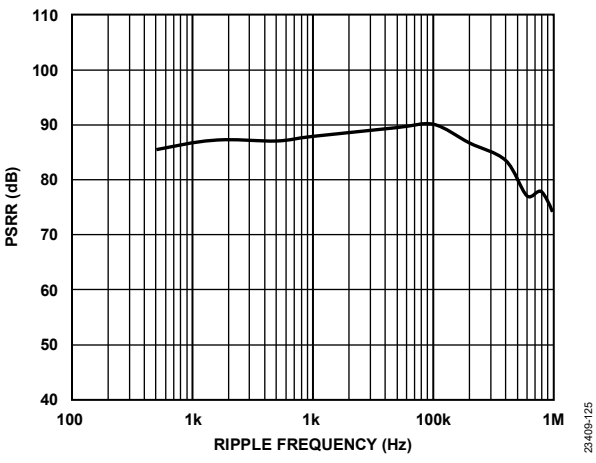


Figure 28. Power Supply Rejection Ratio (PSRR) vs. Ripple Frequency

## TERMINOLOGY

### Differential Nonlinearity (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

### Integral Nonlinearity (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs  $\frac{1}{2}$  LSB before the first code transition. Positive full scale is defined as a level  $1\frac{1}{2}$  LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

### Gain Error

The first transition (from 100 ... 000 to 100 ... 001) occurs at a level  $\frac{1}{2}$  LSB above nominal negative full scale. The last transition (from 011 ... 110 to 011 ... 111) occurs for an analog voltage  $1\frac{1}{2}$  LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

### Gain Error Drift

The gain error drift is the gain error change due to a temperature change of 1°C.

### Gain Error Matching

Gain error matching is the difference in negative full-scale error between the input channels and the difference in positive full-scale error between the input channels.

### Zero Error

Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

### Zero Error Drift

The zero error drift is the zero error change due to a temperature change of 1°C.

### Zero Error Matching

Zero error matching is the difference in zero error between the input channels.

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels (dB).

### Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in dB, between the rms amplitude of the input signal and the peak spurious signal.

### Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

### Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

### Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the ADC output at the frequency,  $f$ , to the power of a 200 mV p-p sine wave applied to the common-mode voltage of  $A_{INX+}$  and  $A_{INX-}$  of frequency,  $f$ . CMRR is expressed in dB.

$$CMRR = 10\log(P_{ADC\_IN}/P_{ADC\_OUT})$$

where:

$P_{ADC\_IN}$  is the common-mode power at the frequency,  $f$ , applied to the  $A_{INX+}$  and  $A_{INX-}$  inputs.

$P_{ADC\_OUT}$  is the power at the frequency,  $f$ , in the ADC output.

### Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the CS input and when the input signal is held for a conversion.

### Aperture Delay Match

Aperture delay match is the difference of the aperture delay between ADC A and ADC B.

### Aperture Jitter

Aperture jitter is the variation in aperture delay.

## THEORY OF OPERATION

### CIRCUIT INFORMATION

The AD4680/AD4681 are high speed, dual simultaneous sampling, fully differential 16-bit, SAR ADCs. The AD4680/AD4681 operate from a 3.0 V to 3.6 V power supply and feature throughput rates of 1 MSPS (AD4680) and 500 kSPS (AD4681).

The AD4680/AD4681 contain two SAR ADCs and a serial interface with two separate data output pins. The device is housed in a 16-lead LFCSP, offering the user considerable space-saving advantages over alternative solutions.

Data is accessed from the device via the serial interface. The interface can operate with one or two serial outputs. The AD4680/AD4681 have an on-chip, 2.5 V, internal  $V_{REF}$ . If an external reference is desired, the internal reference can be disabled, and a reference value ranging from 2.5 V to 3.3 V can be supplied. If the internal reference is used elsewhere in the system, the reference output must be buffered. The differential analog input range for the AD4680/AD4681 is the common-mode voltage ( $V_{CM}$ )  $\pm V_{REF}/2$ .

The AD4680/AD4681 feature on-chip oversampling blocks to improve performance. Rolling average oversampling mode and power-down options that allow power saving between conversions are also available. Configuration of the device is implemented via the standard serial interface (see the Interface section).

### CONVERTER OPERATION

The AD4680/AD4681 have two SAR ADCs, each based around two capacitive digital-to-analog converters (DACs). Figure 30 and Figure 31 show simplified schematics of one of the ADCs in acquisition and conversion phases, respectively. The ADC comprises control logic, an SAR, and two capacitive DACs. In Figure 30 (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor ( $C_s$ ) arrays can acquire the differential signal on the input.

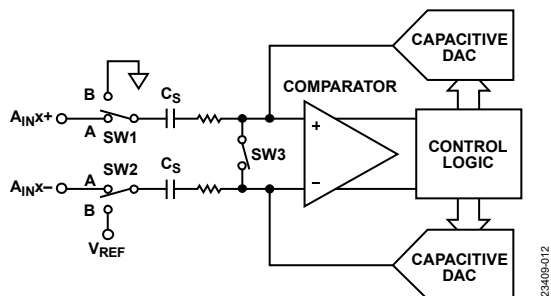


Figure 30. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 31), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected when the conversion begins. The control logic and charge redistribution

DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the  $A_{INX+}$  and  $A_{INX-}$  pins must be matched. Otherwise, the two inputs have different settling times, resulting in errors.

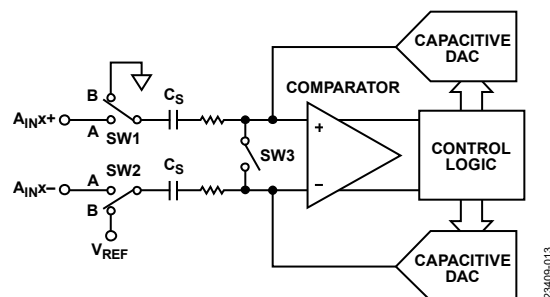


Figure 31. ADC Conversion Phase

### ANALOG INPUT STRUCTURE

Figure 32 shows the equivalent circuit of the analog input structure of the AD4680/AD4681. The four diodes (D) provide ESD protection for the analog inputs. Ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the device.

The C1 capacitors in Figure 32 are typically 3 pF and can primarily be attributed to pin capacitance. The R1 resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 200  $\Omega$ . The C2 capacitors are the sampling capacitors of the ADC with a capacitance of 15 pF typically.

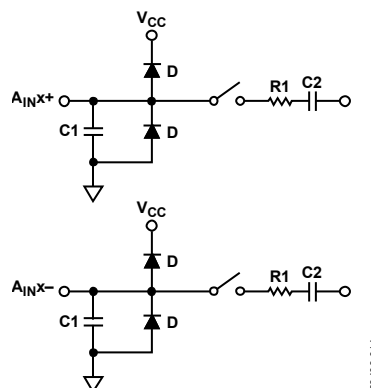


Figure 32. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

## ADC TRANSFER FUNCTION

The AD4680/AD4681 can use a 2.5 V to 3.3 V  $V_{REF}$ . The AD4680/AD4681 convert the differential voltage of the analog inputs ( $A_{IN}A+$ ,  $A_{IN}A-$ ,  $A_{IN}B+$ , and  $A_{IN}B-$ ) into a digital output.

The conversion result is MSB first, two's complement. The LSB size is  $(2 \times V_{REF})/2^N$ , where N is the ADC resolution. The ADC resolution is determined by the resolution of the device chosen, and if resolution boost mode is enabled. Table 8 outlines the LSB size expressed in microvolts for different resolutions and reference voltages options.

The ideal transfer characteristic for the AD4680/AD4681 is shown in Figure 33.

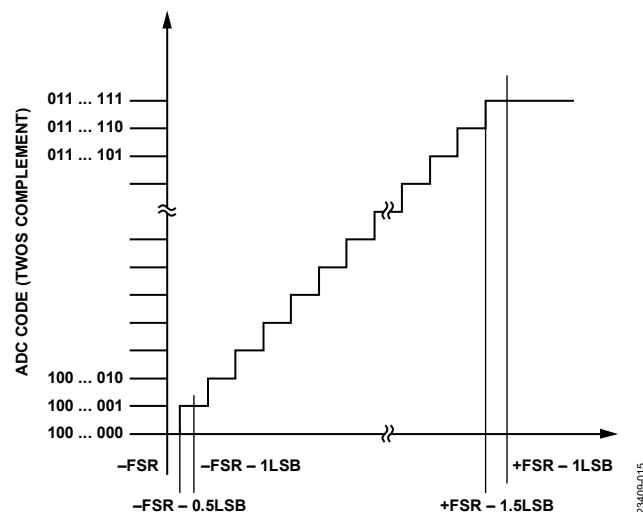


Figure 33. ADC Ideal Transfer Function (FSR = Full-Scale Range)

Table 8. LSB Size

| Resolution (Bits) | 2.5 V Reference ( $\mu V$ ) | 3.3 V Reference ( $\mu V$ ) |
|-------------------|-----------------------------|-----------------------------|
| 16                | 76.3                        | 100.7                       |
| 18                | 19.1                        | 25.2                        |

## APPLICATIONS INFORMATION

Figure 34 shows an example of a typical application circuit for the AD4680/AD4681. Decouple the  $V_{CC}$ ,  $V_{LOGIC}$ , REGCAP, and REFIO pins with suitable decoupling capacitors as shown.

The exposed pad is a ground reference point for circuitry on the device and must be connected to the board ground.

A differential RC filter must be placed on the analog inputs to ensure optimal performance is achieved. On a typical application, it is recommended that resistance ( $R$ ) = 33  $\Omega$ ,  $C1$  = 68 pF, and  $C2$  = 330 pF.

The performance of the AD4680/AD4681 devices may be impacted by noise on the digital interface. This impact depends on the on-board layout and design. Keep a minimal distance between the digital line and the digital interface, or place a 100  $\Omega$  resistor in series and close to the SDOA pin and SDOB/ALERT pin to reduce noise from the digital interface coupling of the AD4680/AD4681.

The two differential channels of the AD4680/AD4681 can accept an input voltage range from 0 V to  $V_{REF}$ , and have a wide common-mode range that allows the conversion of a variety of signals. These analog input pins can easily be driven with an amplifier. Table 9 lists the recommended driver amplifiers that best fit and add value to the application.

The AD4680 and the AD4681 have a buffered internal 2.5 V reference that can be accessed via the REFIO pin. The buffered internal 2.5V reference must use an external buffer like the [ADA4807-2](#), when connecting it to the external circuitry. Both devices have an option to use an ultralow noise, high accuracy voltage reference as an external voltage source, ranging from 2.5 V to 3.3 V, such as the [ADR4533](#) and [ADR4525](#).

## POWER SUPPLY

The typical application circuit in Figure 34 can be powered by a single 5 V ( $V_{+}$ ) voltage source that supplies the entire signal chain. The 5 V supply can come from a low noise, CMOS, low dropout (LDO) regulator ([ADP7105](#)). The driver amplifier supply is supplied by the 5 V ( $V_{+}$ ) and  $-2.5$  V ( $V_{-}$ ) derived from the inverter ([ADM660](#)), which then converts the  $+5$  V to  $-5$  V, then to the [ADP7182](#) low noise voltage regulator to output the  $-2.5$  V. The two independent supplies of the AD4680/AD4681,  $V_{CC}$  and  $V_{LOGIC}$ , that supply the analog circuitry and digital interface, respectively, can be supplied by a low quiescent current LDO regulator such as the [ADP166](#). The [ADP166](#) is a suitable supply with a fixed output voltage range from 1.2 V to 3.3 V for typical  $V_{CC}$  and  $V_{LOGIC}$  levels. Decouple both the  $V_{CC}$  supply and the  $V_{LOGIC}$  supply separately with a 1  $\mu$ F capacitor. Additionally, an internal LDO regulator supplies the AD4680/AD4681. The on-chip regulator provides a 1.9 V supply for internal use on the device only. Decouple the REGCAP pin with a 1  $\mu$ F capacitor connected to GND.

### Power-Up

The AD4680/AD4681 are not easily damaged by power supply sequencing.  $V_{CC}$  and  $V_{LOGIC}$  can be applied in any sequence. An external reference must be applied after  $V_{CC}$  and  $V_{LOGIC}$  are applied.

The AD4680/AD4681 require a  $t_{POWERUP}$  time from applying  $V_{CC}$  and  $V_{LOGIC}$  until the ADC conversion results are stable. Applying  $CS$  pulses or interfacing with the AD4680/AD4681 prior to the setup time elapsing does not have a negative impact on ADC operation. Conversion results are not guaranteed to meet data sheet specifications during this time, however, and must be ignored.

**Table 9. Signal Chain Components**

| Companion Devices  | Part Name                 | Description                                              | Typical Application                                |
|--------------------|---------------------------|----------------------------------------------------------|----------------------------------------------------|
| ADC Driver         | <a href="#">ADA4896-2</a> | 1 nV/ $\sqrt{\text{Hz}}$ , rail-to-rail output amplifier | Precision, low noise, high frequency               |
|                    | <a href="#">ADA4940-2</a> | Ultralow power, full differential, low distortion        | Precision, low density, low power                  |
|                    | <a href="#">ADA4807-2</a> | 1 mA, rail-to-rail output amplifier                      | Precision, low power, high frequency               |
|                    | <a href="#">LTC6227</a>   | Low distortion rail-to-rail output op amp                | Precision, low noise, high frequency               |
| External Reference | <a href="#">ADR4525</a>   | Ultralow noise, high accuracy voltage reference          | 2.5 V reference voltage                            |
|                    | <a href="#">ADR4533</a>   | Ultralow noise, high accuracy voltage reference          | 3.3 V reference voltage                            |
| LDO Regulator      | <a href="#">ADP166</a>    | Low quiescent, 150 mA, LDO regulator                     | 3.0 V to 3.6 V supply for $V_{CC}$ and $V_{LOGIC}$ |
|                    | <a href="#">ADP7104</a>   | Low noise, CMOS LDO regulator                            | 5 V supply for driver amplifier                    |
|                    | <a href="#">ADP7182</a>   | Low noise line regulator                                 | $-2.5$ V supply for driver amplifier               |

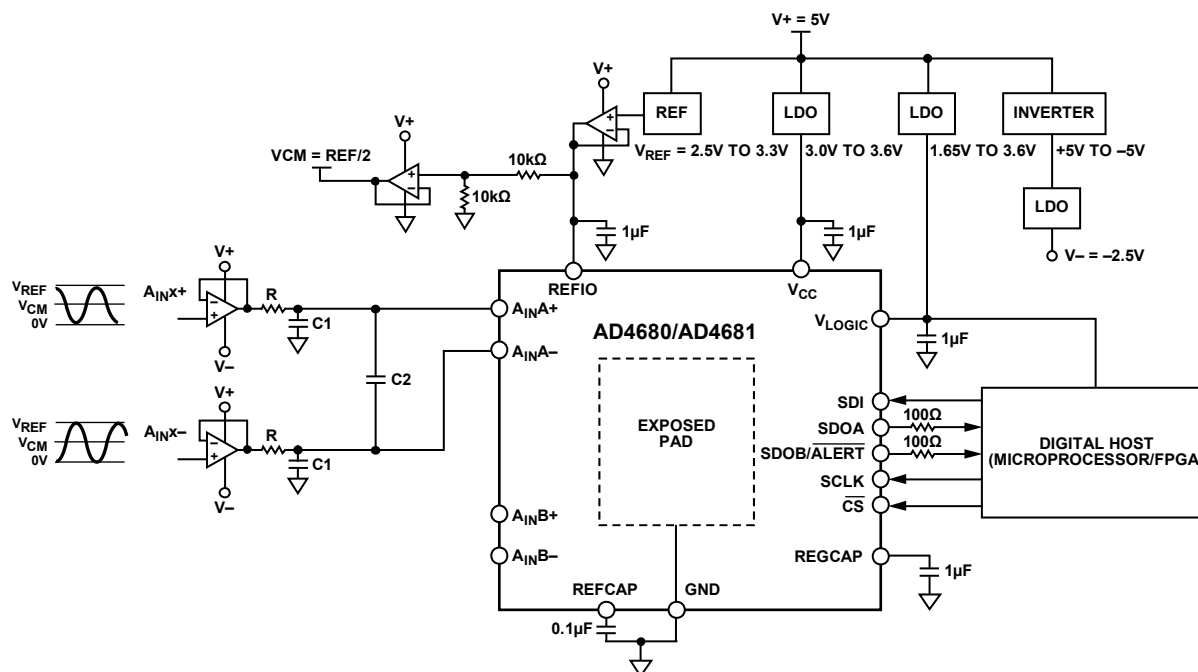


Figure 34. Typical Application Circuit

2340B-016

## MODES OF OPERATION

The AD4680/AD4681 have several on-chip configuration registers for controlling the operational mode of the device.

### OVERSAMPLING

Oversampling is a common method used in analog electronics to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from quantization noise and thermal noise (kTC) of the ADC. The AD4680 and the AD4681 offer an oversampling function on chip, rolling average oversampling.

The rolling average oversampling functionality is enabled by writing a 1 to the OS\_MODE bit and a valid nonzero to the OSR bits, Bits[8:6] in the CONFIGURATION1 register. Oversampling can be disabled by writing 0 to OS\_MODE and a zero value to the OSR bits of the CONFIGURATION1 register.

#### Rolling Average Oversampling

Rolling average oversampling mode can be used in applications where higher output data rates are required and where higher SNR or dynamic range is desirable. Rolling averaging involves taking a number of samples, adding the samples together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is not cleared after the process is completed. The rolling average oversampling mode uses a first in, first out (FIFO) buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same.

The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR (see Table 10). The output result is decimated to 16-bit resolution for the AD4680/AD4681. If additional resolution is required, this resolution can be achieved by configuring the resolution boost bit, RES, in the CONFIGURATION1 register. See the Resolution Boost section for further details.

In rolling average oversampling mode, all ADC conversions are controlled and initiated by the falling edge of  $\overline{CS}$ . After a conversion is complete, the result is loaded into the FIFO. The FIFO length is 8, regardless of the oversampling ratio set. The FIFO is filled on the first conversion after a power-on reset, the first conversion after a software controlled hard or soft reset, or on the first conversion after the REFSEL bit is toggled. A new conversion result is shifted into the FIFO on completion of every ADC conversion, regardless of the status of the OSR bits and the OS\_MODE bit. This conversion allows a seamless transition from no oversampling to rolling average oversampling, or different rolling average oversampling ratios without waiting for the FIFO to fill.

The number of samples,  $n$ , defined by the OSR bits are taken from the FIFO, added together, and the result is divided by  $n$ . The time between  $\overline{CS}$  falling edges is the cycle time, which can be controlled by the user, depending on the desired data output rate.

Table 10. Rolling Average Oversampling Performance Overview

| Oversampling Ratio | AD4680                   |         |                          |         |                                 | AD4681           |         |                                 |
|--------------------|--------------------------|---------|--------------------------|---------|---------------------------------|------------------|---------|---------------------------------|
|                    | SNR (dB Typical)         |         |                          |         | Output Data Rate (kSPS Maximum) | SNR (dB Typical) |         | Output Data Rate (kSPS Maximum) |
|                    | V <sub>REF</sub> = 2.5 V |         | V <sub>REF</sub> = 3.3 V |         |                                 | RES = 0          | RES = 1 |                                 |
|                    | RES = 0                  | RES = 1 | RES = 0                  | RES = 1 |                                 |                  |         |                                 |
| Disabled           | 91                       | 91      | 92.5                     | 92.5    | 1000                            | 85               | 85      | 500                             |
| 2                  | 92                       | 93      | 93.2                     | 94.5    | 1000                            | 84.5             | 87.7    | 500                             |
| 4                  | 94                       | 96      | 94.8                     | 97.2    | 1000                            | 85               | 91      | 500                             |
| 8                  | 95.5                     | 98.6    | 95.9                     | 99.6    | 1000                            | 85.5             | 93      | 500                             |

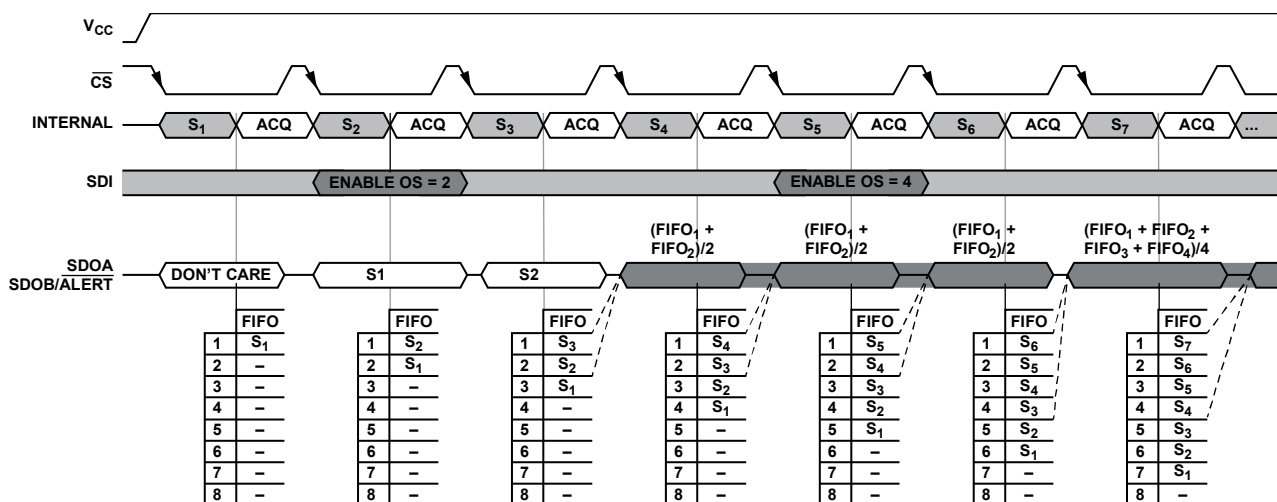


Figure 35. Rolling Average Oversampling Operation  
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## RESOLUTION BOOST

The default conversion result output data size is 16 bits for the AD4680/AD4681. When the on-chip oversampling function is enabled, the performance of the ADC can exceed 16 bits. To accommodate the performance boost achievable, it is possible to enable an additional two bits of resolution. If the RES bit in the CONFIGURATION1 register is set to Logic 1 and the AD4680/AD4681 are in a valid oversampling mode, the conversion result size is 18 bits. In this mode, 18 SCLK cycles are required to propagate the data for the AD4680/AD4681.

## ALERT

The alert functionality is an out of range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the conversion result value register exceeds the alert high limit value in the ALERT\_HIGH\_THRESHOLD register or falls below the alert low limit value in the ALERT\_LOW\_THRESHOLD register. The ALERT\_HIGH\_THRESHOLD register and the ALERT\_LOW\_THRESHOLD register are common to all ADCs. When setting the threshold limits, the alert high threshold must always be greater than the alert low threshold. Detailed alert information is accessible in the ALERT register.

The ALERT register contains two status bits per ADC, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all ADCs creates a common alert value. This value can be configured to drive out on the ALERT function of the SDOB/ALERT pin. The SDOB/ALERT pin is configured as ALERT by configuring the following bits in CONFIGURATION1 and the CONFIGURATION2:

- Set the SDO bit to 1.
- Set the ALERT\_EN bit to 1.
- Set a valid value to the ALERT\_HIGH\_THRESHOLD register and the ALERT\_LOW\_THRESHOLD register.

The alert indication function is available in both rolling average oversampling and in nonoversampling modes.

The ALERT function of the SDOB/ALERT pin is updated at the end of a conversion. The alert indication status bits in the ALERT register are updated as well and must be read before the end of the next conversion. The ALERT function of the SDOB/ALERT pin is cleared with a falling edge of  $\overline{CS}$ . Issuing a software reset also clears the alert status in the ALERT register.

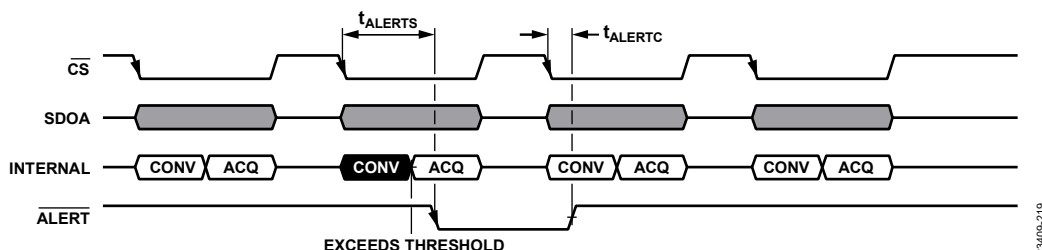


Figure 36. Alert Operation

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## POWER MODES

The AD4680/AD4681 have two power modes, normal mode and shutdown mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the CONFIGURATION1 register to configure the power modes in the AD4680/AD4681. Set PMODE to Logic 0 for normal mode and Logic 1 for shutdown mode.

### Normal Mode

Keep the AD4680/AD4681 in normal mode to achieve the fastest throughput rate. All blocks within the AD4680/AD4681 remain fully powered at all times, and an ADC conversion can be initiated by a falling edge of  $\overline{CS}$ , when required. When the AD4680/AD4681 are not converting, the devices are in static mode, and power consumption is automatically reduced. Additional current is required to perform a conversion, therefore, power consumption on the AD4680/AD4681 scales with throughput.

### Shutdown Mode

When slower throughput rates and lower power consumption are required, use shutdown mode by either powering down the ADC between each conversion or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the AD4680/AD4681 are in shutdown mode, all analog circuitry powers down, including the internal reference, if enabled. The serial interface remains active during shutdown mode to allow the AD4680/AD4681 to exit shutdown mode.

To enter shutdown mode, write to the PMODE bit in the CONFIGURATION1 register. The AD4680/AD4681 shut down and current consumption reduces.

To exit shutdown mode and return to normal mode, set the PMODE bit in the CONFIGURATION1 register to Logic 0. All register configuration settings remain unchanged entering or leaving shutdown mode. After exiting shutdown mode, sufficient time must be allowed for the circuitry to turn on before starting a conversion. If the internal reference is enabled, the reference must be allowed to settle for accurate conversions to happen.

## INTERNAL AND EXTERNAL REFERENCE

The AD4680/AD4681 have a buffered 2.5 V internal reference primarily used as a reference voltage for device operation. When using the buffered internal 2.5 V reference externally via the REFIO pin, the internal 2.5 V reference must use an external buffer before connecting to the external circuitry. Alternatively, if a more accurate reference or higher dynamic range is required, an external reference can be supplied. An externally supplied reference can be in the range of 2.5 V to 3.3 V.

Reference selection (internal or external) is configured by the REFSEL bit in the CONFIGURATION1 register. If REFSEL is set to 0, the internal reference buffer is enabled. If an external reference is preferred, the REFSEL bit must be set to 1, and an external reference must be supplied to the REFIO pin.

## SOFTWARE RESET

The AD4680/AD4681 have two reset modes, a soft reset and a hard reset. A reset is initiated by writing to the reset bits in the CONFIGURATION2 register.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The ALERT register is cleared. The reference and LDO regulator remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to the default status, resets the reference buffer, and resets the internal oscillator block.

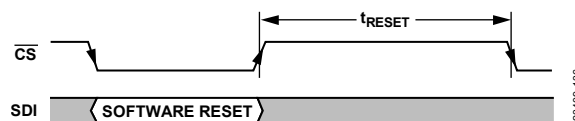


Figure 37. Software Reset Operation

## DIAGNOSTIC SELF TEST

The AD4680/AD4681 run a diagnostic self test after a power-on reset (POR) or after a software hard reset to ensure correct configuration is loaded into the device.

The result of the self test is displayed in the SETUP\_F bit in the ALERT register. If the SETUP\_F bit is set to Logic 1, the diagnostic self test has failed. If the test fails, perform a software hard reset to reset the AD4680/AD4681 registers to the default status.

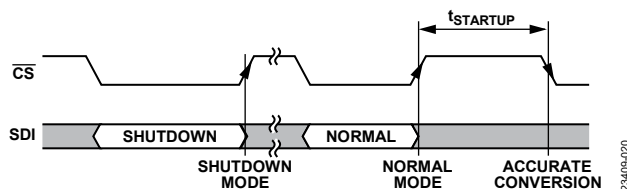


Figure 38. Shutdown Mode Operation

## INTERFACE

The interface to the AD4680/AD4681 is via a serial interface. The interface consists of the  $\overline{CS}$ , SCLK, SDOA, SDOB/ALERT, and SDI pins.

The  $\overline{CS}$  signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of  $\overline{CS}$  puts the track-and-hold into hold mode, at which point the analog input is sampled, and the bus is taken out of three-state.

The SCLK signal synchronizes data in and out of the device via the SDOA, SDOB, and SDI signals. A minimum of 16 SCLK cycles are required for a write to or read from a register. The minimum numbers of SCLK cycles for a conversion read is dependent on the resolution of the device and the configuration settings (see Table 11).

The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The AD4680/AD4681 have two serial output signals, SDOA and SDOB. To achieve the highest throughput of the device, use both SDOA and SDOB, 2-wire mode, to read the conversion results. If a reduced throughput is required or oversampling is used, it is possible to use 1-wire mode, the SDOA signal only, for reading conversion results.

Programming the SDO bit in the CONFIGURATION2 register configures 2-wire or 1-wire mode.

Configuring the cyclic redundancy check (CRC) operation for SPI reads or SPI writes alters the operation of the interface. Consult the relevant CRC Read, CRC Write, and CRC Polynomial sections to ensure proper operation.

### READING CONVERSION RESULTS

The  $\overline{CS}$  signal initiates the conversion process. A high to low transition on the  $\overline{CS}$  signal initiates a simultaneous conversion of both ADCs, ADC A and ADC B. The AD4680/AD4681 have a one-cycle readback latency. Therefore, the conversion results

are available on the next SPI access. Then, take the  $\overline{CS}$  signal low, and the conversion result clocks out on the serial output pins. The next conversion is also initiated at this point.

The conversion result is shifted out of the device as a 16-bit result for the AD4680/AD4681. The MSB of the conversion result is shifted out on the  $\overline{CS}$  falling edge. The remaining data is shifted out of the device under the control of the SCLK input. The data is shifted out on the rising edge of SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take  $\overline{CS}$  high again to return the SDOA and SDOB/ALERT pins to a high impedance state.

The number of SCLK cycles to propagate the conversion results on the SDOA and SDOB/ALERT pins is dependent on the serial mode of operation configured and if resolution boost mode is enabled (see Figure 39 and Table 11 for details). If CRC reading is enabled, additional SCLK cycles are required to propagate the CRC information (see the CRC section for more details).

As the  $\overline{CS}$  signal initiates a conversion, as well as framing the data, any data access must be completed within a single frame.

**Table 11. Number of SCLK Cycles, n, Required for Reading Conversion Results**

| Interface Configuration | Resolution Boost Mode | CRC Read | SCLK Cycles |
|-------------------------|-----------------------|----------|-------------|
| 2-Wire                  | Disabled              | Disabled | 16          |
|                         |                       | Enabled  | 24          |
|                         | Enabled               | Disabled | 18          |
|                         |                       | Enabled  | 26          |
| 1-Wire                  | Disabled              | Disabled | 32          |
|                         |                       | Enabled  | 40          |
|                         | Enabled               | Disabled | 36          |
|                         |                       | Enabled  | 44          |

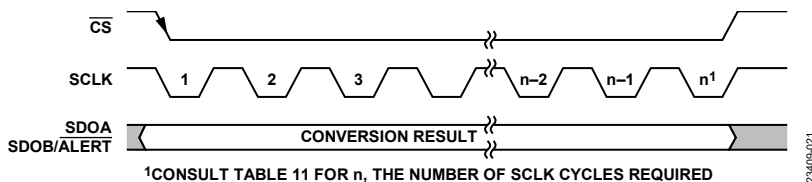


Figure 39. Reading Conversion Result

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### Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO bit to 0 in the CONFIGURATION1 register. In 2-wire mode, the conversion result for ADC A is output on the SDOA pin, and the conversion result for ADC B is output on the SDOB/ALERT pin (see Figure 40).

### Serial 1-Wire Mode

In applications where slower throughput rates are allowed, the serial interface can be configured to operate in 1-wire mode. In 1-wire mode, the conversion results from ADC A and ADC B are output on the serial output, SDOA. Additional SCLK cycles are required to propagate all data. The ADC A data is output first, followed by the ADC B conversion results (see Figure 41).

### LOW LATENCY READBACK

The interface on the AD4680/AD4681 has a one-cycle latency, as shown in Figure 42. For applications that operate at lower throughput rates, the latency of reading the conversion result can be reduced. When the conversion time elapses,  $t_{\text{CONVERT}}$ , a second  $\overline{\text{CS}}$  pulse after the initial  $\overline{\text{CS}}$  pulse that initiates the conversion, can be used to read back the conversion result. This operation is shown in Figure 42.

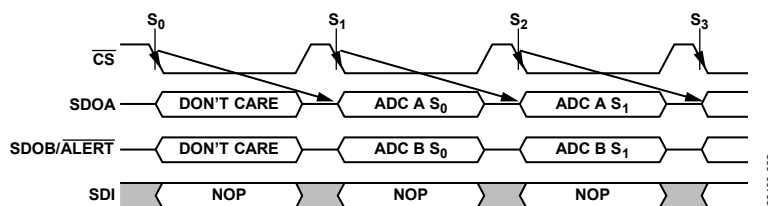


Figure 40. Reading Conversion Results for 2-Wire Mode

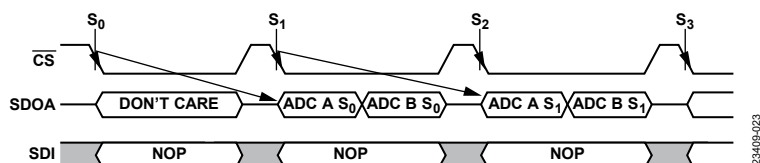


Figure 41. Read Conversion Results for 1-Wire Mode

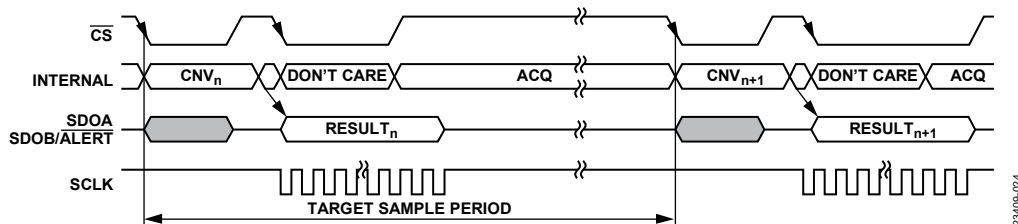


Figure 42. Low Throughput Low Latency

## READING FROM DEVICE REGISTERS

All registers in the device can be read over the serial interface. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or no operation command (NOP). The format for a read command is shown in Table 14. Bit D15 must be set to 0 to select a read command. Bits[D14:D12] contain the register address, and the subsequent 12 bits, Bits[D11:D0], are ignored.

## WRITING TO DEVICE REGISTERS

All read/write registers in the AD4680/AD4681 can be written to over the serial interface. The length of an SPI write access is determined by the CRC write function. An SPI access is 16-bit if CRC write is disabled and is 24-bit when CRC write is enabled. The format for a write command is shown in Table 14. Bit D15 must be set to 1 to select a write command. Bits[D14:D12] contain the register address, and the subsequent 12 bits, Bits[D11:D0], contain the data to be written to the selected register.

## CRC

The AD4680/AD4681 have CRC checksum modes that can be used to improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for SPI interface reads and SPI interface writes. For example, the CRC function for SPI writes can be enabled to prevent unexpected changes to the device configuration but disabled on SPI reads, therefore maintaining a higher throughput rate. The CRC feature is controlled by the programming of the CRC\_W and CRC\_R bits in the CONFIGURATION1 register.

### CRC Read

If enabled, a CRC is appended to the conversion result or register reads and consists of an 8-bit word. The CRC is calculated in the conversion result for ADC A and ADC B and is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 2-wire SPI mode, 1-wire SPI mode, and resolution boost mode.

### CRC Write

To enable the CRC write function, the CRC\_W bit in the CONFIGURATION1 register must be set to 1. To set the CRC\_W bit to 1 to enable the CRC feature, the request frame must have a valid CRC appended to the frame.

After the CRC feature is enabled, all register write requests are ignored unless accompanied by a valid CRC command, requiring a valid CRC to both enable and disable the CRC write feature.

### CRC Polynomial

For CRC checksum calculations, the following polynomial is always used:  $x^8 + x^2 + x + 1$ .

The following is an example of how to generate the checksum on a conversion read. The 16-bit data conversion result of the two channels are combined to produce a 32-bit data. The 8 MSBs of the 32-bit data are inverted and then left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned such that the MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum. The polynomial for this example is 100000111.

Let the original data of two channels be 0xAAAA and 0x5555, that is, 1010 1010 1010 1010 and 0101 0101 0101 0101. The data of the two channels is appended including eight zeros on the right, and then becomes 1010 1010 1010 1010 0101 0101 0101 0101 0000 0000.

Table 12 shows the CRC calculation of 16-bit, 2-channel data for the AD4680/AD4681. In the final XOR operation, the reduced data is less than the polynomial. Therefore, the remainder is the CRC for the assumed data.

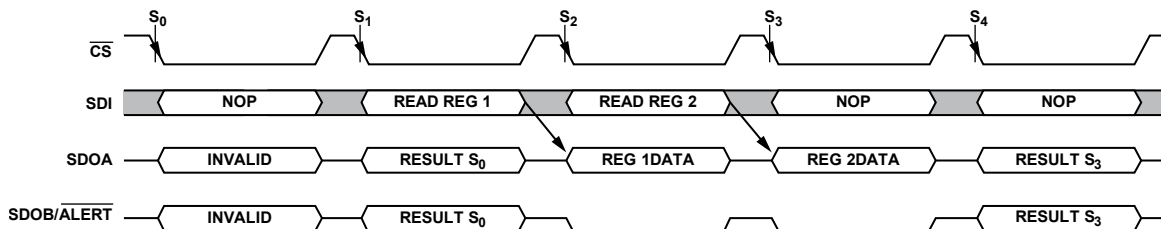


Figure 43. Register Read

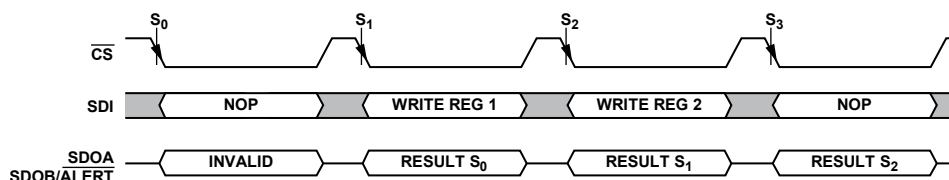


Figure 44. Register Write

**Table 12. Example CRC Calculation for 2-Channel, 16-Bit Data<sup>1</sup>**

|      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 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|------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Data | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
|------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|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<sup>1</sup> X means don't care.

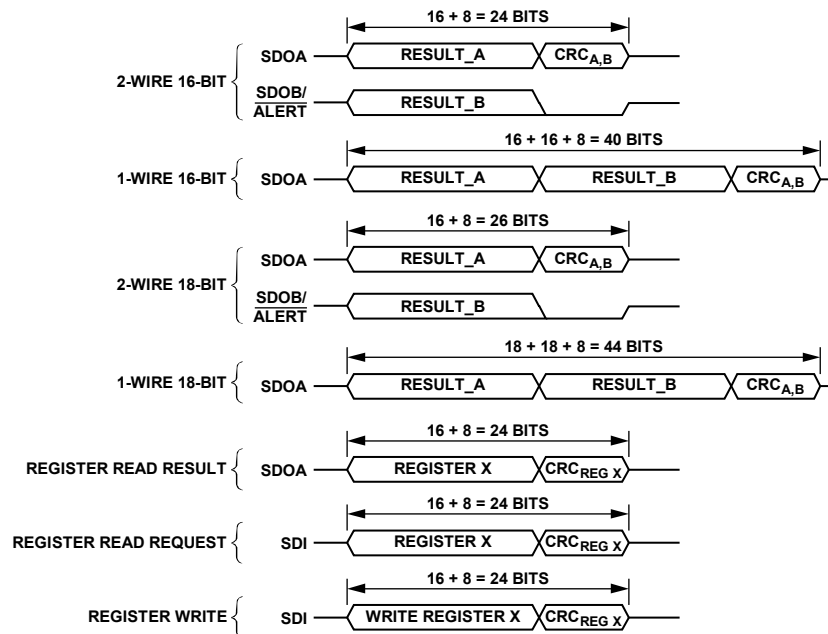


Figure 45. CRC Operation

## REGISTERS

The AD4680/AD4681 have user programmable on-chip registers for configuring the device. Table 13 shows a complete overview of the registers available on the AD4680/AD4681. The registers are either read/write (R/W) or read only (R). Any read request to a write only register is ignored. Any write request to a read only register is ignored. Writes to any other register address are considered an NOP and are ignored. Any read request to a register address, other than those listed in Table 13, are considered an NOP, and the data transmitted in the next SPI frame are the conversion results.

**Table 13. Register Summary**

| Hex. No. | Register Name        | Bits   | Bit 15                | Bit 14 | Bit 13    | Bit 12   | Bit 11                 | Bit 10 | Bit 9     | Bit 8      | Reset  | R/W |
|----------|----------------------|--------|-----------------------|--------|-----------|----------|------------------------|--------|-----------|------------|--------|-----|
|          |                      |        | Bit 7                 | Bit 6  | Bit 5     | Bit 4    | Bit 3                  | Bit 2  | Bit 1     | Bit 0      |        |     |
| 0x1      | CONFIGURATION1       | [15:8] | ADDRESSING            |        |           |          | RESERVED               |        | OS_MODE   | OSR, Bit 2 | 0x0000 | R/W |
|          |                      | [7:0]  | OSR, Bits[1:0]        |        | CRC_W     | CRC_R    | ALERT_EN               | RES    | REFSEL    | PMODE      |        |     |
| 0x2      | CONFIGURATION2       | [15:8] | ADDRESSING            |        |           |          | RESERVED               |        | SDO       |            | 0x0000 | R/W |
|          |                      | [7:0]  | RESET                 |        |           |          |                        |        |           |            |        |     |
| 0x3      | ALERT                | [15:8] | ADDRESSING            |        |           |          | RESERVED               |        | CRCW_F    | SETUP_F    | 0x0000 | R   |
|          |                      | [7:0]  | RESERVED              |        | AL_B_HIGH | AL_B_LOW | RESERVED               |        | AL_A_HIGH | AL_A_LOW   |        |     |
| 0x4      | ALERT_LOW_THRESHOLD  | [15:8] | ADDRESSING            |        |           |          | ALERT_LOW, Bits[11:8]  |        |           |            | 0x0800 | R/W |
|          |                      | [7:0]  | ALERT_LOW, Bits[7:0]  |        |           |          |                        |        |           |            |        |     |
| 0x5      | ALERT_HIGH_THRESHOLD | [15:8] | ADDRESSING            |        |           |          | ALERT_HIGH, Bits[11:8] |        |           |            | 0x07FF | R/W |
|          |                      | [7:0]  | ALERT_HIGH, Bits[7:0] |        |           |          |                        |        |           |            |        |     |

## ADDRESSING REGISTERS

A serial register transfer on the AD4680/AD4681 consists of 16 SCLK cycles. The four MSBs written to the device are decoded to determine which register is addressed. The four MSBs consist of the register address (REGADDR), Bits[14:12], and the read/write bit (WR). The register address bits determine which on-chip register is selected. If the addressed register is a valid write register, the read/write bit determines whether the remaining 12 bits of data on the SDI input are loaded into the addressed register. If the WR bit is 1, the bits load into the register addressed by the register select bits. If the WR bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

**Table 14. Addressing Register Format**

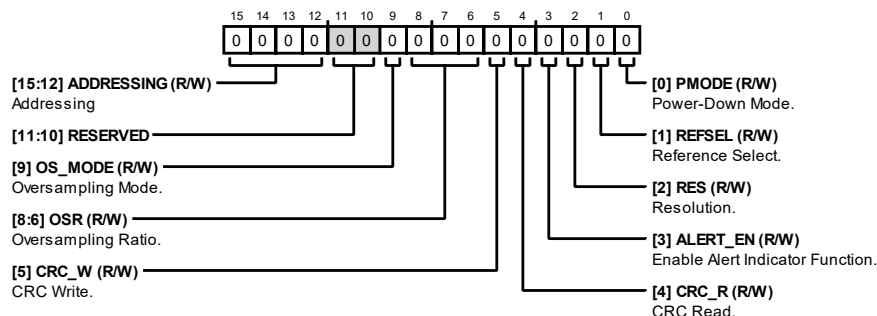
| MSB |         |     |     |      |     |    |    |    |    |    |    |    |    | LSB |    |
|-----|---------|-----|-----|------|-----|----|----|----|----|----|----|----|----|-----|----|
| D15 | D14     | D13 | D12 | D11  | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1  | D0 |
| WR  | REGADDR |     |     | Data |     |    |    |    |    |    |    |    |    |     |    |

**Table 15. Bit Descriptions for Addressing Registers**

| Bit        | Mnemonic | Description                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D15        | WR       | When a 1 is written to this bit, Bits[11:0] of this register are written to the register specified by REGADDR, if it is a valid address. Alternatively, when a 0 is written, the next data sent out on the SDOA pin is a read from the designated register if it is a valid address.                                                                                                                                                              |
| D14 to D12 | REGADDR  | When WR = 1, the contents of REGADDR determine the register for selection as outlined in Table 13.<br>When WR = 0 and REGADDR contains a valid register address, the contents on the requested register are output on the SDOA pin during the next interface access.<br>When WR = 0 and REGADDR contains 0x0, 0x6, or 0x7, the contents on the SDI line are ignored. The next interface access results in the conversion results being read back. |
| D11 to D0  | Data     | These bits are written into the corresponding register specified by the REGADDR bits when the WR bit is equal to 1 and the REGADDR bits contain a valid address.                                                                                                                                                                                                                                                                                  |

**CONFIGURATION1 REGISTER**

Address: 0x1, Reset: 0x0000, Name: CONFIGURATION1

**Table 16. Bit Descriptions for CONFIGURATION1 Register**

| Bits    | Bit Name   | Description                                                                                                                                                                                                                                                                                                                                            | Reset | Access |
|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.                                                                                                                                                                                                                         | 0x0   | R/W    |
| [11:10] | RESERVED   | Reserved.                                                                                                                                                                                                                                                                                                                                              | 0x0   | R      |
| 9       | OS_MODE    | Oversampling Mode. Enables the rolling average oversampling mode of the ADC.<br>0: disable.<br>1: enable.                                                                                                                                                                                                                                              | 0x0   | R/W    |
| [8:6]   | OSR        | Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the rolling average mode. Rolling average mode supports oversampling ratios of $\times 2$ , $\times 4$ , and $\times 8$ .<br>000: disabled.<br>001: $2\times$ .<br>010: $4\times$ .<br>011: $8\times$ .<br>100: disabled.<br>101: disabled.<br>110: disabled.<br>111: disabled.    | 0x0   | R/W    |
| 5       | CRC_W      | CRC Write. Controls the CRC functionality for the SDI interface. When setting this bit from a 0 to a 1, the command must be followed by a valid CRC to set this configuration bit. If a valid CRC is not received, the entire frame is ignored. If the bit is set to 1, it requires a CRC to clear it to 0.<br>0: no CRC function.<br>1: CRC function. | 0x0   | R/W    |
| 4       | CRC_R      | CRC Read. Controls the CRC functionality for the SDOA and SDOB/ALERT interface.<br>0: no CRC function.<br>1: CRC function.                                                                                                                                                                                                                             | 0x0   | R/W    |
| 3       | ALERT_EN   | Enable Alert Indicator Function. This alert function (on the SDOB/ALERT pin) is enabled when the SDO bit (Register 0x2, Bit 8) = 1. Otherwise, the ALERT_EN bit is ignored.<br>0: SDOB.<br>1: ALERT.                                                                                                                                                   | 0x0   | R/W    |
| 2       | RES        | Resolution. Sets the size of the conversion result data. If OSR = 0, these bits are ignored, and the resolution is set to the default resolution.<br>0: normal resolution.<br>1: 2-bit higher resolution.                                                                                                                                              | 0x0   | R/W    |
| 1       | REFSEL     | Reference Select. Selects the ADC reference source.<br>0: selects internal reference.<br>1: selects external reference.                                                                                                                                                                                                                                | 0x0   | R/W    |
| 0       | PMODE      | Power-Down Mode. Sets the power modes.<br>0: normal mode.<br>1: shutdown mode.                                                                                                                                                                                                                                                                         | 0x0   | R/W    |

**CONFIGURATION2 REGISTER**

Address: 0x2, Reset: 0x0000, Name: CONFIGURATION2

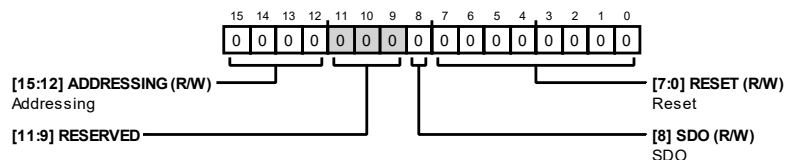
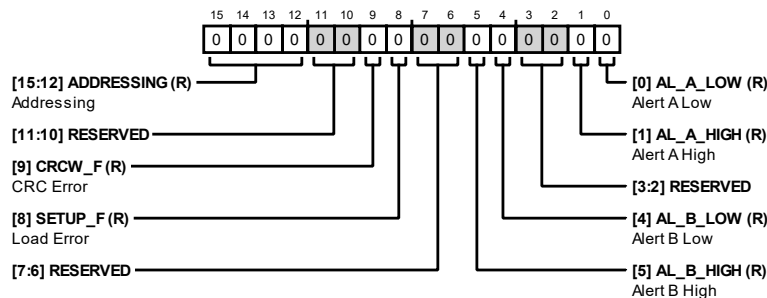


Table 17. Bit Descriptions for CONFIGURATION2 Register

| Bits    | Bit Name   | Description                                                                                                                                                                                                                                                                                                                                                                       | Reset | Access |
|---------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.                                                                                                                                                                                                                                                    | 0x0   | R/W    |
| [11:9]  | RESERVED   | Reserved.                                                                                                                                                                                                                                                                                                                                                                         | 0x0   | R      |
| 8       | SDO        | SDO. Conversion results serial data output.<br>0: 2-wire, conversion data are output on both SDOA and SDOB/ $\overline{\text{ALERT}}$ .<br>1: 1-wire, conversion data are output on SDOA only.                                                                                                                                                                                    | 0x0   | R/W    |
| [7:0]   | RESET      | Reset.<br>Set to 0x3C to perform a soft reset, which refreshes some blocks, and register contents remain unchanged. Clears the ALERT register and flushes any oversampling stored variables or active state machine.<br>Set to 0xFF to perform a hard reset, which resets all possible blocks in the device. Register contents are set to defaults. All other values are ignored. | 0x0   | R/W    |

**ALERT REGISTER**Address: 0x3, Reset: 0x0000, Name:  $\overline{\text{ALERT}}$ Table 18. Bit Descriptions for  $\overline{\text{ALERT}}$ 

| Bits    | Bit Name   | Description                                                                                                                                                                                                                                                                                                        | Reset | Access |
|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.                                                                                                                                                                                     | 0x0   | R      |
| [11:10] | RESERVED   | Reserved.                                                                                                                                                                                                                                                                                                          | 0x0   | R      |
| 9       | CRCW_F     | CRC Error. Indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read.<br>0: no CRC error.<br>1: CRC error.                                                                                                                            | 0x0   | R      |
| 8       | SETUP_F    | Load Error. The SETUP_F indicates that the device configuration data did not load correctly on startup. This bit does not clear on an ALERT register read. A hard reset via the CONFIGURATION2 register is required to clear this bit and restart the device setup again.<br>0: no setup error.<br>1: setup error. | 0x0   | R      |
| [7:6]   | RESERVED   | Reserved.                                                                                                                                                                                                                                                                                                          | 0x0   | R      |

| Bits  | Bit Name  | Description                                                                                                                                                                                                                                                                                       | Reset | Access |
|-------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 5     | AL_B_HIGH | Alert B High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0   | R      |
| 4     | AL_B_LOW  | Alert B Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication.    | 0x0   | R      |
| [3:2] | RESERVED  | Reserved.                                                                                                                                                                                                                                                                                         | 0x0   | R      |
| 1     | AL_A_HIGH | Alert A High. The alert indication high bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0   | R      |
| 0     | AL_A_LOW  | Alert A Low. The alert indication low bit indicates if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication.    | 0x0   | R      |

## ALERT\_LOW\_THRESHOLD REGISTER

Address: 0x4, Reset: 0x0800, Name: ALERT\_LOW\_THRESHOLD

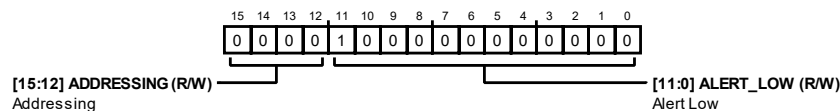


Table 19. Bit Descriptions for ALERT\_LOW\_THRESHOLD

| Bits    | Bit Name   | Description                                                                                                                                                                                                                                                                                                   | Reset | Access |
|---------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.                                                                                                                                                                                | 0x0   | R/W    |
| [11:0]  | ALERT_LOW  | Alert Low. Bits[11:0] from ALERT_LOW move to the MSBs of the internal ALERT_LOW register, Bits[15:4]. The remaining Bits[3:0] of the internal register are fixed at 0x0. Sets an alert when the converter result is below ALERT_LOW_THRESHOLD and the alert is disabled when it is above ALERT_LOW_THRESHOLD. | 0x800 | R/W    |

## ALERT\_HIGH\_THRESHOLD REGISTER

Address: 0x5, Reset: 0x07FF, Name: ALERT\_HIGH\_THRESHOLD

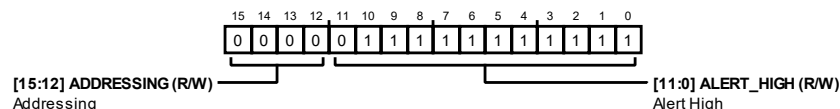


Table 20. Bit Descriptions for ALERT\_HIGH\_THRESHOLD

| Bits    | Bit Name   | Description                                                                                                                                                                                                                                                                                                                                                    | Reset | Access |
|---------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.                                                                                                                                                                                                                                 | 0x0   | R/W    |
| [11:0]  | ALERT_HIGH | Alert High. Bits[11:0] from ALERT_HIGH move to the MSBs of the internal ALERT_HIGH register, Bits[15:4]. The remaining Bits[3:0] of the internal register are fixed at 0xF. Sets an alert when the converter result is above the ALERT_HIGH_THRESHOLD register and the alert is disabled when the converter result is below the ALERT_HIGH_THRESHOLD register. | 0x7FF | R/W    |

## OUTLINE DIMENSIONS

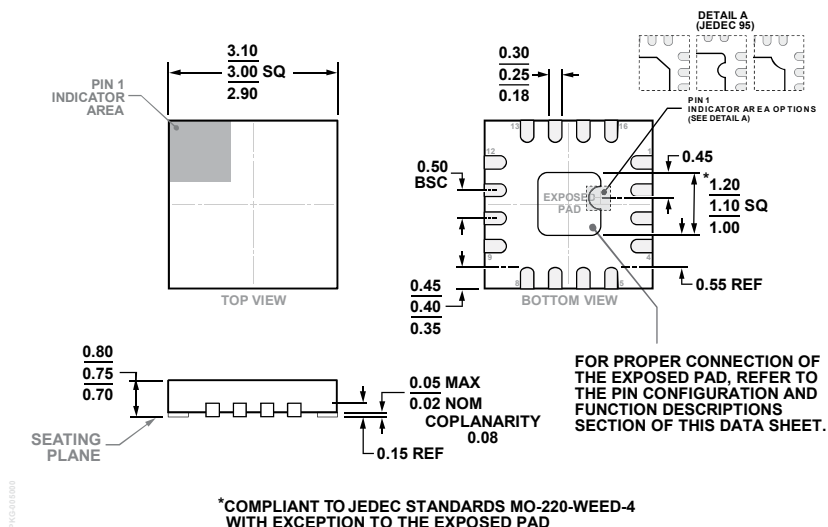


Figure 46. 16-Lead Lead Frame Chip Scale Package [LFCSP]  
3 mm × 3 mm Body and 0.75 mm Package Height  
(CP-16-45)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1,2</sup> | Resolution | Throughput Rate | Temperature Range | Package Description     | Package Option | Marking Code |
|----------------------|------------|-----------------|-------------------|-------------------------|----------------|--------------|
| AD4680BCPZ-RL        | 16-Bit     | 1 MSPS          | −40°C to +125°C   | 16-Lead LFCSP           | CP-16-45       | CAK          |
| AD4680BCPZ-RL7       | 16-Bit     | 1 MSPS          | −40°C to +125°C   | 16-Lead LFCSP           | CP-16-45       | CAK          |
| AD4681BCPZ-RL        | 16-Bit     | 500 kSPS        | −40°C to +125°C   | 16-Lead LFCSP           | CP-16-45       | CAM          |
| AD4681BCPZ-RL7       | 16-Bit     | 500 kSPS        | −40°C to +125°C   | 16-Lead LFCSP           | CP-16-45       | CAM          |
| EVAL-AD7380FMCZ      |            |                 |                   | AD7380 Evaluation Board |                |              |

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> Use the EVAL-AD7380FMCZ to evaluate the AD4680 and AD4681. The EVAL-AD7380FMCZ is compatible with the [EVAL-SDP-CH1Z](#) high speed controller board.