

# IH5208

## 4-Channel Differential Fault Protected CMOS Analog Multiplexer

### GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI549 and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to  $\pm 25V$ , even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

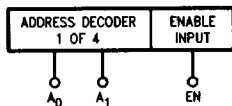
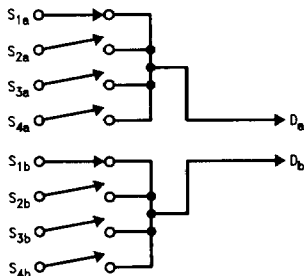
A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

### ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5208MJE	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	16 pin Cerdip
IH5208IJE	$-25^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	16 pin Cerdip
IH5208CPE	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	16 pin plastic DIP

### FEATURES

- All Channels OFF When Power OFF, for Analog Signals Up to  $\pm 25V$
- Power Supply Quiescent Current Less Than  $1\mu\text{A}$
- $\pm 13V$  Analog Signal Range
- No SCR Latchup
- Break-Before-Make Switching
- TTL and CMOS Compatible Strobe Control
- Pin Compatible With HI549
- Any Channel Turns OFF If Input Exceeds Supply Rails by Up to  $\pm 25V$
- TTL and CMOS Compatible Binary Address and ENable Inputs



2 LINE BINARY ADDRESS INPUTS

(0 0) AND EN = 1

ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON

**Figure 1. Functional Diagram**

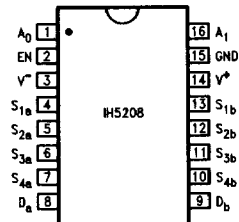
### TRUTH TABLE

A <sub>1</sub>	A <sub>0</sub>	EN	On Switch Pair
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A<sub>0</sub>, A<sub>1</sub>, EN

Logic "1" =  $V_{AH} \geq 2.4V$

Logic "0" =  $V_{AL} \leq 0.8V$



V+ Common to Substrate

TOP VIEW

**Figure 2: Pin Configuration (Outline dwg JE, PE)**

## ABSOLUTE MAXIMUM RATINGS

$V_{IN}$ (A, EN) to Ground	−15V, +15V
$V_S$ or $V_D$ to $V^+$	+25V, −40V
$V_S$ or $V_D$ to $V^-$	−25V, +40V
$V^+$ to Ground	20V
$V^-$ to Ground	−20V
Current (Any Terminal)	20mA
Operating Temperature	
C Suffix	0°C to +70°C
I Suffix	−25°C to +85°C
M Suffix	−55°C to +125°C

## Storage Temperature

C Suffix	−65°C to +125°C
I & M Suffix	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

## Power Dissipation\*

CERDIP Package**	900 mW
Plastic Package***	470 mW

\*Device mounted with all leads soldered or welded to PC board.

\*\*Derate 12 mW/°C above 75°C

\*\*\*Derate 6.3 mW/°C above 75°C

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS  $V^+ = 15V$ ,  $V^- = -15V$ ,  $V_{EN} = 2.4V$ , unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units	
					M Suffix			C Suffix				
					−55°C	25°C	125°C	−25°C/ 0°C	25°C	85°C/ 70°C		
SWITCH												
$R_{DS(on)}$	S to D	8	$V_D = 10V$ , $I_S = -100\mu A$	Sequence each switch on	900	1200	1200	1800	1500	1500	2000	$\Omega$
		8	$V_D = -10V$ , $I_S = -100\mu A$	$V_{AL} = 0.8V$ , $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	
$\Delta R_{DS(on)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg}}$ $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	8	$V_S = 10V$ , $V_D = -10V$	$V_{EN} = 0.8V$	$\pm 0.02$		$\pm 0.5$	$\pm 50$		$\pm 1.0$	$\pm 50$	nA
		8	$V_S = -10V$ , $V_D = 10V$		$\pm 0.02$		$\pm 0.5$	$\pm 50$		$\pm 1.0$	$\pm 50$	
$I_{D(off)}$	D	1	$V_D = 10V$ , $V_S = -10V$		$\pm 0.02$		$\pm 1.0$	$\pm 100$		$\pm 2.0$	$\pm 100$	
		1	$V_D = -10V$ , $V_S = 10V$		$\pm 0.05$		$\pm 1.0$	$\pm 100$		$\pm 2.0$	$\pm 100$	
$I_{D(on)}$	D	8	$V_{S(AH)} = V_D = 10V$	Sequence each switch on	$\pm 0.1$		$\pm 2.0$	$\pm 100$		$\pm 5.0$	$\pm 100$	
		8	$V_{S(AH)} = V_D = -10V$	$V_{AL} = 0.8V$ , $V_{AH} = 2.4V$	$\pm 0.1$		$\pm 2.0$	$\pm 100$		$\pm 5.0$	$\pm 100$	
FAULT												
$I_S$ with Power OFF	S	8	$V_{SUPP} = 0V$ , $V_{IN} = \pm 25V$ , $V_{EN} = V_O = 0V$ , $A_0$ , $A_1$ , $A_2 = 0V$		$\pm 1.0$		$\pm 2$			$\pm 5$		$\mu A$
$I_{S(off)}$ with Overvoltage	S	8	$V_{IN} = \pm 25V$ , $V_O = \pm 10V$		$\pm 1.0$		$\pm 5$			$\pm 10$		
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	$A_0$ , $A_1$ , $A_2$ or EN	4	$V_A = 0V$		0.01		−10	−30		−10	−30	$\mu A$
		4	$V_A = 15V$		0.01		10	30		10	30	

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V, VEN = 2.4V, unless otherwise specified. (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units	
					M Suffix			C Suffix				
					-55°C	25°C	125°C	-20°C/0°C	25°C	85°C/70°C		
DYNAMIC												
t <sub>transition</sub>	D		See Figure 3	0.3								μS
t <sub>open</sub>	D		See Figure 4	0.2								
t <sub>on(EN)</sub>	D		See Figure 5	0.6		1.5						
t <sub>off(EN)</sub>	D			0.4		1						
t <sub>on-toff Break-Before-Make Delay Settling Time</sub>	D		V <sub>EN</sub> = +5V, A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> Strobed V <sub>IN</sub> = ±10V, See Figure 6	10								ns
“OFF” Isolation	D		V <sub>EN</sub> = 0V, R <sub>L</sub> = 200Ω, C <sub>L</sub> = 3pF, V <sub>S</sub> = 3VRMS, f = 500kHz	60								dB
C <sub>S(off)</sub>	S		V <sub>S</sub> = 0V	5								pF
C <sub>D(off)</sub>	D		V <sub>D</sub> = 0V	25								
C <sub>DS(off)</sub>	D to S		V <sub>S</sub> = 0V, V <sub>D</sub> = 0V	1								
SUPPLY												
Supply Current	+	I+	1	V <sub>EN</sub> = 5V All V <sub>A</sub> = 0V/5V	0.5	0.7	0.6	0.5		1.0		mA
	-	I-	1		0.02	0.7	0.6	0.5		1.0		

Note 1. Readings taken 400ms after the overvoltage occurs.

SWITCHING INFORMATION

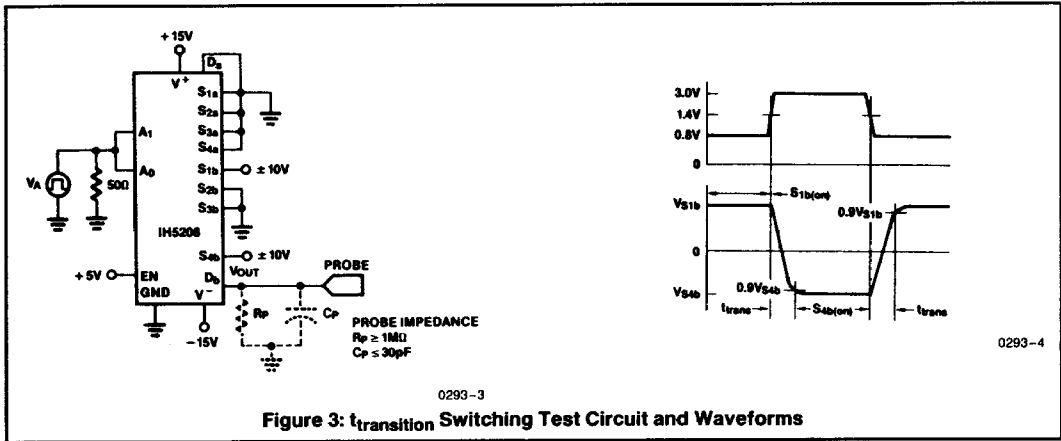
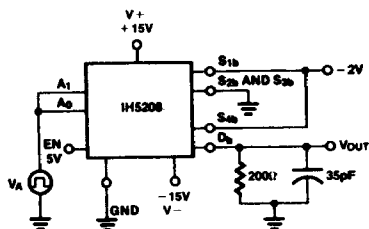


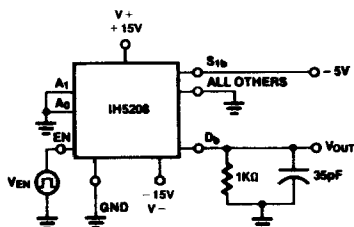
Figure 3: t<sub>transition</sub> Switching Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

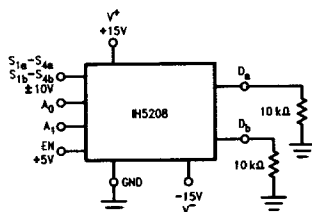
## SWITCHING INFORMATION (Continued)



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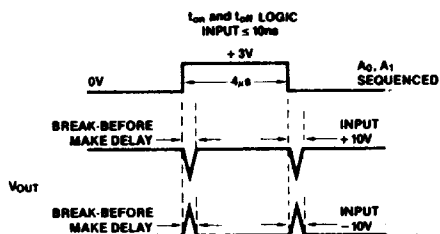
Figure 4:  $t_{open}$  (Break-Before-Make) Switching Test Circuit and Waveforms

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Figure 5: Enable  $t_{on}$  and  $t_{off}$  Switching Test Circuit and Waveforms

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Figure 6: Break-Before-Make Delay Test Circuit and Waveforms



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## DETAILED DESCRIPTION

The IH5208, like all Harris' multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5208 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5208 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with the dielectrically isolated process to eliminate these problems.

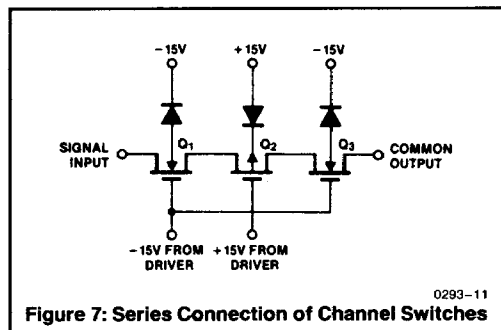


Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

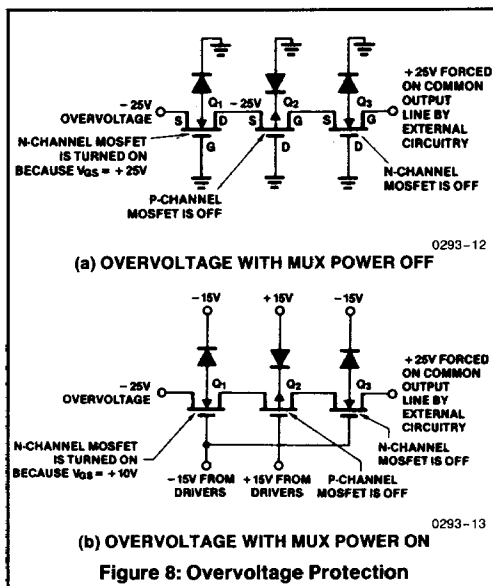


Figure 8: Overvoltage Protection

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

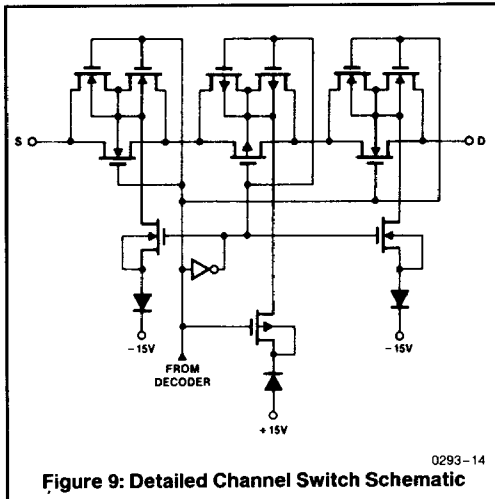


Figure 9: Detailed Channel Switch Schematic

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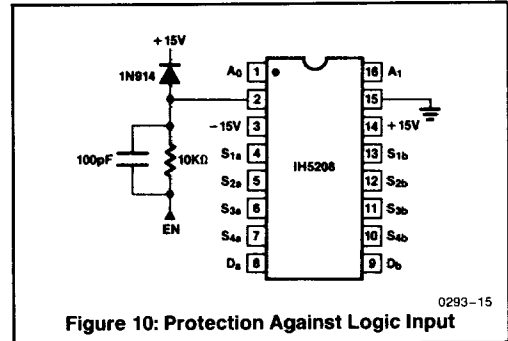


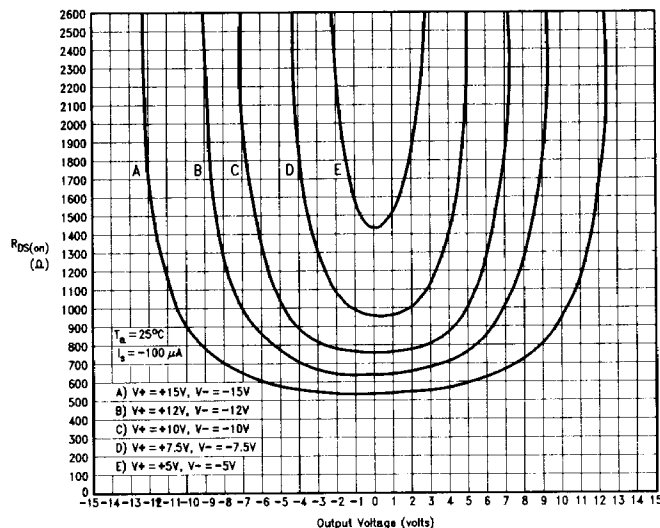
Figure 10: Protection Against Logic Input

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## MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5208 is designed to handle signals in the  $\pm 10V$  range, with a typical  $r_{DS(on)}$  of  $900\Omega$ ; it can successfully handle signals up to  $\pm 12V$ , however,  $r_{DS(on)}$  will increase to about  $1.8k\Omega$ . Beyond  $\pm 12V$  the device approaches an open circuit, and thus  $\pm 12V$  is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

Figure 11:  $R_{DS(on)}$  vs Analog Signal Voltage

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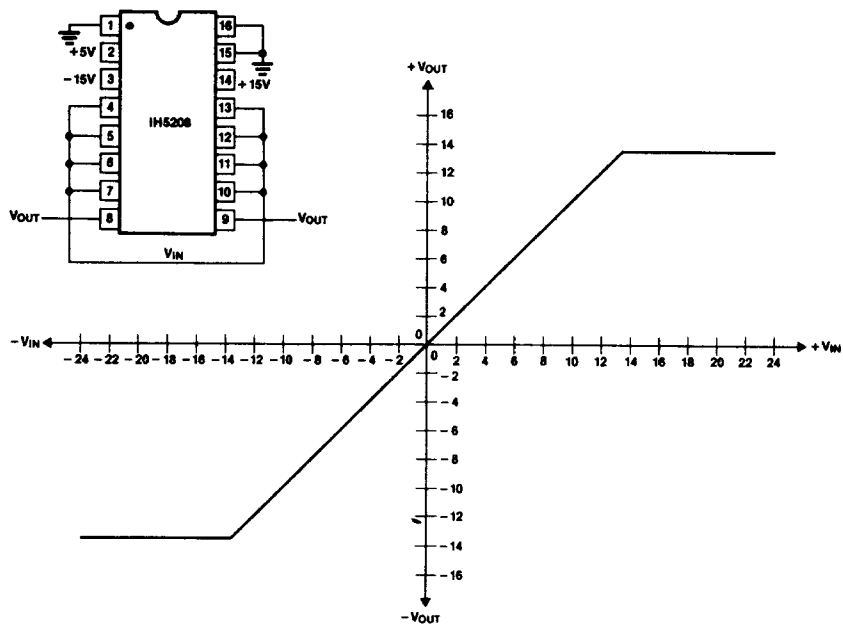


Figure 12: MUX Output Voltage vs Input Voltage Channel 1 Shown; All Channels Similar

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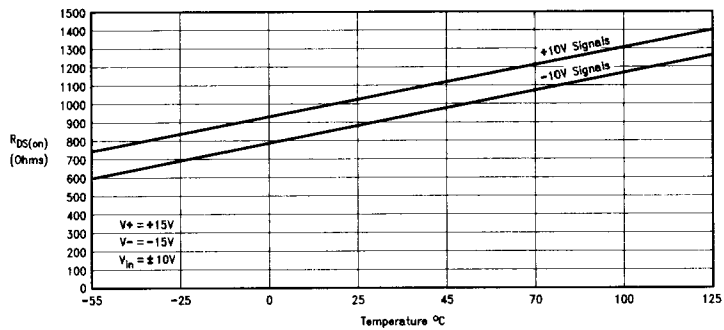


Figure 13: Typical  $R_{DS(on)}$  Variation with Temperature

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NOTE: All typical values have been characterized but are not tested.

## USING THE IH5208 WITH SUPPLIES OTHER THAN $\pm 15V$

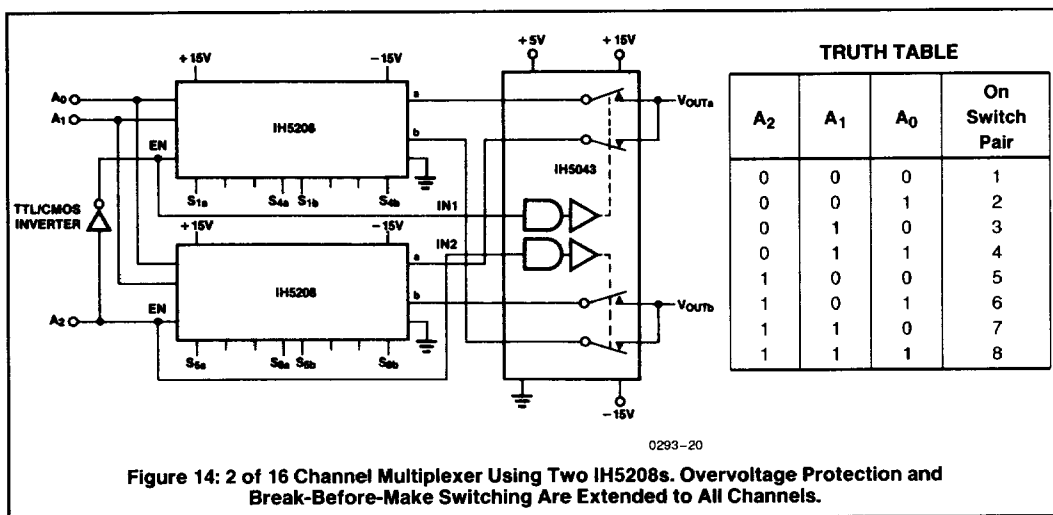
The IH5208 will operate successfully with supply voltages from  $\pm 5V$  to  $\pm 15V$ , however  $r_{DS(on)}$  increases as supply voltage decreases, as shown in Figure 11. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of  $r_{DS(on)}$  and leakage current remains reasonably constant.  $r_{DS(on)}$  also decreases as signal levels decrease. For high system accuracy [acceptable levels of  $r_{DS(on)}$ ] the maximum input signal should be 3V less than the supply voltages. The logic thresholds remain TTL compatible.

## IH5208 APPLICATIONS INFORMATION

## APPLICATION NOTES

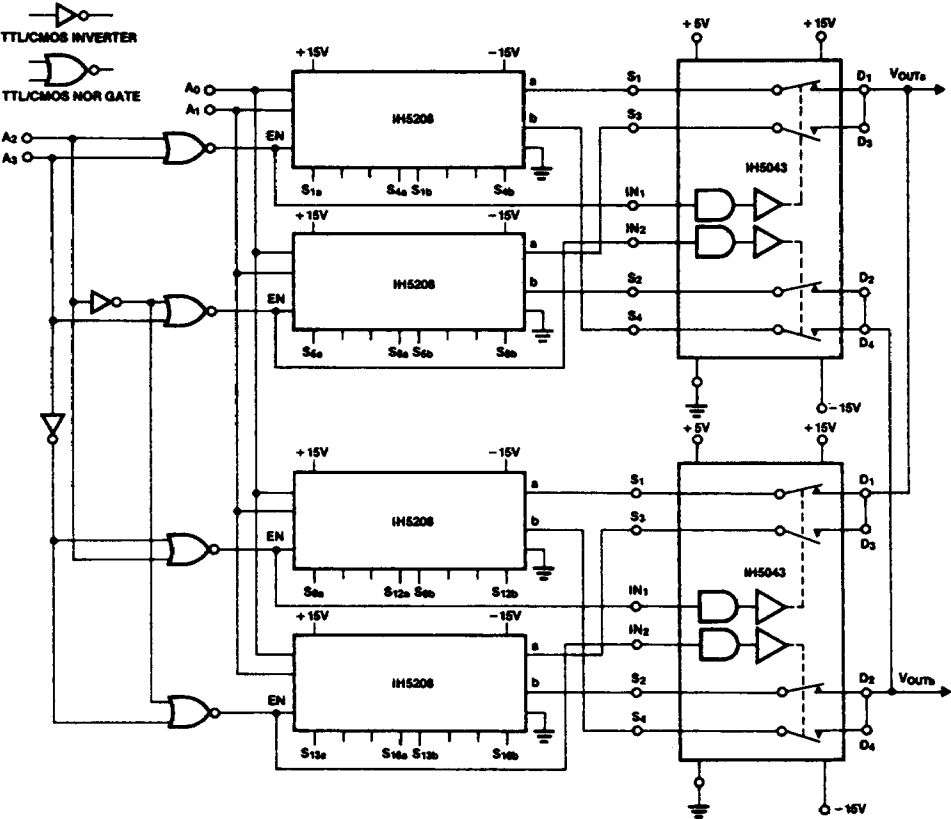
Further information may be found in:

- A003** "Understanding and Applying the Analog Switch"
- A006** "A New CMOS Analog Gate Technology"
- A020** "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"





IH5208 APPLICATIONS INFORMATION (Continued)



TRUTH TABLE

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	On Switch		On Switch	
0	0	0	0	S1a	V <sub>OUTa</sub>	S1b	V <sub>OUTb</sub>
0	0	0	1	S2a		S2b	
0	0	1	0	S3a		S3b	
0	0	1	1	S4a		S4b	
0	1	0	0	S5a		S5b	
0	1	0	1	S6a		S6b	
0	1	1	0	S7a		S7b	
0	1	1	1	S8a		S8b	
1	0	0	0	S9a		S9b	
1	0	0	1	S10a		S10b	
1	0	1	0	S11a		S11b	
1	0	1	1	S12a		S12b	
1	1	0	0	S13a		S13b	
1	1	0	1	S14a		S14b	
1	1	1	0	S15a		S15b	
1	1	1	1	S16a		S16b	

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Figure 15: Submultiplexed 2 of 32 System. The Two IH5043s Are Overvoltage Protected By The IH5208s. Submultiplexing Reduces Output Capacitance and Leakage Currents.

NOTE: All typical values have been characterized but are not tested.