

LME49721 High-Performance, High-Fidelity Rail-to-Rail Input/Output Audio Operational Amplifier

Check for Samples: [LME49721](#)

FEATURES

- Rail-to-Rail Input and Output
- Easily Drives 10kΩ Loads to Within 10mV of Each Power Supply Voltage
- Optimized for Superior Audio Signal Fidelity
- Output Short Circuit Protection

APPLICATIONS

- Ultra High-Quality Portable Audio Amplification
- High-Fidelity Preamplifiers
- High-Fidelity Multimedia
- State-of-the-Art Phono Pre Amps
- High-Performance Professional Audio
- High-Fidelity Equalization and Crossover Networks
- High-Performance Line Drivers
- High-Performance Line Receivers
- High-Fidelity Active Filters
- DAC I–V Converter
- ADC Front-End Signal Conditioning

KEY SPECIFICATIONS

- Power Supply Voltage Range: 2.2V to 5.5V
- Quiescent Current: 2.15mA (typ)
- THD+N ($A_V = 2$, $V_{OUT} = 4V_{p-p}$, $f_{IN} = 1kHz$)
 - $R_L = 2k\Omega$: 0.00008% (typ)
 - $R_L = 600\Omega$: 0.0001% (typ)
- Input Noise Density: 4nV/ $\sqrt{Hz}$ (typ), @ 1kHz
- Slew Rate: $\pm 8.5V/\mu s$ (typ)
- Gain Bandwidth Product: 20MHz (typ)
- Open Loop Gain ($R_L = 600\Omega$): 118dB (typ)
- Input Bias Current: 40fA (typ)
- Input Offset Voltage: 0.3mV (typ)
- PSRR: 103dB (typ)

DESCRIPTION

The LME49721 is a low-distortion, low-noise Rail-to-Rail Input/Output operational amplifier optimized and fully specified for high-performance, high-fidelity applications. Combining advanced leading-edge process technology with state-of-the-art circuit design, the LME49721 Rail-to-Rail Input/Output operational amplifier delivers superior signal amplification for outstanding performance. The LME49721 combines a very high slew rate with low THD+N to easily satisfy demanding applications. To ensure that the most challenging loads are driven without compromise, the LME49721 has a high slew rate of $\pm 8.5V/\mu s$ and an output current capability of $\pm 9.7mA$. Further, dynamic range is maximized by an output stage that drives 10kΩ loads to within 10mV of either power supply voltage.

The LME49721 has a wide supply range of 2.2V to 5.5V. Over this supply range the LME49721's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49721 is unity gain stable.



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TYPICAL CONNECTION AND PINOUT

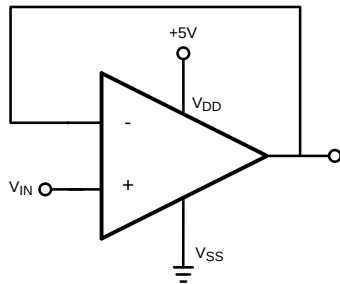


Figure 1. Buffer Amplifier

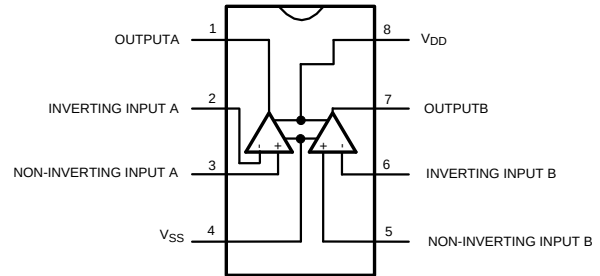


Figure 2. 8-Pin SOIC (D Package)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾⁽³⁾

Power Supply Voltage ($V_S = V^+ - V^-$)	6V
Storage Temperature	-65°C to 150°C
Input Voltage	(V-) - 0.7V to (V+) + 0.7V
Output Short Circuit ⁽⁴⁾	Continuous
Power Dissipation	Internally Limited
ESD Rating ⁽⁵⁾	2000V
ESD Rating ⁽⁶⁾	200V
Junction Temperature	150°C
Thermal Resistance, θ_{JA} (SOIC)	165°C/W
Temperature Range, $T_{MIN} \leq T_A \leq T_{MAX}$	-40°C $\leq T_A \leq$ 85°C
Supply Voltage Range	2.2V $\leq V_S \leq$ 5.5V

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified
- (2) The Electrical Characteristics table lists ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.
- (5) Human body model, applicable std. JESD22-A114C.
- (6) Machine model, applicable std. JESD22-A115-A.

ELECTRICAL CHARACTERISTICS FOR THE LME49721

The following specifications apply for the circuit shown in [Figure 1](#). $V_S = 5V$, $R_L = 10k\Omega$, $R_{SOURCE} = 10\Omega$, $f_{IN} = 1kHz$, and $T_A = 25^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	LME49721		Units (Limits)
			Typical ⁽¹⁾	Limit ⁽²⁾	
THD+N	Total Harmonic Distortion + Noise	$A_V = +1$, $V_{OUT} = 2V_{P-P}$, $R_L = 2k\Omega$ $R_L = 600\Omega$	0.0002 0.0002	0.001	% (max)
IMD	Intermodulation Distortion	$A_V = +1$, $V_{OUT} = 2V_{P-P}$, Two-tone, 60Hz & 7kHz 4:1	0.0004		%
GBWP	Gain Bandwidth Product		20	15	MHz (min)
SR	Slew Rate	$A_V = +1$	8.5		V/ μs (min)
FPBW	Full Power Bandwidth	$V_{OUT} = 1V_{P-P}$, -3dB referenced to output magnitude at $f = 1kHz$	2.2		MHz
t_s	Settling time	$A_V = 1$, 4V step 0.1% error range	800		ns
e_n	Equivalent Input Noise Voltage	$f_{BW} = 20Hz$ to $20kHz$, A-weighted	.707	1.13	μV_{P-P} (max)
	Equivalent Input Noise Density	$f = 1kHz$ A-weighted	4	6	$nV/\sqrt{Hz}$ (max)
i_n	Current Noise Density	$f = 10kHz$	4.0		$fA/\sqrt{Hz}$
V_{OS}	Offset Voltage		0.3	1.5	mV (max)
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Voltage Drift vs Temperature	$40^\circ C \leq T_A \leq 85^\circ C$	1.1		$\mu V/^\circ C$
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage		103	85	dB (min)
ISO _{CH-CH}	Channel-to-Channel Isolation	$f_{IN} = 1kHz$	117		dB
I_B	Input Bias Current	$V_{CM} = V_S/2$	40		fA
$\Delta I_{OS}/\Delta Temp$	Input Bias Current Drift vs Temperature	$-40^\circ C \leq T_A \leq 85^\circ C$	48		fA/ $^\circ C$
I_{OS}	Input Offset Current	$V_{CM} = V_S/2$	60		fA
V_{IN-CM}	Common-Mode Input Voltage Range			(V+) - 0.1 (V-) + 0.1	V (min)
CMRR	Common-Mode Rejection	$V_{SS} - 100mV < V_{CM} < V_{DD} + 100mV$	93	70	dB (min)
	1/f Corner Frequency		2000		Hz
A_{VOL}	Open Loop Voltage Gain	$V_{SS} - 200mV < V_{OUT} < V_{DD} + 200mV$			
		$R_L = 600\Omega$	118	100	dB (min)
		$R_L = 2k\Omega$	122		dB (min)
		$R_L = 10k\Omega$	130	115	dB (min)
V_{OUTMIN}	Output Voltage Swing	$R_L = 600\Omega$	$V_{DD} - 30mV$	$V_{DD} - 80mV$	V (min)
			$V_{SS} + 30mV$	$V_{SS} + 80mV$	V (min)
		$R_L = 10k\Omega$, $V_S = 5.0V$	$V_{DD} - 10mV$	$V_{DD} - 20mV$	V (min)
			$V_{SS} + 10mV$	$V_{SS} + 20mV$	V (min)
I_{OUT}	Output Current	$R_L = 250\Omega$, $V_S = 5.0V$	9.7	9.3	mA (min)
I_{OUT-SC}	Short Circuit Current		100		mA
R_{OUT}	Output Impedance	$f_{IN} = 10kHz$ Closed-Loop Open-Loop	0.01 46		Ω
I_S	Quiescent Current per Amplifier	$I_{OUT} = 0mA$	2.15	3.25	mA (max)

(1) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(2) Datasheet min/max specification limits are ensured by test or statistical analysis.

TYPICAL PERFORMANCE CHARACTERISTICS

Graphs were taken in dual supply configuration.

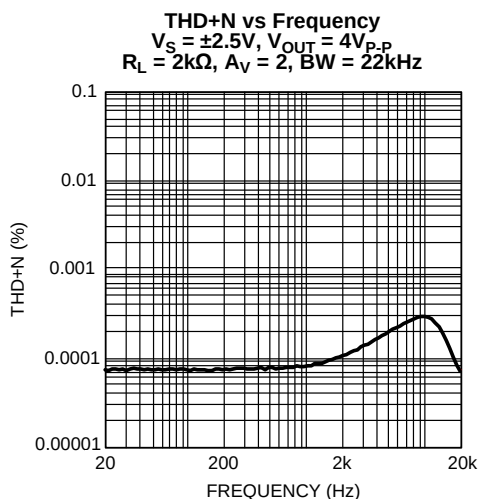


Figure 3.

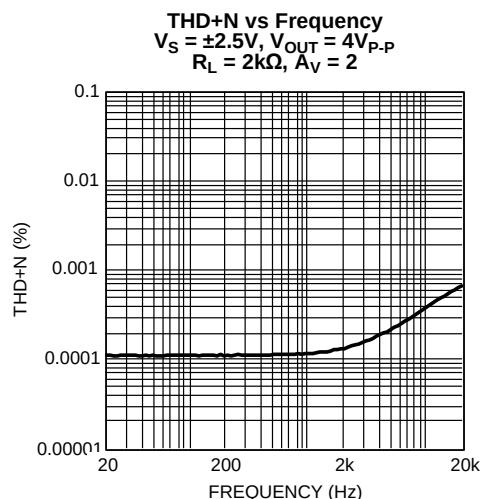


Figure 4.

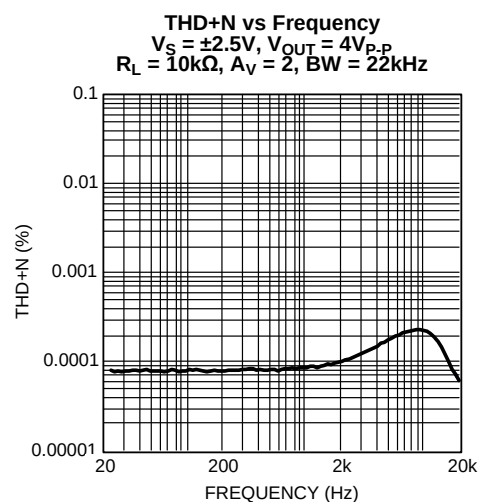


Figure 5.

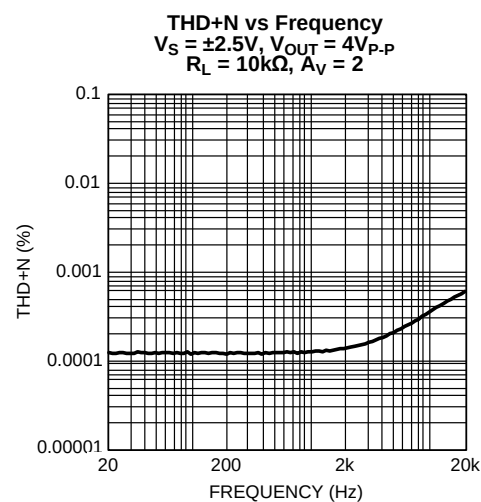


Figure 6.

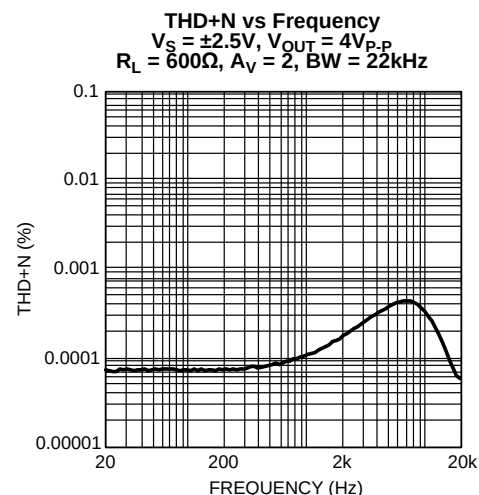


Figure 7.

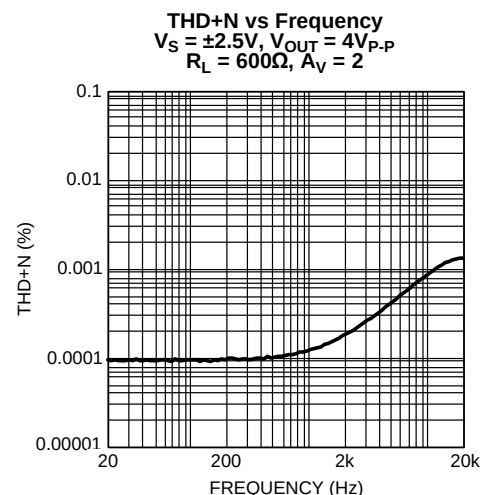


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.

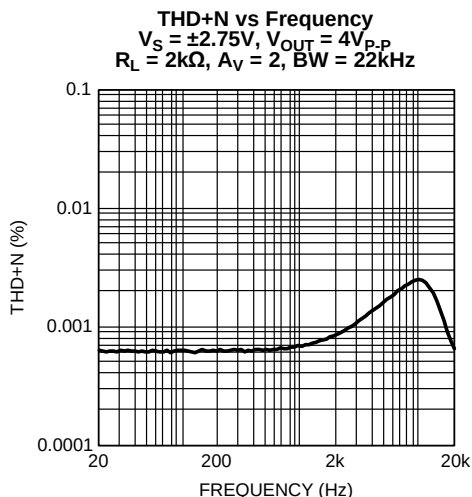


Figure 9.

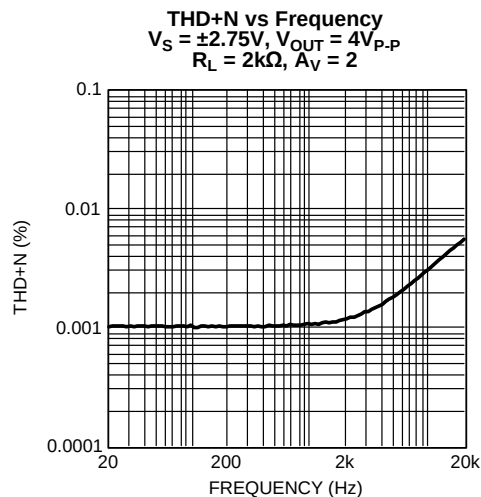


Figure 10.

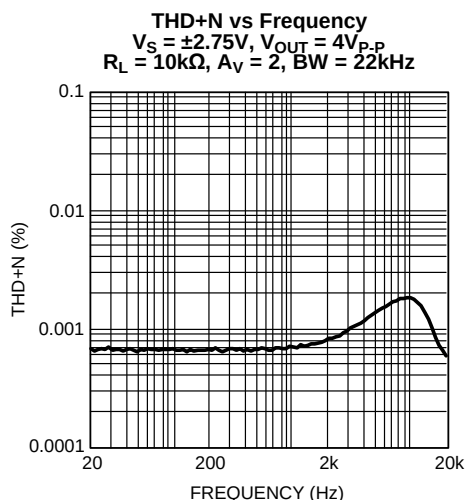


Figure 11.

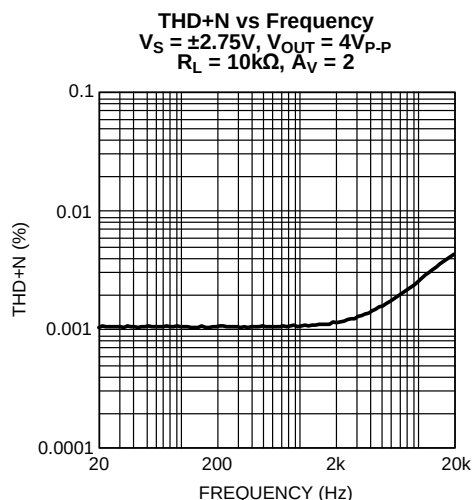


Figure 12.

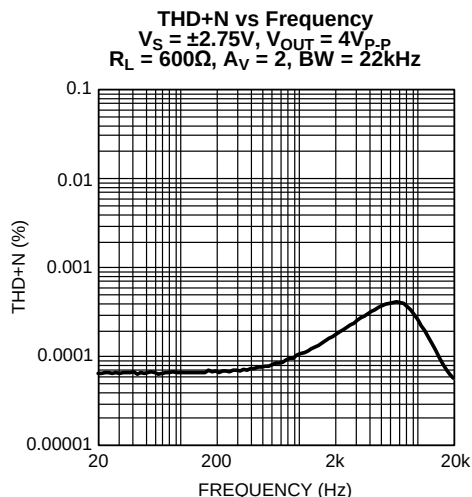


Figure 13.

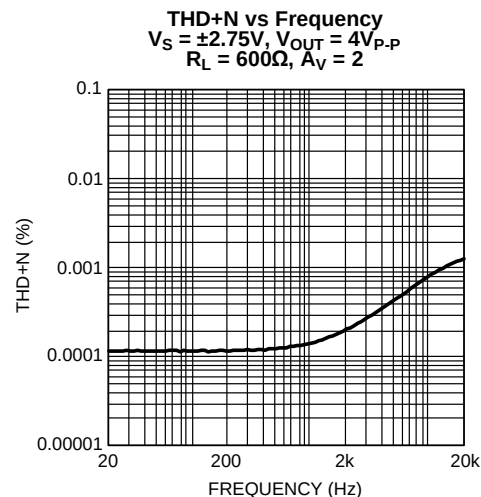


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.

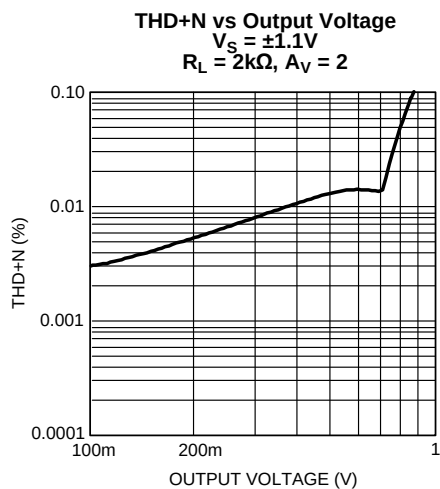


Figure 15.

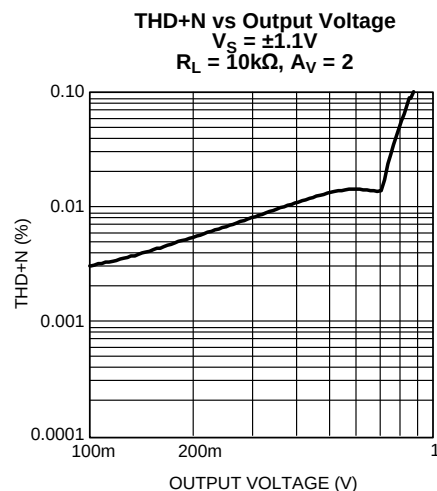


Figure 16.

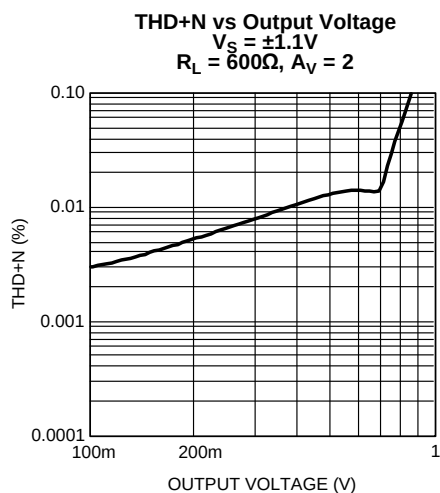


Figure 17.

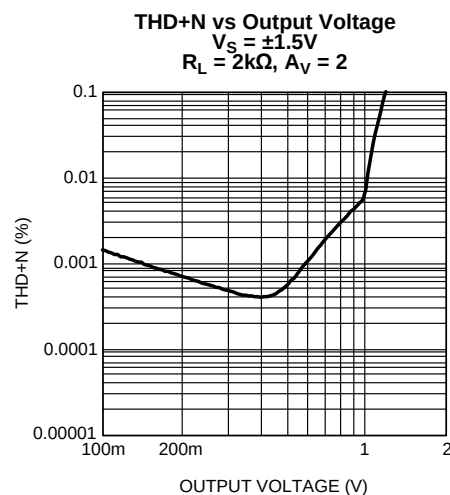


Figure 18.

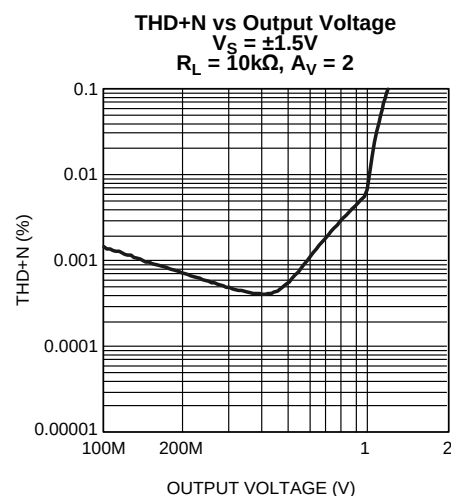


Figure 19.

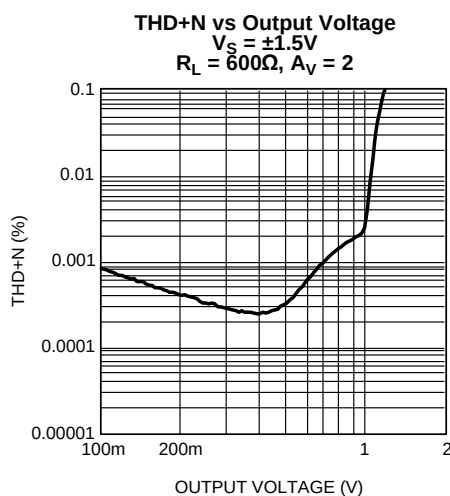


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.

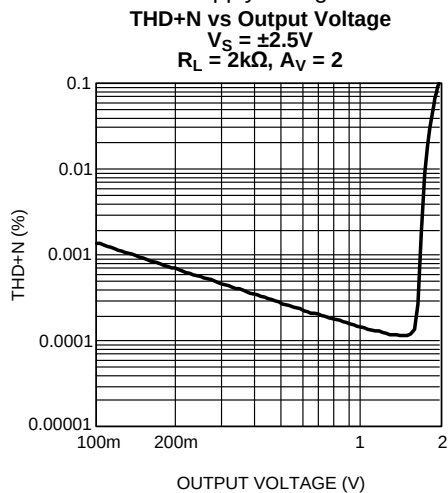


Figure 21.

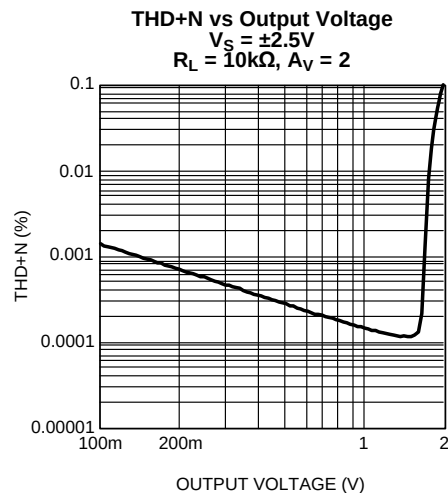


Figure 22.

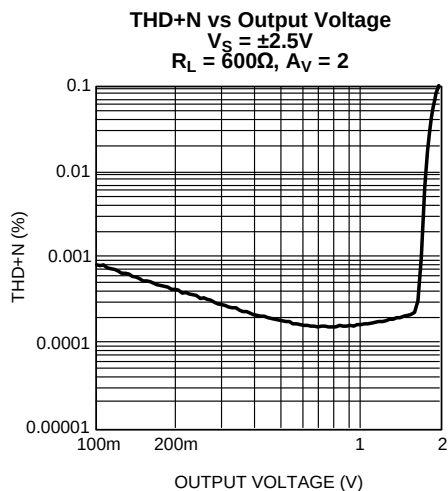


Figure 23.

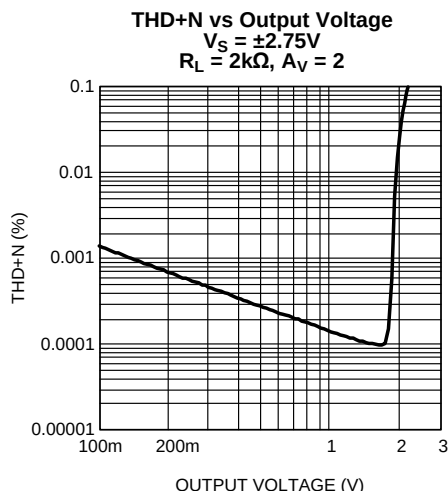


Figure 24.

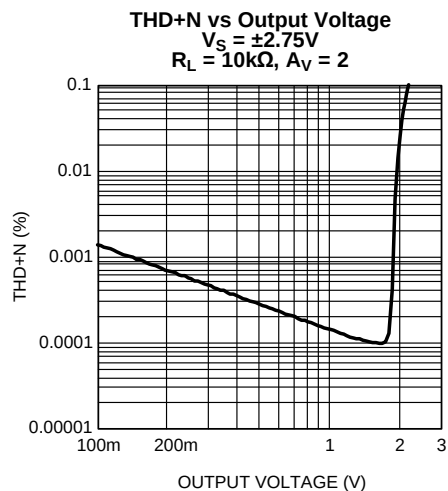


Figure 25.

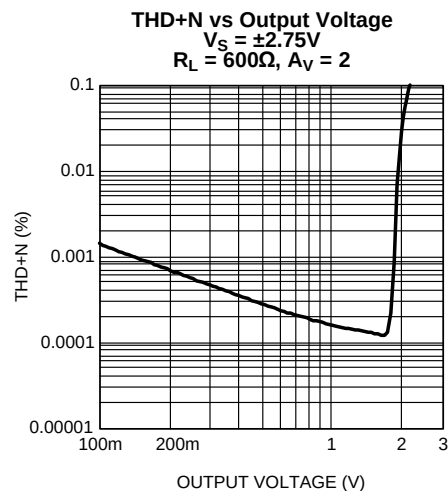


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.

Crosstalk vs Frequency

$$\begin{aligned} V_S &= \pm 1.1V \\ V_{OUT} &= 2V_{p-p} \\ R_L &= 2k\Omega \end{aligned}$$

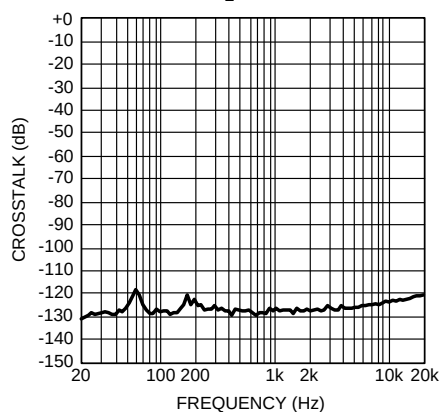


Figure 27.

Crosstalk vs Frequency

$$\begin{aligned} V_S &= \pm 1.1V \\ V_{OUT} &= 2V_{p-p} \\ R_L &= 10k\Omega \end{aligned}$$

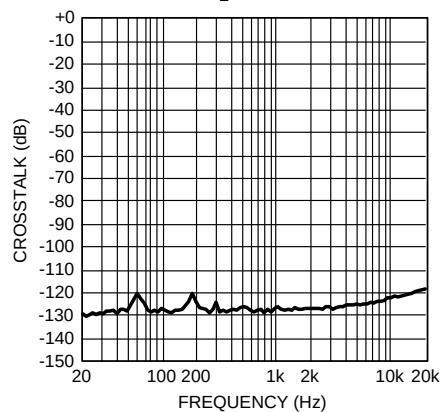


Figure 28.

Crosstalk vs Frequency

$$\begin{aligned} V_S &= \pm 1.1V \\ V_{OUT} &= 2V_{p-p} \\ R_L &= 600\Omega \end{aligned}$$

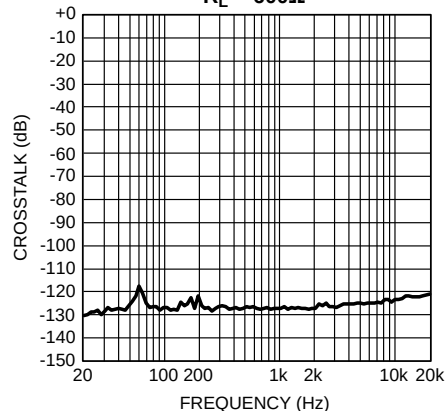


Figure 29.

Crosstalk vs Frequency

$$\begin{aligned} V_S &= \pm 1.5V \\ V_{OUT} &= 2V_{p-p} \\ R_L &= 2k\Omega \end{aligned}$$

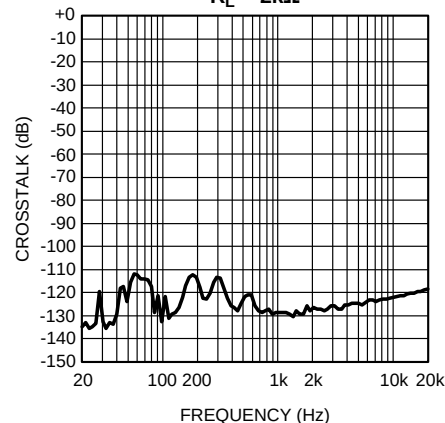


Figure 30.

Crosstalk vs Frequency

$$\begin{aligned} V_S &= \pm 1.5V \\ V_{OUT} &= 2V_{p-p} \\ R_L &= 10k\Omega \end{aligned}$$

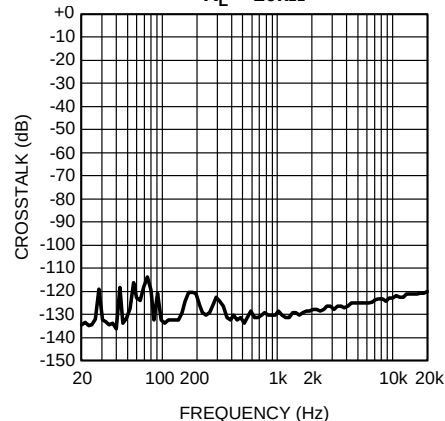


Figure 31.

Crosstalk vs Frequency

$$\begin{aligned} V_S &= \pm 1.5V \\ V_{OUT} &= 2V_{p-p} \\ R_L &= 600\Omega \end{aligned}$$

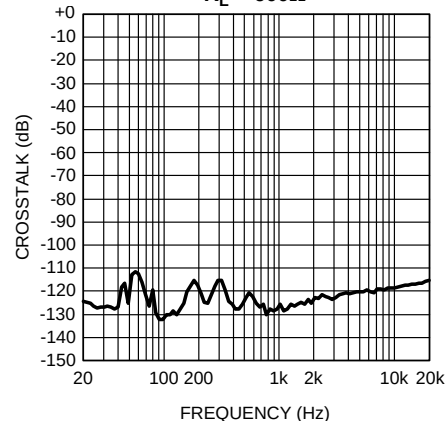


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.

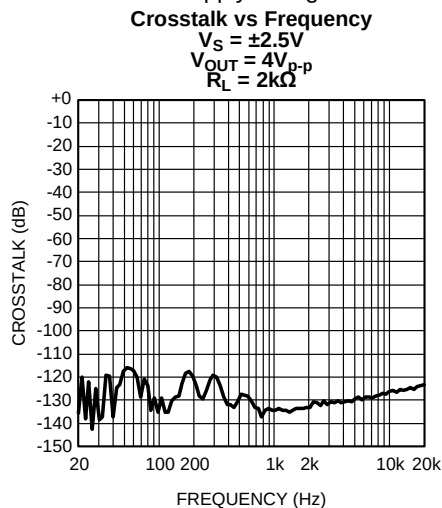


Figure 33.

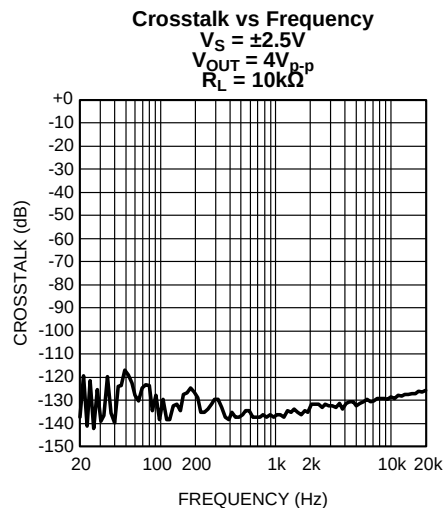


Figure 34.

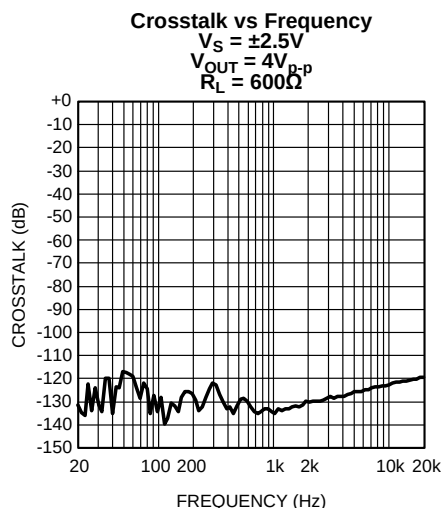


Figure 35.

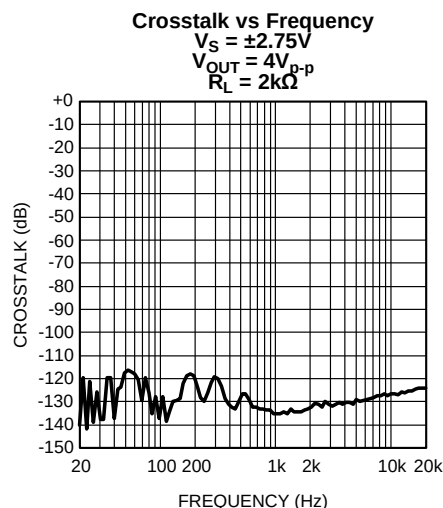


Figure 36.

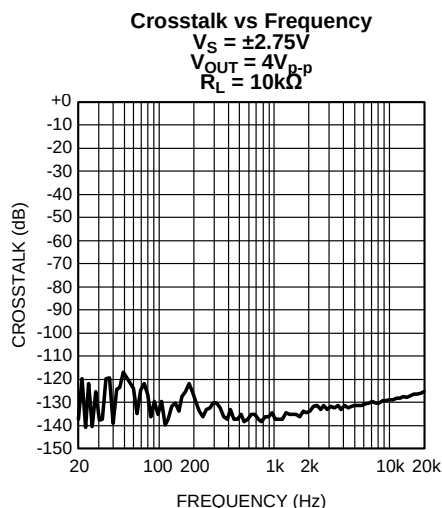


Figure 37.

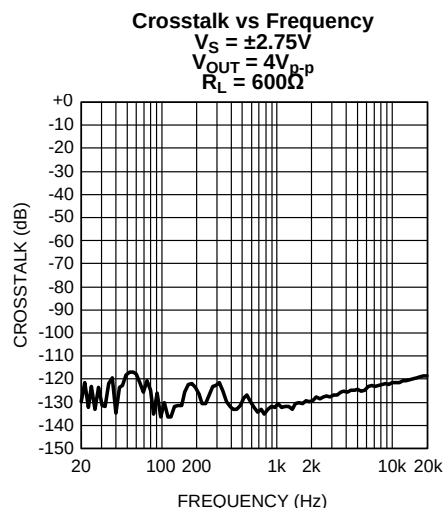


Figure 38.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.

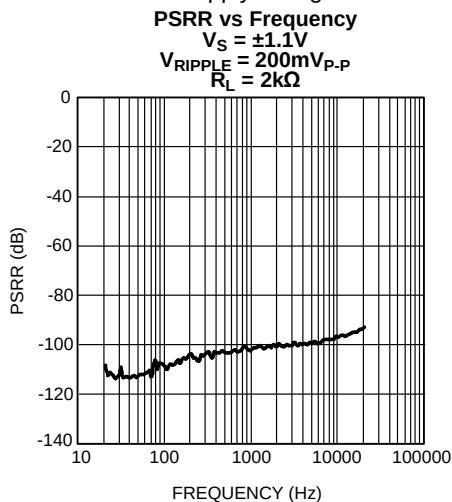


Figure 39.

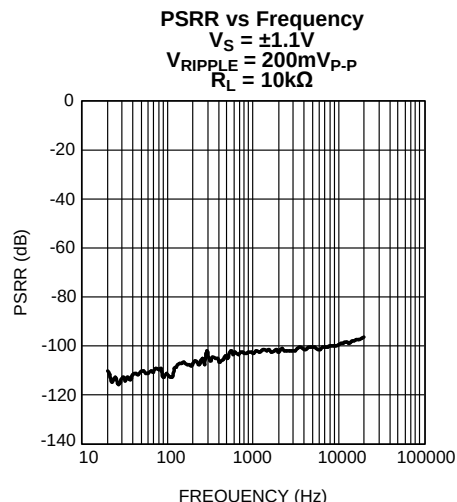


Figure 40.

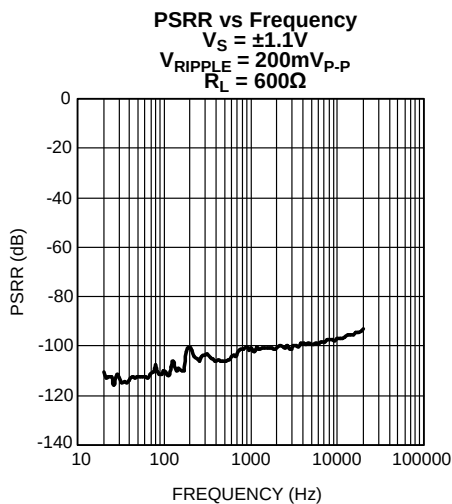


Figure 41.

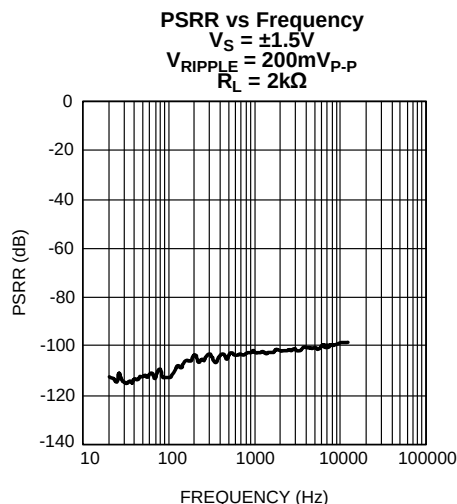


Figure 42.

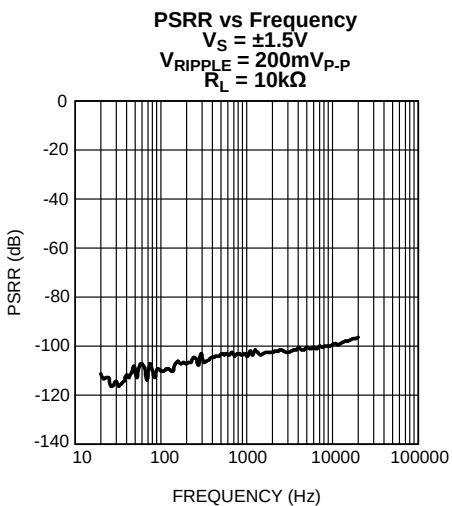


Figure 43.

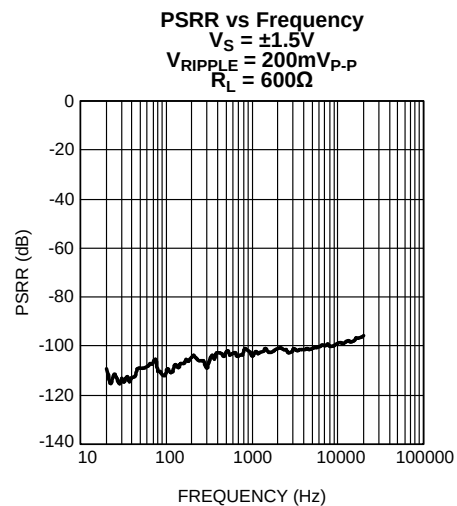
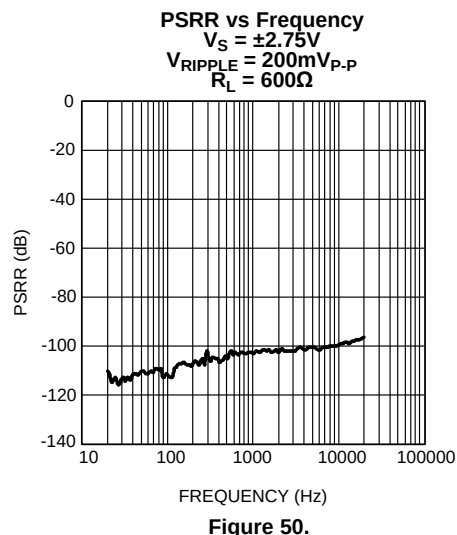
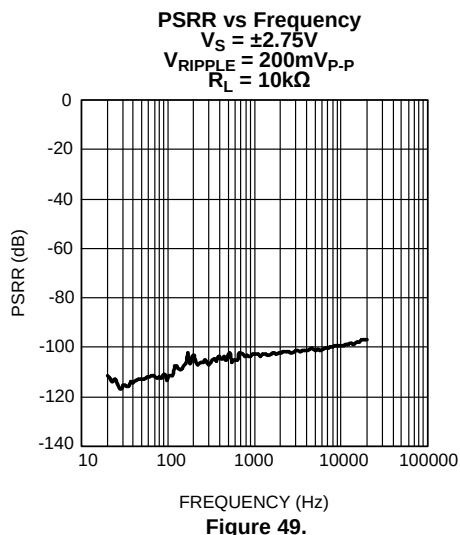
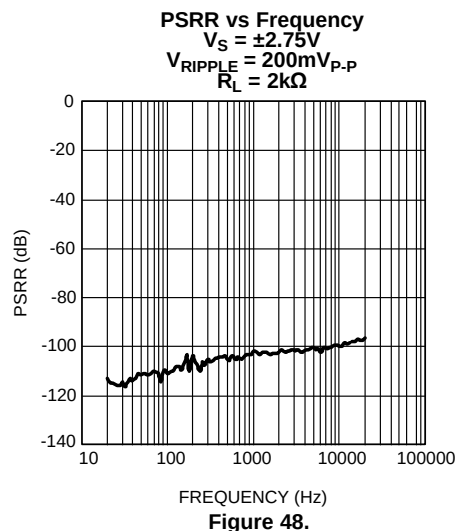
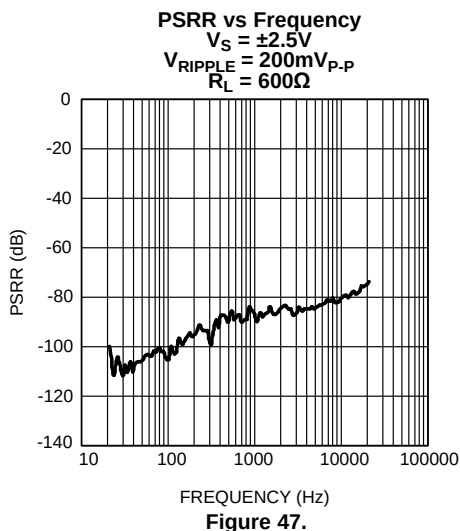
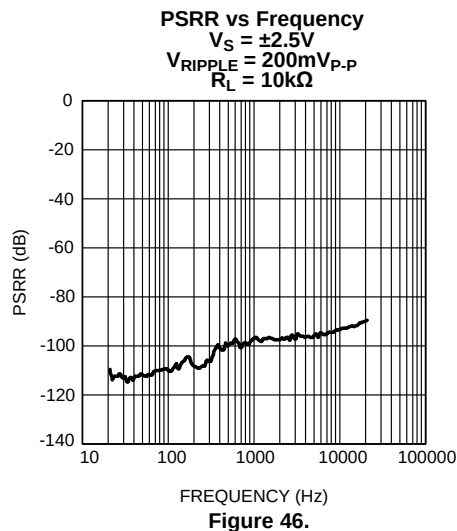
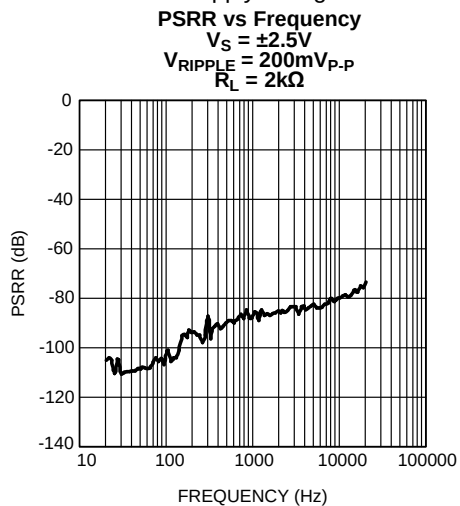


Figure 44.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.

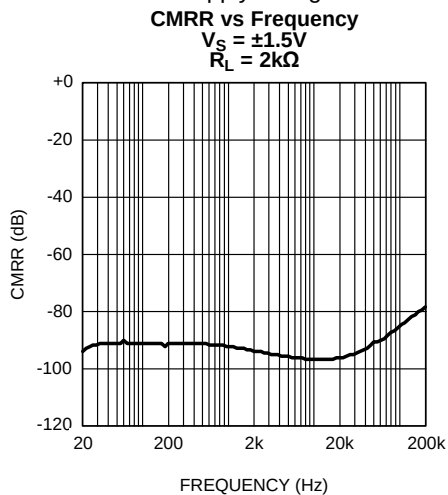


Figure 51.

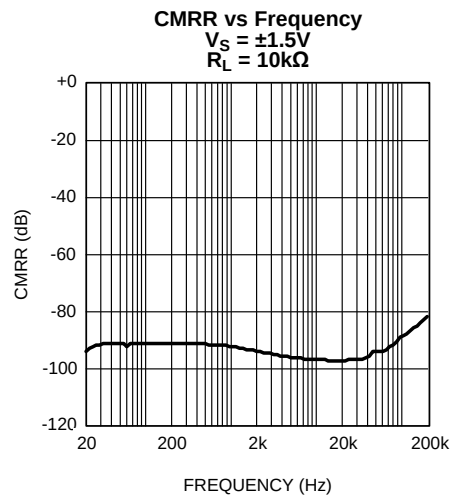


Figure 52.

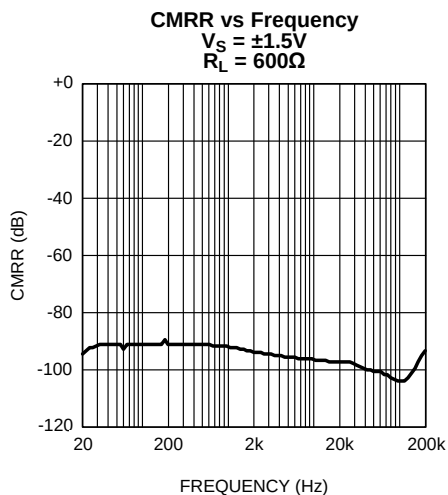


Figure 53.

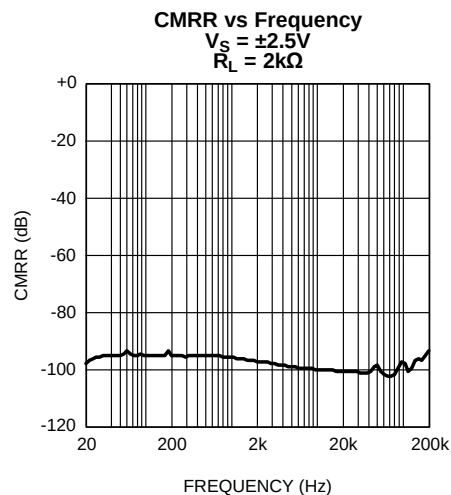


Figure 54.

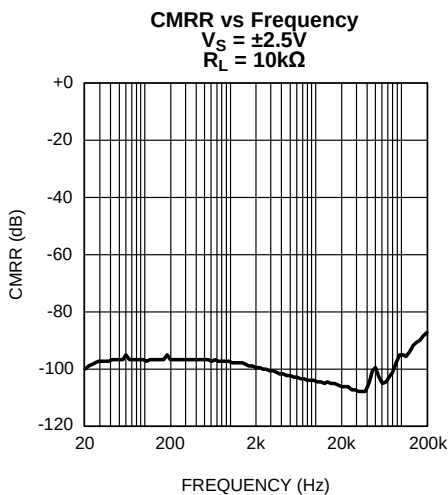


Figure 55.

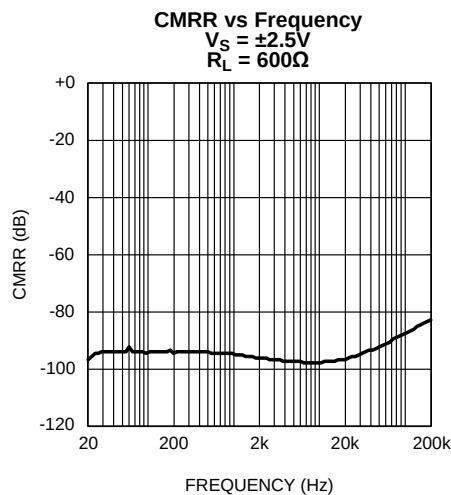
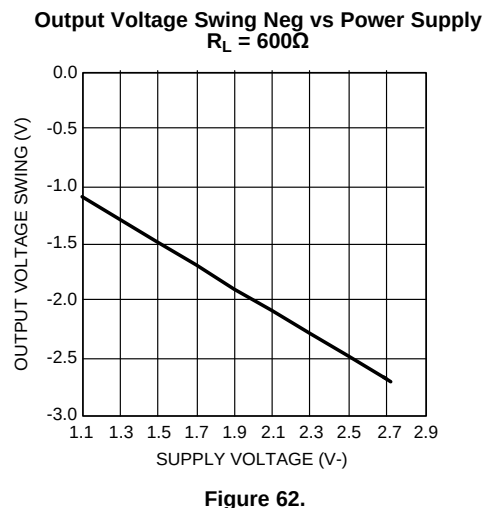
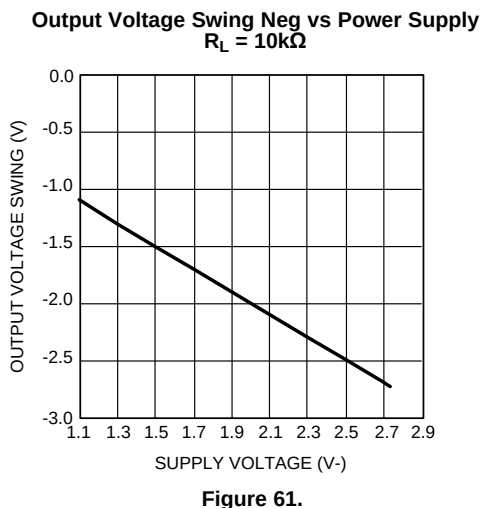
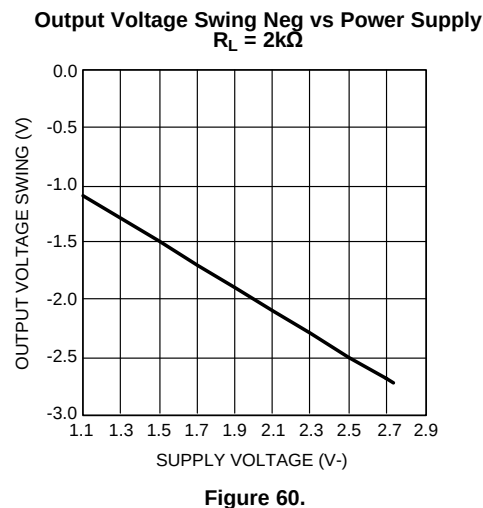
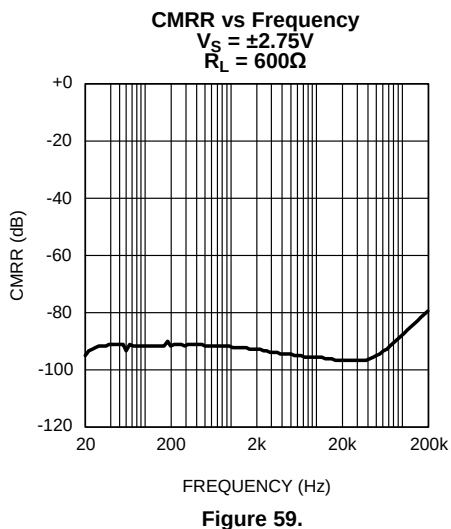
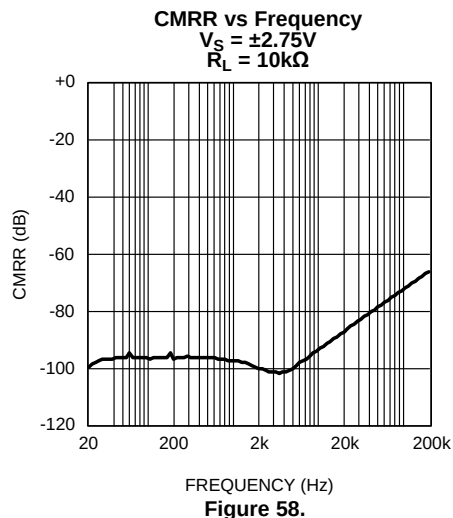
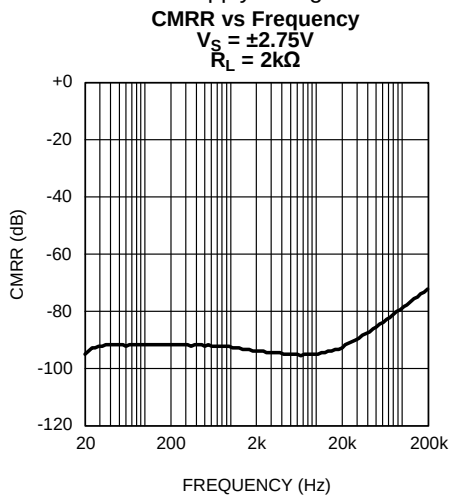


Figure 56.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.

Output Voltage Swing Pos vs Power Supply
 $R_L = 2k\Omega$

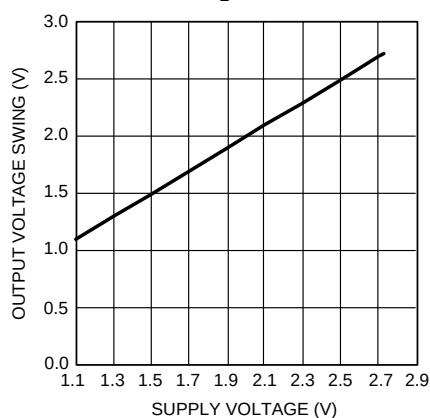


Figure 63.

Output Voltage Swing Pos vs Power Supply
 $R_L = 10k\Omega$

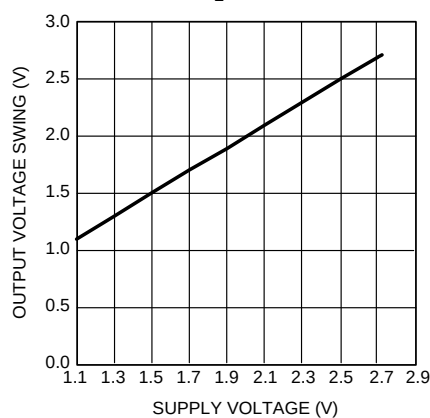


Figure 64.

Output Voltage Swing Pos vs Power Supply
 $R_L = 600\Omega$

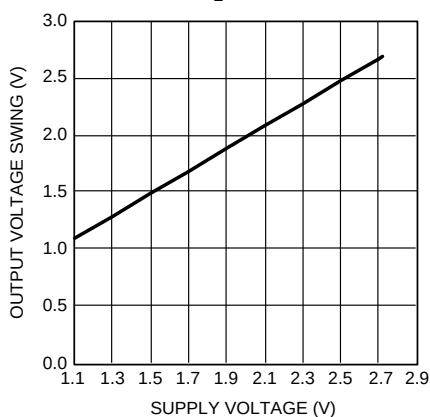


Figure 65.

Supply Current per amplifier vs Power Supply
 $R_L = 2k\Omega$, Dual Supply

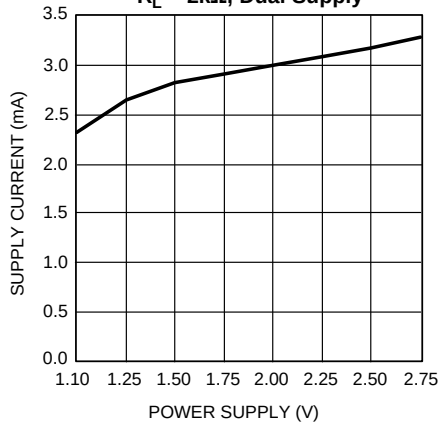


Figure 66.

Supply Current per amplifier vs Power Supply
 $R_L = 10k\Omega$, Dual Supply

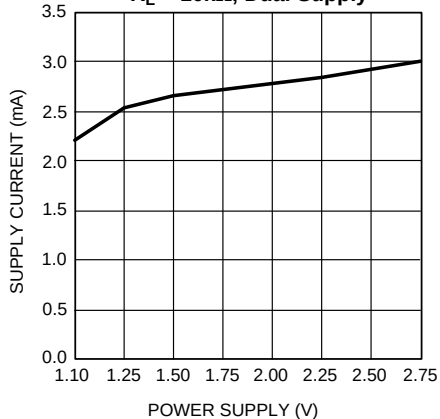


Figure 67.

Supply Current per amplifier vs Power Supply
 $R_L = 600\Omega$, Dual Supply

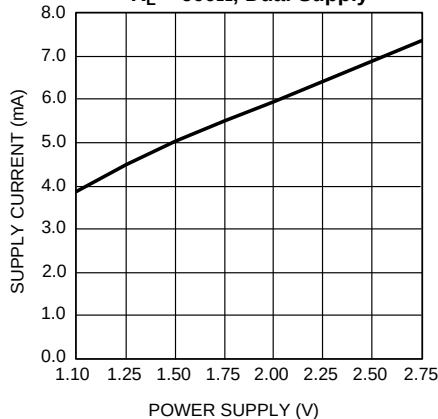


Figure 68.

APPLICATION INFORMATION

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49721 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49721's low residual is an input referred internal error. As shown in Figure 69, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 69.

This technique is verified by duplicating the measurements with high closed-loop gain and/or making the measurements at high frequencies. Doing so, produces distortion components that are within equipments capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

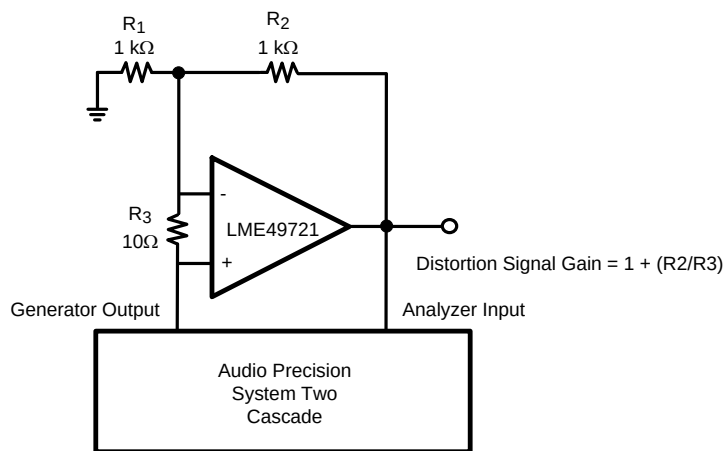


Figure 69. THD+N and IMD Distortion Test Circuit with $A_v = 2$

OPERATING RATINGS AND BASIC DESIGN GUIDELINES

The LME49721 has a supply voltage range from +2.2V to +5.5V single supply or ± 1.1 to ± 2.75 V dual supply.

Bypassed capacitors for the supplies should be placed as close to the amplifier as possible. This will help minimize any inductance between the power supply and the supply pins. In addition to a 10μF capacitor, a 0.1μF capacitor is also recommended in CMOS amplifiers.

The amplifier's inputs lead lengths should also be as short as possible. If the op amp does not have a bypass capacitor, it may oscillate.

BASIC AMPLIFIER CONFIGURATIONS

The LME49721 may be operated with either a single supply or dual supplies. Figure 70 shows the typical connection for a single supply inverting amplifier. The output voltage for a single supply amplifier will be centered around the common-mode voltage V_{cm} . Note: the voltage applied to the V_{cm} insures the output stays above ground. Typically, the V_{cm} should be equal to $V_{DD}/2$. This is done by putting a resistor divider ckt at this node, see Figure 70.

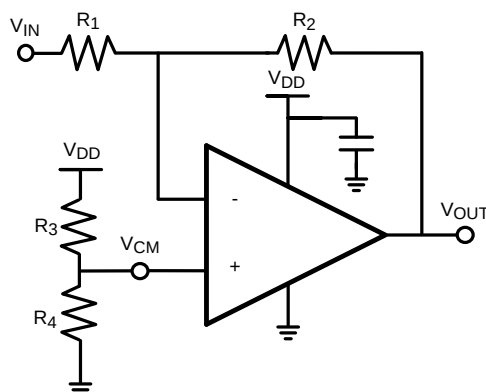
**Figure 70. Single-Supply Inverting Op Amp**

Figure 71 shows the typical connection for a dual supply inverting amplifier. The output voltage is centered on zero.

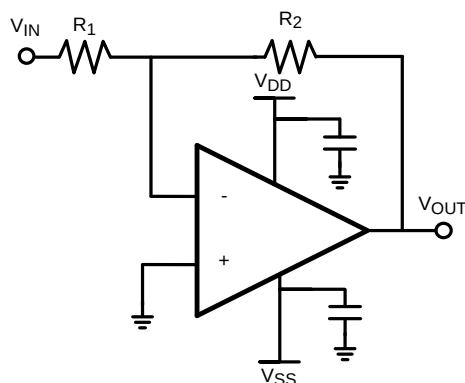
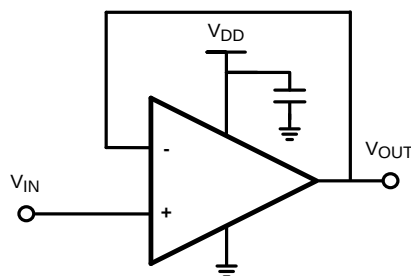
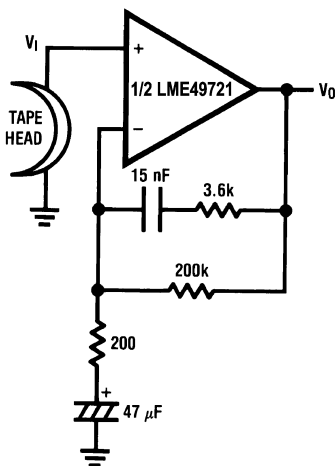
**Figure 71. Dual-Supply Inverting Op Amp**

Figure 72 shows the typical connection for the Buffer Amplifier or also called a Voltage Follower. A Buffer Amplifier can be used to solve impedance matching problems, to reduce power consumption in the source, or to drive heavy loads. The input impedance of the op amp is very high. Therefore, the input of the op amp does not load down the source. The output impedance on the other hand is very low. It allows the load to either supply or absorb energy to a circuit while a secondary voltage source dissipates energy from a circuit. The Buffer is a unity stable amplifier, $1V/V$. Although the feedback loop is tied from the output of the amplifier to the inverting input, the gain is still positive. Note: if a positive feedback is used, the amplifier will most likely drive to either rail at the output.

**Figure 72. Buffer**

TYPICAL APPLICATIONS



$A_V = 34.5$
 $F = 1 \text{ kHz}$
 $E_n = 0.38 \mu\text{V}$
 A Weighted

Figure 73. ANAB Preamp

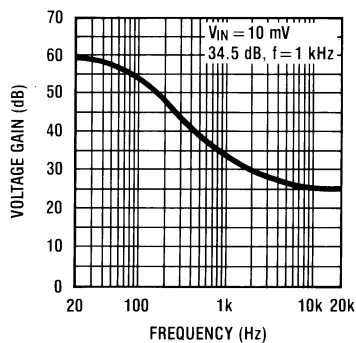
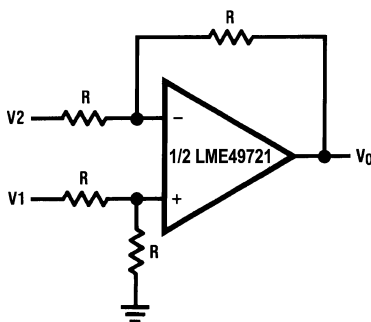
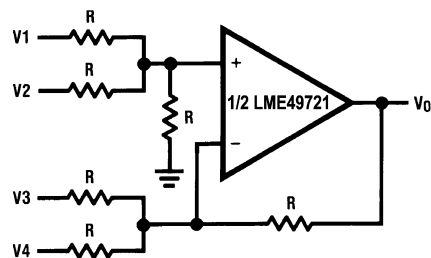


Figure 74. NAB Preamp Voltage Gain vs Frequency



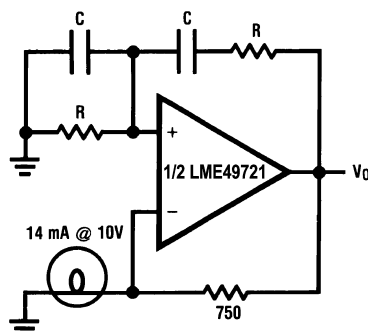
$$V_O = V1 - V2$$

Figure 75. Balanced to Single-Ended Converter



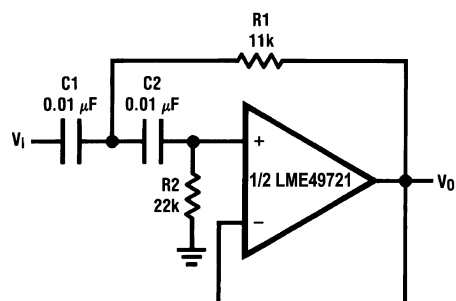
$$V_O = V_1 + V_2 - V_3 - V_4$$

Figure 76. Adder/Subtractor



$$f_o = \frac{1}{2\pi RC}$$

Figure 77. Sine Wave Oscillator



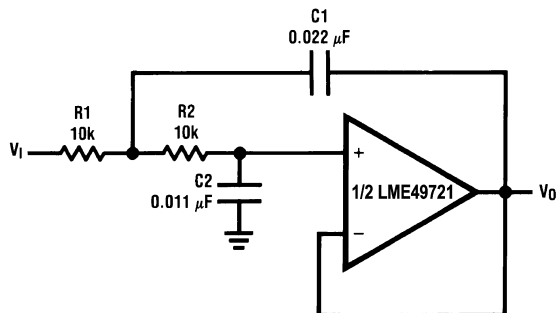
if $C_1 = C_2 = C$

$$R_1 = \frac{\sqrt{2}}{2\omega_o C}$$

$$R_2 = 2 \cdot R_1$$

Illustration is $f_o = 1 \text{ kHz}$

Figure 78. Second-Order High-Pass Filter (Butterworth)



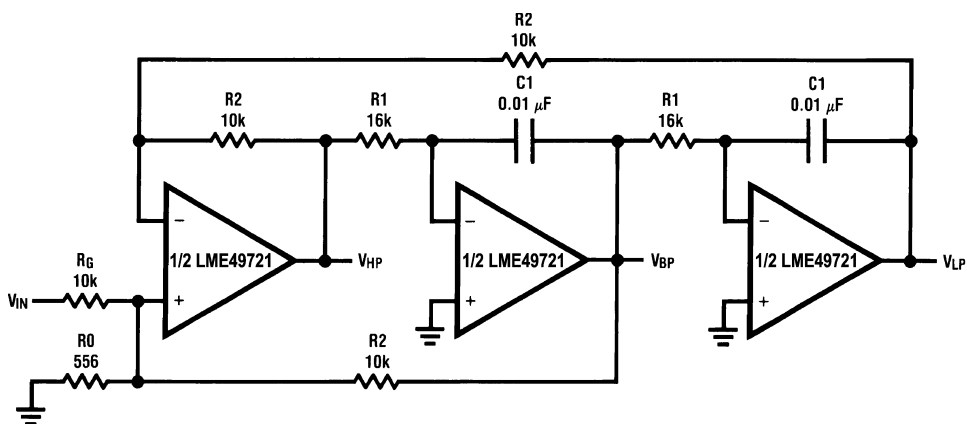
if $R1 = R2 = R$

$$C1 = \frac{\sqrt{2}}{\omega_0 R}$$

$$C2 = \frac{C1}{2}$$

Illustration is $f_0 = 1 \text{ kHz}$

Figure 79. Second-Order Low-Pass Filter (Butterworth)



$$f_0 = \frac{1}{2\pi C1 R1}, Q = \frac{1}{2} \left(1 + \frac{R2}{R0} + \frac{R2}{RG} \right), A_{BP} = Q A_{LP} = Q A_{LH} = \frac{R2}{RG}$$

Illustration is $f_0 = 1 \text{ kHz}$, $Q = 10$, $A_{BP} = 1$

Figure 80. State Variable Filter

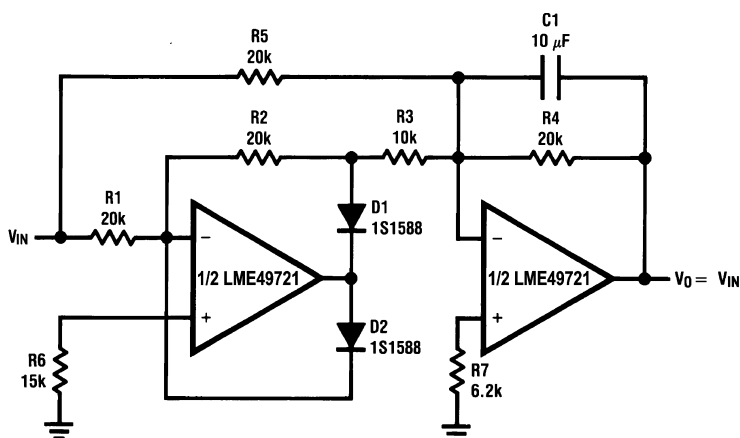


Figure 81. AC/DC Converter

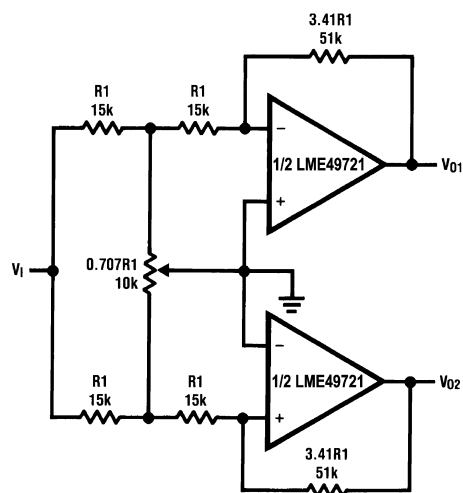


Figure 82. 2-Channel Panning Circuit (Pan Pot)

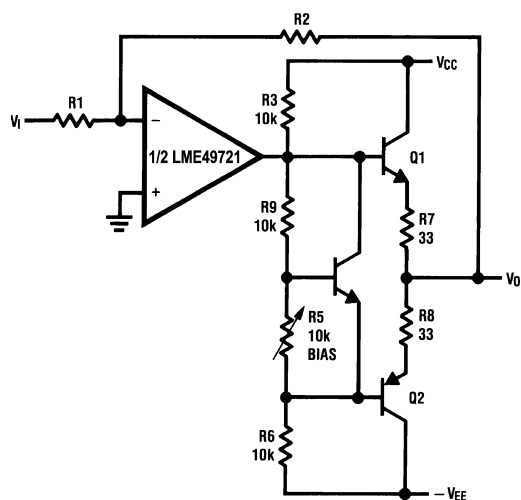
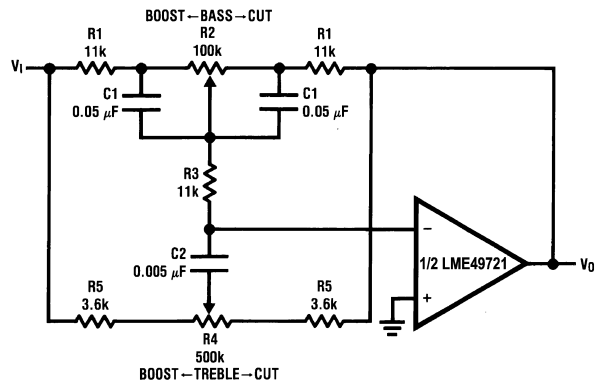


Figure 83. Line Driver



$$f_L = \frac{1}{2\pi R_2 C_1}, f_{LB} = \frac{1}{2\pi R_1 C_1}$$

$$f_H = \frac{1}{2\pi R_5 C_2}, f_{HB} = \frac{1}{2\pi (R_1 + R_5 + 2R_3) C_2}$$

Illustration is:

$$f_L = 32 \text{ Hz}, f_{LB} = 320 \text{ Hz}$$

$$f_H = 11 \text{ kHz}, f_{HB} = 1.1 \text{ kHz}$$

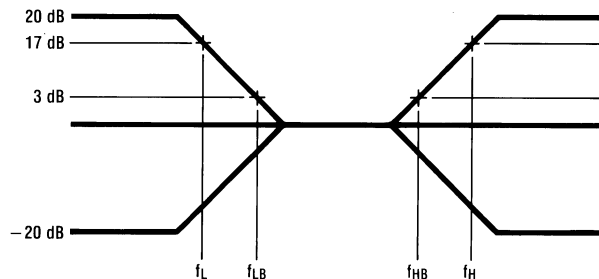
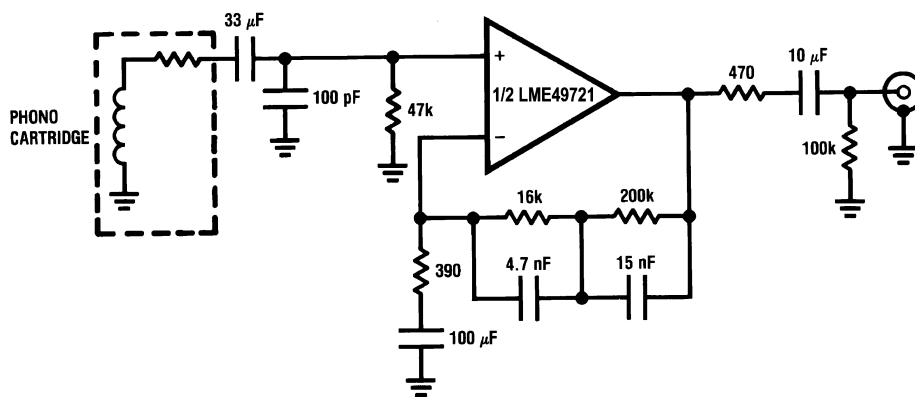
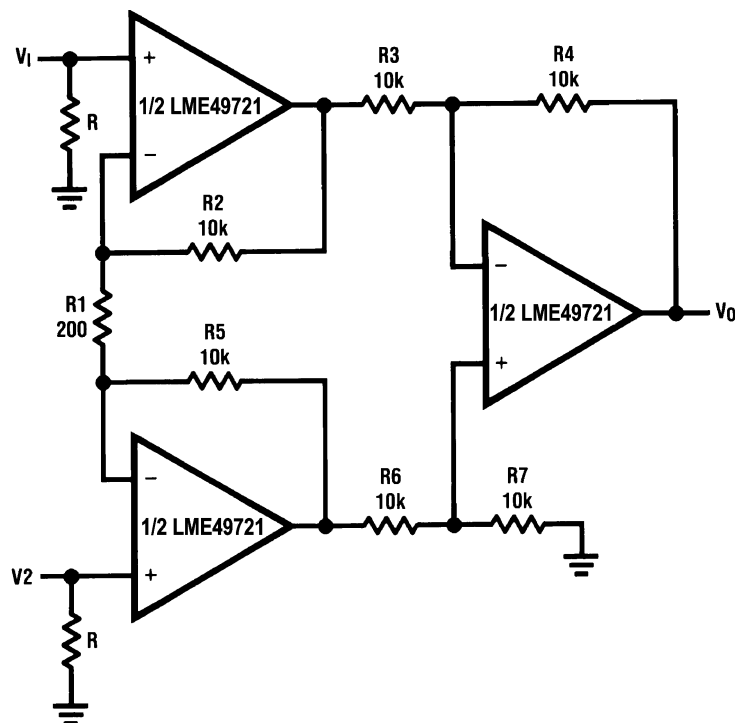


Figure 84. Tone Control



$A_v = 35 \text{ dB}$
 $E_n = 0.33 \text{ } \mu\text{V}$
 $S/N = 90 \text{ dB}$
 $f = 1 \text{ kHz}$
 A Weighted
 A Weighted, $V_{IN} = 10 \text{ mV}$
 @ $f = 1 \text{ kHz}$

Figure 85. RIAA Preamp



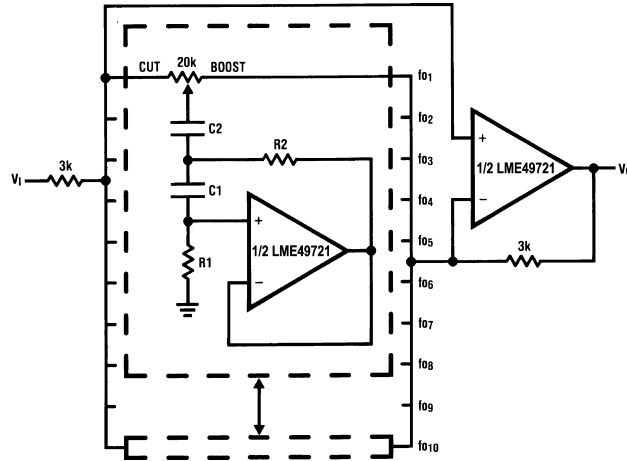
If $R2 = R5$, $R3 = R6$, $R4 = R7$

$$V_0 = \left(1 + \frac{2R2}{R1}\right) \frac{R4}{R3} (V2 - V1)$$

Illustration is:

$$V_0 = 101(V2 - V1)$$

Figure 86. Balanced Input Mic Amp



A. See [Table 1](#).

Figure 87. 10-Band Graphic Equalizer

Table 1. C_1 , C_2 , R_1 , and R_2 Values for [Figure 87](#)⁽¹⁾

fo (Hz)	C_1	C_2	R_1	R_2
32	0.12 μ F	4.7 μ F	75k Ω	500 Ω
64	0.056 μ F	3.3 μ F	68k Ω	510 Ω
125	0.033 μ F	1.5 μ F	62k Ω	510 Ω
250	0.015 μ F	0.82 μ F	68k Ω	470 Ω
500	8200pF	0.39 μ F	62k Ω	470 Ω
1k	3900pF	0.22 μ F	68k Ω	470 Ω
2k	2000pF	0.1 μ F	68k Ω	470 Ω
4k	1100pF	0.056 μ F	62k Ω	470 Ω
8k	510pF	0.022 μ F	68k Ω	510 Ω
16k	330pF	0.012 μ F	51k Ω	510 Ω

(1) At volume of change = ± 12 dB $Q = 1.7$

REVISION HISTORY

Rev	Date	Description
1.0	09/26/07	Initial release.
1.1	10/01/07	Input more info under the Buffer Amplifier.
1.2	04/21/10	Added the Ordering Information table.
C	04/04/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49721MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L49721 MA	Samples
LME49721MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L49721 MA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

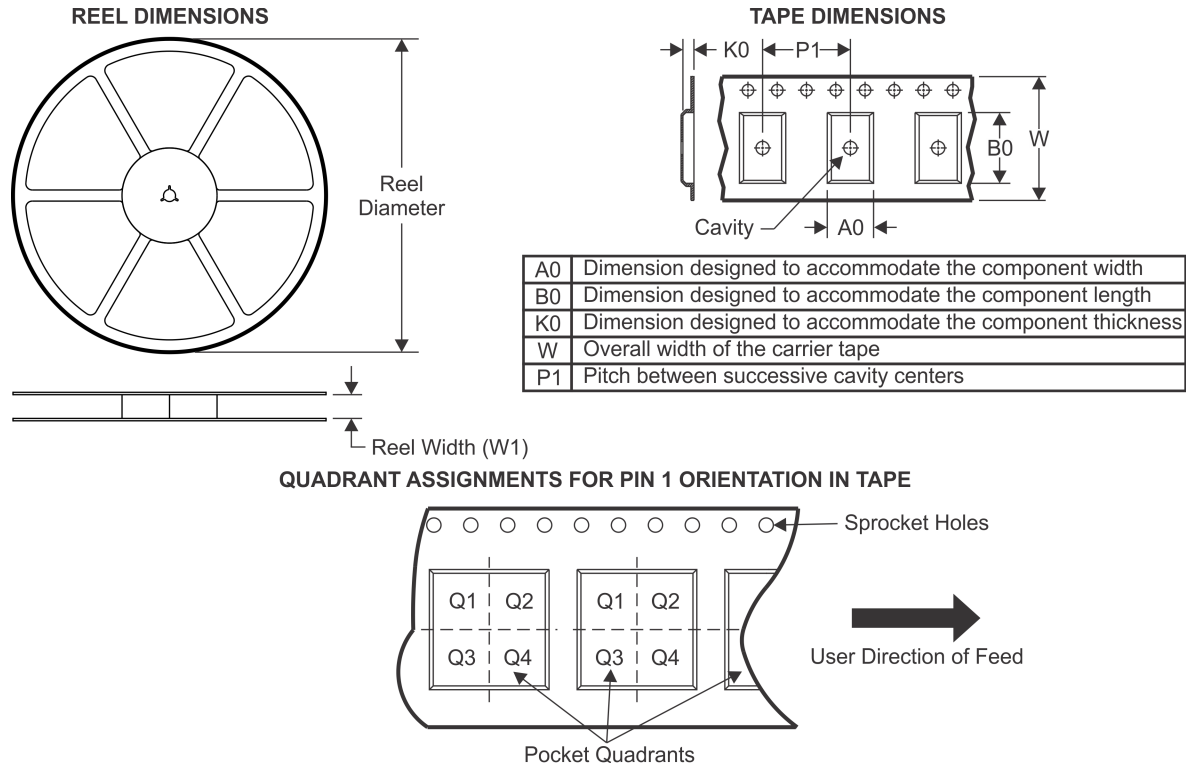
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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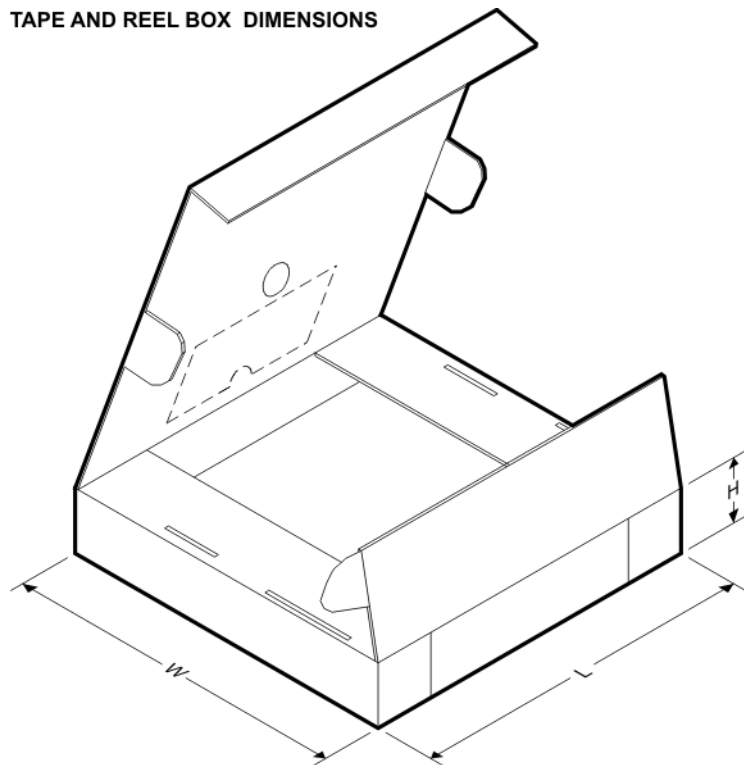
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49721MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

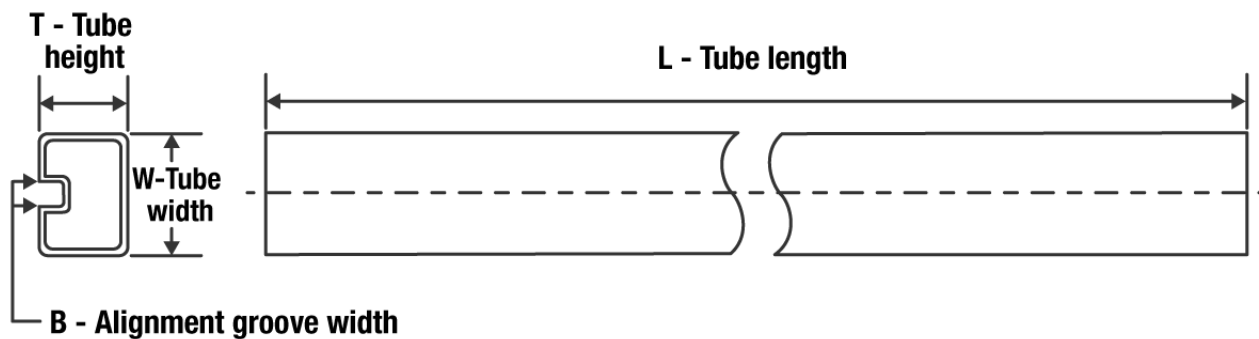
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

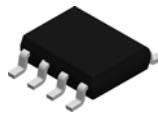
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49721MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LME49721MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

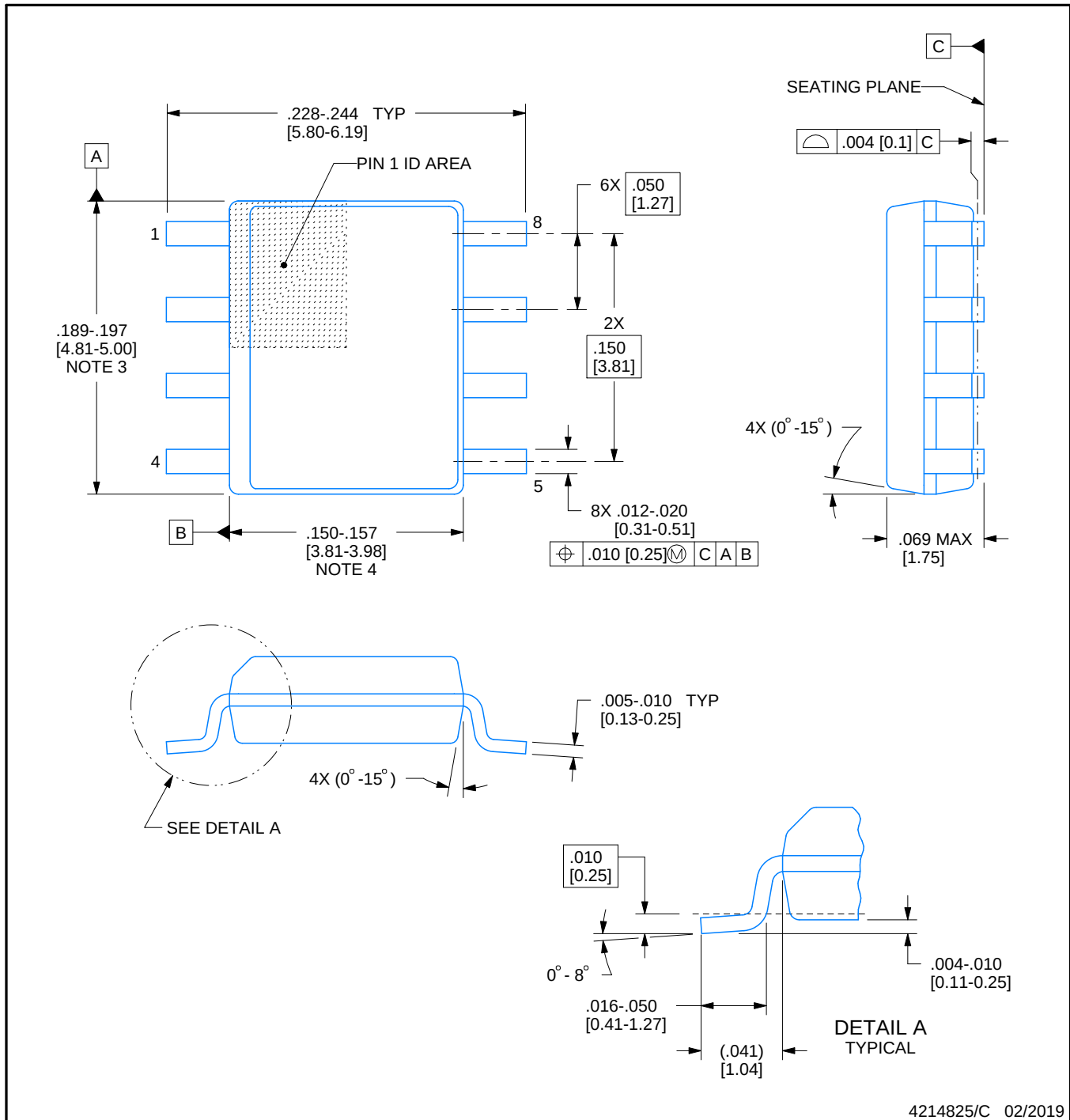


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

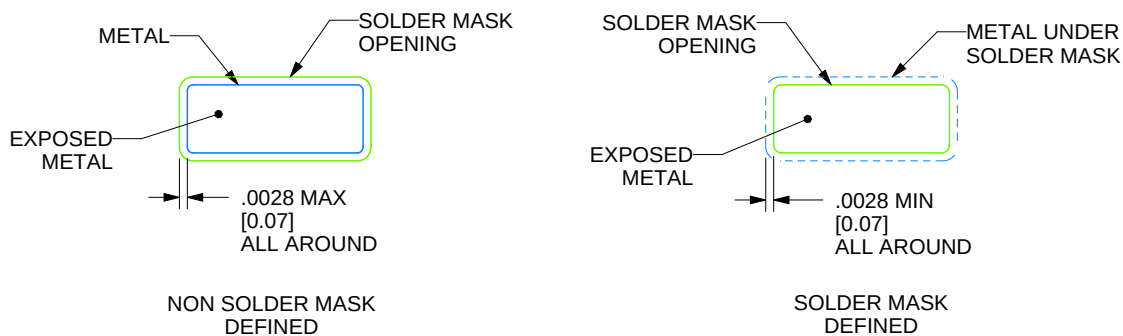
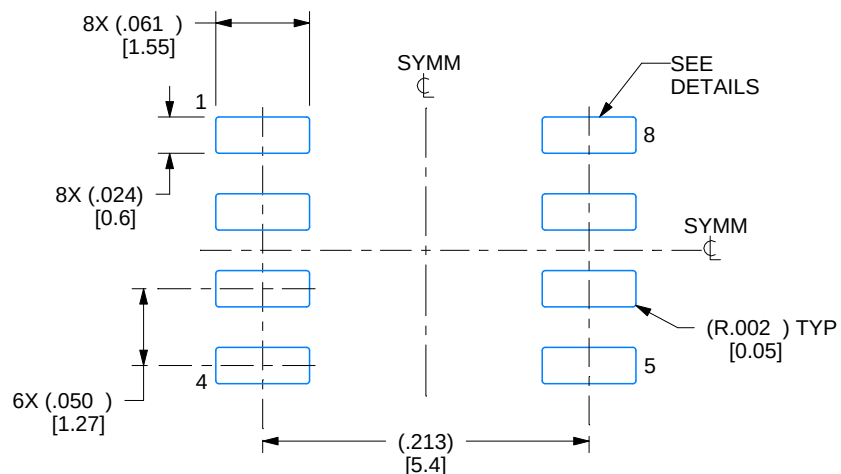
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

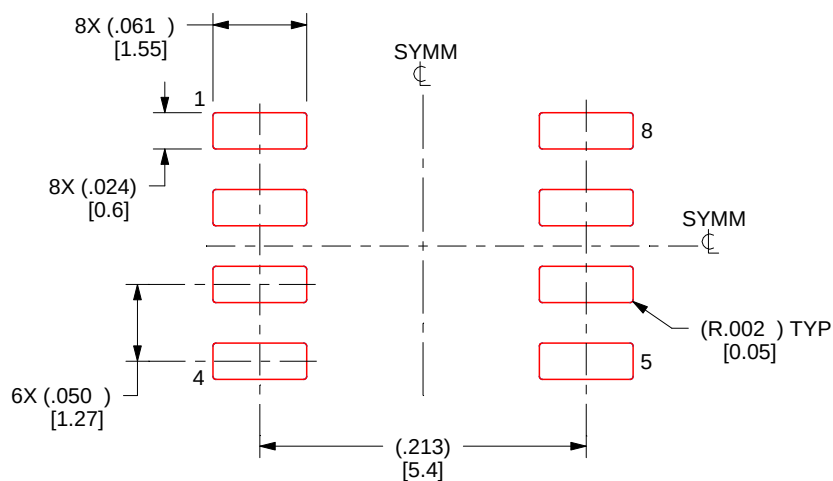
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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