



PRELIMINARY

M8751H-8

SINGLE-COMPONENT 8-BIT MICROCOMPUTER

T-49-19-59

Military

- 8 MHz Operation
- Program Memory Security
- 4K x 8 EPROM
- 128 x 8 RAM
- 32 I/O Lines (Four 8-Bit Ports)
- Two 16-Bit Timer/Counters
- Boolean Processor
- Programmable Full-Duplex Serial Channel
- 128K Accessible External Memory
- Multiply and Divide
- 256 User Bit-Addressable Locations
- Military Temperature Range:
-55°C to +125°C (T_C)

The M8751H-8 is a pin compatible EPROM version of M8051AH. Intel's advanced +5V, depletion load, N-channel, HMOS* technology allows the M8751H-8 to remain fully compatible with its M8751-8 predecessor in addition to incorporating two new features: A program memory security bit that can be used to protect the EPROM against unauthorized readout, and a programmable baud rate modification bit, which doubles the range of baud rates available to the serial port.

Specifically, the M8751H-8 features: 4K byte program memory space; 32 I/O lines; two 16-bit timer/event counters; a 5-source, 2-level interrupt structure; a full duplex serial channel; a Boolean processor; and on-chip oscillator and clock circuitry. Standard TTL and most byte-oriented MCS®-80 and MCS-85 peripherals can be used for I/O and memory expansion.

The M8751H-8 is available in a hermetically sealed, ceramic, 40-lead dual in-line package which includes a window that allows for EPROM erasure when exposed to ultraviolet light (see Erasure Characteristics). During normal operation, ambient light may adversely affect the functionality of the chip. Therefore, applications which expose the M8751H-8 to ambient light may require an opaque label over the window.

*HMOS is a patented process of Intel Corporation.

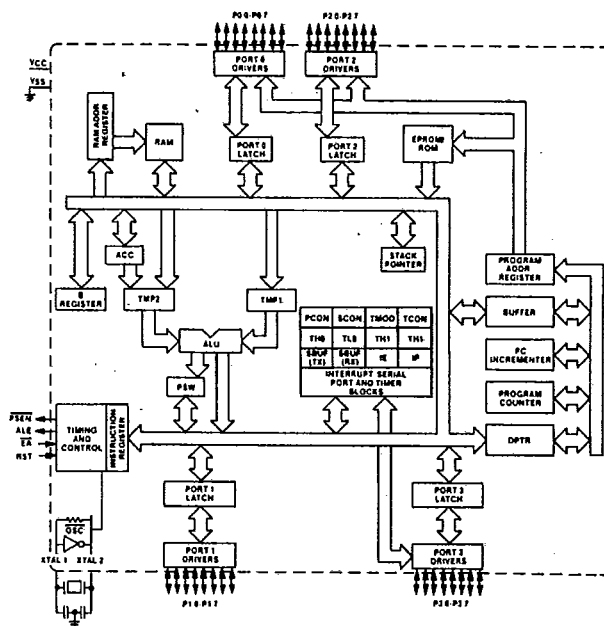


Figure 1. Block Diagram

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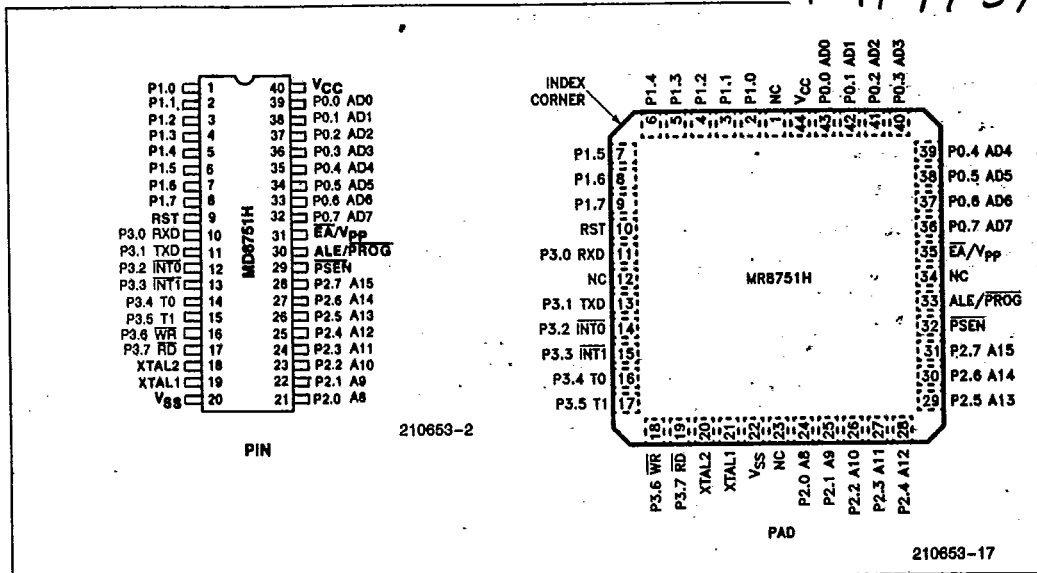


Figure 2. Pin Configurations

M8751H PIN DESCRIPTIONS

V_{SS}

Circuit ground potential.

V_{CC}

Supply voltage during programming, verification, and normal operation.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory. It also receives the instruction bytes during EPROM programming, and outputs instruction bytes during program verification. (External pullups are required during program verification.) Port 0 can sink (and in bus operations can source) eight LS TTL inputs.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the low-order address byte during EPROM programming and program verification. Port 1 can sink/source four LS TTL inputs.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. It emits the high-order address byte during accesses to external memory. It also receives the high-order address bits during EPROM programming and program verification. Port 2 can sink/source four LS TTL inputs.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt)
P3.3	INT1 (external interrupt)
P3.4	T0 (Timer/counter 0 external input)
P3.5	T1 (Timer/counter 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Port 3 can sink/source four LS TTL inputs.



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RST

A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor ($\approx 8.2 \text{ K}\Omega$) from RST to V_{SS} permits power-on reset when a capacitor ($\approx 10 \mu\text{f}$) is also connected from this pin to V_{CC} .

ALE/PROG

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated at a constant rate of $1/6$ the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. This pin is also the program pulse input (PROG) during EPROM programming.

PSEN

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, even when executing out of external Program Memory two activations of PSEN are skipped during each access to external data memory.)

 $\overline{\text{EA}}/\text{VPP}$

External Access enable. $\overline{\text{EA}}$ must be externally held low in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. Note, however, that if the Security Bit is programmed, the device will not fetch code from any location in external Program Memory.

This pin also receives the 21V programming supply voltage (V_{PP}) during EPROM programming.

XTAL1

Input to the inverting oscillator amplifier.

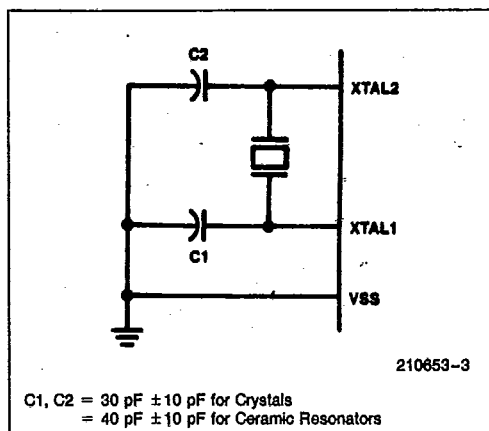
XTAL2

Output from the inverting oscillator amplifier.

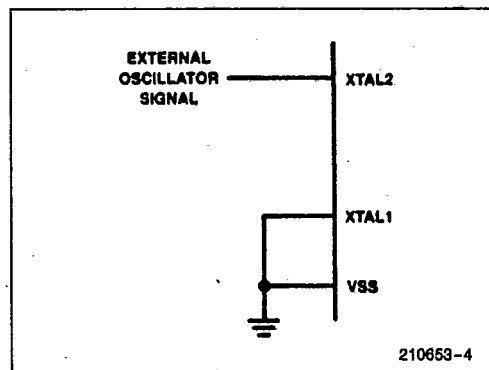
OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers", published in the Embedded Controller Handbook.

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven,

**Figure 3. Oscillator Connections**

as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

**Figure 4. External Drive Configuration**

Datum	Emittng Ports	Degraded I/O Lines	VOL (Peak) (Max)
Address	P2, P0	P1, P3	0.8V
Write Data	P0	P1, P3, ALE	0.8V



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ABSOLUTE MAXIMUM RATINGS*

Case Temperature	
Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin to V_{SS}	
(Except V_{PP})	-0.5V to +7V
Voltage from V_{PP} to V_{SS}	21.5V
Power Dissipation	2W

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	-55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Unit	Comments
V_{IL}	Input Low Voltage	-0.5	0.7	V	
V_{IL1}	Input Low Voltage to $\overline{EA}$	0	0.7	V	
V_{IH}	Input High Voltage (Except XTAL2, RST)	2.2	$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage to XTAL2, RST	2.5	$V_{CC} + 0.5$	V	XTAL1 = V_{SS}
V_{OL}	Output Low Voltage Ports 1, 2, 3 (Note 1)		0.45	V	$I_{OL} = 1.2 \text{ mA}$
V_{OL1}	Output Low Voltage Port 0, ALE, $\overline{PSEN}$ (Note 1)		0.60 0.45	V V	$I_{OL} = 2.8 \text{ mA}$ $I_{OL} = 2.4 \text{ mA}$
V_{OH}	Output High Voltage Ports 1, 2, 3	2.4		V	$I_{OH} = -60 \mu\text{A}$
V_{OH1}	Output High Voltage Port 0 (in External Bus Mode), ALE, $\overline{PSEN}$	2.4		V	$I_{OH} = -300 \mu\text{A}$
I_{IL}	Logical 0 Input Current P1, P2, P3		-500	μA	$V_{IN} = 0.45\text{V}$
I_{IL1}	Logical 0 Input Current to $\overline{EA}/V_{PP}$		-15	mA	$V_{IN} = 0.45\text{V}$
I_{IL2}	Logical 0 Input Current to XTAL2		-4.5	mA	XTAL1 = V_{SS} , $V_{IN} = 0.45\text{V}$
I_{LI}	Input Leakage Current to Port 0		± 125	μA	$0.45\text{V} < V_{IN} < V_{CC}$
I_{IH}	Logical Input Current to $\overline{EA}/V_{PP}$		500	μA	$V_{IN} = 2.4\text{V}$
I_{IH1}	Input Current to RST/ V_{PD} to Activate Reset		500	μA	$V_{IN} < (V_{CC} - 1.5\text{V})$
I_{CC}	Power Supply Current		275	mA	All Outputs Disconnected, $\overline{EA} = V_{CC}$
C_{IO}	Capacitance of I/O Buffers		10	pF	$f_c = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.



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A.C. CHARACTERISTICS (Over Specified Operating Conditions), Load Capacitance for Port 0, ALE, and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for all other outputs = 80 pF

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	8 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	8	MHz
TLHLL	ALE Pulse Width	195		2TCLCL-55		ns
TAVLL	Address Valid to ALE	70		TCLCL-55		ns
TLLAX	Address Hold after ALE	75		TCLCL-50		ns
TLLIV	ALE to Valid Instr In		335		4TCLCL-165	ns
TLLPL	ALE to $\overline{\text{PSEN}}$	85		TCLCL-40		ns
TPLPH	$\overline{\text{PSEN}}$ Pulse Width	300		3TCLCL-75		ns
TPLIV	$\overline{\text{PSEN}}$ to Valid Instr In		210		3TCLCL-165	ns
TPXIX	Input Instr Hold after $\overline{\text{PSEN}}$	0		0		ns
TPXIZ	Input Instr Float after $\overline{\text{PSEN}}$		90		TCLCL-35	ns
TPXAV	$\overline{\text{PSEN}}$ to Address Valid	100		TCLCL-25		ns
TAVIV	Address to Valid Instr In		460		5TCLCL-165	ns
TPLAZ	$\overline{\text{PSEN}}$ Low to Address Float		20		20	ns

EXTERNAL DATA MEMORY CHARACTERISTICS

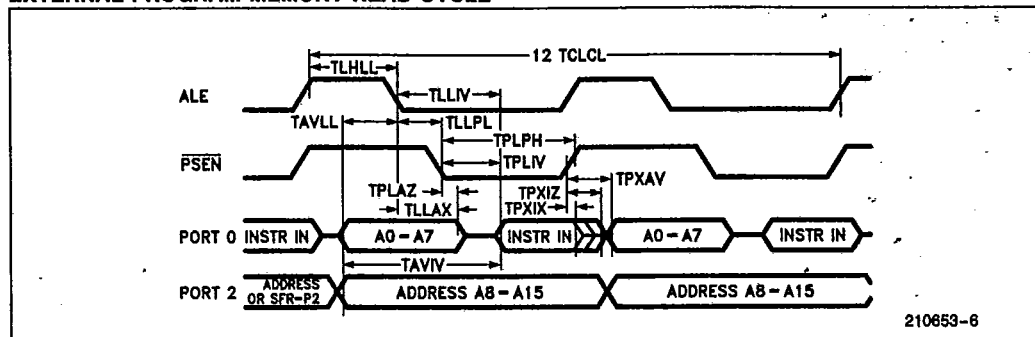
Symbol	Parameter	8 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
TRLRH	$\overline{\text{RD}}$ Pulse Width	650		6TCLCL-100		ns
TWLWH	$\overline{\text{WR}}$ Pulse Width	650		6TCLCL-100		ns
TLLAX	Address Hold after ALE	75		TCLCL-50		ns
TRLDV	$\overline{\text{RD}}$ to Valid Data In		440		5TCLCL-185	ns
TRHDX	Data Hold after $\overline{\text{RD}}$	0		0		ns
TRHDZ	Data Float after $\overline{\text{RD}}$		165		2TCLCL-85	ns
TLLDV	ALE to Valid Data In		830		8TCLCL-170	ns
TAVDV	Address to Valid Data In		940		9TCLCL-185	ns
TLLWL	ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	310	440	3TCLCL-65	3TCLCL+65	ns
TAVWL	Address to $\overline{\text{WR}}$ or $\overline{\text{RD}}$	355		4TCLCL-145		ns
TQVWX	Data Valid to $\overline{\text{WR}}$ Transition	40		TCLCL-85		ns
TQVWH	Data Setup to $\overline{\text{WR}}$ High	800		7TCLCL-75		ns
TWHQX	Data Held after $\overline{\text{WR}}$	60		TCLCL-65		ns
TRLAZ	$\overline{\text{RD}}$ Low to Address Float		20		20	ns
TWHLH	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	60	190	TCLCL-65	TCLCL+65	ns



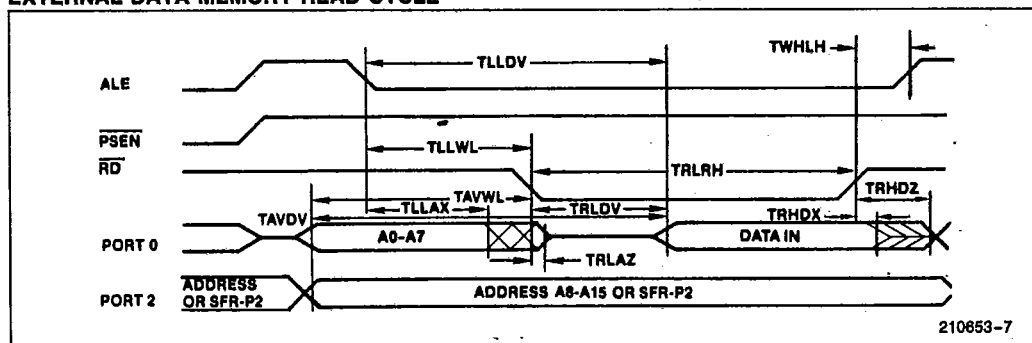
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A.C. TIMING DIAGRAMS

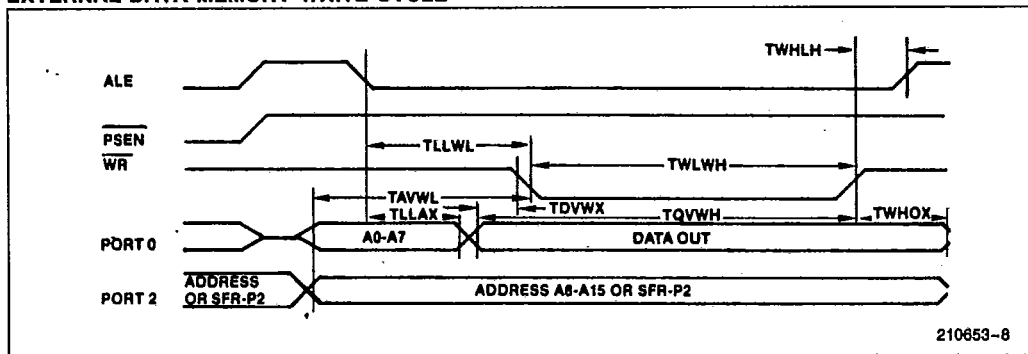
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



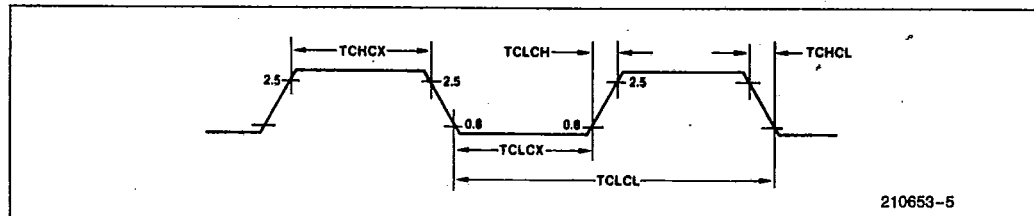
EXTERNAL DATA MEMORY WRITE CYCLE



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EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL2)

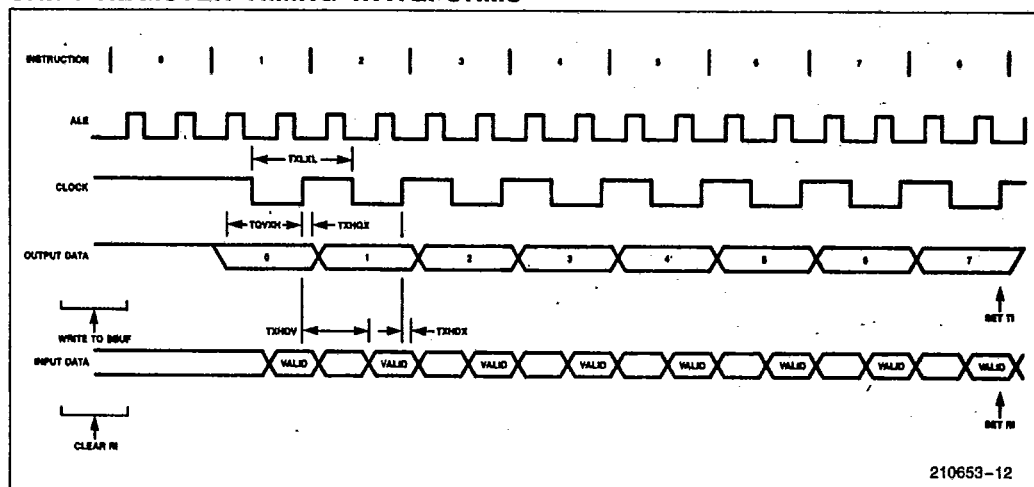
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	8	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns



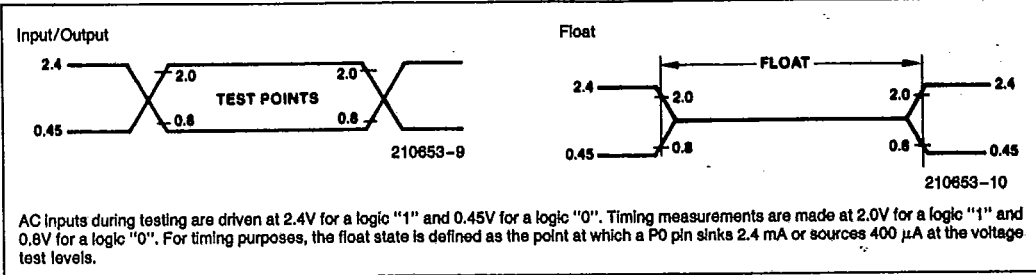
SERIAL PORT TIMING—SHIFT REGISTER MODE Load Capacitance = 80 pF

Symbol	Parameter	8 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μ s
TQVXH	Output Data Setup to Clock Rising Edge	1117		10TCLCL-133		ns
TXHQX	Output Data Hold after Clock Rising Edge	133		2TCLCL-117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		1117		10TCLCL-133	ns

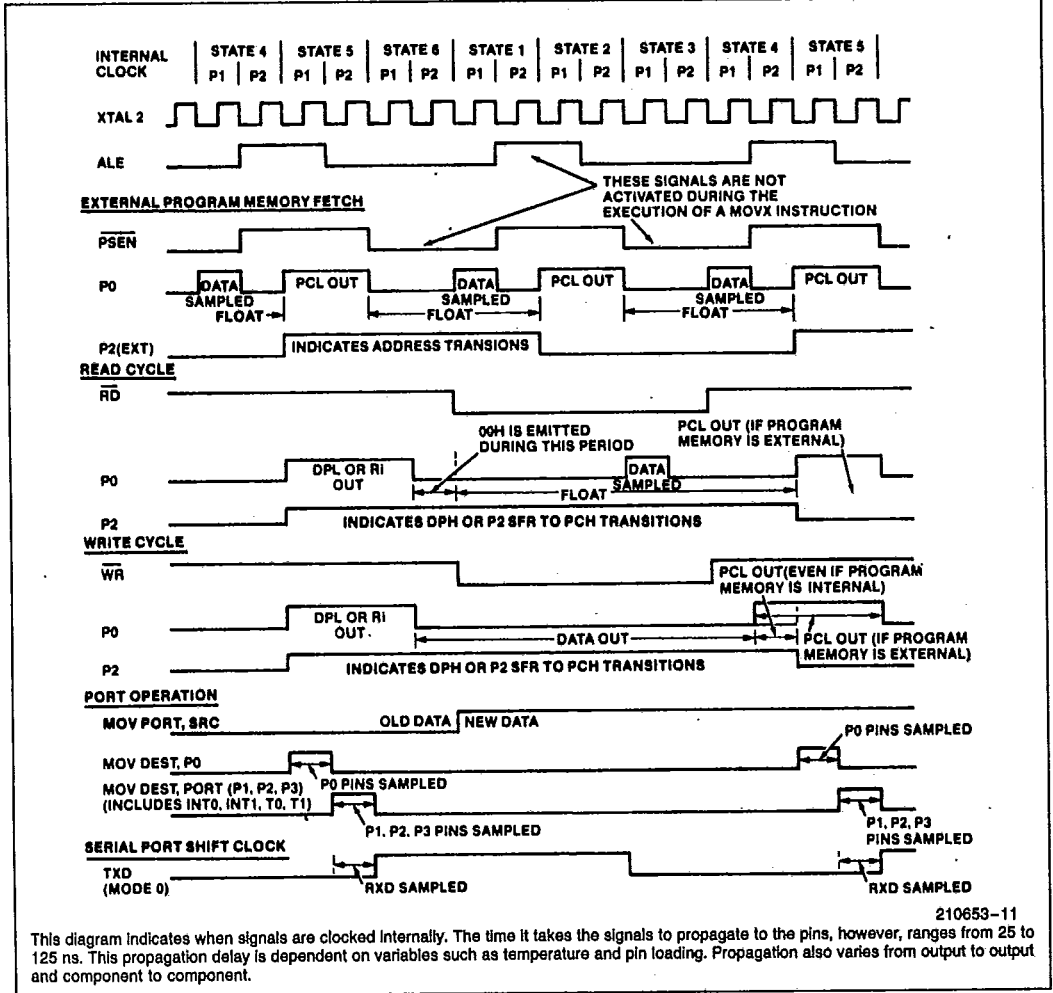
SHIFT REGISTER TIMING WAVEFORMS



A.C. TESTING INPUT/OUTPUT, FLOAT WAVEFORMS



CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component.



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EPROM CHARACTERISTICS

Table 1. EPROM Programming Modes

Mode	RST	PSEN	ALE	$\overline{EA}$	P2.7	P2.6	P2.5	P2.4
Program	1	0	0*	V_{PP}	1	0	X	X
Inhibit	1	0	1	X	1	0	X	X
Verify	1	0	1	1	0	0	X	X
Security Set	1	0	0*	V_{PP}	1	1	X	X

NOTES:

"1" = logic high for that pin

"0" = logic low for that pin

"X" = "don't care"

" V_{PP} " = +21V $\pm$ 0.5V

*ALE is pulsed low for 50 ms.

Programming the EPROM

To be programmed, the part must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate internal registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0–P2.3 of Port 2, while the code byte to be programmed into that location is applied to Port 0. The other Port 2 pins, and RST, PSEN, and $\overline{EA}$ should be held at the "Program" levels indicated in Table 1. ALE is pulsed low for 50 ms to program the code byte into the addressed EPROM location. The setup is shown in Figure 5.

Normally $\overline{EA}$ is held at a logic high until just before ALE is to be pulsed. Then $\overline{EA}$ is raised to +21V,

ALE is pulsed, and then $\overline{EA}$ is returned to a logic high. Waveforms and detailed timing specifications are shown in later sections of this data sheet.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level of 21.5V for any amount of time. Even a narrow glitch above that voltage level can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches.

Program Verification

If the Security Bit has not been programmed, the on-chip Program Memory can be read out for verification purposes, if desired, either during or after the

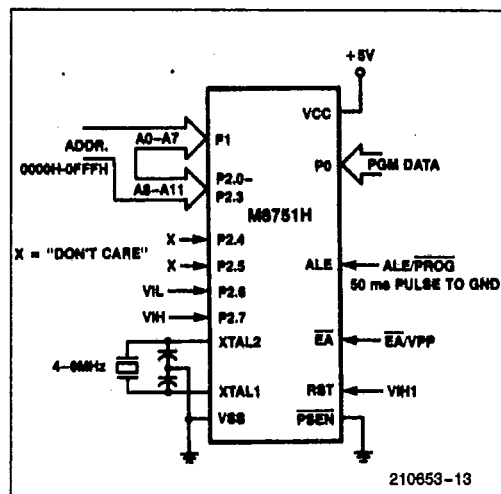


Figure 5. Programming Configuration

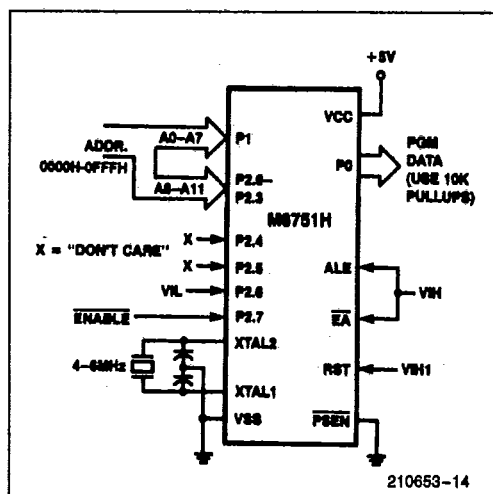


Figure 6. Program Verification

programming operation. The address of the Program Memory location to be read is applied to Port 1 and pins P2.0–P2.3. The other pins should be held at the "Verify" levels indicated in Table 1. The contents of the addressed location will come out on Port 0. External pullups are required on Port 0 for this operation.

The setup, which is shown in Figure 6, is the same as for programming the EPROM except that pin P2.7 is held at a logic low, or may be used as an active-low read strobe.

EPROM Security

The security feature consists of a "locking" bit which when programmed denies electrical access by any external means to the on-chip Program Memory. The bit is programmed as shown in Figure 7. The setup and procedure are the same as for normal EPROM programming, except that P2.6 is held at a logic high. Port 0, Port 1, and pins P2.0–P2.3 may be in any state. The other pins should be held at the "Security" levels indicated in Table 1.

Once the Security Bit has been programmed, it can be cleared only by full erasure of the Program Mem-

ory. While it is programmed, the internal Program Memory cannot be read out, the device cannot be further programmed, and it cannot execute out of external program memory. Erasing the EPROM, thus clearing the Security Bit, restores the device's full functionality. It can then be reprogrammed.

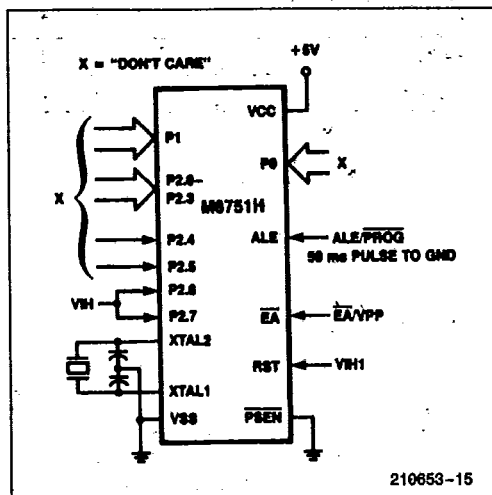


Figure 7. Programming the Security Bit

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	20.5	21.5	V
I_{PP}	Programming Supply Current		30	mA
$1/TCLCL$	Oscillator Frequency	4	6	MHz
$\cdot TAVGL$	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		μs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		μs
TGLGH	$\overline{PROG}$ Width	45	55	ms
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float after $\overline{ENABLE}$	0	48TCLCL	

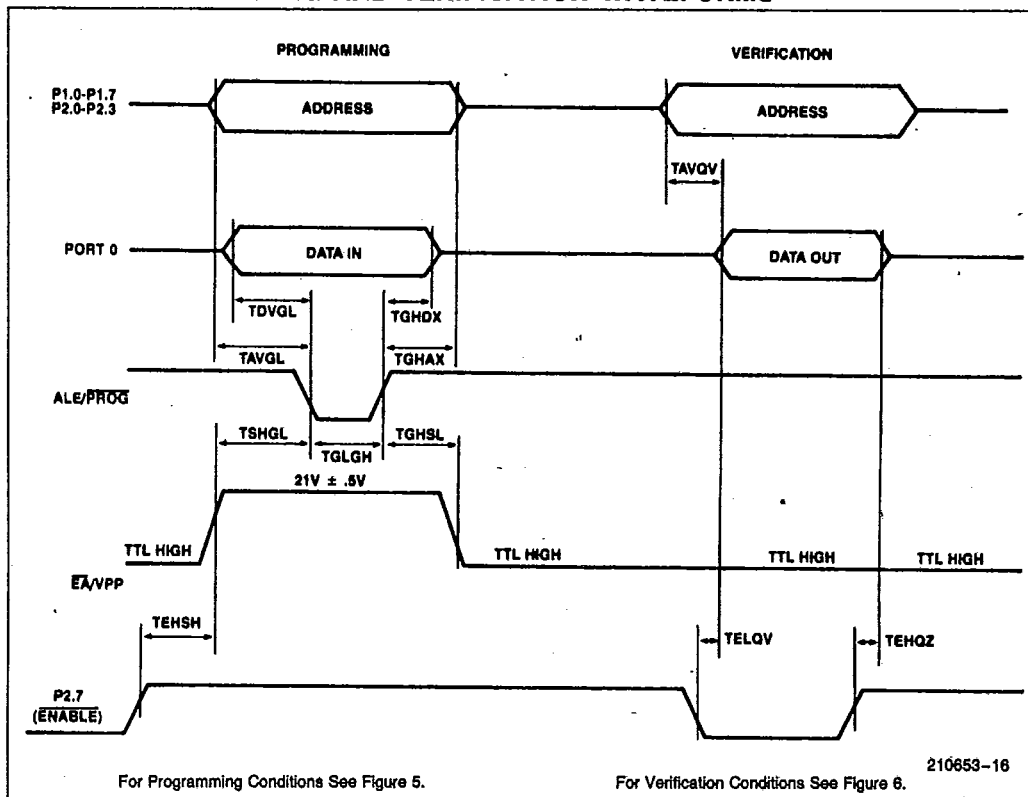
Erase Characteristics

Erase of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000 μ W/cm² rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

Erase leaves the array in an all 1s state.

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS





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Table 1. MCS-51 Instruction Set Description

ARITHMETIC OPERATIONS				LOGICAL OPERATIONS (Continued)			
Mnemonic	Description	Byte	Cyc	Mnemonic	Description	Byte	Cyc
ADD A,Rn	Add register to Accumulator	1	1	ORL A,@Ri	OR indirect RAM to Accumulator	1	1
ADD A,direct	Add direct byte to Accumulator	2	1	ORL A,#data	OR immediate data to Accumulator	2	1
ADD A,@Ri	Add indirect RAM to Accumulator	1	1	ORL direct,A	OR Accumulator to direct byte	2	1
ADD A,#data	Add immediate data to Accumulator	2	1	ORL direct,#data	OR immediate data to direct byte	3	2
ADDC A,Rn	Add register to Accumulator with Carry	1	1	XRL A,Rn	Exclusive-OR register to Accumulator	1	1
ADDC A,direct	Add direct byte to A with Carry flag	2	1	XRL A,direct	Exclusive-OR direct byte to Accumulator	2	1
ADDC A,@Ri	Add indirect RAM to A with Carry flag	1	1	XRL A,@Ri	Exclusive-OR indirect RAM to A	1	1
ADDC A,#data	Add immediate data to A with Carry flag	2	1	XRL A,#data	Exclusive-OR immediate data to A	2	1
SUBB A,Rn	Subtract register from A with Borrow	1	1	XRL direct,A	Exclusive-OR Accumulator to direct byte	2	1
SUBB A,direct	Subtract direct byte from A with Borrow	2	1	XRL direct,#data	Exclusive-OR immediate data to direct	3	2
SUBB A,@Ri	Subtract indirect RAM from A with Borrow	1	1	CLR A	Clear Accumulator	1	1
SUBB A,#data	Subtract immed data from A with Borrow	2	1	CPL A	Complement Accumulator	1	1
INC A	Increment Accumulator	1	1	RL A	Rotate Accumulator Left	1	1
INC Rn	Increment register	1	1	RLC A	Rotate A Left through the Carry flag	1	1
INC direct	Increment direct byte	2	1	RR A	Rotate Accumulator Right	1	1
INC @Ri	Increment indirect RAM	1	1	RRC A	Rotate A Right through Carry flag	1	1
INC DPTR	Increment Data Pointer	1	2	SWAP A	Swap nibbles within the Accumulator	1	1
DEC A	Decrement Accumulator	1	1	DATA TRANSFER			
DEC Rn	Decrement register	1	1	Mnemonic	Description	Byte	Cyc
DEC direct	Decrement direct byte	2	1	MOV A,Rn	Move register to Accumulator	1	1
DEC @Ri	Decrement indirect RAM	1	1	MOV A,direct	Move direct byte to Accumulator	2	1
MUL AB	Multiply A & B	1	4	MOV A,@Ri	Move indirect RAM to Accumulator	1	1
DIV AB	Divide A by B	1	4	MOV A,#data	Move immediate data to Accumulator	2	1
DA A	Decimal Adjust Accumulator	1	1	MOV Rn,A	Move Accumulator to register	1	1
LOGICAL OPERATIONS				MOV Rn,direct	Move direct byte to register	2	2
Mnemonic	Destination	Byte	Cyc	MOV Rn,#data	Move immediate data to register	2	1
ANL A,Rn	AND register to Accumulator	1	1	MOV direct,A	Move Accumulator to direct byte	2	1
ANL A,direct	AND direct byte to Accumulator	2	1	MOV direct,Rn	Move register to direct byte	2	2
ANL A,@Ri	AND indirect RAM to Accumulator	1	1	MOV direct,direct	Move direct byte to direct	3	2
ANL A,#data	AND immediate data to Accumulator	2	1	MOV direct,@Ri	Move indirect RAM to direct byte	2	2
ANL direct,A	AND Accumulator to direct byte	2	1				
ANL direct,#data	AND immediate data to direct byte	3	2				
ORL A,Rn	OR register to Accumulator	1	1				
ORL A,direct	OR direct byte to Accumulator	2	1				



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Table 1. MCS®-51 Instruction Set Description (Continued)

DATA TRANSFER (Continued)				PROGRAM AND MACHINE CONTROL			
Mnemonic	Description	Byte	Cyc	Mnemonic	Description	Byte	Cyc
MOV direct, #data	Move immediate data to direct byte	3	2	ACALL addr11	Absolute Subroutine Call	2	2
MOV @Ri,A	Move Accumulator to indirect RAM	1	1	LCALL addr16	Long Subroutine Call	3	2
MOV @Ri,direct	Move direct byte to indirect RAM	2	2	RET	Return from subroutine	1	2
MOV @Ri, #data	Move immediate data to indirect RAM	2	1	RETI	Return from interrupt	1	2
MOV DPTR, #data16	Load Data Pointer with a 16-bit constant	3	2	AJMP addr11	Absolute Jump	2	2
MOVC A,@A+DPTR	Move Code byte relative to DPTR to A	1	2	LJMP addr16	Long Jump	3	2
MOVC A,@A+PC	Move Code byte relative to PC to A	1	2	SJMP rel	Short Jump (relative addr)	2	2
MOVX A,@Ri	Move External RAM (8-bit addr) to A	1	2	JMP @A+DPTR	Jump indirect relative to the DPTR	1	2
MOVX A,@DPTR	Move External RAM (16-bit addr) to A	1	2	JZ rel	Jump if Accumulator is Zero	2	2
MOVX @Ri,A	Move A to External RAM (8-bit addr)	1	2	JNZ rel	Jump if Accumulator is Not Zero	2	2
MOVX @DPTR,A	Move A to External RAM (16-bit addr)	1	2	JC rel	Jump if Carry flag is set	2	2
PUSH direct	Push direct byte onto stack	2	2	JNC rel	Jump if No Carry flag	2	2
POP direct	Pop direct byte from stack	2	2	JB bit,rel	Jump if direct Bit set	3	2
XCH A,Rn	Exchange register with Accumulator	1	1	JNB bit,rel	Jump if direct Bit Not set	3	2
XCH A,direct	Exchange direct byte with Accumulator	2	1	JBC bit,rel	Jump if direct Bit is set & Clear bit	3	2
XCH A,@Ri	Exchange indirect RAM with A	1	1	CJNE A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
XCHD A,@Ri	Exchange low-order Digit ind RAM w A	1	1	CJNE A, #data,rel	Comp, immed, to A & Jump if Not Equal	3	2
BOOLEAN VARIABLE MANIPULATION				CJNE Rn, #data,rel	Comp, immed, to reg & Jump if Not Equal	3	2
Mnemonic	Description	Byte	Cyc	CJNE @Ri, #data,rel	Comp, immed, to ind, & Jump if Not Equal	3	2
CLR C	Clear Carry Flag	1	1	DJNZ Rn,rel	Decrement register & Jump if Not Zero	2	2
CLR bit	Clear direct bit	2	1	DJNZ direct,rel	Decrement direct & Jump if Not Zero	3	2
SETB C	Set Carry flag	1	1	NOP	No operation	1	1
SETB bit	Set direct bit	2	1	NOTES ON DATA ADDRESSING MODES			
CPL C	Complement Carry flag	1	1	Rn	— Working register R0–R7		
CPL bit	Complement direct bit	2	1	direct	— 128 internal RAM locations, any I/O port, control or status register		
ANL C,bit	AND direct bit to Carry flag	2	2	@Ri	— Indirect internal RAM location addressed by register R0 or R1		
ANL C,/bit	AND complement of direct bit to Carry flag	2	2	#data	— 8-bit constant included in instruction		
ORL C,bit	OR direct bit to Carry flag	2	2	#data16	— 16-bit constant included as bytes 2 & 3 of instruction		
ORL C,/bit	OR complement of direct bit to Carry flag	2	2	bit	— 128 software flags, any I/O pin, control or status bit		
MOV C,/bit	Move direct bit to Carry flag	2	1	NOTES ON PROGRAM ADDRESSING MODES			
MOV bit,C	Move Carry flag to direct bit	2	2	addr16	— Destination address for LCALL & LJMP may be anywhere within the 64-K program memory address space		
				addr11	— Destination address for ACALL & AJMP will be within the same 2-K page of program memory as the first byte of the following instruction		
				rel	— SJMP and all conditional jumps include an 8-bit offset byte, Range is +127–128 bytes relative to first byte of the following instruction		
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Table 2. Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands	Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP		33	1	RLC	A
01	2	AJMP	code addr	34	2	ADDC	A, #data
02	3	LJMP	code addr	35	2	ADDC	A, data addr
03	1	RR	A	36	1	ADDC	A, @R0
04	1	INC	A	37	1	ADDC	A, @R1
05	2	INC	data addr	38	1	ADDC	A, R0
06	1	INC	@R0	39	1	ADDC	A, R1
07	1	INC	@R1	3A	1	ADDC	A, R2
08	1	INC	R0	3B	1	ADDC	A, R3
09	1	INC	R1	3C	1	ADDC	A, R4
0A	1	INC	R2	3D	1	ADDC	A, R5
0B	1	INC	R3	3E	1	ADDC	A, R6
0C	1	INC	R4	3F	1	ADDC	A, R7
0D	1	INC	R5	40	2	JC	code addr
0E	1	INC	R6	41	2	AJMP	code addr
0F	1	INC	R7	42	2	ORL	data addr, A
10	3	JBC	bit addr, code addr	43	3	ORL	data addr, #data
11	2	ACALL	code addr	44	2	ORL	A, #data
12	3	LCALL	code addr	45	2	ORL	A, data addr
13	1	RRC	A	46	1	ORL	A, @R0
14	1	DEC	A	47	1	ORL	A, @R1
15	2	DEC	data addr	48	1	ORL	A, R0
16	1	DEC	@R0	49	1	ORL	A, R1
17	1	DEC	@R1	4A	1	ORL	A, R2
18	1	DEC	R0	4B	1	ORL	A, R3
19	1	DEC	R1	4C	1	ORL	A, R4
1A	1	DEC	R2	4D	1	ORL	A, R5
1B	1	DEC	R3	4E	1	ORL	A, R6
1C	1	DEC	R4	4F	1	ORL	A, R7
1D	1	DEC	R5	50	2	JNC	code addr
1E	1	DEC	R6	51	2	ACALL	code addr
1F	1	DEC	R7	52	2	ANL	data addr, A
20	3	JB	bit addr, code addr	53	3	ANL	data addr, #data
21	2	AJMP	code addr	54	2	ANL	A, #data
22	1	RET		55	2	ANL	A, data addr
23	1	RL	A	56	1	ANL	A, @R0
24	2	ADD	A, #data	57	1	ANL	A, @R1
25	2	ADD	A, data addr	58	1	ANL	A, R0
26	1	ADD	A, @R0	59	1	ANL	A, R1
27	1	ADD	A, @R1	5A	1	ANL	A, R2
28	1	ADD	A, R0	5B	1	ANL	A, R3
29	1	ADD	A, R1	5C	1	ANL	A, R4
2A	1	ADD	A, R2	5D	1	ANL	A, R5
2B	1	ADD	A, R3	5E	1	ANL	A, R6
2C	1	ADD	A, R4	5F	1	ANL	A, R7
2D	1	ADD	A, R5	60	2	JZ	code addr
2E	1	ADD	A, R6	61	2	AJMP	code addr
2F	1	ADD	A, R7	62	2	XRL	data addr, A
30	3	JNB	bit addr, code addr	63	3	XRL	data addr, #data
31	2	ACALL	code addr	64	2	XRL	A, #data
32	1	RETI		65	2	XRL	A, data addr



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Table 2. Instruction Opcodes in Hexadecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	ORL	C,bit addr
73	1	JMP	@A+DPTR
74	2	MOV	A,#data
75	3	MOV	data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data
7F	2	MOV	R7,#data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	data addr, data addr
86	2	MOV	data addr,@R0
87	2	MOV	data addr,@R1
88	2	MOV	data addr,R0
89	2	MOV	data addr,R1
8A	2	MOV	data addr,R2
8B	2	MOV	data addr,R3
8C	2	MOV	data addr,R4
8D	2	MOV	data addr,R5
8E	2	MOV	data addr,R6
8F	2	MOV	data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	code addr
92	2	MOV	bit addr,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0

Hex Code	Number of Bytes	Mnemonic	Operands
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/bit addr
A1	2	AJMP	code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,/bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3



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Table 2. Instruction Opcodes in Hexadecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr

Hex Code	Number of Bytes	Mnemonic	Operands
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A