



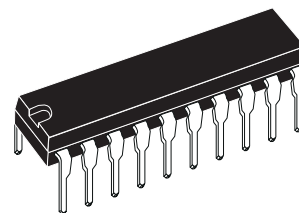
# TEA6425

## VIDEO CELLULAR MATRIX

- 6 Video Inputs - 8 Video Outputs
- 2 Internal Selectable YC Adders
- 15MHz Bandwidth @ -3dB
- Selectable 0.5/6.5dB Gain FOR EACH Output
- High Impedance Switch for each Output (3-state operation)
- Programmable Clamp Mode on each Input (sync bottom or average value)
- -60dB Crosstalk @ 5MHz
- 4 Sub-address Capability
- I<sup>2</sup>C Bus Control

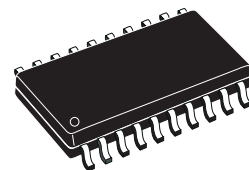
### DESCRIPTION

This device is intended for switching between video and chroma signals such as CVBS, SVHS, baseband CVBS, MAC. Each input clamp mode, each output gain, all switching are controlled through the I<sup>2</sup>C bus. The 8 outputs can be set separately in high impedance state, to enable parallel DC connection of several devices (up to 4).



**DIP20**  
**(Plastic Package)**

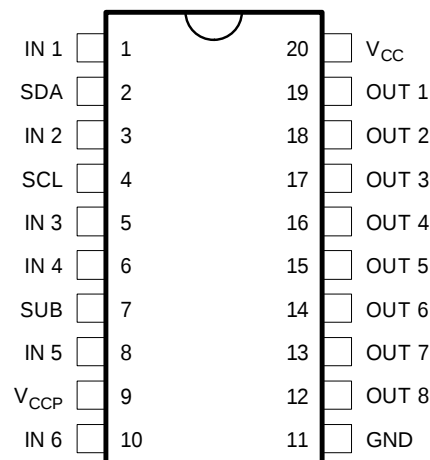
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**Figure 1. Pin Connections**



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TEA6425

Figure 2. Block Diagram

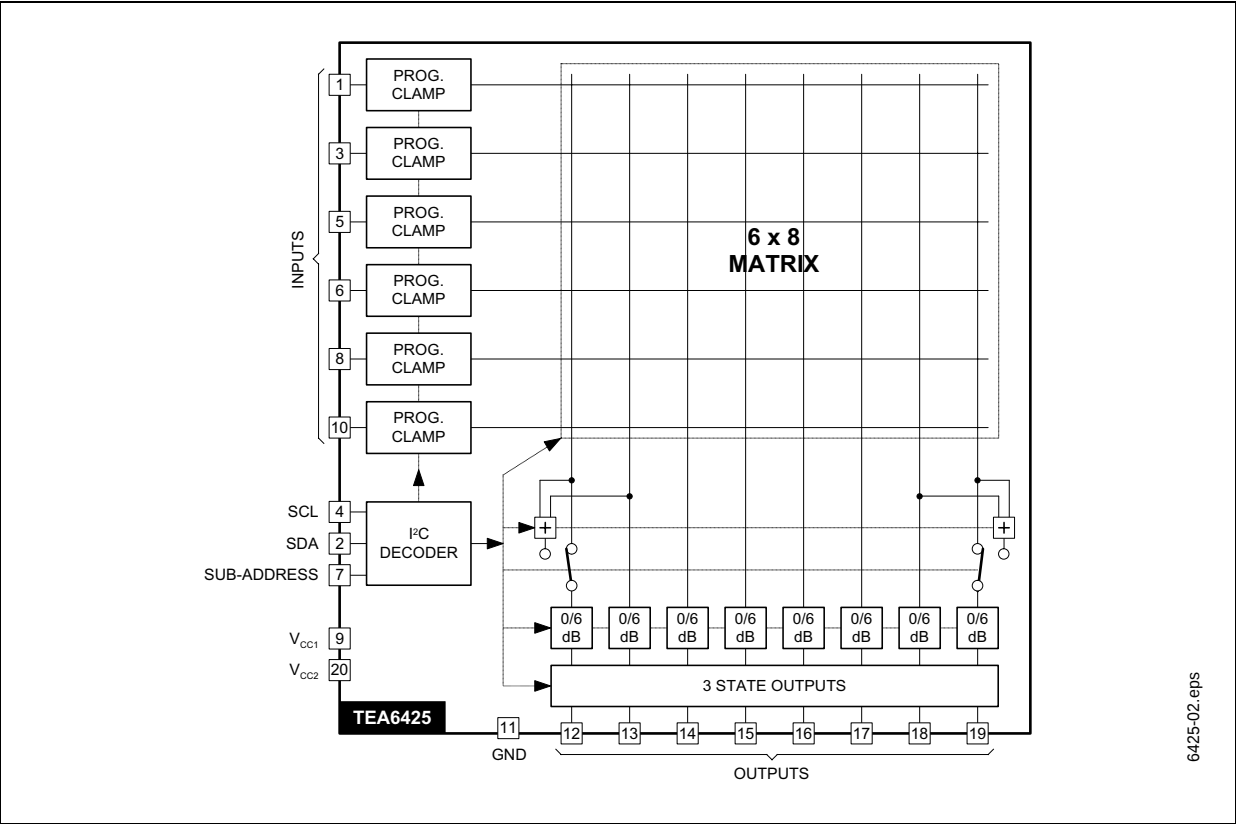
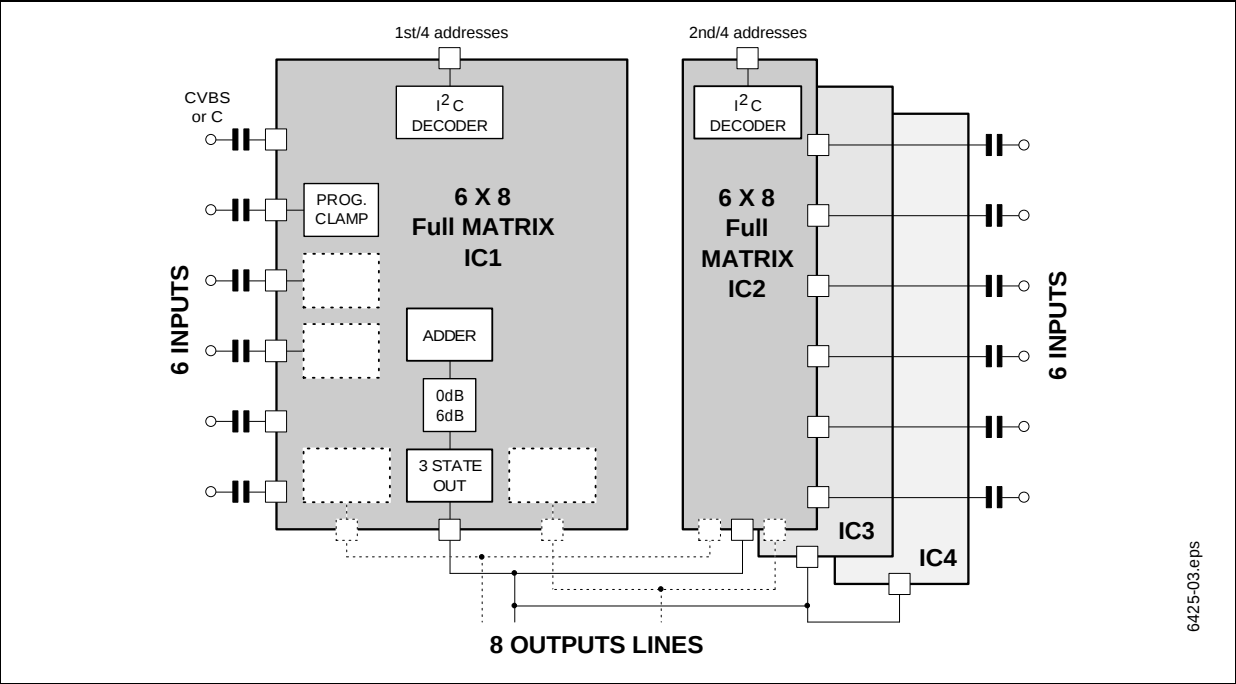


Figure 3. Cellular Matrix Connections



**ABSOLUTE MAXIMUM RATINGS**

| Symbol     | Parameter                     | Value       | Unit |
|------------|-------------------------------|-------------|------|
| $V_{CC}$   | Supply Voltage                | 12          | V    |
| $V_I$      | Voltage at Pin i to GND       | 0, $V_{CC}$ | V    |
| $T_{oper}$ | Operating Ambient Temperature | 0, + 70     | °C   |
| $T_{stg}$  | Storage Temperature           | -20, + 150  | °C   |

**THERMAL DATA**

| Symbol         | Parameter                                | Value | Unit |
|----------------|------------------------------------------|-------|------|
| $R_{th} (j-a)$ | Junction-ambient Thermal Resistance Min. | 80    | °C/W |

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 8V$ ,  $T_{amb} = 25^{\circ}C$ ,  $V_{IN} = 1V$ , Gain = 6.5dB,  $C_{load} = 20pF$ ,  $R_{load} = 4.7k\Omega$  ; Gain condition, clamp and 3-state are controlled by  $I^2C$  bus, unless otherwise specified)

| Symbol                                              | Parameter                              | Test Conditions                                                             | Min. | Typ.          | Max. | Unit       |
|-----------------------------------------------------|----------------------------------------|-----------------------------------------------------------------------------|------|---------------|------|------------|
| <b>SUPPLY</b>                                       |                                        |                                                                             |      |               |      |            |
| $V_{CC}$                                            | Supply Voltage                         |                                                                             | 7.2  | 8             | 8.8  | V          |
| $I_{CC}$                                            | Supply Current                         |                                                                             |      | 45            | 60   | mA         |
| RR                                                  | Supply Voltage Rejection               | f = 1kHz                                                                    | 40   | 46            |      | dB         |
| <b>VIDEO INPUTS (clamping at bottom sync level)</b> |                                        |                                                                             |      |               |      |            |
| $V_{IN}$                                            | Max. Signal Amplitude                  | Clamp Active                                                                | 2    |               |      | $V_{PP}$   |
| $V_{clamp}$                                         | Clamp Level                            | Clamp Active                                                                | 1.7  | 2             | 2.3  | V          |
| $V_{DC}$                                            | Input DC Level                         | Clamp Inactive                                                              | 2.7  | 3             | 3.3  | V          |
| $I_{IN}$                                            | Leakage Current                        | 1 input connected to 1 output                                               |      | 2             | 5    | $\mu A$    |
| $I_{clamp}$                                         | Clamp Current                          | $V_{clamp} - 200mV$                                                         |      | 0.9           | 3    | mA         |
| <b>VIDEO OUTPUTS</b>                                |                                        |                                                                             |      |               |      |            |
| $R_{OUT}$                                           | Output Resistance                      |                                                                             |      | 15            | 50   | W          |
| $Z_{HI}$                                            | Output "off" Impedance                 | no load                                                                     | 50   |               |      | k $\Omega$ |
| $C_{HI}$                                            | $C_{OUT}$ in 3-state                   | no load                                                                     |      | 3             |      | pF         |
| G1                                                  | Voltage Gain                           | f = 100kHz                                                                  | 0    | 0.5           | 1    | dB         |
| G2                                                  | Voltage Gain                           | f = 100kHz                                                                  | 6    | 6.5           | 7    | dB         |
| $V_{sync}$                                          | Top Level Sync (Y or CVBS)             | G = 6.5dB, Clamp Active                                                     | 1    | 1.25          | 2    | V          |
| $V_{bias}$                                          | Output Mean Level (chroma)             | G = 0.5dB, Clamp Inactive                                                   | 2    | 2.4           | 3    | V          |
|                                                     |                                        | G = 6.5dB, Clamp Inactive                                                   | 3    | 3.4           | 4    | V          |
|                                                     | Isolation "off" State                  | f = 5MHz                                                                    | 60   |               |      | dB         |
|                                                     | Crosstalk Attenuation between Channels | f = 5MHz                                                                    | 50   | 60            |      | dB         |
| B                                                   | Bandwidth                              | $C_{load} = 20pF$ , G = 6.5dB<br>at $\pm 0.5dB$<br>at $\pm 1dB$<br>at - 3dB |      | 5<br>10<br>21 |      | MHz        |

**FUNCTIONAL DESCRIPTION**

This device is controlled via the  $I^2C$  bus. 4 addresses can be selected by a 4-level detector on Pin 7, thus enabling parallel connection of 4 devices.

Via the  $I^2C$  bus :

- The input signals can be clamped at their negative peak (top sync).
- The gain factor of the outputs can be selected between 0.5 and 6.5dB.

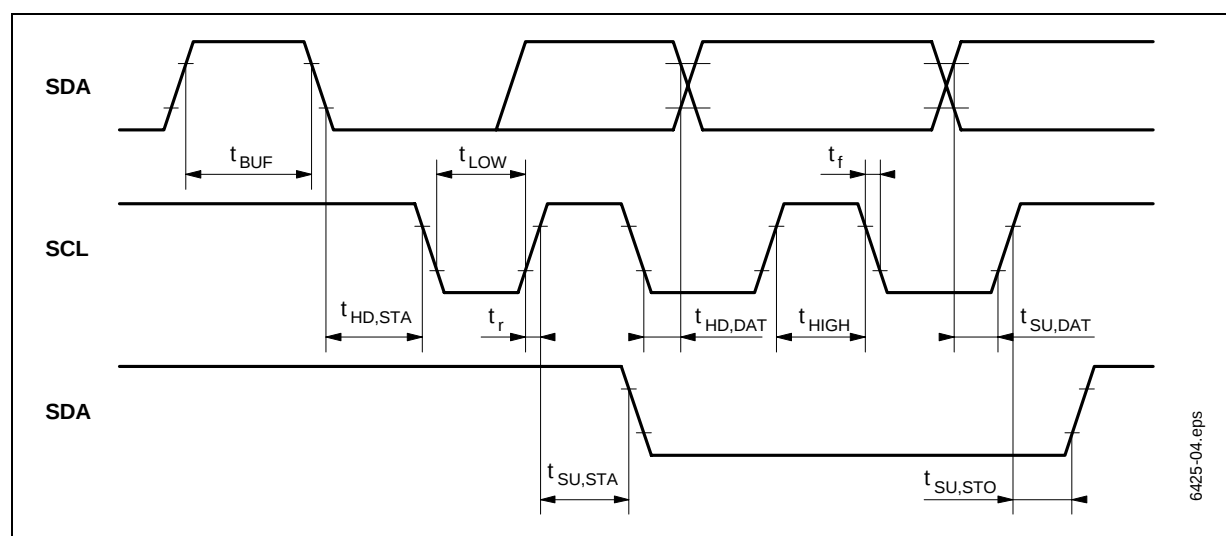
– Each of the 6 inputs can be connected to the 8 outputs.

– Each output can individually be set in a high impedance state.

Two internal SVHS mixers will add the selected Y and C inputs. Two dedicated outputs will have the option to select this added signal also.

**I<sup>2</sup>C BUS CHARACTERISTICS**

| Symbol               | Parameter                                                | Test Conditions                       | Standard Mode |                       | Fast Mode |                       | Unit |
|----------------------|----------------------------------------------------------|---------------------------------------|---------------|-----------------------|-----------|-----------------------|------|
|                      |                                                          |                                       | Min.          | Max.                  | Min.      | Max.                  |      |
| SCL                  |                                                          |                                       |               |                       |           |                       |      |
| V <sub>IL</sub>      | Low Level Input Voltage                                  |                                       | - 0.3         | + 1.5                 | - 0.3     | + 1.5                 | V    |
| V <sub>IH</sub>      | High Level Input Voltage                                 |                                       | 3.0           | V <sub>CC</sub> + 0.5 | 3.0       | V <sub>CC</sub> + 0.5 | V    |
| I <sub>LI</sub>      | Input Leakage Current                                    | V <sub>I</sub> = 0 to V <sub>DD</sub> | - 10          | + 10                  | - 10      | + 10                  | μA   |
| f <sub>SCL</sub>     | Clock Frequency                                          |                                       | 0             | 100                   | 0         | 400                   | kHz  |
| t <sub>R</sub>       | Input Rise Time                                          | 1.5V to 3V                            |               | 1000                  |           | 300                   | ns   |
| t <sub>F</sub>       | Input Fall Time                                          | 1.5V to 3V                            |               | 300                   |           | 300                   | ns   |
| C <sub>I</sub>       | Input Capacitance                                        |                                       |               | 10                    |           | 10                    | pF   |
| SDA                  |                                                          |                                       |               |                       |           |                       |      |
| V <sub>IL</sub>      | Low Level Input Voltage                                  |                                       | - 0.3         | + 1.5                 | - 0.3     | + 1.5                 | V    |
| V <sub>IH</sub>      | High Level Input Voltage                                 |                                       | 3.0           | V <sub>CC</sub> + 0.5 | 3.0       | V <sub>CC</sub> + 0.5 | V    |
| I <sub>LI</sub>      | Input Leakage Current                                    | V <sub>I</sub> = 0 to V <sub>DD</sub> | - 10          | + 10                  | - 10      | + 10                  | μA   |
| C <sub>I</sub>       | Input Capacitance                                        |                                       |               | 10                    |           | 10                    | pF   |
| t <sub>R</sub>       | Input Rise Time                                          | 1.5V to 3V                            |               | 1000                  |           | 300                   | ns   |
| t <sub>F</sub>       | Input Fall Time                                          | 1.5V to 3V                            |               | 300                   |           | 300                   | ns   |
| V <sub>OL</sub>      | Low Level Output Voltage                                 | I <sub>OL</sub> = 3mA                 |               | 0.4                   |           | 0.4                   | V    |
| t <sub>F</sub>       | Output Fall Time                                         | 3V to 1.5V                            |               | 250                   |           | 250                   | ns   |
| C <sub>L</sub>       | Load Capacitance                                         |                                       |               | 400                   |           | 400                   | pF   |
| TIMING               |                                                          |                                       |               |                       |           |                       |      |
| t <sub>LOW</sub>     | Clock Low Period                                         |                                       | 4.7           |                       | 1.3       |                       | μs   |
| t <sub>HIGH</sub>    | Clock High Period                                        |                                       | 4.0           |                       | 0.6       |                       | μs   |
| t <sub>SU, DAT</sub> | Data Set-up Time                                         |                                       | 250           |                       | 100       |                       | ns   |
| t <sub>HD, DAT</sub> | Data Hold Time                                           |                                       | 0             | 340                   | 0         | 340                   | ns   |
| t <sub>SU, STO</sub> | Set-up Time from Clock High to Stop                      |                                       | 4.0           |                       | 0.6       |                       | μs   |
| t <sub>BUF</sub>     | Start Set-up Time following a Stop                       |                                       | 4.7           |                       | 1.3       |                       | μs   |
| t <sub>HD, STA</sub> | Start Hold Time                                          |                                       | 4.0           |                       | 0.6       |                       | μs   |
| t <sub>SU, STA</sub> | Start Set-up Time following Clock Low-to-High Transition |                                       | 4.7           |                       | 0.6       |                       | μs   |

**Figure 4. I<sup>2</sup>C Bus Timing**

**I<sup>2</sup>C BUS SELECTION****I<sup>2</sup>C Bus Slave Address**

| Address | A6 | A5 | A4 | A3 | A2 | A1  | A0 | R/W |
|---------|----|----|----|----|----|-----|----|-----|
| Value   | 1  | 0  | 0  | 1  | 0  | A 1 | A0 | 0   |

**I<sup>2</sup>C Sub-Address**

| Symbol | Parameter          | Conditions                | Pin 7 Voltage (Typ) | Unit            |
|--------|--------------------|---------------------------|---------------------|-----------------|
| Vsub   | Slave address HEXA | Sub-address<br>(see note) |                     |                 |
|        |                    | A1      A0                |                     |                 |
| 1      | 90                 | 0      0                  | GND                 | V               |
| 2      | 96                 | 1      1                  | V <sub>CC</sub>     | V               |
| 3      | 94                 | 1      0                  | 1/3                 | V <sub>CC</sub> |
| 4      | 92                 | 0      1                  | 2/3                 | V <sub>CC</sub> |

**Note:** The first 3 levels are defined by connecting the sub-address pin to the appropriate level. Sub-address 4 will be selected when this pin is left open.

**1st Data Byte**

|               | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Selected Output |
|---------------|----|----|----|----|----|----|----|----|-----------------|
|               | a2 | a1 | a0 | *  | *  | *  | *  | I  |                 |
| Output Select | 0  | 0  | 0  | *  | *  | *  | *  | 0  | OUT1            |
|               | 0  | 0  | 1  | *  | *  | *  | *  | 0  | OUT2            |
|               | 0  | 1  | 0  | *  | *  | *  | *  | 0  | OUT3            |
|               | 0  | 1  | 1  | *  | *  | *  | *  | 0  | OUT4            |
|               | 1  | 0  | 0  | *  | *  | *  | *  | 0  | OUT5            |
|               | 1  | 0  | 1  | *  | *  | *  | *  | 0  | OUT6            |
|               | 1  | 1  | 0  | *  | *  | *  | *  | 0  | OUT7            |
|               | 1  | 1  | 1  | *  | *  | *  | *  | 0  | OUT8            |

**2nd Data Byte**

|              | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Selected Output |
|--------------|----|----|----|----|----|----|----|----|-----------------|
|              | a2 | a1 | a0 | *  | *  | *  | *  | I  |                 |
| Input Select | 0  | 0  | 0  | *  | *  | *  | *  | 1  | IN1             |
|              | 0  | 0  | 1  | *  | *  | *  | *  | 1  | IN2             |
|              | 0  | 1  | 0  | *  | *  | *  | *  | 1  | IN3             |
|              | 0  | 1  | 1  | *  | *  | *  | *  | 1  | IN4             |
|              | 1  | 0  | 0  | *  | *  | *  | *  | 1  | IN5             |
|              | 1  | 0  | 1  | *  | *  | *  | *  | 1  | IN6             |
| Clamp        | *  | *  | *  | 0  | *  | *  | *  | 1  | Free            |
|              | *  | *  | *  | 1  | *  | *  | *  | 1  | Clamped         |
| Gain         | *  | *  | *  | *  | 0  | *  | *  | 1  | 0.5dB           |
|              | *  | *  | *  | *  | 1  | *  | *  | 1  | 6.5dB           |
| Mixer        | *  | *  | *  | *  | *  | 0  | *  | 1  | Disabled        |
|              | *  | *  | *  | *  | *  | 1  | *  | 1  | Enabled         |
| Tri-state    | *  | *  | *  | *  | *  | *  | 0  | 1  | Low impedance   |
|              | *  | *  | *  | *  | *  | *  | 1  | 1  | Tri-state       |

**Power-on-Reset**

When active: outputs in 3-state, inputs are clamped

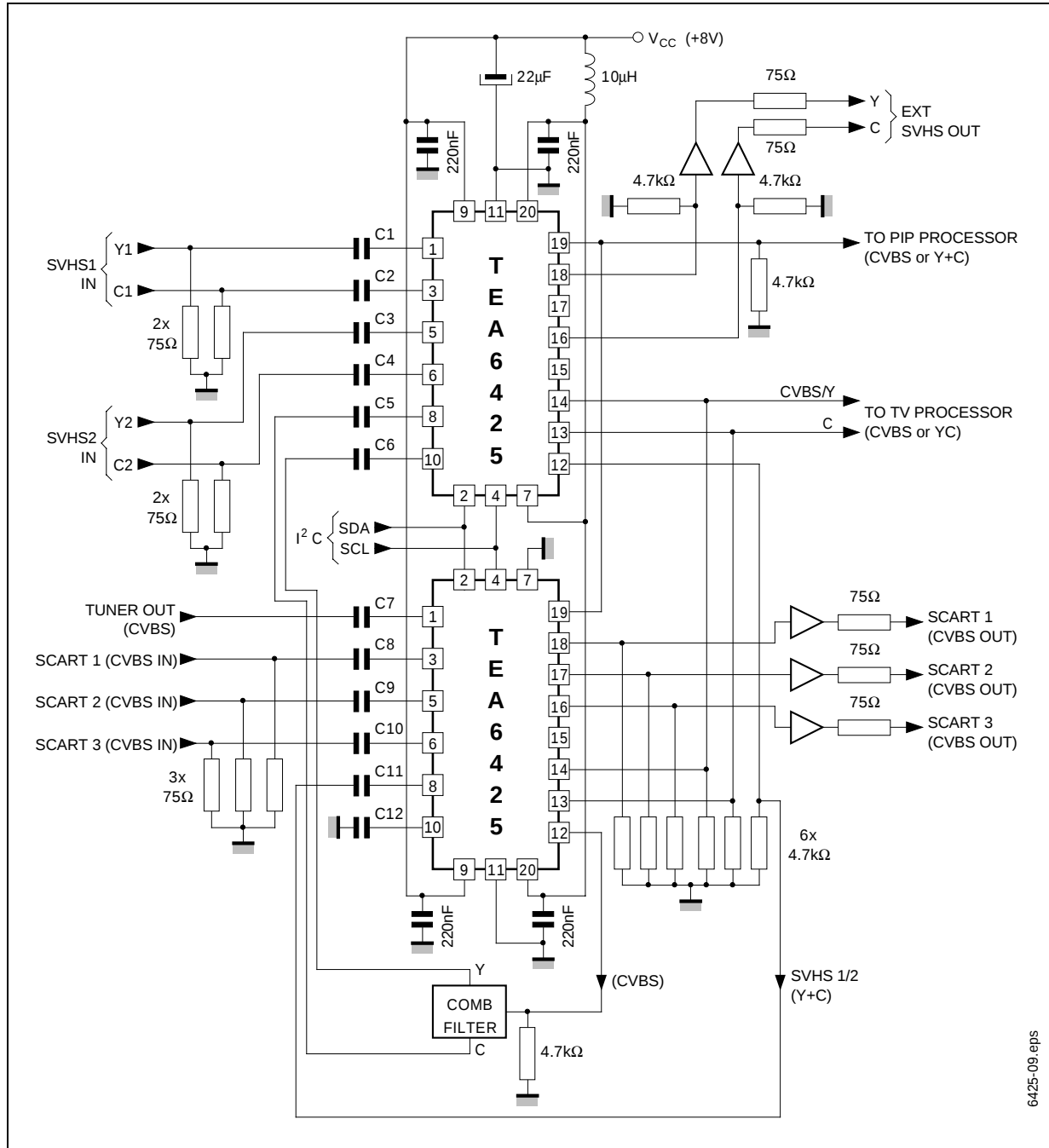
| Symbol | Parameter      | Test Conditions       | Min. | Typ. | Max. | Unit |
|--------|----------------|-----------------------|------|------|------|------|
| Reset  | Start of Reset | Incr. V <sub>CC</sub> |      |      | 2.5  | V    |
|        |                | Decr. V <sub>CC</sub> |      |      | 4.2  | V    |
|        | End of Reset   | Incr. V <sub>CC</sub> | 4.5  |      |      | V    |

[illegible]

The schematic diagram illustrates the output driver circuit for pins 12-19. It features a differential pair of PMOS and NMOS transistors, a current source, and a feedback loop with an op-amp and a TRISTATE switch. The output is connected to pins 12-19. Labels include TRI-STATE, From Matrix,  $V_{REF}$ , and TRISTATE.

The diagram shows a 3-bit DAC circuit. It features a current mirror with two input branches. The left branch consists of a 20kΩ resistor in series with a 40kΩ resistor, connected to a node labeled '7'. The right branch consists of a 20kΩ resistor connected to a node labeled 'V<sub>REF</sub>'. The output of the current mirror is connected to a node labeled 'to CMOS'. The circuit is powered by V<sub>CC</sub> and ground. A note at the bottom indicates '3 TIMES IN //', suggesting the circuit is repeated three times in parallel.

Figure 9. Typical Application



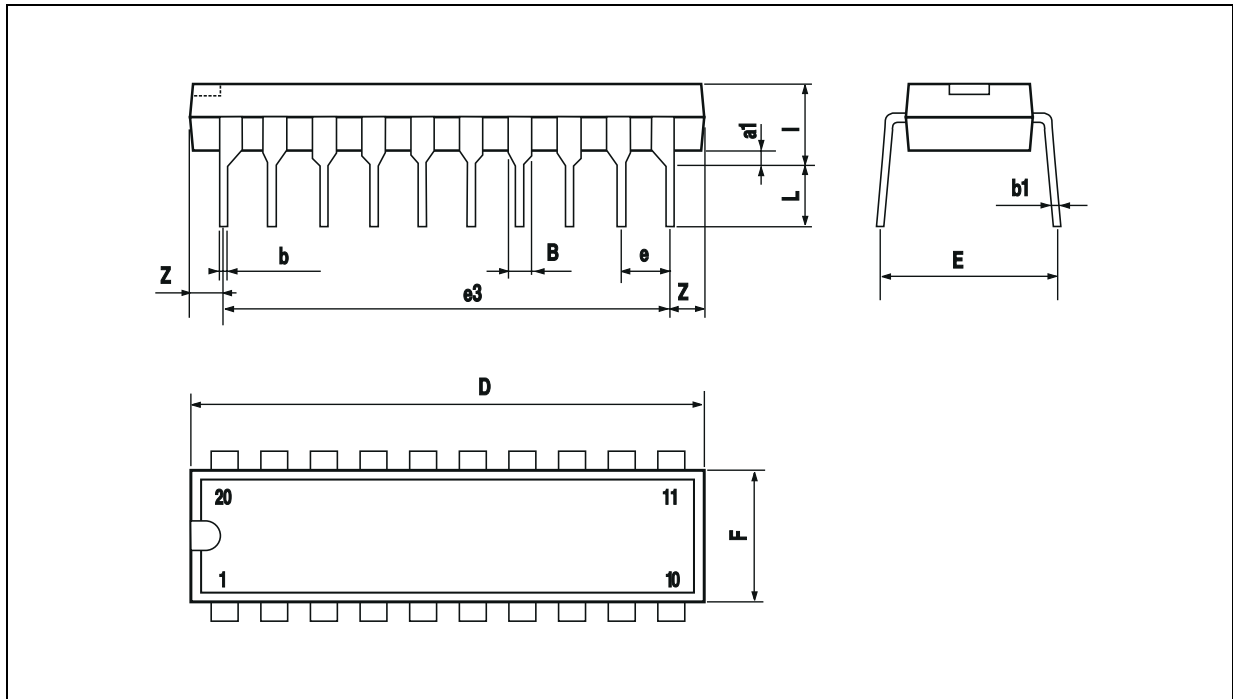
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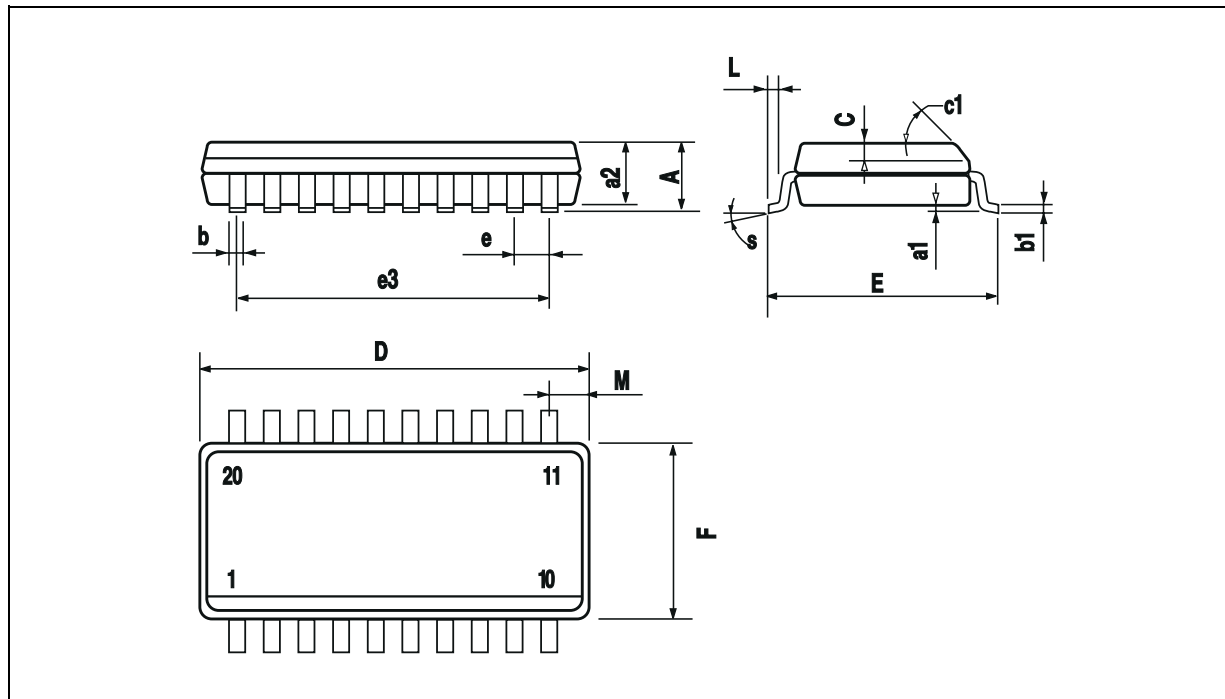
## TEA6425

### PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP

Figure 10. 20-Pin Package



**PACKAGE MECHANICAL DATA (Cont'd)****20 PINS - PLASTIC MICROPACKAGE****Figure 11. 20-Pin Package**

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