

## ID8751H

### *Single-Chip 8-Bit Microcontroller with 4K/8K Bytes of EPROM*

The 8751H and 8753H are members of a family of advanced single-chip microcontrollers. Both the 8751H, which has 4K bytes of EPROM, and the 8753H, which has 8K bytes of EPROM, are pin-compatible EPROM versions of the 8051 AH and 8053AH, respectively. Thus, the 8751H/8753H are full-speed prototyping tools which provide effective single-chip solutions for controller applications that require code modification flexibility. Refer to the block diagram of the 8051 family.

The 8751H/8753H devices feature: thirty-two I/O lines; two 18-bit timer/event counters; a Boolean processor; a 5-source, bi-level interrupt structure; a full-duplex serial channel; and on-chip oscillator and clock circuitry.

#### **Rochester Electronics Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

#### **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

#### **FOR REFERENCE ONLY**

# 8751H/8753H

Single-Chip 8-Bit Microcontroller with  
4K/8K Bytes of EPROM

## DISTINCTIVE CHARACTERISTICS

- 4K x 8 EPROM (8751H); 8K x 8 EPROM (8753H)
- 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines; programmable serial port
- Two 16-bit Timer/Event counters
- 64K addressable Program and Data Memory
- Boolean processor
- Five interrupt sources/two priority levels
- 4-cycle multiply and divide
- Program memory security feature
- Fast EPROM programming: 12 sec for 4K bytes
- Supports silicon signature verification
- Pin compatible with 8051

## GENERAL DESCRIPTION

The 8751H and 8753H are members of a family of advanced single-chip microcontrollers. Both the 8751H, which has 4K bytes of EPROM, and the 8753H, which has 8K bytes of EPROM, are pin-compatible EPROM versions of the 8051AH and 8053AH, respectively. Thus, the 8751H/8753H are full-speed prototyping tools which provide effective single-chip solutions for controller applications that require code modification flexibility. Refer to the block diagram of the 8051 family.

The 8751H/8753H devices feature: thirty-two I/O lines; two 16-bit timer/event counters; a Boolean processor; a 5-source, bi-level interrupt structure; a full-duplex serial channel; and on-chip oscillator and clock circuitry.

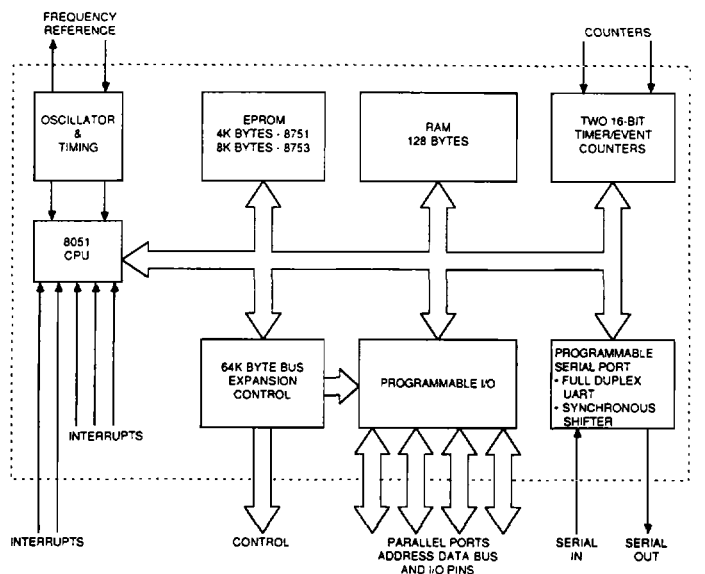
Program and Data Memory are located in independent addresses. The AMD family of microcontrollers can access up to 64K bytes of external Program Memory and up to 64K

bytes of external Data Memory. The 8751H and the 8753H contain the lower 4K and 8K bytes of Program Memory, respectively, on-chip. Both parts have 128 bytes of on-chip read/write data memory.

The AMD 8051 Microcontroller Family is specifically suited for control applications. A variety of fast addressing modes, which access the internal RAM, facilitates byte processing and numerical operations on small data structures. Included in the instruction set is a menu of 8-bit arithmetic instructions, including 4-cycle multiply and divide instructions.

Extensive on-chip support enables direct bit manipulation and testing of 1-bit variables as separate data types. Thus, the device is also suited for control and logic systems that require Boolean processing.

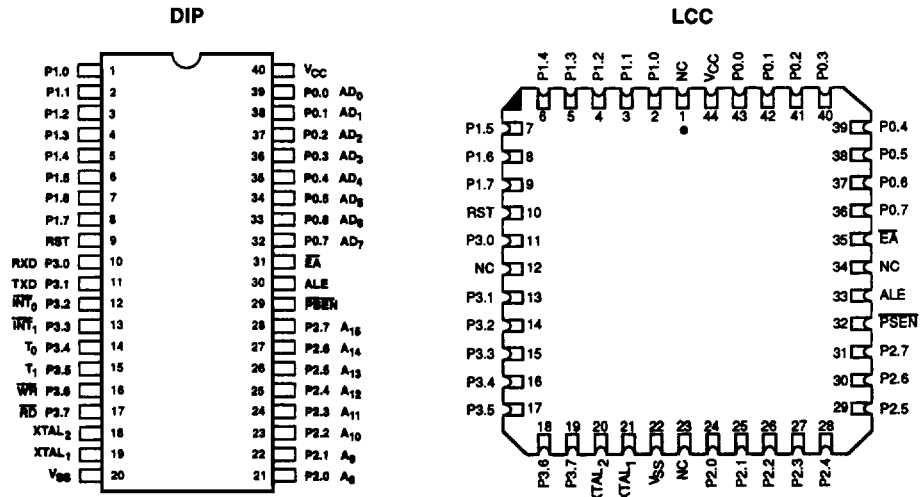
## BLOCK DIAGRAM



BD007250

## CONNECTION DIAGRAMS

### Top View

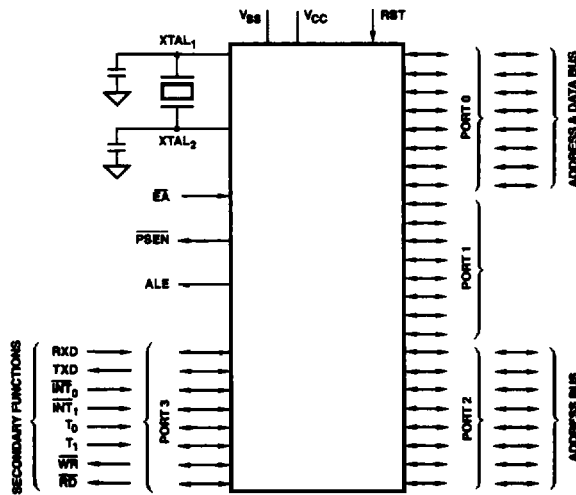


CD005551

CD010870

Note: Pin 1 is marked for orientation.

## LOGIC SYMBOL



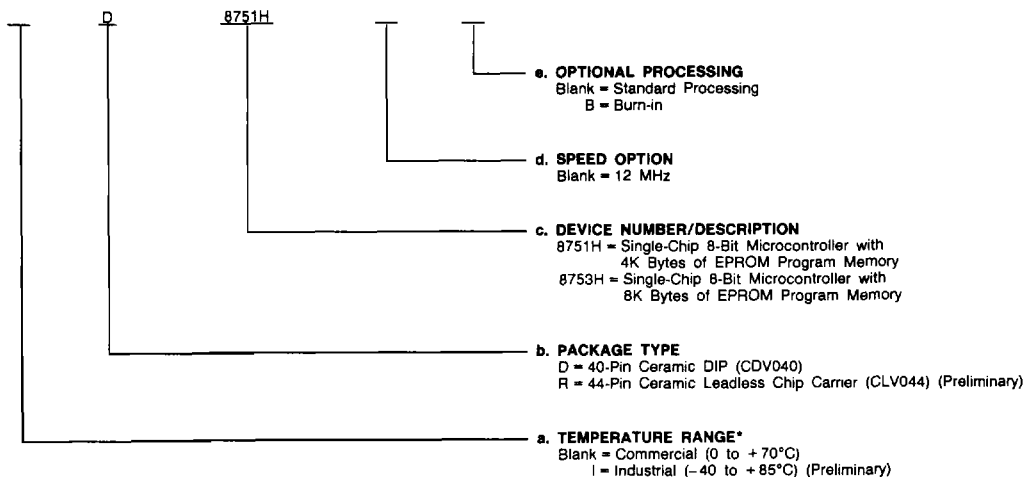
LS001325

## ORDERING INFORMATION

### Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Temperature Range
- b. Package Type
- c. Device Number
- d. Speed Option
- e. Optional Processing



| Valid Combinations |        |
|--------------------|--------|
| D, R               | 8751H  |
|                    | 8753H  |
| ID                 | 8751H  |
|                    | 8751HB |
|                    | 8753H  |
|                    | 8753HB |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

\*This device is also available in Military temperature range. See MOS Microprocessors and Peripherals Military Handbook (Order #09275A/0) for electrical performance characteristics.

## PIN DESCRIPTION

### Port 0 (Bidirectional; Open Drain)

Port 0 is an open-drain I/O port. Port 0 pins that have "1"s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed LOW-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting "1"s. Port 0 also outputs the code bytes during program verification in the 8751H and 8753H. External pullups are required during program verification.

### Port 1 (Bidirectional)

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four LS TTL inputs. Port 1 pins that have "1"s written to them are pulled HIGH by the internal pullups and — while in this state — can be used as inputs. As inputs, Port 1 pins that are externally being pulled LOW will source current ( $I_{IL}$  on the data sheet) because of the internal pullups.

Port 1 also receives the LOW-order address bytes during program verification.

### Port 2 (Bidirectional)

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four LS TTL inputs. Port 2 pins having "1"s written to them are pulled HIGH by the internal pullups and — while in this state — can be used as inputs. As inputs, Port 2 pins externally being pulled LOW will source current ( $I_{IL}$ ) because of internal pullups.

Port 2 emits the HIGH-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting "1"s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function register.

Port 2 also receives the HIGH-order address bits during the programming of the EPROM and during program verification of the EPROM.

### Port 3 (Bidirectional)

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four LS TTL inputs. Port 3 pins having "1"s written to them are pulled HIGH by the internal pullups and — while in this state — can be used as inputs. As inputs, Port 3 pins externally being pulled LOW will source current ( $I_{IL}$ ) because of the pullups.

Port 3 also serves the functions of various special features as listed below:

| Port Pin         | Alternate Function                      |
|------------------|-----------------------------------------|
| P <sub>3,0</sub> | RxD (Serial Input Port)                 |
| P <sub>3,1</sub> | TxD (Serial Output Port)                |
| P <sub>3,2</sub> | INT <sub>0</sub> (External Interrupt 0) |
| P <sub>3,3</sub> | INT <sub>1</sub> (External Interrupt 1) |
| P <sub>3,4</sub> | T <sub>0</sub> (Timer 0 External Input) |
| P <sub>3,5</sub> | T <sub>1</sub> (Timer 1 External Input) |
| P <sub>3,6</sub> | WR (External Data Memory Write Strobe)  |
| P <sub>3,7</sub> | RD (External Data Memory Read Strobe)   |

### RST/V<sub>PP</sub> Reset (Input; Active HIGH)

This pin is used to reset the device when held HIGH for two machine cycles while the oscillator is running. If RST/V<sub>PP</sub> is held within the V<sub>PP</sub> spec, it will supply standby power to the RAM in the event that V<sub>CC</sub> drops below its spec. When RST/V<sub>PP</sub> is LOW, the RAM's bias is drawn from V<sub>CC</sub>.

### ALE/PROG Address Latch Enable/Program Pulse (Input/Output)

Address Latch Enable output pulse for latching the LOW byte of the address during accesses to external memory. ALE can drive eight LS TTL inputs.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, allowing use for external-timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. This pin also accepts the program pulse input (PROG) when programming the EPROM.

### PSEN Program Store Enable (Output; Active LOW)

PSEN is the read strobe to external Program Memory. PSEN can drive eight LS TTL inputs. When the device is executing code from an external program memory, PSEN is activated twice each machine cycle — except that two PSEN activations are skipped during each access to external Data Memory. PSEN is not activated during fetches from internal Program Memory.

### EA/V<sub>pp</sub> External Access Enable (Input; Active LOW)

EA must be externally held LOW to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH (0000H to 1FFFFH in the 8753H). If EA is held HIGH, the 8751H executes from internal Program Memory unless the program counter contains an address greater than 0FFFFH (1FFFFH in the 8753H).

### XTAL<sub>1</sub> Crystal (Input)

Input to the inverting oscillator amplifier. When an external oscillator is used, XTAL<sub>1</sub> should be grounded.

### XTAL<sub>2</sub> Crystal (Output)

Output of the inverting oscillator amplifier. XTAL<sub>2</sub> is also the input for the oscillator signal when using an external oscillator.

### V<sub>CC</sub> Power Supply

### V<sub>SS</sub> Circuit Ground

## PROGRAMMING

### Programming the EPROM

To program the EPROM, either the internal or external oscillator must be running at 4 to 6 MHz because the internal bus is used to transfer address and program data to the appropriate internal registers.

The 8751H and 8753H devices support an adaptive EPROM programming algorithm in addition to the conventional EPROM programming algorithm. Adaptive device programming (sometimes called interactive or intelligent programming) adapts to the actual charge storage efficiency of each byte, so that no wasted programming time occurs and minimum device programming time is realized.

The typical resulting device programming time is a mere 7% of what is required for a conventional programming algorithm. For example, to program a 4K byte EPROM using the conventional programming algorithm will require  $4K \times 50 \text{ ms} = 200 \text{ sec}$ . If adaptive programming is used, the theoretical programming time required will be  $4K \times 3 \text{ ms} = 12 \text{ sec}$ . The actual speed advantage of the adaptive programming is still very significant even allowing for the additional software overhead to implement the adaptive algorithm (2 to 8 sec depending on the brand of EPROM programmer).

To program the 8751H, pins  $P_{2.4} - P_{2.6}$  and  $PSEN$  should be held LOW, and  $P_{2.7}$  and  $RST$  held HIGH as shown in Table 2. The address of the location to be programmed is applied to Port 1 and  $P_{2.0} - P_{2.3}$  while the code byte to be programmed is applied to Port 0 (see Figure 1).

$V_{pp}$  should be at 21 V during device programming and the  $ALE/\overline{PROG}$  pin should be pulsed LOW for 1 ms to program the code byte into the addressed EPROM location. The programmed byte is verified immediately after programming.

Figure 3 illustrates the flow of the adaptive programming algorithm. At each address, up to 15 program/verify loops are attempted to verify the programmability of the byte using 1 ms  $\overline{PROG}$  pulses. After the programmability of a byte is determined, an overprogramming pulse of 2 ms is applied to  $\overline{PROG}$  to guarantee data retention. (This conforms with the AMD standard of 2 ms/byte overprogramming for all N-channel EPROMs.)

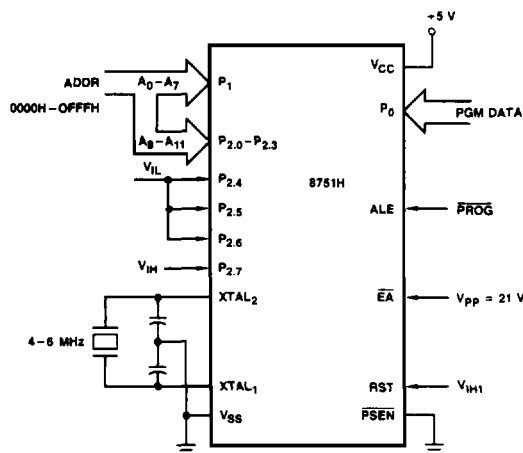
The programming of 8753H is similar to the above procedures except that pin  $P_{2.4}$  is the additional address pin ( $A_{12}$ ) for accessing the upper 4K bytes of the EPROM (see Figure 2).

The 8751H and 8753H can also be programmed using the less efficient conventional EPROM programming algorithm. In this method,  $V_{pp}$  is held at 21 V and  $\overline{PROG}$  is pulsed low for 50 ms to program each code byte into the addressed EPROM location. After the memory is programmed, all addresses would be sequenced and verified.

### A Note of Caution When Programming

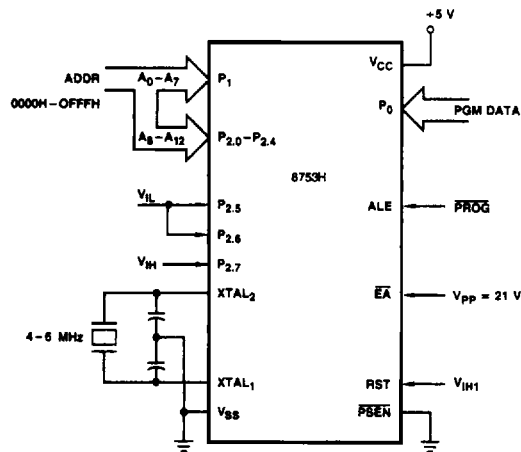
The maximum voltage applied to the  $\overline{EA}/V_{pp}$  pin must not exceed 21.5 V at any time as specified for  $V_{pp}$ . Even a slight spike can cause permanent damage to the device. The  $V_{pp}$  source should thus be well-regulated and glitch-free.

When programming, a  $0.1 \times 10^{-6} \text{ F}$  capacitor is required across  $V_{pp}$  and ground to suppress spurious transients which may damage the device.



LS001453

Figure 1. 8751H Programming Configuration



LS001444

Figure 2. 8753H Programming Configuration

TABLE 1. EPROM PROGRAMMING MODES FOR THE 8751H

| Mode         | RST  | PSEN | ALE | EA   | P2.7 | P2.6 | P2.5 | P2.4 |
|--------------|------|------|-----|------|------|------|------|------|
| Program      | VIH1 | L    | L*  | Vpp  | H    | L    | L    | L    |
| Inhibit      | VIH1 | L    | H   | X    | H    | L    | L    | L    |
| Verify       | VIH1 | L    | H   | VppX | L    | L    | L    | L    |
| Security Set | VIH1 | L    | L†  | Vpp  | H    | H    | L    | X    |

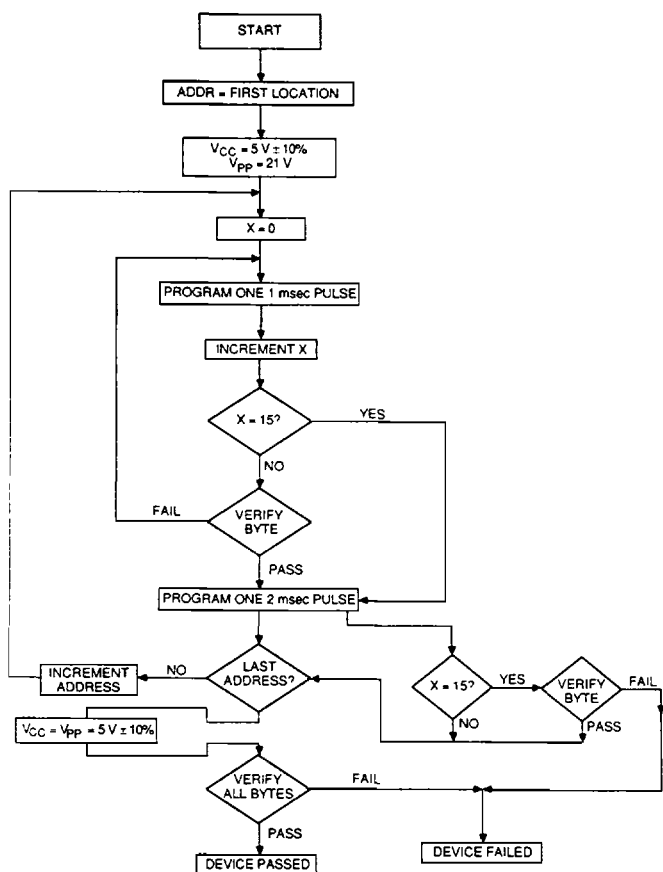
Note: See notes below Table 2.

TABLE 2. EPROM PROGRAMMING MODES FOR THE 8753H

| Mode         | RST  | PSEN | ALE | EA   | P2.7 | P2.6 | P2.5 |
|--------------|------|------|-----|------|------|------|------|
| Program      | VIH1 | L    | L*  | Vpp  | H    | L    | L    |
| Inhibit      | VIH1 | L    | H   | X    | H    | L    | L    |
| Verify       | VIH1 | L    | H   | VppX | L    | L    | L    |
| Security Set | VIH1 | L    | L†  | Vpp  | H    | H    | L    |

Note: H = Logic HIGH for that pin  
 L = Logic LOW for that pin  
 X = Don't Care  
 Vpp = +21 V ±0.5 V  
 2.0 V < VppX < 21.5 V

\*ALE is pulsed LOW for 1 msec in the programming loop of the adaptive programming algorithm and is pulsed LOW for 50 msec if conventional EPROM programming algorithm is used.  
 †ALE is pulsed LOW for 50 msec.



PF002510

**Figure 3. Adaptive Programming Algorithm for 8751H and 8753H**

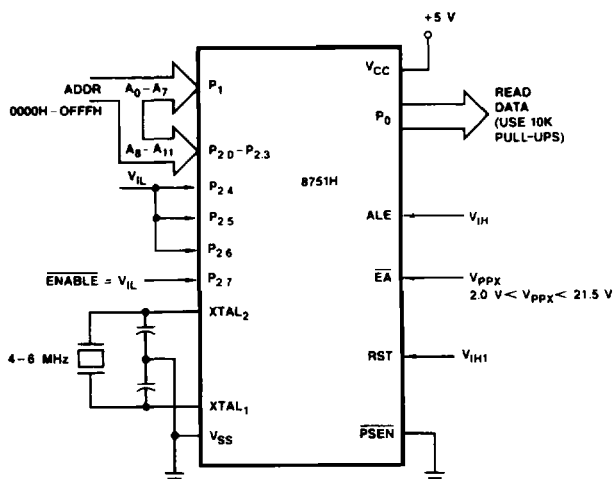
## Program Verification

The Program Memory may be read out for verification purposes when the security bit has not been programmed. Reading the Program Memory may occur during or after programming of the EPROM. When the oscillator is running at 4 – 6 MHz, the 8751H Program Memory address location to be read is applied to Port 1 and pins P<sub>2,0</sub> – P<sub>2,3</sub> of Port 2. Pins P<sub>2,4</sub> – P<sub>2,6</sub> and  $\overline{\text{PSEN}}$  are held at TTL LOW (see Figure 4). The 8753H utilizes Port 1 and pins P<sub>2,0</sub> – P<sub>2,4</sub> to address the EPROM, while P<sub>2,5</sub> – P<sub>2,6</sub> and  $\overline{\text{PSEN}}$  are held LOW (see Figure 5).

The ALE/ $\overline{\text{PROG}}$  and RST pins of both devices are held HIGH (RST requires only 2.5 V for HIGH) and the  $\overline{\text{EA}}$ / $V_{\text{PP}}$  pin voltage can have any value from 2.0 V to 21.5 V as shown in Tables 1 and 2.

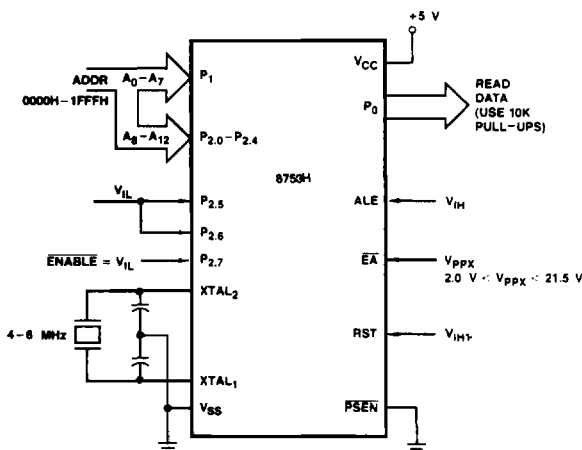
Port 0 will then output the contents of the address location. External pull-ups are needed on Port 0 when verifying the 8751H and 8753H EPROM.

Note: Since  $V_{\text{PP}}$  can be held at 21 V during program verification, the  $V_{\text{PP}}$  pin can be connected to a static 21 V power supply for device programming and verification in the adaptive device programming technique (see Figures 4 and 5).



LS001382

Figure 4. 8751H Program Verification



LS001394

Figure 5. 8753H Program Verification

The 8751H and 8753H incorporates a security bit, which when activated, prohibits all external readout of the on-chip EPROM contents. Figure 6 illustrates the security bit programming configuration for both the 8751H and 8753H. To activate the security bit, the same setup is used as when programming the EPROM except that  $P_{2,6}$  is held HIGH. Port 0, Port 1 and pins  $P_{2,0} - P_{2,3}$  may assume any state.  $V_{pp}$  should be at 21 V and the ALE/PROG pin should be pulsed LOW for 50 msec. The logic states of the other pins are detailed in Tables 1 and 2.

A secured Program Memory looks like a blank array of all ones, and this property can be used to verify that the EPROM is secured. The programmed security bit also prohibits further device programming and the execution of external Program Memory.

Full functionality and programmability may be restored by erasing the EPROM and thus clearing the security bit.



### Figure 6. Programming the Security Bit



## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65 to +150°C  
 Voltage on  $\overline{EA}/V_{PP}$  Pin to  $V_{SS}$  ..... -0.5 to +21.5 V  
 Voltage on Any Other Pin to  $V_{SS}$  ..... -0.5 to +7 V  
 Power Dissipation ..... 1.5 W

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices

Temperature ( $T_A$ ) ..... 0 to +70°C  
 Supply Voltage ( $V_{CC}$ ) ..... +4.5 to +5.5 V  
 Ground ( $V_{SS}$ ) ..... 0 V

Industrial (I) Devices (Preliminary)

Temperature ( $T_A$ ) ..... -40 to +85°C  
 Supply Voltage ( $V_{CC}$ ) ..... +4.5 to +5.5 V  
 Ground ( $V_{SS}$ ) ..... 0 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Parameter Symbol | Parameter Description                                                      | Test Conditions                                       | Min. | Max.           | Units   |
|------------------|----------------------------------------------------------------------------|-------------------------------------------------------|------|----------------|---------|
| $V_{IL}$         | Input LOW Voltage (Except $\overline{EA}$ )                                |                                                       | -0.5 | 0.8            | V       |
| $V_{IL1}$        | Input LOW Voltage to $\overline{EA}$                                       |                                                       | 0    | 0.7            | V       |
| $V_{IH}$         | Input HIGH Voltage (Except XTAL <sub>2</sub> , RST)                        |                                                       | 2.0  | $V_{CC} + 0.5$ | V       |
| $V_{IH1}$        | Input HIGH Voltage to XTAL <sub>2</sub> , RST                              | XTAL <sub>1</sub> = $V_{SS}$                          | 2.5  | $V_{CC} + 0.5$ | V       |
| $V_{OL}$         | Output LOW Voltage (Ports 1, 2, 3) (Note 1)                                | $I_{OL} = 1.6$ mA                                     |      | 0.45           | V       |
| $V_{OL1}$        | Output LOW Voltage (Port 0, ALE, $\overline{PSEN}$ )                       | $I_{OL} = 3.2$ mA<br>$I_{OL} = 2.4$ mA                |      | 0.60<br>0.45   | V       |
| $V_{OH}$         | Output HIGH Voltage (Ports 1, 2, 3)                                        | $I_{OH} = -80$ $\mu$ A                                | 2.4  |                | V       |
| $V_{OH1}$        | Output HIGH Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$ ) | $I_{OH} = -400$ $\mu$ A                               | 2.4  |                | V       |
| $I_{iL}$         | Logical 0 Input Current (Ports 1, 2, 3)                                    | $V_{IN} = 0.45$ V                                     |      | -500           | $\mu$ A |
| $I_{iL1}$        | Logical 0 Input Current ( $\overline{EA}$ )                                |                                                       |      | -15            | mA      |
| $I_{iL2}$        | Logical 0 Input Current (XTAL <sub>2</sub> )                               | $V_{IN} = 0.45$ V                                     |      | -3.2           | mA      |
| $I_{LI}$         | Input Leakage Current (Port 0)                                             | $0.45 < V_{IN} < V_{CC}$                              |      | $\pm 100$      | $\mu$ A |
| $I_{iH}$         | Logical 1 Input Current ( $\overline{EA}$ )                                |                                                       |      | 500            | $\mu$ A |
| $I_{iH1}$        | Input Current to RST to Activate Reset                                     | $V_{IN} < (V_{CC} - 1.5$ V)                           |      | 500            | $\mu$ A |
| $I_{CC}$         | Power Supply Current                                                       | All Outputs Disconnected;<br>$\overline{EA} = V_{CC}$ |      | 250            | mA      |
| $C_{iO}$         | Pin Capacitance                                                            | Test Freq = 1 MHz                                     |      | 10             | pF      |
| $I_{PD}$         | Power Down Current                                                         | $V_{CC} = 0$ V, $V_{PD} = 5$ V                        |      | 10             | mA      |

Notes: 1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the  $V_{OL}$ s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified  
(Load Capacitance for Port 0, ALE, and  $\overline{\text{PSEN}}$  = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

| Parameter Symbol | Parameter Description                                             | 12 MHz Osc. |      | Variable Oscillator |            | Units |
|------------------|-------------------------------------------------------------------|-------------|------|---------------------|------------|-------|
|                  |                                                                   | Min.        | Max. | Min.                | Max.       |       |
| 1/TCLCL          | Oscillator Frequency                                              |             |      | 1.2                 | 12         | MHz   |
| TLHLL            | ALE Pulse Width                                                   | 127         |      | 2TCLCL-40           |            | ns    |
| TAVLL            | Address Setup to ALE                                              | 43          |      | TCLCL-40            |            | ns    |
| TLLAX            | Address Hold After ALE                                            | 48          |      | TCLCL-35            |            | ns    |
| TLLIV            | ALE to Valid Instr In                                             |             | 183  |                     | 4TCLCL-150 | ns    |
| TLLPL            | ALE to $\overline{\text{PSEN}}$                                   | 58          |      | TCLCL-25            |            | ns    |
| TPLP             | $\overline{\text{PSEN}}$ Pulse Width                              | 190         |      | 3TCLCL-80           |            | ns    |
| TPLIV            | $\overline{\text{PSEN}}$ to Valid Instr In                        |             | 100  |                     | 3TCLCL-150 | ns    |
| TPXIX            | Input Instr Hold After $\overline{\text{PSEN}}$                   | 0           |      | 0                   |            | ns    |
| TPXIZ            | Input Instr Float After $\overline{\text{PSEN}}$                  |             | 63   |                     | TCLCL-20   | ns    |
| TPXAV            | Address Valid After $\overline{\text{PSEN}}$                      | 75          |      | TCLCL-8             |            | ns    |
| TAVIV            | Address to Valid Instr In                                         |             | 267  |                     | 5TCLCL-150 | ns    |
| TPLAZ            | Addr Float After $\overline{\text{PSEN}}$                         |             | 20   |                     | 20         | ns    |
| TRLRH            | $\overline{\text{RD}}$ Pulse Width                                | 400         |      | 6TCLCL-100          |            | ns    |
| TWLWH            | $\overline{\text{WR}}$ Pulse Width                                | 400         |      | 6TCLCL-100          |            | ns    |
| TRLDV            | $\overline{\text{RD}}$ to Valid Data In                           |             | 252  |                     | 5TCLCL-165 | ns    |
| TRHDX            | Data Hold After $\overline{\text{RD}}$                            | 0           |      | 0                   |            | ns    |
| TRHDZ            | Data Float After $\overline{\text{RD}}$                           |             | 97   |                     | 2TCLCL-70  | ns    |
| TLLDV            | ALE to Valid Data In                                              |             | 517  |                     | 8TCLCL-150 | ns    |
| TAVDV            | Address to Valid Data In                                          |             | 585  |                     | 9TCLCL-165 | ns    |
| TLLWL            | ALE to $\overline{\text{RD}}$ or $\overline{\text{WR}}$           | 200         | 300  | 3TCLCL-50           | 3TCLCL+50  | ns    |
| TAVWL            | Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$       | 203         |      | 4TCLCL-130          |            | ns    |
| TQVWX            | Data Valid to $\overline{\text{WR}}$ Transition                   | 13          |      | TCLCL-70            |            | ns    |
| TQVWH            | Data Setup Before $\overline{\text{WR}}$                          | 433         |      | 7TCLCL-150          |            | ns    |
| TWHQX            | Data Hold After $\overline{\text{WR}}$                            | 33          |      | TCLCL-50            |            | ns    |
| TRLAZ            | Address Float After $\overline{\text{RD}}$                        |             | 20   |                     | 20         | ns    |
| TWHLH            | $\overline{\text{RD}}$ or $\overline{\text{WR}}$ HIGH to ALE HIGH | 33          | 133  | TCLCL-50            | TCLCL+50   | ns    |

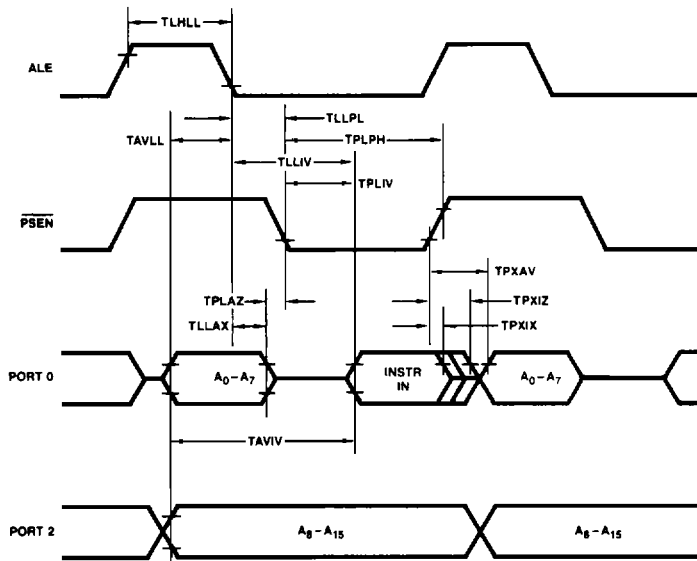
## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS                           | OUTPUTS                                   |
|----------|----------------------------------|-------------------------------------------|
|          | MUST BE STEADY                   | WILL BE STEADY                            |
|          | MAY CHANGE FROM H TO L           | WILL BE CHANGING FROM H TO L              |
|          | MAY CHANGE FROM L TO H           | WILL BE CHANGING FROM L TO H              |
|          | DON'T CARE, ANY CHANGE PERMITTED | CHANGING, STATE UNKNOWN                   |
|          | DOES NOT APPLY                   | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

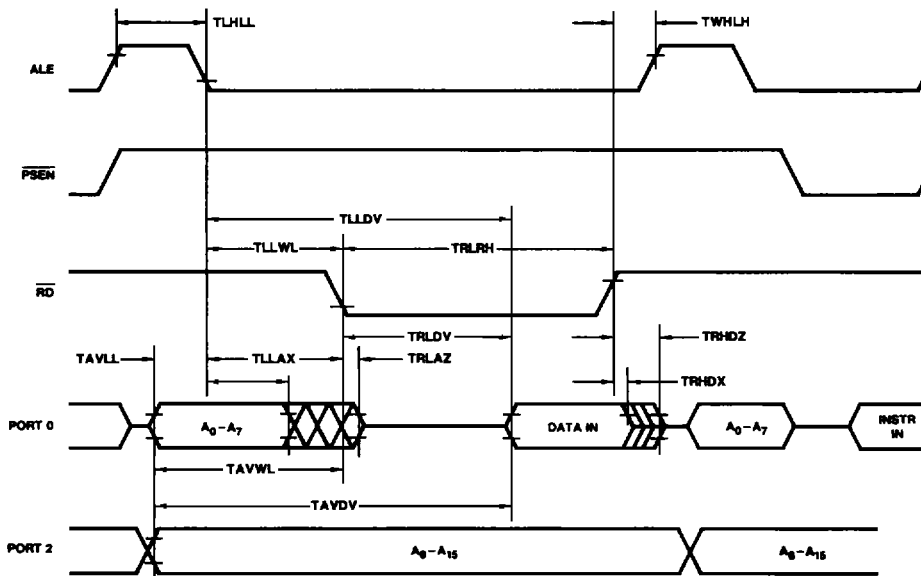
KS000010

## SWITCHING WAVEFORMS



WF008744

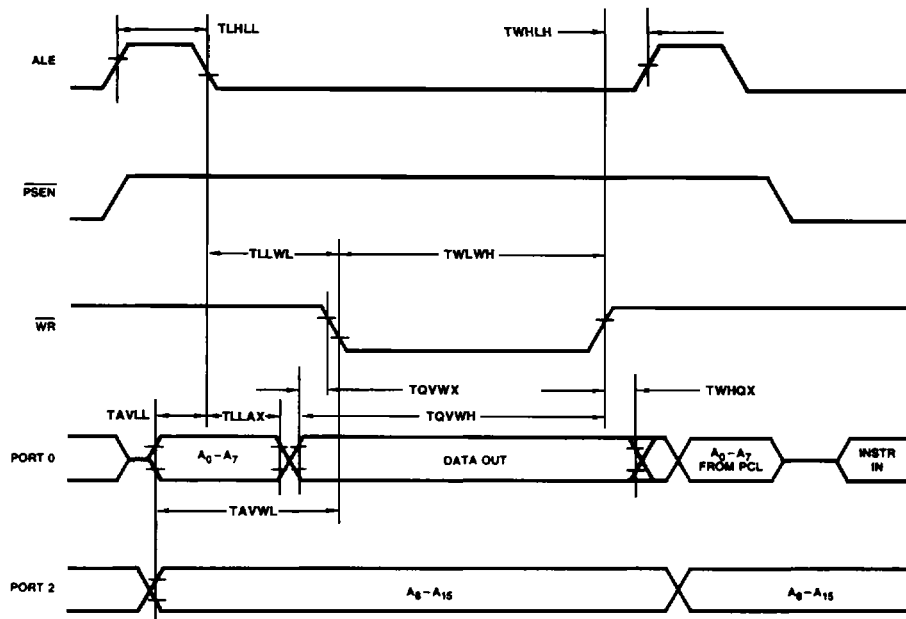
External Program Memory Read Cycle



WF008733

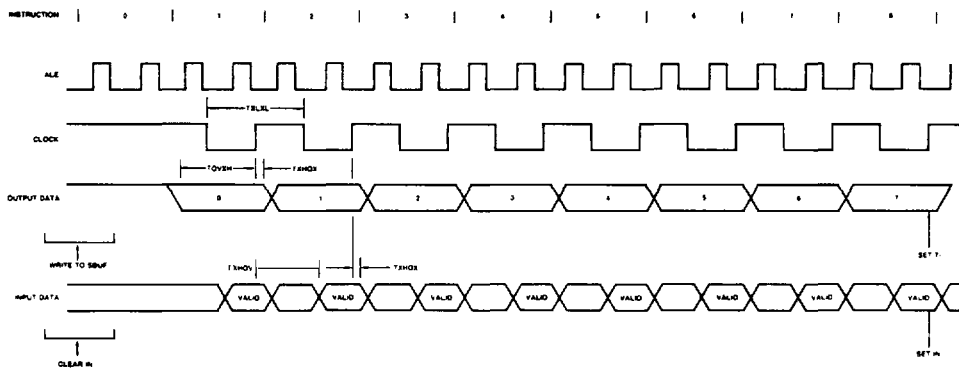
External Data Memory Read Cycle

## SWITCHING WAVEFORMS (Cont'd)



WF008757

External Data Memory Write Cycle

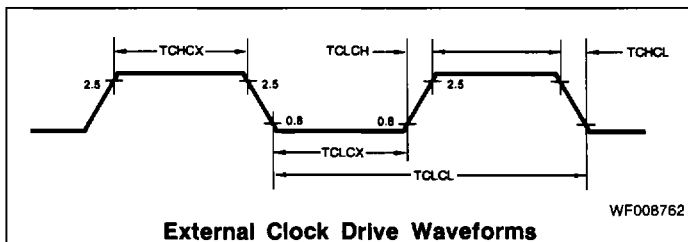


WF008723

Shift Register Timing Waveforms

## EXTERNAL CLOCK DRIVE

| Parameter Symbol | Parameter Description | Min. | Max. | Units |
|------------------|-----------------------|------|------|-------|
| 1/TCLCL          | Oscillator Frequency  | 1.2  | 12   | MHz   |
| TCHCX            | HIGH Time             | 20   |      | ns    |
| TCLCX            | LOW Time              | 20   |      | ns    |
| TCLCH            | Rise Time             |      | 20   | ns    |
| TCHCL            | Fall Time             |      | 20   | ns    |



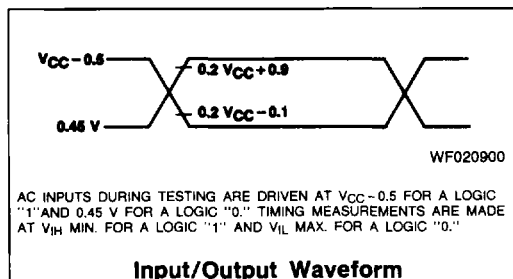
External Clock Drive Waveforms

## SERIAL PORT TIMING — SHIFT REGISTER MODE

(Load Capacitance = 80 pF)

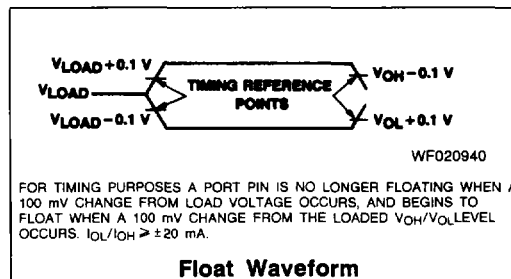
| Parameter Symbol | Parameter Description                    | 12 MHz Osc. |      | Variable Oscillator |             | Units   |
|------------------|------------------------------------------|-------------|------|---------------------|-------------|---------|
|                  |                                          | Min.        | Max. | Min.                | Max.        |         |
| TXLXL            | Serial Port Clock Cycle Time             | 1.0         |      | 12TCLCL             |             | $\mu$ s |
| TQVXH            | Output Data Setup to Clock Rising Edge   | 700         |      | 10TCLCL-133         |             | ns      |
| TXHQX            | Output Data Hold After Clock Rising Edge | 50          |      | 2TCLCL-117          |             | ns      |
| TXHDX            | Input Data Hold After Clock Rising Edge  | 0           |      | 0                   |             | ns      |
| TXHDV            | Clock Rising Edge to Input Data Valid    |             | 700  |                     | 10TCLCL-133 | ns      |

## AC Testing



AC INPUTS DURING TESTING ARE DRIVEN AT  $V_{CC} - 0.5$  FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT  $V_{IH}$  MIN. FOR A LOGIC "1" AND  $V_{IL}$  MAX. FOR A LOGIC "0."

Input/Output Waveform



FOR TIMING PURPOSES A PORT PIN IS NO LONGER FLOATING WHEN A 100 mV CHANGE FROM LOAD VOLTAGE OCCURS, AND BEGINS TO FLOAT WHEN A 100 mV CHANGE FROM THE LOADED  $V_{OH}/V_{OL}$  LEVEL OCCURS.  $I_{OL}/I_{OH} \geq \pm 20$  mA.

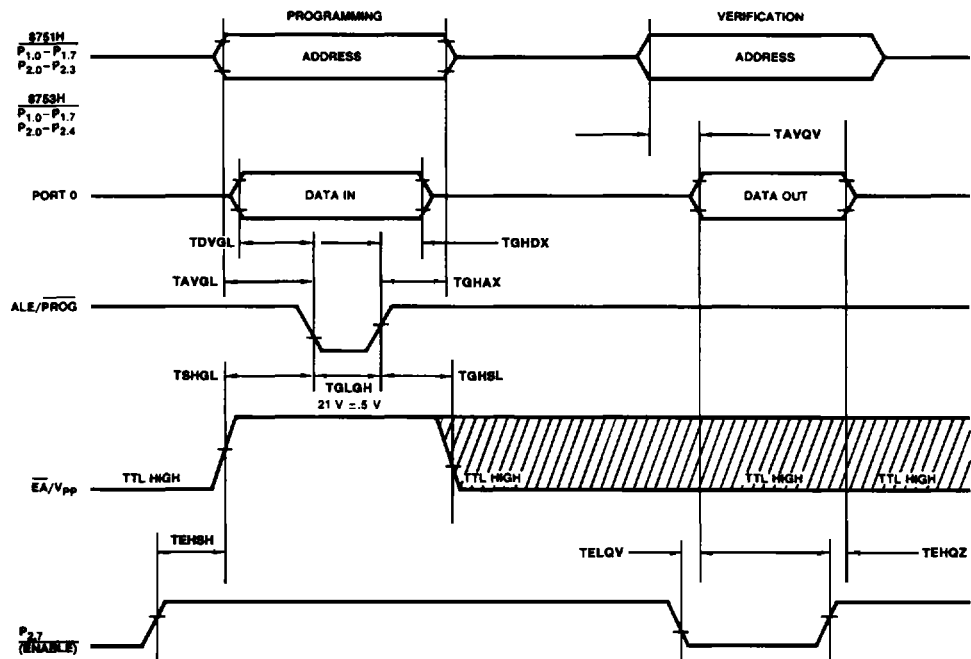
Float Waveform

## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

( $T_A = +21$  to  $+27^\circ\text{C}$ ,  $V_{CC} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )

| Parameter Symbol | Parameter Description                      | Min.    | Max.    | Units           |
|------------------|--------------------------------------------|---------|---------|-----------------|
| $V_{pp}$         | Programming Supply Voltage                 | 20.5    | 21.5    | V               |
| $I_{pp}$         | Programming Supply Current                 |         | 30      | mA              |
| $1/\text{TCLCL}$ | Oscillator Frequency                       | 4       | 6       | MHz             |
| TAVGL            | Address Setup to PROG                      | 48TCLCL |         |                 |
| TGHAX            | Address Hold After PROG                    | 48TCLCL |         |                 |
| TDVGL            | Data Setup to PROG                         | 48TCLCL |         |                 |
| TGHDX            | Data Hold After PROG                       | 48TCLCL |         |                 |
| TEHSH            | P <sub>2.7</sub> (ENABLE) HIGH to $V_{pp}$ | 48TCLCL |         |                 |
| TSHGL            | $V_{pp}$ Setup to PROG                     | 10      |         | $\mu\text{sec}$ |
| TGHSL            | $V_{pp}$ Hold after PROG                   | 10      |         | $\mu\text{sec}$ |
| TGLGH            | PROG Width                                 | 45      | 55      | msec            |
| TAVQV            | Address to Data Valid                      |         | 48TCLCL |                 |
| TELQV            | ENABLE to Data Valid                       |         | 48TCLCL |                 |
| TEHQZ            | Data Float After ENABLE                    | 0       | 48TCLCL |                 |

### EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



WF008713

For Programming conditions, see Figures 1, 2, and 3.

For Verification conditions, see Figures 4 and 5.

For Security Bit Programming, see Figure 6.