32-Bit

Microcontroller

TC212 / TC213 / TC214 / TC222 / TC223 / TC224

32-Bit Single-Chip Micocontroller
AC-Step

32-Bit Single-Chip Micocontroller

Data Sheet

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
V 1.0, 2017-09	
	The history is documented in the last chapter

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1 Summary of Features

The TC22x / TC21x product family has the following features:

- High Performance Microcontroller with one CPU core
- Power Efficient scalar TriCore CPU (TC1.6E), having the following features:
  - Binary code compatibility with TC1.6P
  - 133 MHz operation at full temperature range
  - 88 Kbyte Data Scratch-Pad RAM (DSPR)
  - 8 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 8 Kbyte Instruction Cache (ICACHE)
  - 4 line read buffer (DRB)
- Lockstepped shadow core for TC1.6E
- Multiple on-chip memories
  - All embedded NVM and SRAM are ECC protected
  - 1 Mbyte Program Flash Memory (PFLASH)
  - 96 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - BootROM (BROM)
- 16-Channel DMA Controller with safe data transfer
- Sophisticated interrupt system (ECC protected)
- High performance on-chip bus structure
  - 64-bit Cross Bar Interconnect (SRI) giving fast parallel access between bus masters, CPUs and memories
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Safety Management Unit (SMU) handling safety monitor alarms
- Memory Test Unit with ECC, Memory Initialization and MBIST functions (MTU)
- Hardware I/O Monitor (IOM) for checking of digital I/O
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASCLIN) with hardware LIN support (V1.3, V2.0, V2.1 and J2602) up to 50 MBaud
  - Four Queued SPI Interface Channels (QSPI) with master and slave capability up to 50 Mbit/s
  - One MultiCAN+ Module with 3 CAN nodes each and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - 4 Single Edge Nibble Transmission (SENT) channels for connection to sensors
  - One Generic Timer Module (GTM) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One Capture / Compare 6 module (Two kernels CCU60 and CCU61)
  - One General Purpose 12 Timer Unit (GPT120)
- Versatile Successive Approximation ADC (VADC)
  - Cluster of 2 independent ADC kernels
  - Input voltage range from 0 V to 5.5V (ADC supply)
- Digital programmable I/O ports
- On-chip debug support for OCDS Level 1 (CPUs, DMA, On Chip Buses)
- Four/five wire JTAG (IEEE 1149.1) or DAP (Device Access Port) interface

- Power Management System and on-chip regulators
- Clock Generation Unit with System PLL
- Embedded Voltage Regulator

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC212 / TC213 / TC214 / TC222 / TC223 / TC224 please refer to the **“AURIX™ TC2x Data Sheet Addendum”**, which summarizes all available variants.

Table 1-1 Overview of TC21x / TC22x Functions

Feature		
CPU Core	Type	TC1.6E
	E Cores / Checker Cores	1 / 1
	Max. Freq.	133 MHz
	FPU	yes
Program Flash	Size	1 Mbyte
Data Flash	Size	96 Kbyte
Cache	Instruction	8 Kbyte
	Data	4 line read buffer
SRAM	Size TC1.6E (DSPR/PSPR)	88 Kbyte / 8 Kbyte [1]
DMA	Channels	16
ADC	Channels	12+12
	Converter	2
GTM	TIM	1
	TOM	2
	DTM	2
	CMU / ICM	1 / 1
	TBU	1
Timer	GPT12	1
	CCU6	1
STM	Modules	1
CAN	Modules	1
	Nodes per Module	3
	Message Objects	128
	CAN FD	yes
QSPI	Channels	4
ASCLIN	Interfaces	2
SENT	Channels	4
ASIL	Level	up to ASIL-D

Table 1-1 Overview of TC21x / TC22x Functions

Feature		
Safety support	SMU	1
	IOM	1
FFT		0
HSIC	Channels	2
Embedded Voltage Regulator	LDO from 3.3 V to 1.3 V	Yes
Low Power Feature	Standby RAM	Yes
Packages	Type	PG-TQFP-80-7 / PG-TQFP-100-23 / PG-TQFP-144-27
I/O	Type	3.3 V CMOS (5V input supported on ADC pins)
$T_{ambient}$	Range	−40 … +125°C / +150°C

1) To ensure the processor cores are provided with a constant stream of instructions the Instruction Fetch Units will speculatively fetch instructions from the up to 64 bytes ahead of the current PC.
If the current PC is within 64 bytes of the top of an instruction memory the Instruction Fetch Unit may attempt to speculatively fetch instruction from beyond the physical range. This may then lead to error conditions and alarms being triggered by the bus and memory systems.
It is therefore recommended that the upper 64 bytes of any memory be unused for instruction storage.

2 Package and Pinning Definitions

This chapter gives a pinning of the different packages of the TC212 / TC213 / TC214 / TC222 / TC223 / TC224.

2.1 PG-TQFP-80-7 Package Variant Pin Configuration of TC212 / TC222

Figure 2-1 is showing the TC212 / TC222 pinout for the package variant PG-TQFP-80-7.

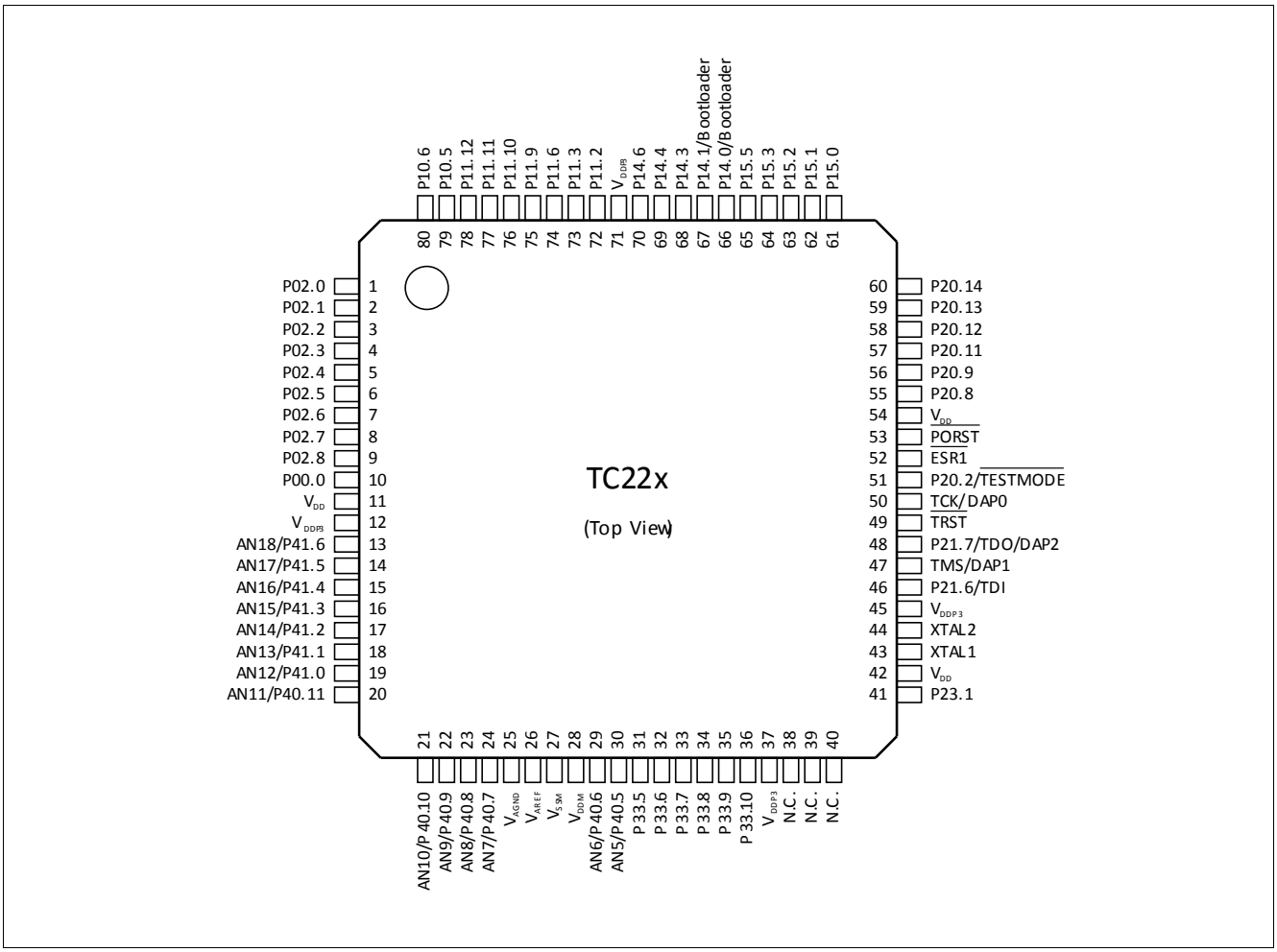


Figure 2-1 TC212 / TC222 Pinout for the package variant PG-TQFP-80-7

2.1.1 Port Functions and Pinning Tables

2.1.1.1 How to Read the Following Port Function Tables

Some hints for interpreting the following tables.

Column “Ctrl.”:

I = Input (for GPIO port Lines with IOCR bit field Selection PCx = $0XXX_B$)

AI = Analog input

O = Output
O0 = Output with IOCR bit field selection PCx = $1X000_B$
O1 = Output with IOCR bit field selection PCx = $1X001_B$ (ALT1)
O2 = Output with IOCR bit field selection PCx = $1X010_B$ (ALT2)
O3 = Output with IOCR bit field selection PCx = $1X011_B$ (ALT3)
O4 = Output with IOCR bit field selection PCx = $1X100_B$ (ALT4)
O5 = Output with IOCR bit field selection PCx = $1X101_B$ (ALT5)
O6 = Output with IOCR bit field selection PCx = $1X110_B$ (ALT6)
O7 = Output with IOCR bit field selection PCx = $1X111_B$ (ALT7)

Table 2-1 Example Port Table

Pin	Symbol	Ctrl.	Buffer Type	Function
10	Pxx.y	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIMm_n			**GTM_TIN**
	TOMa_b	O1		**GTM_TOUT**
	TOMc_d			**GTM_TOUT**
	IOM_REFv_w			**IOM reference input**
	ASCLINz_RTS	O2		**ASCLIN0 output (aka ARTSz)**

To each input several functions can be connected. The peripherals’ configuration defines if this input is used.

The port module (see corresponding chapter) decides which of the 8 output signals O0 to O7 drives the pad.

Some Ox rows list more than one function, e.g. several GTM_TOUT outputs and IOM reference inputs. The GTM module (see corresponding chapter) has its own sub-multiplexer structure that defines which of the GTM sub-units drives this signal. Additionally the IOM modules “listens” on these output signals (see IOM chapter).

Some pin symbol names were changed in this AURIX device compared to other AURIX devices to improve naming systematics. The previously used symbol name is documented in the “Function” column with the text “(aka …)”[1].

Column “Type”:

IN = Input only
A1 = Pad class A1 (3.3V)
A1+ = Pad class A1+ (3.3V)
S = ADC with digital input. Pad class D for analog input “AI”, pad class S for digital input “I”.
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)

1) “aka” as abbreviation for “also known as”.

High-Z = High-Z during reset ($\overline{\text{PORST}}$ = 0)
V_x = Supply (the Exposed Pad is also considered as VSS and shall be connected to ground)

2.1.1.2 Tables

Port function and pinning tables.

Table 2-2 Port 00 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
10	P00.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	CCU61_CTRAPA			**CCU61 input**
	CCU60_T12HRE			**CCU60 input**
	P00.0	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_REF0_9			**IOM reference input**
	ASCLIN0_SCLK	O2		**ASCLIN0 output (aka: ASCLK0)**
	ASCLIN0_TX	O3		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**

Table 2-3 Port 02 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	SCU_REQ6			**SCU input**
	CCU60_CC60INA			**CCU60 input**
	CCU61_CC60INB			**CCU61 input**
	P02.0	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_8			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_REF0_0			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO1	O3		**QSPI3 output (aka: SLSO31)**
	—	O4		**Reserved**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-3 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	CAN0_RXDA			**CAN node 0 input (aka: RXDCAN0A)**
	SCU_REQ14			**SCU input**
	P02.1	O0		**General-purpose output**
	TOM0_9	O1		**GTM_TOUT**
	TOM1_9			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_REF0_1			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**QSPI3 output (aka: SLSO32)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**CCU60 output**
	IOM_MON1_3			**IOM monitor input**
	IOM_REF1_3			**IOM reference input**

Table 2-3 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	CCU60_CC61INA			**CCU60 input**
	CCU61_CC61INB			**CCU61 input**
	P02.2	O0		**General-purpose output**
	TOM0_10	O1		**GTM_TOUT**
	TOM1_10			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_REF0_2			**IOM reference input**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI3_SLSO3	O3		**QSPI3 output (aka: SLSO33)**
	—	O4		**Reserved**
	CAN2_TXD	O5		**CAN node 2 output (aka: TXDCAN2)**
	IOM_MON2_7			**IOM monitor input**
	IOM_REF2_7			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-3 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	ASCLIN1_RXG			**ASCLIN1 input (aka: ARX1G)**
	CAN2_RXDB			**CAN node 2 input (aka: RXDCAN2B)**
	P02.3	O0		**General-purpose output**
	TOM0_11	O1		**GTM_TOUT**
	TOM1_11			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_REF0_3			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO4	O3		**QSPI3 output (aka: SLSO34)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**CCU60 output**
	IOM_MON1_4			**IOM monitor input**
	IOM_REF1_2			**IOM reference input**
5	P02.4	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	QSPI3_SLSIA			**QSPI3 input (aka: SLSI3A)**
	CAN0_RXDD			**CAN node 0 input (aka: RXDCAN0D)**
	CCU60_CC62INA			**CCU60 input**
	CCU61_CC62INB			**CCU61 input**
	P02.4	O0		**General-purpose output**
	TOM0_12	O1		**GTM_TOUT**
	TOM1_12			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_REF0_4			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO0	O3		**QSPI3 output (aka: SLSO30)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**

Table 2-3 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_5			**GTM_TIN**
	QSPI3_MRSTA			**QSPI3 input (aka: MRST3A)**
	SENT_SENT3C			**SENT input**
	P02.5	O0		**General-purpose output**
	TOM0_13	O1		**GTM_TOUT**
	TOM1_13			**GTM_TOUT**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_REF0_5			**IOM reference input**
	CAN0_TXD	O2		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	QSPI3_MRST	O3		**QSPI3 output (aka: MRST3)**
	IOM_MON2_3			**IOM monitor input**
	IOM_REF2_3			**IOM reference input**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**

Table 2-3 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	QSPI3_MTSRA			**QSPI3 input (aka: MTSR3A)**
	SENT_SENT2C			**SENT input**
	CCU60_CC60INC			**CCU60 input**
	CCU60_CCPOS0A			**CCU60 input**
	CCU61_T12HRB			**CCU61 input**
	GPT120_T3INA			**GPT120 input**
	P02.6	O0		**General-purpose output**
	TOM0_14	O1		**GTM_TOUT**
	TOM1_14			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_REF0_6			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**QSPI3 output (aka: MTSR3)**
	—	O4		**Reserved**
	VADC_EMUX00	O5		**VADC output**
	—	O6		**Reserved**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-3 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	QSPI3_SCLKA			**QSPI3 input (aka: SCLK3A)**
	SENT_SENT1C			**SENT input**
	CCU60_CC61INC			**CCU60 input**
	CCU60_CCPOS1A			**CCU60 input**
	CCU61_T13HRB			**CCU61 input**
	GPT120_T3EUDA			**GPT120 input**
	PMU_FDEST			**PMU input**
	P02.7	O0		**General-purpose output**
	TOM0_15	O1		**GTM_TOUT**
	TOM1_15			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_REF0_7			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**QSPI3 output (aka: SCLK3)**
	—	O4		**Reserved**
	VADC_EMUX01	O5		**VADC output**
	SENT_SPC1	O6		**SENT output**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-3 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	SENT_SENT0C			**SENT input**
	CCU60_CC62INC			**CCU60 input**
	CCU60_CCPOS2A			**CCU60 input**
	CCU61_T12HRC			**CCU61 input**
	CCU61_T13HRC			**CCU61 input**
	GPT120_T4INA			**GPT120 input**
	P02.8	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_REF0_8			**IOM reference input**
	QSPI3_SLSO5	O2		**QSPI3 output (aka: SLSO35)**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_EMUX02	O5		**VADC output**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**

Table 2-4 Port 10 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
79	P10.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	SCU_HWCFG4			**SCU input**
	P10.5	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_10			**GTM_TOUT**
	IOM_REF2_9			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO8	O3		**QSPI3 output (aka: SLSO38)**
	QSPI1_SLSO9	O4		**QSPI1 output (aka: SLSO19)**
	GPT120_T6OUT	O5		**GPT120 output**
	—	O6		**Reserved**
	—	O7		**Reserved**
80	P10.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	QSPI3_MTSRB			**QSPI3 input (aka: MTSR3B)**
	SCU_HWCFG5			**SCU input**
	P10.6	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_11			**GTM_TOUT**
	IOM_REF2_10			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**QSPI3 output (aka: MTSR3)**
	GPT120_T3OUT	O4		**GPT120 output**
	—	O5		**Reserved**
	QSPI1_MRST	O6		**QSPI1 output (aka: MRST1)**
	IOM_MON2_1			**IOM monitor input**
	IOM_REF2_1			**IOM reference input**
	—	O7		**Reserved**

Table 2-5 Port 11 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
72	P11.2	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.2	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**QSPI0 output (aka: SLSO05)**
	QSPI1_SLSO5	O4		**QSPI1 output (aka: SLSO15)**
	CCU61_COUT63	O5		**CCU61 output**
	IOM_MON1_7			**IOM monitor input**
	IOM_REF1_7			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**
73	P11.3	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_MRSTB			**QSPI1 input (aka: MRST1B)**
	P11.3	O0		**General-purpose output**
	TOM0_10	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**QSPI1 output (aka: MRST1)**
	IOM_MON2_1			**IOM monitor input**
	IOM_REF2_1			**IOM reference input**
	—	O4		**Reserved**
	CCU61_COUT62	O5		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**

Table 2-5 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P11.6	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_SCLKB			**QSPI1 input (aka: SCLK1B)**
	P11.6	O0		**General-purpose output**
	TOM0_11	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**QSPI1 output (aka: SCLK1)**
	—	O4		**Reserved**
	CCU61_COUT61	O5		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**CCU60 output**
	IOM_MON1_4			**IOM monitor input**
	IOM_REF1_2			**IOM reference input**
75	P11.9	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_MTSRB			**QSPI1 input (aka: MTSR1B)**
	P11.9	O0		**General-purpose output**
	TOM0_12	O1		**GTM_TOUT**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**QSPI1 output (aka: MTSR1)**
	—	O4		**Reserved**
	CCU61_COUT60	O5		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**CCU60 output**
	IOM_MON1_3			**IOM monitor input**
	IOM_REF1_3			**IOM reference input**

Table 2-5 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P11.10	I	A1+ / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXE			**ASCLIN1 input (aka: ARX1E)**
	SCU_REQ12			**SCU input**
	P11.10	O0		**General-purpose output**
	TOM0_13	O1		**GTM_TOUT**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**QSPI0 output (aka: SLSO03)**
	QSPI1_SLSO3	O4		**QSPI1 output (aka: SLSO13)**
	CCU61_CC62	O5		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**
77	P11.11	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.11	O0		**General-purpose output**
	TOM0_14	O1		**GTM_TOUT**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**QSPI0 output (aka: SLSO04)**
	QSPI1_SLSO4	O4		**QSPI1 output (aka: SLSO14)**
	CCU61_CC61	O5		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-5 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
78	P11.12	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.12	O0		**General-purpose output**
	TOM0_15	O1		**GTM_TOUT**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	GTM_CLK2	O3		**GTM output**
	—	O4		**Reserved**
	CCU61_CC60	O5		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**
	SCU_EXTCLK1	O6		**SCU output**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-6 Port 14 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
66	P14.0	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	P14.0	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	ASCLIN0_SCLK	O6		**ASCLIN0 output (aka: ASCLK0)**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**

Table 2-6 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
67	P14.1	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	ASCLIN0_RXA			**ASCLIN0 input (aka: ARX0A)**
	CAN1_RXDB			**CAN node 1 input (aka: RXDCAN1B)**
	SCU_REQ15			**SCU input**
	SCU_EVRWUPA	AI		**SCU input**
	P14.1	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_REF1_14			**IOM reference input**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**
68	P14.3	I	A1 / PU / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	SCU_REQ10			**SCU input**
	SCU_HWCFG3_BMI			**SCU input**
	P14.3	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_REF2_4			**IOM reference input**
	—	O2		**Reserved**
	QSPI2_SLSO3	O3		**QSPI2 output (aka: SLSO23)**
	ASCLIN1_SLSO	O4		**ASCLIN1 output (aka: ASLSO1)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-6 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
69	P14.4	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	P14.4	O0		**General-purpose output**
	TOM0_7	O1		**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_REF2_8			**IOM reference input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
70	P14.6	I	A1+ / PU / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI0_MRSTD			**QSPI0 input (aka: MRST0D)**
	P14.6	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	IOM_REF2_14			**IOM reference input**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**QSPI2 output (aka: SLSO22)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-7 Port 15 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
61	P15.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	P15.0	O0		**General-purpose output**
	TOM1_3	O1		**GTM_TOUT**
	TOM0_11			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI0_SLSO13	O3		**QSPI0 output (aka: SLSO013)**
	—	O4		**Reserved**
	CAN2_TXD	O5		**CAN node 2 output (aka: TXDCAN2)**
	IOM_MON2_7			**IOM monitor input**
	IOM_REF2_7			**IOM reference input**
	ASCLIN1_SCLK	O6		**ASCLIN1 output (aka: ASCLK1)**
	—	O7		**Reserved**
62	P15.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXA			**ASCLIN1 input (aka: ARX1A)**
	QSPI2_SLSIB			**QSPI2 input (aka: SLSI2B)**
	CAN2_RXDA			**CAN node 2 input (aka: RXDCAN2A)**
	SCU_REQ16			**SCU input**
	SCU_EVRWUPB	AI		**SCU input**
	P15.1	O0		**General-purpose output**
	TOM1_4	O1		**GTM_TOUT (= DTM5_OUT4)**
	TOM0_12			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI2_SLSO5	O3		**QSPI2 output (aka: SLSO25)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-7 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
63	P15.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI2_MRSTE			**QSPI2 input (aka: MRST2E)**
	QSPI2_SLSIA			**QSPI2 input (aka: SLSI2A)**
	QSPI2_HSICINA			**QSPI2 input (aka: HSIC2INA)**
	P15.2	O0		**General-purpose output**
	TOM1_5	O1		**GTM_TOUT (= DTM5_OUT5)**
	TOM0_13			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	QSPI2_SLSO0	O3		**QSPI2 output (aka: SLSO20)**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	ASCLIN0_SCLK	O6		**ASCLIN0 output (aka: ASCLK0)**
	—	O7		**Reserved**
64	P15.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN0_RXB			**ASCLIN0 input (aka: ARX0B)**
	QSPI2_SCLKA			**QSPI2 input (aka: SCLK2A)**
	QSPI2_HSICINB			**QSPI2 input (aka: HSIC2INB)**
	CAN1_RXDA			**CAN node 1 input (aka: RXDCAN1A)**
	P15.3	O0		**General-purpose output**
	TOM1_6	O1		**GTM_TOUT (= DTM5_OUT6)**
	TOM0_14			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	QSPI2_SCLK	O3		**QSPI2 output (aka: SCLK2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-7 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
65	P15.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXB			**ASCLIN1 input (aka: ARX1B)**
	QSPI2_MTSRA			**QSPI2 input (aka: MTSR2A)**
	SCU_REQ13			**SCU input**
	P15.5	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI2_MTSR	O3		**QSPI2 output (aka: MTSR2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-8 Port 20 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
51	P20.2	I	Input Only / PU / VDDP3	**General-purpose input**
	$\overline{\text{TESTMODE}}$			**Factory Test Mode Enable**

Table 2-8 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
55	P20.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	P20.8	O0		**General-purpose output**
	TOM1_7	O1		**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_MON2_8			**IOM monitor input**
	ASCLIN1_SLSO	O2		**ASCLIN1 output (aka: ASLSO1)**
	QSPI0_SLSO0	O3		**QSPI0 output (aka: SLSO00)**
	QSPI1_SLSO0	O4		**QSPI1 output (aka: SLSO10)**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	SCU_WDT0LCK	O6		**SCU output**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**
56	P20.9	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXC			**ASCLIN1 input (aka: ARX1C)**
	QSPI0_SLSIB			**QSPI0 input (aka: SLSI0B)**
	SCU_REQ11			**SCU input**
	P20.9	O0		**General-purpose output**
	TOM1_13	O1		**GTM_TOUT**
	TOM0_13			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_MON2_11			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**QSPI0 output (aka: SLSO01)**
	QSPI1_SLSO1	O4		**QSPI1 output (aka: SLSO11)**
	—	O5		**Reserved**
	SCU_WDTSLCK	O6		**SCU output**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**

Table 2-8 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
57	P20.11	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_SCLKA			**QSPI0 input (aka: SCLK0A)**
	P20.11	O0		**General-purpose output**
	TOM1_15	O1		**GTM_TOUT**
	TOM0_15			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_MON2_15			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**QSPI0 output (aka: SCLK0)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**
58	P20.12	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI0_MRSTA			**QSPI0 input (aka: MRST0A)**
	IOM_PIN13			**IOM pad input**
	P20.12	O0		**General-purpose output**
	TOM1_0	O1		**GTM_TOUT**
	TOM0_8			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_MON0_13			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**QSPI0 output (aka: MRST0)**
	IOM_MON2_0			**IOM monitor input**
	IOM_REF2_0			**IOM reference input**
	QSPI0_MTSR	O4		**QSPI0 output (aka: MTSR0)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**

Table 2-8 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
59	P20.13	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_SLSIA			**QSPI0 input (aka: SLSI0A)**
	IOM_PIN14			**IOM pad input**
	P20.13	O0		**General-purpose output**
	TOM1_1	O1		**GTM_TOUT**
	TOM0_9			**GTM_TOUT**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_MON0_14			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**QSPI0 output (aka: SLSO02)**
	QSPI1_SLSO2	O4		**QSPI1 output (aka: SLSO12)**
	QSPI0_SCLK	O5		**QSPI0 output (aka: SCLK0)**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**
60	P20.14	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_MTSRA			**QSPI0 input (aka: MTSR0A)**
	IOM_PIN15			**IOM pad input**
	P20.14	O0		**General-purpose output**
	TOM1_2	O1		**GTM_TOUT**
	TOM0_10			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_MON0_15			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**QSPI0 output (aka: MTSR0)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-9 Port 21 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
46	P21.6	I	A1 / PU / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	TDI			**OCDS input**
	$\overline{\text{OCDS\_TGI2}}$			**OCDS input**
	GPT120_T5EUDA			**GPT120 input**
	P21.6	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**GPT120 output**
	$\overline{\text{OCDS\_TGO2}}$	O		**OCDS**
48	P21.7	I	A1+ / PU / VDDP3	**General-purpose input**
	TIM0_5			**GTM_TIN**
	OCDS_DAP2			**OCDS input**
	$\overline{\text{OCDS\_TGI3}}$			**OCDS input**
	GPT120_T5INA			**GPT120 input**
	P21.7	O0		**General-purpose output**
	TOM0_5	O1		**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**GPT120 output**
	$\overline{\text{OCDS\_TGO3}}$	O		**OCDS**
	OCDS_DAP2	O		**OCDS Output**
	TDO	O		**JTAG Output**

Table 2-10 Port 23 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
41	P23.1	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	P23.1	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM0_15			**GTM_TOUT**
	ASCLIN1_RTS	O2		**ASCLIN1 output (aka: ARTS1)**
	QSPI3_SLSO13	O3		**QSPI3 output (aka: SLSO313)**
	GTM_CLK0	O4		**GTM output**
	SCU_EXTCLK1	O5		**SCU output**
	SCU_EXTCLK0	O6		**SCU output**
	—	O7		**Reserved**

Table 2-11 Port 33 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
31	P33.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	CCU61_CCPOS2C			**CCU61 input**
	GPT120_T4EUDB			**GPT120 input**
	IOM_PIN5			**IOM pad input**
	P33.5	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_MON0_5			**IOM monitor input**
	QSPI0_SLSO7	O2		**QSPI0 output (aka: SLSO07)**
	QSPI1_SLSO7	O3		**QSPI1 output (aka: SLSO17)**
	—	O4		**Reserved**
	VADC_EMUX11	O5		**VADC output**
	VADC_G0BFL1	O6		**VADC output**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**

Table 2-11 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
32	P33.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	ASCLIN1_RXF			**ASCLIN1 input (aka: ARX1F)**
	CCU61_CCPOS1C			**CCU61 input**
	GPT120_T2EUDB			**GPT120 input**
	IOM_PIN6			**IOM pad input**
	P33.6	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_MON0_6			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	ASCLIN1_TX	O4		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	VADC_EMUX10	O5		**VADC output**
	VADC_G0BFL2	O6		**VADC output**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**

Table 2-11 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
33	P33.7	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	CAN0_RXDE			**CAN node 0 input (aka: RXDCAN0E)**
	SCU_REQ8			**SCU input**
	CCU61_CCPOS0C			**CCU61 input**
	GPT120_T2INB			**GPT120 input**
	IOM_PIN7			**IOM pad input**
	P33.7	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_MON0_7			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO7	O3		**QSPI3 output (aka: SLSO37)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	VADC_G0BFL3	O6		**VADC output**
	CCU61_COUT60	O7		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**

Table 2-11 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
34	P33.8	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	SCU_EMGSTOPA			**SCU input**
	IOM_PIN8			**IOM pad input**
	P33.8	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_MON0_8			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**QSPI3 output (aka: SLSO32)**
	—	O4		**Reserved**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**
	SMU_FSP	O		**SMU**

Table 2-11 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
35	P33.9	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI3_HSICINA			**QSPI3 input (aka: HSIC3INA)**
	IOM_PIN9			**IOM pad input**
	P33.9	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_MON0_9			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO1	O3		**QSPI3 output (aka: SLSO31)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC62	O7		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**
36	P33.10	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	QSPI3_SLSIC			**QSPI3 input (aka: SLSI3C)**
	QSPI3_HSICINB			**QSPI3 input (aka: HSIC3INB)**
	IOM_PIN10			**IOM pad input**
	P33.10	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_MON0_10			**IOM monitor input**
	QSPI1_SLSO6	O2		**QSPI1 output (aka: SLSO16)**
	QSPI3_SLSO11	O3		**QSPI3 output (aka: SLSO311)**
	ASCLIN1_SLSO	O4		**ASCLIN1 output (aka: ASLSO1)**
	GTM_CLK1	O5		**GTM output**
	SCU_EXTCLK1	O6		**SCU output**
	CCU61_COUT61	O7		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**

Table 2-12 Port 40 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
30	P40.5	I	S / VDDM	**General-purpose input**
	VADCG0_5	AI		**VADC input channel 5 of group 0**
29	P40.6	I	S / VDDM	**General-purpose input**
	VADCG0_6	AI		**VADC input channel 6 of group 0**
24	P40.7	I	S / VDDM	**General-purpose input**
	VADCG0_7	AI		**VADC input channel 7 of group 0** (with pull down diagnostics)
23	P40.8	I	S / VDDM	**General-purpose input**
	VADCG0_8	AI		**VADC input channel 8 of group 0**
22	P40.9	I	S / VDDM	**General-purpose input**
	VADCG0_9	AI		**VADC input channel 9 of group 0** (with multiplexer diagnostics)
21	P40.10	I	S / VDDM	**General-purpose input**
	VADCG0_10	AI		**VADC input channel 10 of group 0** (with multiplexer diagnostics)
20	P40.11	I	S / VDDM	**General-purpose input**
	SENT_SENT0A			**SENT input**
	CCU60_CCPOS0D			**CCU60 input**
	VADCG0_11	AI		**VADC input channel 11 of group 0**

Table 2-13 Port 41 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
19	P41.0	I	S / VDDM	**General-purpose input**
	SENT_SENT1A			**SENT input**
	CCU60_CCPOS1B			**CCU60 input**
	VADCG1_0	AI		**VADC input channel 0 of group 1**
18	P41.1	I	S / VDDM	**General-purpose input**
	VADCG1_1	AI		**VADC input channel 1 of group 1** (with multiplexer diagnostics)
17	P41.2	I	S / VDDM	**General-purpose input**
	SENT_SENT2A			**SENT input**
	CCU61_CCPOS1B			**CCU61 input**
	VADCG1_2	AI		**VADC input channel 2 of group 1** (with multiplexer diagnostics)

Table 2-13 Port 41 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
16	P41.3	I	S / VDDM	**General-purpose input**
	SENT_SENT3A			**SENT input**
	CCU61_CCPOS1D			**CCU61 input**
	VADCG1_3	AI		**VADC input channel 3 of group 1** (with pull down diagnostics)
15	P41.4	I	S / VDDM	**General-purpose input**
	VADCG1_4	AI		**VADC input channel 4 of group 1**
14	P41.5	I	S / VDDM	**General-purpose input**
	VADCG1_5	AI		**VADC input channel 5 of group 1**
13	P41.6	I	S / VDDM	**General-purpose input**
	VADCG1_6	AI		**VADC input channel 6 of group 1**

Table 2-14 System I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
43	XTAL1	I	VDDP3	**Main Oscillator/PLL/Clock Generator Input**
44	XTAL2	O	VDDP3	**Main Oscillator/PLL/Clock Generator Output**
47	TMS/DAP1	I	A1+ / PD / VDDP3	**Debug Interface**
	DAP1	I/O		**Device Access Port LIne 1**
49	$\overline{\text{TRST}}$	I	Input Only / PD / VDDP3	**JTAG Module Reset/Enable Input**
50	TCK/DAP0	I	Input Only / PD / VDDP3	**OCDS input**
	DAP0	I		**Device Access Port LIne 0**
52	$\overline{\text{ESR1}}$	I/O	A1+ / PU / VDDP3	**SCU input**
	EVRWUP	I		**EVR Wakeup Pin**
53	$\overline{\text{PORST}}$	I	Input Only / PD / VDDP3	**Power On Reset** Additional strong PD in case of power fail.

Table 2-15 Supply

Pin	Symbol	Ctrl.	Buffer Type	Function
25	V_{AGND}	I	—	**Negative Analog Reference Voltage 0**
26	V_{AREF}	I	—	**Positive Analog Reference Voltage 0**
12	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)**
11	V_{DD}	I	—	**Digital Core Power Supply (1.3V)**
27	V_{SSM}	I	—	**Analog Ground for VDDM**

Table 2-15 Supply (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
28	V_{DDM}	I	—	**ADC Power Supply (5.0V)**
37	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)**
42	V_{DD}	I	—	**Digital Core Power Supply (1.3V)** This pin supplies also the main XTAL Oscillator/PLL (1.3V). A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity.
45	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)** This pin supplies also the main XTAL Oscillator/PLL (3.3V). A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity.
54	V_{DD}	I	—	**Digital Core Power Supply (1.3V)**
71	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)** This pin supplies also the Flash 3.3V.

2.1.2 Pull-Up/Pull-Down Reset Behavior of the Pins

Table 2-16 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
$\overline{\text{all GPIOs}}$	High-Z	
$\overline{\text{TDI}}$, $\overline{\text{TESTMODE}}$	Pull-up	
$\overline{\text{PORST}}$[1)]	Pull-down with I_{PORST} relevant	Pull-down with I_{PDLI} relevant
$\overline{\text{TRST}}$, TCK, TMS	Pull-down	
$\overline{\text{ESR0}}$	The open-drain driver is used to drive low.[2)]	Pull-up[3)]
$\overline{\text{ESR1}}$	Pull-up[3)]	
P14.2, P14.3, P14.6	Pull-up	
P21.7 / TDO	Pull-up	High-Z/Pull-up[4)]

1) Pull-down with I_{PORST} relevant is always activated when a primary supply monitor detects a violation.
2) Valid additionally after deactivation of PORST until the internal reset phase has finished. See the SCU chapter for details.
3) See the SCU_IOCR register description.
4) Depends on JTAG/DAP selection with $\overline{\text{TRST}}$.

2.2 PG-TQFP-100-23 Package Variant Pin Configuration of TC213 / TC223

Figure 2-1 is showing the TC213 / TC223 pinout for the package variant: PG-TQFP-100-23.

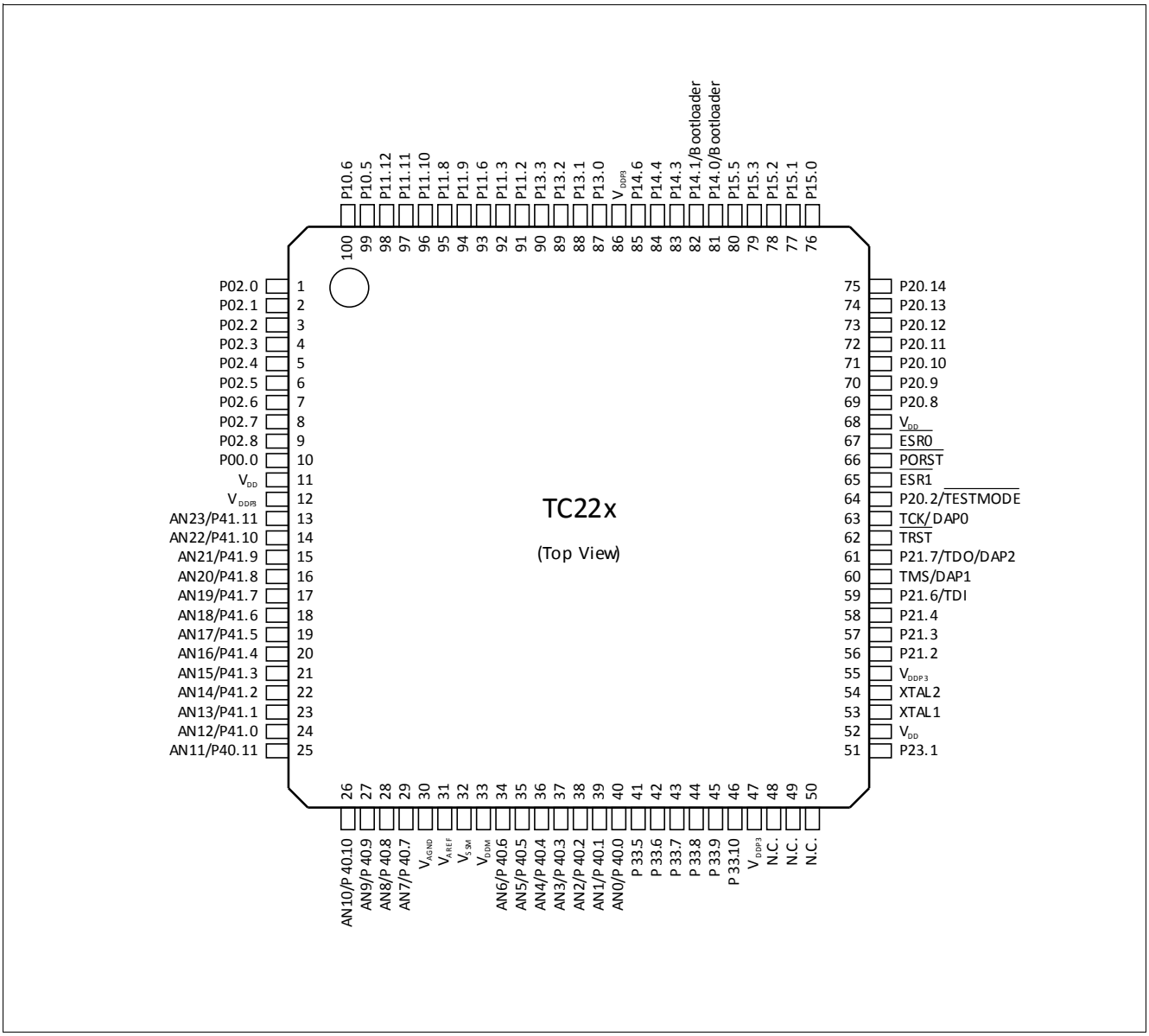


Figure 2-2 TC213 / TC223 Pinout for the package variant: PG-TQFP-100-23.

2.2.1 Port Functions and Pinning Tables

2.2.1.1 How to Read the Following Port Function Tables

Some hints for interpreting the following tables.

Column “Ctrl.”:

I = Input (for GPIO port Lines with IOCR bit field Selection PCx = $0XXX_B$)

AI = Analog input

O = Output
O0 = Output with IOCR bit field selection PCx = $1X000_B$
O1 = Output with IOCR bit field selection PCx = $1X001_B$ (ALT1)
O2 = Output with IOCR bit field selection PCx = $1X010_B$ (ALT2)
O3 = Output with IOCR bit field selection PCx = $1X011_B$ (ALT3)
O4 = Output with IOCR bit field selection PCx = $1X100_B$ (ALT4)
O5 = Output with IOCR bit field selection PCx = $1X101_B$ (ALT5)
O6 = Output with IOCR bit field selection PCx = $1X110_B$ (ALT6)
O7 = Output with IOCR bit field selection PCx = $1X111_B$ (ALT7)

Table 2-17 Example Port Table

Pin	Symbol	Ctrl.	Buffer Type	Function
10	Pxx.y	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIMm_n			**GTM_TIN**
	TOMa_b	O1		**GTM_TOUT**
	TOMc_d			**GTM_TOUT**
	IOM_REFv_w			**IOM reference input**
	ASCLINz_RTS	O2		**ASCLIN0 output (aka ARTSz)**

To each input several functions can be connected. The peripherals’ configuration defines if this input is used.

The port module (see corresponding chapter) decides which of the 8 output signals O0 to O7 drives the pad.

Some Ox rows list more than one function, e.g. several GTM_TOUT outputs and IOM reference inputs. The GTM module (see corresponding chapter) has its own sub-multiplexer structure that defines which of the GTM sub-units drives this signal. Additionally the IOM modules “listens” on these output signals (see IOM chapter).

Some pin symbol names were changed in this AURIX device compared to other AURIX devices to improve naming systematics. The previously used symbol name is documented in the “Function” column with the text “(aka …)”[1].

Column “Type”:

IN = Input only
A1 = Pad class A1 (3.3V)
A1+ = Pad class A1+ (3.3V)
S = ADC with digital input. Pad class D for analog input “AI”, pad class S for digital input “I”.
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)

1) “aka” as abbreviation for “also known as”.

High-Z = High-Z during reset ($\overline{\text{PORST}}$ = 0)
V_x = Supply (the Exposed Pad is also considered as VSS and shall be connected to ground)

2.2.1.2 Tables

Port function and pinning tables.

Table 2-18 Port 00 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
10	P00.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	CCU61_CTRAPA			**CCU61 input**
	CCU60_T12HRE			**CCU60 input**
	P00.0	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_REF0_9			**IOM reference input**
	ASCLIN0_SCLK	O2		**ASCLIN0 output (aka: ASCLK0)**
	ASCLIN0_TX	O3		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**

Table 2-19 Port 02 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	SCU_REQ6			**SCU input**
	CCU60_CC60INA			**CCU60 input**
	CCU61_CC60INB			**CCU61 input**
	P02.0	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_8			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_REF0_0			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO1	O3		**QSPI3 output (aka: SLSO31)**
	—	O4		**Reserved**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-19 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	CAN0_RXDA			**CAN node 0 input (aka: RXDCAN0A)**
	SCU_REQ14			**SCU input**
	P02.1	O0		**General-purpose output**
	TOM0_9	O1		**GTM_TOUT**
	TOM1_9			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_REF0_1			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**QSPI3 output (aka: SLSO32)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**CCU60 output**
	IOM_MON1_3			**IOM monitor input**
	IOM_REF1_3			**IOM reference input**

Table 2-19 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	CCU60_CC61INA			**CCU60 input**
	CCU61_CC61INB			**CCU61 input**
	P02.2	O0		**General-purpose output**
	TOM0_10	O1		**GTM_TOUT**
	TOM1_10			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_REF0_2			**IOM reference input**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI3_SLSO3	O3		**QSPI3 output (aka: SLSO33)**
	—	O4		**Reserved**
	CAN2_TXD	O5		**CAN node 2 output (aka: TXDCAN2)**
	IOM_MON2_7			**IOM monitor input**
	IOM_REF2_7			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-19 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	ASCLIN1_RXG			**ASCLIN1 input (aka: ARX1G)**
	CAN2_RXDB			**CAN node 2 input (aka: RXDCAN2B)**
	P02.3	O0		**General-purpose output**
	TOM0_11	O1		**GTM_TOUT**
	TOM1_11			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_REF0_3			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO4	O3		**QSPI3 output (aka: SLSO34)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**CCU60 output**
	IOM_MON1_4			**IOM monitor input**
	IOM_REF1_2			**IOM reference input**
5	P02.4	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	QSPI3_SLSIA			**QSPI3 input (aka: SLSI3A)**
	CAN0_RXDD			**CAN node 0 input (aka: RXDCAN0D)**
	CCU60_CC62INA			**CCU60 input**
	CCU61_CC62INB			**CCU61 input**
	P02.4	O0		**General-purpose output**
	TOM0_12	O1		**GTM_TOUT**
	TOM1_12			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_REF0_4			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO0	O3		**QSPI3 output (aka: SLSO30)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**

Table 2-19 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_5			**GTM_TIN**
	QSPI3_MRSTA			**QSPI3 input (aka: MRST3A)**
	SENT_SENT3C			**SENT input**
	P02.5	O0		**General-purpose output**
	TOM0_13	O1		**GTM_TOUT**
	TOM1_13			**GTM_TOUT**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_REF0_5			**IOM reference input**
	CAN0_TXD	O2		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	QSPI3_MRST	O3		**QSPI3 output (aka: MRST3)**
	IOM_MON2_3			**IOM monitor input**
	IOM_REF2_3			**IOM reference input**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**

Table 2-19 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	QSPI3_MTSRA			**QSPI3 input (aka: MTSR3A)**
	SENT_SENT2C			**SENT input**
	CCU60_CC60INC			**CCU60 input**
	CCU60_CCPOS0A			**CCU60 input**
	CCU61_T12HRB			**CCU61 input**
	GPT120_T3INA			**GPT120 input**
	P02.6	O0		**General-purpose output**
	TOM0_14	O1		**GTM_TOUT**
	TOM1_14			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_REF0_6			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**QSPI3 output (aka: MTSR3)**
	—	O4		**Reserved**
	VADC_EMUX00	O5		**VADC output**
	—	O6		**Reserved**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-19 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	QSPI3_SCLKA			**QSPI3 input (aka: SCLK3A)**
	SENT_SENT1C			**SENT input**
	CCU60_CC61INC			**CCU60 input**
	CCU60_CCPOS1A			**CCU60 input**
	CCU61_T13HRB			**CCU61 input**
	GPT120_T3EUDA			**GPT120 input**
	PMU_FDEST			**PMU input**
	P02.7	O0		**General-purpose output**
	TOM0_15	O1		**GTM_TOUT**
	TOM1_15			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_REF0_7			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**QSPI3 output (aka: SCLK3)**
	—	O4		**Reserved**
	VADC_EMUX01	O5		**VADC output**
	SENT_SPC1	O6		**SENT output**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-19 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	SENT_SENT0C			**SENT input**
	CCU60_CC62INC			**CCU60 input**
	CCU60_CCPOS2A			**CCU60 input**
	CCU61_T12HRC			**CCU61 input**
	CCU61_T13HRC			**CCU61 input**
	GPT120_T4INA			**GPT120 input**
	P02.8	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_REF0_8			**IOM reference input**
	QSPI3_SLSO5	O2		**QSPI3 output (aka: SLSO35)**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_EMUX02	O5		**VADC output**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**

Table 2-20 Port 10 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
99	P10.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	SCU_HWCFG4			**SCU input**
	P10.5	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_10			**GTM_TOUT**
	IOM_REF2_9			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO8	O3		**QSPI3 output (aka: SLSO38)**
	QSPI1_SLSO9	O4		**QSPI1 output (aka: SLSO19)**
	GPT120_T6OUT	O5		**GPT120 output**
	—	O6		**Reserved**
	—	O7		**Reserved**
100	P10.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	QSPI3_MTSRB			**QSPI3 input (aka: MTSR3B)**
	SCU_HWCFG5			**SCU input**
	P10.6	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_11			**GTM_TOUT**
	IOM_REF2_10			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**QSPI3 output (aka: MTSR3)**
	GPT120_T3OUT	O4		**GPT120 output**
	—	O5		**Reserved**
	QSPI1_MRST	O6		**QSPI1 output (aka: MRST1)**
	IOM_MON2_1			**IOM monitor input**
	IOM_REF2_1			**IOM reference input**
	—	O7		**Reserved**

Table 2-21 Port 11 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
91	P11.2	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.2	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**QSPI0 output (aka: SLSO05)**
	QSPI1_SLSO5	O4		**QSPI1 output (aka: SLSO15)**
	CCU61_COUT63	O5		**CCU61 output**
	IOM_MON1_7			**IOM monitor input**
	IOM_REF1_7			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**
92	P11.3	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_MRSTB			**QSPI1 input (aka: MRST1B)**
	P11.3	O0		**General-purpose output**
	TOM0_10	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**QSPI1 output (aka: MRST1)**
	IOM_MON2_1			**IOM monitor input**
	IOM_REF2_1			**IOM reference input**
	—	O4		**Reserved**
	CCU61_COUT62	O5		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**

Table 2-21 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
93	P11.6	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_SCLKB			**QSPI1 input (aka: SCLK1B)**
	P11.6	O0		**General-purpose output**
	TOM0_11	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**QSPI1 output (aka: SCLK1)**
	—	O4		**Reserved**
	CCU61_COUT61	O5		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**CCU60 output**
	IOM_MON1_4			**IOM monitor input**
	IOM_REF1_2			**IOM reference input**
95	P11.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI1_MTSRC			**QSPI1 input (aka: MTSR1C)**
	P11.8	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	QSPI1_SLSO10	O3		**QSPI1 output (aka: SLSO110)**
	QSPI1_MTSR	O4		**QSPI1 output (aka: MTSR1)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-21 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
94	P11.9	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_MTSRB			**QSPI1 input (aka: MTSR1B)**
	P11.9	O0		**General-purpose output**
	TOM0_12	O1		**GTM_TOUT**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**QSPI1 output (aka: MTSR1)**
	—	O4		**Reserved**
	CCU61_COUT60	O5		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**CCU60 output**
	IOM_MON1_3			**IOM monitor input**
	IOM_REF1_3			**IOM reference input**
96	P11.10	I	A1+ / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXE			**ASCLIN1 input (aka: ARX1E)**
	SCU_REQ12			**SCU input**
	P11.10	O0		**General-purpose output**
	TOM0_13	O1		**GTM_TOUT**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**QSPI0 output (aka: SLSO03)**
	QSPI1_SLSO3	O4		**QSPI1 output (aka: SLSO13)**
	CCU61_CC62	O5		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**

Table 2-21 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
97	P11.11	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.11	O0		**General-purpose output**
	TOM0_14	O1		**GTM_TOUT**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**QSPI0 output (aka: SLSO04)**
	QSPI1_SLSO4	O4		**QSPI1 output (aka: SLSO14)**
	CCU61_CC61	O5		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**
98	P11.12	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.12	O0		**General-purpose output**
	TOM0_15	O1		**GTM_TOUT**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	GTM_CLK2	O3		**GTM output**
	—	O4		**Reserved**
	CCU61_CC60	O5		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**
	SCU_EXTCLK1	O6		**SCU output**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-22 Port 13 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
87	P13.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CTRAPA			**CCU60 input**
	GPT120_T6EUDB			**GPT120 input**
	P13.0	O0		**General-purpose output**
	TOM0_5	O1		**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**QSPI2 output (aka: SCLK2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
88	P13.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CCPOS0C			**CCU60 input**
	GPT120_T3INB			**GPT120 input**
	P13.1	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-22 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
89	P13.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CCPOS1C			**CCU60 input**
	GPT120_T3EUDB			**GPT120 input**
	GPT120_CAPINA			**GPT120 input**
	P13.2	O0		**General-purpose output**
	TOM0_7	O1		**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
90	P13.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CCPOS2C			**CCU60 input**
	GPT120_T4INB			**GPT120 input**
	P13.3	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	QSPI2_MTSR	O3		**QSPI2 output (aka: MTSR2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-23 Port 14 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
81	P14.0	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	P14.0	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	ASCLIN0_SCLK	O6		**ASCLIN0 output (aka: ASCLK0)**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**

Table 2-23 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
82	P14.1	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	ASCLIN0_RXA			**ASCLIN0 input (aka: ARX0A)**
	CAN1_RXDB			**CAN node 1 input (aka: RXDCAN1B)**
	SCU_REQ15			**SCU input**
	SCU_EVRWUPA	AI		**SCU input**
	P14.1	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_REF1_14			**IOM reference input**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**
83	P14.3	I	A1 / PU / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	SCU_REQ10			**SCU input**
	SCU_HWCFG3_BMI			**SCU input**
	P14.3	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_REF2_4			**IOM reference input**
	—	O2		**Reserved**
	QSPI2_SLSO3	O3		**QSPI2 output (aka: SLSO23)**
	ASCLIN1_SLSO	O4		**ASCLIN1 output (aka: ASLSO1)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-23 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
84	P14.4	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	P14.4	O0		**General-purpose output**
	TOM0_7	O1		**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_REF2_8			**IOM reference input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
85	P14.6	I	A1+ / PU / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI0_MRSTD			**QSPI0 input (aka: MRST0D)**
	P14.6	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	IOM_REF2_14			**IOM reference input**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**QSPI2 output (aka: SLSO22)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-24 Port 15 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P15.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	P15.0	O0		**General-purpose output**
	TOM1_3	O1		**GTM_TOUT**
	TOM0_11			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI0_SLSO13	O3		**QSPI0 output (aka: SLSO013)**
	—	O4		**Reserved**
	CAN2_TXD	O5		**CAN node 2 output (aka: TXDCAN2)**
	IOM_MON2_7			**IOM monitor input**
	IOM_REF2_7			**IOM reference input**
	ASCLIN1_SCLK	O6		**ASCLIN1 output (aka: ASCLK1)**
	—	O7		**Reserved**
77	P15.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXA			**ASCLIN1 input (aka: ARX1A)**
	QSPI2_SLSIB			**QSPI2 input (aka: SLSI2B)**
	CAN2_RXDA			**CAN node 2 input (aka: RXDCAN2A)**
	SCU_REQ16			**SCU input**
	SCU_EVRWUPB	AI		**SCU input**
	P15.1	O0		**General-purpose output**
	TOM1_4	O1		**GTM_TOUT (= DTM5_OUT4)**
	TOM0_12			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI2_SLSO5	O3		**QSPI2 output (aka: SLSO25)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-24 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
78	P15.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI2_MRSTE			**QSPI2 input (aka: MRST2E)**
	QSPI2_SLSIA			**QSPI2 input (aka: SLSI2A)**
	QSPI2_HSICINA			**QSPI2 input (aka: HSIC2INA)**
	P15.2	O0		**General-purpose output**
	TOM1_5	O1		**GTM_TOUT (= DTM5_OUT5)**
	TOM0_13			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	QSPI2_SLSO0	O3		**QSPI2 output (aka: SLSO20)**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	ASCLIN0_SCLK	O6		**ASCLIN0 output (aka: ASCLK0)**
	—	O7		**Reserved**
79	P15.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN0_RXB			**ASCLIN0 input (aka: ARX0B)**
	QSPI2_SCLKA			**QSPI2 input (aka: SCLK2A)**
	QSPI2_HSICINB			**QSPI2 input (aka: HSIC2INB)**
	CAN1_RXDA			**CAN node 1 input (aka: RXDCAN1A)**
	P15.3	O0		**General-purpose output**
	TOM1_6	O1		**GTM_TOUT (= DTM5_OUT6)**
	TOM0_14			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	QSPI2_SCLK	O3		**QSPI2 output (aka: SCLK2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-24 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
80	P15.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXB			**ASCLIN1 input (aka: ARX1B)**
	QSPI2_MTSRA			**QSPI2 input (aka: MTSR2A)**
	SCU_REQ13			**SCU input**
	P15.5	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI2_MTSR	O3		**QSPI2 output (aka: MTSR2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-25 Port 20 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
64	P20.2	I	InputOnly / PU / VDDP3	**General-purpose input**
	$\overline{\text{TESTMODE}}$			**Factory Test Mode Enable**

Table 2-25 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
69	P20.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	P20.8	O0		**General-purpose output**
	TOM1_7	O1		**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_MON2_8			**IOM monitor input**
	ASCLIN1_SLSO	O2		**ASCLIN1 output (aka: ASLSO1)**
	QSPI0_SLSO0	O3		**QSPI0 output (aka: SLSO00)**
	QSPI1_SLSO0	O4		**QSPI1 output (aka: SLSO10)**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	SCU_WDT0LCK	O6		**SCU output**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**
70	P20.9	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXC			**ASCLIN1 input (aka: ARX1C)**
	QSPI0_SLSIB			**QSPI0 input (aka: SLSI0B)**
	SCU_REQ11			**SCU input**
	P20.9	O0		**General-purpose output**
	TOM1_13	O1		**GTM_TOUT**
	TOM0_13			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_MON2_11			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**QSPI0 output (aka: SLSO01)**
	QSPI1_SLSO1	O4		**QSPI1 output (aka: SLSO11)**
	—	O5		**Reserved**
	SCU_WDTSLCK	O6		**SCU output**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**

Table 2-25 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
71	P20.10	I	A1 / HighZ / VDDP3	**General-purpose input**
	P20.10	O0		**General-purpose output**
	TOM1_14	O1		**GTM_TOUT**
	TOM0_14			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_MON2_14			**IOM monitor input**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI0_SLSO6	O3		**QSPI0 output (aka: SLSO06)**
	QSPI2_SLSO7	O4		**QSPI2 output (aka: SLSO27)**
	—	O5		**Reserved**
	ASCLIN1_SCLK	O6		**ASCLIN1 output (aka: ASCLK1)**
	CCU61_CC62	O7		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**
72	P20.11	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_SCLKA			**QSPI0 input (aka: SCLK0A)**
	P20.11	O0		**General-purpose output**
	TOM1_15	O1		**GTM_TOUT**
	TOM0_15			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_MON2_15			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**QSPI0 output (aka: SCLK0)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**

Table 2-25 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P20.12	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI0_MRSTA			**QSPI0 input (aka: MRST0A)**
	IOM_PIN13			**IOM pad input**
	P20.12	O0		**General-purpose output**
	TOM1_0	O1		**GTM_TOUT**
	TOM0_8			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_MON0_13			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**QSPI0 output (aka: MRST0)**
	IOM_MON2_0			**IOM monitor input**
	IOM_REF2_0			**IOM reference input**
	QSPI0_MTSR	O4		**QSPI0 output (aka: MTSR0)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**
74	P20.13	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_SLSIA			**QSPI0 input (aka: SLSI0A)**
	IOM_PIN14			**IOM pad input**
	P20.13	O0		**General-purpose output**
	TOM1_1	O1		**GTM_TOUT**
	TOM0_9			**GTM_TOUT**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_MON0_14			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**QSPI0 output (aka: SLSO02)**
	QSPI1_SLSO2	O4		**QSPI1 output (aka: SLSO12)**
	QSPI0_SCLK	O5		**QSPI0 output (aka: SCLK0)**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**

Table 2-25 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
75	P20.14	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_MTSRA			**QSPI0 input (aka: MTSR0A)**
	IOM_PIN15			**IOM pad input**
	P20.14	O0		**General-purpose output**
	TOM1_2	O1		**GTM_TOUT**
	TOM0_10			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_MON0_15			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**QSPI0 output (aka: MTSR0)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-26 Port 21 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
56	P21.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	SCU_EMGSTOPB			**SCU input**
	P21.2	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-26 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
57	P21.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	P21.3	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
58	P21.4	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	P21.4	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-26 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
59	P21.6	I	A1 / PU / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	TDI			**OCDS input**
	$\overline{\text{OCDS\_TGI2}}$			**OCDS input**
	GPT120_T5EUDA			**GPT120 input**
	P21.6	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**GPT120 output**
	$\overline{\text{OCDS\_TGO2}}$	O		**OCDS**
61	P21.7	I	A1+ / PU / VDDP3	**General-purpose input**
	TIM0_5			**GTM_TIN**
	OCDS_DAP2			**OCDS input**
	$\overline{\text{OCDS\_TGI3}}$			**OCDS input**
	GPT120_T5INA			**GPT120 input**
	P21.7	O0		**General-purpose output**
	TOM0_5	O1		**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**GPT120 output**
	$\overline{\text{OCDS\_TGO3}}$	O		**OCDS**
	OCDS_DAP2	O		**OCDS Output**
	TDO	O		**JTAG Output**

Table 2-27 Port 23 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
51	P23.1	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	P23.1	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM0_15			**GTM_TOUT**
	ASCLIN1_RTS	O2		**ASCLIN1 output (aka: ARTS1)**
	QSPI3_SLSO13	O3		**QSPI3 output (aka: SLSO313)**
	GTM_CLK0	O4		**GTM output**
	SCU_EXTCLK1	O5		**SCU output**
	SCU_EXTCLK0	O6		**SCU output**
	—	O7		**Reserved**

Table 2-28 Port 33 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
41	P33.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	CCU61_CCPOS2C			**CCU61 input**
	GPT120_T4EUDB			**GPT120 input**
	IOM_PIN5			**IOM pad input**
	P33.5	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_MON0_5			**IOM monitor input**
	QSPI0_SLSO7	O2		**QSPI0 output (aka: SLSO07)**
	QSPI1_SLSO7	O3		**QSPI1 output (aka: SLSO17)**
	—	O4		**Reserved**
	VADC_EMUX11	O5		**VADC output**
	VADC_G0BFL1	O6		**VADC output**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**

Table 2-28 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
42	P33.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	ASCLIN1_RXF			**ASCLIN1 input (aka: ARX1F)**
	CCU61_CCPOS1C			**CCU61 input**
	GPT120_T2EUDB			**GPT120 input**
	IOM_PIN6			**IOM pad input**
	P33.6	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_MON0_6			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	ASCLIN1_TX	O4		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	VADC_EMUX10	O5		**VADC output**
	VADC_G0BFL2	O6		**VADC output**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**

Table 2-28 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
43	P33.7	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	CAN0_RXDE			**CAN node 0 input (aka: RXDCAN0E)**
	SCU_REQ8			**SCU input**
	CCU61_CCPOS0C			**CCU61 input**
	GPT120_T2INB			**GPT120 input**
	IOM_PIN7			**IOM pad input**
	P33.7	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_MON0_7			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO7	O3		**QSPI3 output (aka: SLSO37)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	VADC_G0BFL3	O6		**VADC output**
	CCU61_COUT60	O7		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**

Table 2-28 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
44	P33.8	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	SCU_EMGSTOPA			**SCU input**
	IOM_PIN8			**IOM pad input**
	P33.8	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_MON0_8			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**QSPI3 output (aka: SLSO32)**
	—	O4		**Reserved**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**
	SMU_FSP	O		**SMU**

Table 2-28 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
45	P33.9	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI3_HSICINA			**QSPI3 input (aka: HSIC3INA)**
	IOM_PIN9			**IOM pad input**
	P33.9	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_MON0_9			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO1	O3		**QSPI3 output (aka: SLSO31)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC62	O7		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**
46	P33.10	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	QSPI3_SLSIC			**QSPI3 input (aka: SLSI3C)**
	QSPI3_HSICINB			**QSPI3 input (aka: HSIC3INB)**
	IOM_PIN10			**IOM pad input**
	P33.10	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_MON0_10			**IOM monitor input**
	QSPI1_SLSO6	O2		**QSPI1 output (aka: SLSO16)**
	QSPI3_SLSO11	O3		**QSPI3 output (aka: SLSO311)**
	ASCLIN1_SLSO	O4		**ASCLIN1 output (aka: ASLSO1)**
	GTM_CLK1	O5		**GTM output**
	SCU_EXTCLK1	O6		**SCU output**
	CCU61_COUT61	O7		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**

Table 2-29 Port 40 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
40	P40.0	I	S / VDDM	**General-purpose input**
	VADCG0_0	AI		**VADC input channel 0 of group 0**
39	P40.1	I	S / VDDM	**General-purpose input**
	VADCG0_1	AI		**VADC input channel 1 of group 0** (with multiplexer diagnostics)
38	P40.2	I	S / VDDM	**General-purpose input**
	VADCG0_2	AI		**VADC input channel 2 of group 0** (with multiplexer diagnostics)
37	P40.3	I	S / VDDM	**General-purpose input**
	VADCG0_3	AI		**VADC input channel 3 of group 0**
36	P40.4	I	S / VDDM	**General-purpose input**
	VADCG0_4	AI		**VADC input channel 4 of group 0**
35	P40.5	I	S / VDDM	**General-purpose input**
	VADCG0_5	AI		**VADC input channel 5 of group 0**
34	P40.6	I	S / VDDM	**General-purpose input**
	VADCG0_6	AI		**VADC input channel 6 of group 0**
29	P40.7	I	S / VDDM	**General-purpose input**
	VADCG0_7	AI		**VADC input channel 7 of group 0** (with pull down diagnostics)
28	P40.8	I	S / VDDM	**General-purpose input**
	VADCG0_8	AI		**VADC input channel 8 of group 0**
27	P40.9	I	S / VDDM	**General-purpose input**
	VADCG0_9	AI		**VADC input channel 9 of group 0** (with multiplexer diagnostics)
26	P40.10	I	S / VDDM	**General-purpose input**
	VADCG0_10	AI		**VADC input channel 10 of group 0** (with multiplexer diagnostics)
25	P40.11	I	S / VDDM	**General-purpose input**
	SENT_SENT0A			**SENT input**
	CCU60_CCPOS0D			**CCU60 input**
	VADCG0_11	AI		**VADC input channel 11 of group 0**

Table 2-30 Port 41 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
24	P41.0	I	S / VDDM	**General-purpose input**
	SENT_SENT1A			**SENT input**
	CCU60_CCPOS1B			**CCU60 input**
	VADCG1_0	AI		**VADC input channel 0 of group 1**
23	P41.1	I	S / VDDM	**General-purpose input**
	VADCG1_1	AI		**VADC input channel 1 of group 1** (with multiplexer diagnostics)
22	P41.2	I	S / VDDM	**General-purpose input**
	SENT_SENT2A			**SENT input**
	CCU61_CCPOS1B			**CCU61 input**
	VADCG1_2	AI		**VADC input channel 2 of group 1** (with multiplexer diagnostics)
21	P41.3	I	S / VDDM	**General-purpose input**
	SENT_SENT3A			**SENT input**
	CCU61_CCPOS1D			**CCU61 input**
	VADCG1_3	AI		**VADC input channel 3 of group 1** (with pull down diagnostics)
20	P41.4	I	S / VDDM	**General-purpose input**
	VADCG1_4	AI		**VADC input channel 4 of group 1**
19	P41.5	I	S / VDDM	**General-purpose input**
	VADCG1_5	AI		**VADC input channel 5 of group 1**
18	P41.6	I	S / VDDM	**General-purpose input**
	VADCG1_6	AI		**VADC input channel 6 of group 1**
17	P41.7	I	S / VDDM	**General-purpose input**
	VADCG1_7	AI		**VADC input channel 7 of group 1**
16	P41.8	I	S / VDDM	**General-purpose input**
	VADCG1_8	AI		**VADC input channel 8 of group 1**
15	P41.9	I	S / VDDM	**General-purpose input**
	VADCG1_9	AI		**VADC input channel 9 of group 1** (with multiplexer diagnostics)
14	P41.10	I	S / VDDM	**General-purpose input**
	VADCG1_10	AI		**VADC input channel 10 of group 1** (with multiplexer diagnostics)
13	P41.11	I	S / VDDM	**General-purpose input**
	VADCG1_11	AI		**VADC input channel 11 of group 1**

Table 2-31 System I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
53	XTAL1	I	VDDP3	**Main Oscillator/PLL/Clock Generator Input**
54	XTAL2	O	VDDP3	**Main Oscillator/PLL/Clock Generator Output**
60	TMS/DAP1	I	A1+ / PD / VDDP3	**Debug Interface**
	DAP1	I/O		**Device Access Port LIne 1**
62	$\overline{\text{TRST}}$	I	Input Only / PD / VDDP3	**JTAG Module Reset/Enable Input**
63	TCK/DAP0	I	Input Only / PD / VDDP3	**OCDS input**
	DAP0	I		**Device Access Port LIne 0**
65	$\overline{\text{ESR1}}$	I/O	A1+ / PU / VDDP3	**SCU input**
	EVRWUP	I		**EVR Wakeup Pin**
66	$\overline{\text{PORST}}$	I	Input Only / PD / VDDP3	**Power On Reset** Additional strong PD in case of power fail.
67	$\overline{\text{ESR0}}$	I/O	A1+ / OD / VDDP3	**SCU input/output**
	EVRWUP	I		**EVR Wakeup Pin**

Table 2-32 Supply

Pin	Symbol	Ctrl.	Buffer Type	Function
30	V_{AGND}	I	—	**Negative Analog Reference Voltage 0**
31	V_{AREF}	I	—	**Positive Analog Reference Voltage 0**
86	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)** This pin supplies also the Flash 3.3V.
47	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)**
52	V_{DD}	I	—	**Digital Core Power Supply (1.3V)** This pin supplies also the main XTAL Oscillator/PLL (1.3V). A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity.
55	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)** This pin supplies also the main XTAL Oscillator/PLL (3.3V). A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity.
33	V_{DDM}	I	—	**ADC Power Supply (5.0V)**
12	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)**
11	V_{DD}	I	—	**Digital Core Power Supply (1.3V)**
68	V_{DD}	I	—	**Digital Core Power Supply (1.3V)**
32	V_{SSM}	I	—	**Analog Ground for VDDM**

2.2.2 Pull-Up/Pull-Down Reset Behavior of the Pins

Table 2-33 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
all GPIOs	High-Z	
TDI, TESTMODE	Pull-up	
PORST[1)]	Pull-down with I_{PORST} relevant	Pull-down with I_{PDLI} relevant
TRST, TCK, TMS	Pull-down	
ESR0	The open-drain driver is used to drive low.[2)]	Pull-up[3)]
ESR1	Pull-up[3)]	
P14.2, P14.3, P14.6	Pull-up	
P21.7 / TDO	Pull-up	High-Z/Pull-up[4)]

1) Pull-down with I_{PORST} relevant is always activated when a primary supply monitor detects a violation.
2) Valid additionally after deactivation of PORST until the internal reset phase has finished. See the SCU chapter for details.
3) See the SCU_IOCR register description.
4) Depends on JTAG/DAP selection with TRST.

2.3 PG-TQFP-144-27 Package Variant Pin Configuration of TC214 / TC224

Figure 2-1 is showing the TC214 / TC224 pinout for the package variant: PG-TQFP-144-27.

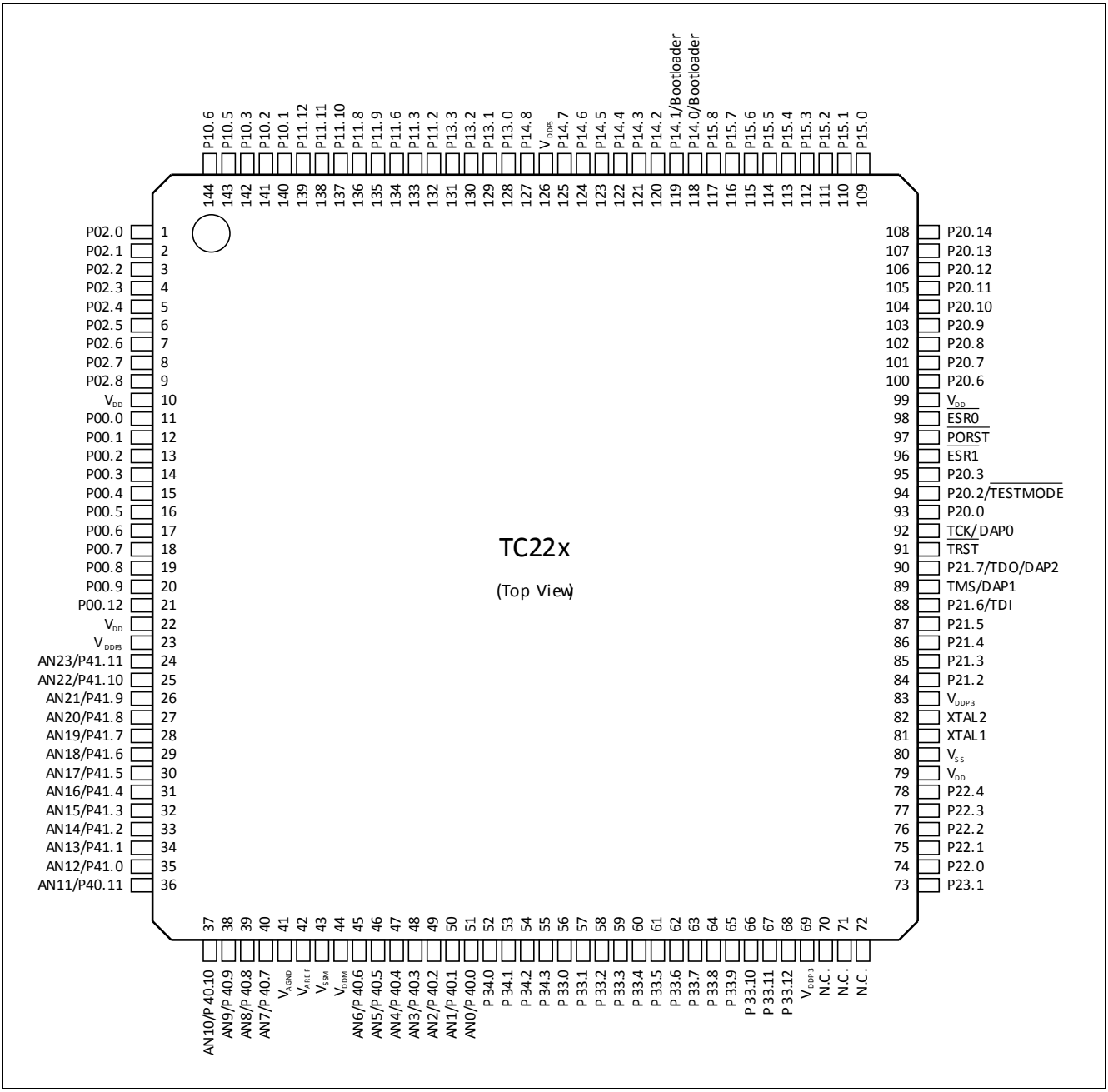


Figure 2-3 TC214 / TC224 Pinout for the package variant PG-TQFP-144-27.

2.3.1 Port Functions and Pinning Tables

2.3.1.1 How to Read the Following Port Function Tables

Some hints for interpreting the following tables.

Column “Ctrl.”:

I = Input (for GPIO port Lines with IOCR bit field Selection PCx = $0XXX_B$)

AI = Analog input

O = Output
O0 = Output with IOCR bit field selection PCx = $1X000_B$
O1 = Output with IOCR bit field selection PCx = $1X001_B$ (ALT1)
O2 = Output with IOCR bit field selection PCx = $1X010_B$ (ALT2)
O3 = Output with IOCR bit field selection PCx = $1X011_B$ (ALT3)
O4 = Output with IOCR bit field selection PCx = $1X100_B$ (ALT4)
O5 = Output with IOCR bit field selection PCx = $1X101_B$ (ALT5)
O6 = Output with IOCR bit field selection PCx = $1X110_B$ (ALT6)
O7 = Output with IOCR bit field selection PCx = $1X111_B$ (ALT7)

Table 2-34 Example Port Table

Pin	Symbol	Ctrl.	Buffer Type	Function
10	Pxx.y	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIMm_n			**GTM_TIN**
	TOMa_b	O1		**GTM_TOUT**
	TOMc_d			**GTM_TOUT**
	IOM_REFv_w			**IOM reference input**
	ASCLINz_RTS	O2		**ASCLIN0 output (aka ARTSz)**

To each input several functions can be connected. The peripherals’ configuration defines if this input is used.

The port module (see corresponding chapter) decides which of the 8 output signals O0 to O7 drives the pad.

Some Ox rows list more than one function, e.g. several GTM_TOUT outputs and IOM reference inputs. The GTM module (see corresponding chapter) has its own sub-multiplexer structure that defines which of the GTM sub-units drives this signal. Additionally the IOM modules “listens” on these output signals (see IOM chapter).

Some pin symbol names were changed in this AURIX device compared to other AURIX devices to improve naming systematics. The previously used symbol name is documented in the “Function” column with the text “(aka …)”[1].

Column “Type”:

IN = Input only
A1 = Pad class A1 (3.3V)
A1+ = Pad class A1+ (3.3V)
S = ADC with digital input. Pad class D for analog input “AI”, pad class S for digital input “I”.
PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)

1) “aka” as abbreviation for “also known as”.

High-Z = High-Z during reset ($\overline{\text{PORST}}$ = 0)
V_x = Supply (the Exposed Pad is also considered as VSS and shall be connected to ground)

2.3.1.2 Tables

Port function and pinning tables.

Table 2-35 Port 00 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
11	P00.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	CCU61_CTRAPA			**CCU61 input**
	CCU60_T12HRE			**CCU60 input**
	P00.0	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_REF0_9			**IOM reference input**
	ASCLIN0_SCLK	O2		**ASCLIN0 output (aka: ASCLK0)**
	ASCLIN0_TX	O3		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**

Table 2-35 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
12	P00.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	ASCLIN0_RXC			**ASCLIN0 input (aka: ARX0C)**
	CAN1_RXDD			**CAN node 1 input (aka: RXDCAN1D)**
	SENT_SENT0B			**SENT input**
	CCU60_CC60INB			**CCU60 input**
	CCU61_CC60INA			**CCU61 input**
	P00.1	O0		**General-purpose output**
	TOM0_9	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_REF0_10			**IOM reference input**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC0	O6		**SENT output**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**

Table 2-35 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
13	P00.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	SENT_SENT1B			**SENT input**
	P00.2	O0		**General-purpose output**
	TOM0_9	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_REF0_11			**IOM reference input**
	ASCLIN0_SCLK	O2		**ASCLIN0 output (aka: ASCLK0)**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**
14	P00.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	SENT_SENT2B			**SENT input**
	CCU60_CC61INB			**CCU60 input**
	CCU61_CC61INA			**CCU61 input**
	P00.3	O0		**General-purpose output**
	TOM0_10	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_REF0_12			**IOM reference input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC2	O6		**SENT output**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**

Table 2-35 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
15	P00.4	I	A1 / HighZ / VDDP3	**General-purpose input**
	SCU_REQ7			**SCU input**
	SENT_SENT3B			**SENT input**
	P00.4	O0		**General-purpose output**
	TOM0_11	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_REF0_13			**IOM reference input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_G1BFL0	O5		**VADC output**
	SENT_SPC3	O6		**SENT output**
	CCU61_COUT61	O7		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**
16	P00.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CC62INB			**CCU60 input**
	CCU61_CC62INA			**CCU61 input**
	P00.5	O0		**General-purpose output**
	TOM0_12	O1		**GTM_TOUT**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_REF0_14			**IOM reference input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_G1BFL1	O5		**VADC output**
	—	O6		**Reserved**
	CCU61_CC62	O7		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**

Table 2-35 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
17	P00.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	P00.6	O0		**General-purpose output**
	TOM0_13	O1		**GTM_TOUT**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_REF0_15			**IOM reference input**
	—	O2		**Reserved**
	VADC_G1BFL2	O3		**VADC output**
	—	O4		**Reserved**
	VADC_EMUX10	O5		**VADC output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**
18	P00.7	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU61_CC60INC			**CCU61 input**
	CCU61_CCPOS0A			**CCU61 input**
	CCU60_T12HRB			**CCU60 input**
	GPT120_T2INA			**GPT120 input**
	P00.7	O0		**General-purpose output**
	TOM0_14	O1		**GTM_TOUT**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	—	O2		**Reserved**
	VADC_G1BFL3	O3		**VADC output**
	—	O4		**Reserved**
	VADC_EMUX11	O5		**VADC output**
	—	O6		**Reserved**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**

Table 2-35 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
19	P00.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU61_CC61INC			**CCU61 input**
	CCU61_CCPOS1A			**CCU61 input**
	CCU60_T13HRB			**CCU60 input**
	GPT120_T2EUDA			**GPT120 input**
	P00.8	O0		**General-purpose output**
	TOM0_15	O1		**GTM_TOUT**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	QSPI3_SLSO6	O2		**QSPI3 output (aka: SLSO36)**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_EMUX12	O5		**VADC output**
	—	O6		**Reserved**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**
20	P00.9	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	CCU61_CC62INC			**CCU61 input**
	CCU61_CCPOS2A			**CCU61 input**
	CCU60_T13HRC			**CCU60 input**
	CCU60_T12HRC			**CCU60 input**
	GPT120_T4EUDA			**GPT120 input**
	P00.9	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	QSPI3_SLSO7	O2		**QSPI3 output (aka: SLSO37)**
	ASCLIN0_RTS	O3		**ASCLIN0 output (aka: ARTS0)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC62	O7		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**

Table 2-35 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
21	P00.12	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	ASCLIN0_CTSA			**ASCLIN0 input (aka: ACTS0A)**
	P00.12	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**CCU61 output**
	IOM_MON1_7			**IOM monitor input**
	IOM_REF1_7			**IOM reference input**

Table 2-36 Port 02 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	SCU_REQ6			**SCU input**
	CCU60_CC60INA			**CCU60 input**
	CCU61_CC60INB			**CCU61 input**
	P02.0	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_8			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_REF0_0			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO1	O3		**QSPI3 output (aka: SLSO31)**
	—	O4		**Reserved**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-36 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	CAN0_RXDA			**CAN node 0 input (aka: RXDCAN0A)**
	SCU_REQ14			**SCU input**
	P02.1	O0		**General-purpose output**
	TOM0_9	O1		**GTM_TOUT**
	TOM1_9			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_REF0_1			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**QSPI3 output (aka: SLSO32)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**CCU60 output**
	IOM_MON1_3			**IOM monitor input**
	IOM_REF1_3			**IOM reference input**

Table 2-36 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	CCU60_CC61INA			**CCU60 input**
	CCU61_CC61INB			**CCU61 input**
	P02.2	O0		**General-purpose output**
	TOM0_10	O1		**GTM_TOUT**
	TOM1_10			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_REF0_2			**IOM reference input**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI3_SLSO3	O3		**QSPI3 output (aka: SLSO33)**
	—	O4		**Reserved**
	CAN2_TXD	O5		**CAN node 2 output (aka: TXDCAN2)**
	IOM_MON2_7			**IOM monitor input**
	IOM_REF2_7			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-36 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	ASCLIN1_RXG			**ASCLIN1 input (aka: ARX1G)**
	CAN2_RXDB			**CAN node 2 input (aka: RXDCAN2B)**
	P02.3	O0		**General-purpose output**
	TOM0_11	O1		**GTM_TOUT**
	TOM1_11			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_REF0_3			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO4	O3		**QSPI3 output (aka: SLSO34)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**CCU60 output**
	IOM_MON1_4			**IOM monitor input**
	IOM_REF1_2			**IOM reference input**
5	P02.4	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	QSPI3_SLSIA			**QSPI3 input (aka: SLSI3A)**
	CAN0_RXDD			**CAN node 0 input (aka: RXDCAN0D)**
	CCU60_CC62INA			**CCU60 input**
	CCU61_CC62INB			**CCU61 input**
	P02.4	O0		**General-purpose output**
	TOM0_12	O1		**GTM_TOUT**
	TOM1_12			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_REF0_4			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO0	O3		**QSPI3 output (aka: SLSO30)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**

Table 2-36 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_5			**GTM_TIN**
	QSPI3_MRSTA			**QSPI3 input (aka: MRST3A)**
	SENT_SENT3C			**SENT input**
	P02.5	O0		**General-purpose output**
	TOM0_13	O1		**GTM_TOUT**
	TOM1_13			**GTM_TOUT**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_REF0_5			**IOM reference input**
	CAN0_TXD	O2		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	QSPI3_MRST	O3		**QSPI3 output (aka: MRST3)**
	IOM_MON2_3			**IOM monitor input**
	IOM_REF2_3			**IOM reference input**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**

Table 2-36 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	QSPI3_MTSRA			**QSPI3 input (aka: MTSR3A)**
	SENT_SENT2C			**SENT input**
	CCU60_CC60INC			**CCU60 input**
	CCU60_CCPOS0A			**CCU60 input**
	CCU61_T12HRB			**CCU61 input**
	GPT120_T3INA			**GPT120 input**
	P02.6	O0		**General-purpose output**
	TOM0_14	O1		**GTM_TOUT**
	TOM1_14			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_REF0_6			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**QSPI3 output (aka: MTSR3)**
	—	O4		**Reserved**
	VADC_EMUX00	O5		**VADC output**
	—	O6		**Reserved**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-36 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	QSPI3_SCLKA			**QSPI3 input (aka: SCLK3A)**
	SENT_SENT1C			**SENT input**
	CCU60_CC61INC			**CCU60 input**
	CCU60_CCPOS1A			**CCU60 input**
	CCU61_T13HRB			**CCU61 input**
	GPT120_T3EUDA			**GPT120 input**
	PMU_FDEST			**PMU input**
	P02.7	O0		**General-purpose output**
	TOM0_15	O1		**GTM_TOUT**
	TOM1_15			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_REF0_7			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**QSPI3 output (aka: SCLK3)**
	—	O4		**Reserved**
	VADC_EMUX01	O5		**VADC output**
	SENT_SPC1	O6		**SENT output**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-36 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	SENT_SENT0C			**SENT input**
	CCU60_CC62INC			**CCU60 input**
	CCU60_CCPOS2A			**CCU60 input**
	CCU61_T12HRC			**CCU61 input**
	CCU61_T13HRC			**CCU61 input**
	GPT120_T4INA			**GPT120 input**
	P02.8	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_REF0_8			**IOM reference input**
	QSPI3_SLSO5	O2		**QSPI3 output (aka: SLSO35)**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_EMUX02	O5		**VADC output**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**

Table 2-37 Port 10 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
140	P10.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI1_MRSTA			**QSPI1 input (aka: MRST1A)**
	GPT120_T5EUDB			**GPT120 input**
	P10.1	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_9			**GTM_TOUT**
	QSPI1_MTSR	O2		**QSPI1 output (aka: MTSR1)**
	QSPI1_MRST	O3		**QSPI1 output (aka: MRST1)**
	IOM_MON2_1			**IOM monitor input**
	IOM_REF2_1			**IOM reference input**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
141	P10.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	QSPI1_SCLKA			**QSPI1 input (aka: SCLK1A)**
	CAN2_RXDE			**CAN node 2 input (aka: RXDCAN2E)**
	SCU_REQ2			**SCU input**
	GPT120_T6INB			**GPT120 input**
	P10.2	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_10			**GTM_TOUT**
	IOM_MON2_9			**IOM monitor input**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**QSPI1 output (aka: SCLK1)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-37 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
142	P10.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	QSPI1_MTSRA			**QSPI1 input (aka: MTSR1A)**
	SCU_REQ3			**SCU input**
	GPT120_T5INB			**GPT120 input**
	P10.3	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_11			**GTM_TOUT**
	IOM_MON2_10			**IOM monitor input**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**QSPI1 output (aka: MTSR1)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN2_TXD	O6		**CAN node 2 output (aka: TXDCAN2)**
	IOM_MON2_7			**IOM monitor input**
	IOM_REF2_7			**IOM reference input**
	—	O7		**Reserved**
143	P10.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	SCU_HWCFG4			**SCU input**
	P10.5	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_10			**GTM_TOUT**
	IOM_REF2_9			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_SLSO8	O3		**QSPI3 output (aka: SLSO38)**
	QSPI1_SLSO9	O4		**QSPI1 output (aka: SLSO19)**
	GPT120_T6OUT	O5		**GPT120 output**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-37 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
144	P10.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	QSPI3_MTSRB			**QSPI3 input (aka: MTSR3B)**
	SCU_HWCFG5			**SCU input**
	P10.6	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_11			**GTM_TOUT**
	IOM_REF2_10			**IOM reference input**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**QSPI3 output (aka: MTSR3)**
	GPT120_T3OUT	O4		**GPT120 output**
	—	O5		**Reserved**
	QSPI1_MRST	O6		**QSPI1 output (aka: MRST1)**
	IOM_MON2_1			**IOM monitor input**
	IOM_REF2_1			**IOM reference input**
	—	O7		**Reserved**

Table 2-38 Port 11 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
132	P11.2	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.2	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**QSPI0 output (aka: SLSO05)**
	QSPI1_SLSO5	O4		**QSPI1 output (aka: SLSO15)**
	CCU61_COUT63	O5		**CCU61 output**
	IOM_MON1_7			**IOM monitor input**
	IOM_REF1_7			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**

Table 2-38 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
133	P11.3	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_MRSTB			**QSPI1 input (aka: MRST1B)**
	P11.3	O0		**General-purpose output**
	TOM0_10	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**QSPI1 output (aka: MRST1)**
	IOM_MON2_1			**IOM monitor input**
	IOM_REF2_1			**IOM reference input**
	—	O4		**Reserved**
	CCU61_COUT62	O5		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**
134	P11.6	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_SCLKB			**QSPI1 input (aka: SCLK1B)**
	P11.6	O0		**General-purpose output**
	TOM0_11	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**QSPI1 output (aka: SCLK1)**
	—	O4		**Reserved**
	CCU61_COUT61	O5		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**CCU60 output**
	IOM_MON1_4			**IOM monitor input**
	IOM_REF1_2			**IOM reference input**

Table 2-38 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
136	P11.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI1_MTSRC			**QSPI1 input (aka: MTSR1C)**
	P11.8	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	QSPI1_SLSO10	O3		**QSPI1 output (aka: SLSO110)**
	QSPI1_MTSR	O4		**QSPI1 output (aka: MTSR1)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
135	P11.9	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI1_MTSRB			**QSPI1 input (aka: MTSR1B)**
	P11.9	O0		**General-purpose output**
	TOM0_12	O1		**GTM_TOUT**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**QSPI1 output (aka: MTSR1)**
	—	O4		**Reserved**
	CCU61_COUT60	O5		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**CCU60 output**
	IOM_MON1_3			**IOM monitor input**
	IOM_REF1_3			**IOM reference input**

Table 2-38 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
137	P11.10	I	A1+ / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXE			**ASCLIN1 input (aka: ARX1E)**
	SCU_REQ12			**SCU input**
	P11.10	O0		**General-purpose output**
	TOM0_13	O1		**GTM_TOUT**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**QSPI0 output (aka: SLSO03)**
	QSPI1_SLSO3	O4		**QSPI1 output (aka: SLSO13)**
	CCU61_CC62	O5		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**
138	P11.11	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.11	O0		**General-purpose output**
	TOM0_14	O1		**GTM_TOUT**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**QSPI0 output (aka: SLSO04)**
	QSPI1_SLSO4	O4		**QSPI1 output (aka: SLSO14)**
	CCU61_CC61	O5		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**

Table 2-38 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
139	P11.12	I	A1+ / HighZ / VDDP3	**General-purpose input**
	P11.12	O0		**General-purpose output**
	TOM0_15	O1		**GTM_TOUT**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	GTM_CLK2	O3		**GTM output**
	—	O4		**Reserved**
	CCU61_CC60	O5		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**
	SCU_EXTCLK1	O6		**SCU output**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-39 Port 13 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
128	P13.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CTRAPA			**CCU60 input**
	GPT120_T6EUDB			**GPT120 input**
	P13.0	O0		**General-purpose output**
	TOM0_5	O1		**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**QSPI2 output (aka: SCLK2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-39 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
129	P13.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CCPOS0C			**CCU60 input**
	GPT120_T3INB			**GPT120 input**
	P13.1	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
130	P13.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CCPOS1C			**CCU60 input**
	GPT120_T3EUDB			**GPT120 input**
	GPT120_CAPINA			**GPT120 input**
	P13.2	O0		**General-purpose output**
	TOM0_7	O1		**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-39 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
131	P13.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	CCU60_CCPOS2C			**CCU60 input**
	GPT120_T4INB			**GPT120 input**
	P13.3	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	QSPI2_MTSR	O3		**QSPI2 output (aka: MTSR2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-40 Port 14 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
118	P14.0	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	P14.0	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	ASCLIN0_SCLK	O6		**ASCLIN0 output (aka: ASCLK0)**
	CCU60_COUT62	O7		**CCU60 output**
	IOM_MON1_5			**IOM monitor input**
	IOM_REF1_1			**IOM reference input**

Table 2-40 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
119	P14.1	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	ASCLIN0_RXA			**ASCLIN0 input (aka: ARX0A)**
	CAN1_RXDB			**CAN node 1 input (aka: RXDCAN1B)**
	SCU_REQ15			**SCU input**
	SCU_EVRWUPA	AI		**SCU input**
	P14.1	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_REF1_14			**IOM reference input**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**CCU60 output**
	IOM_MON1_6			**IOM monitor input**
	IOM_REF1_0			**IOM reference input**
120	P14.2	I	A1 / PU / VDDP3	**General-purpose input**
	TIM0_5			**GTM_TIN**
	SCU_HWCFG2_EVR13			**SCU input**
	P14.2	O0		**General-purpose output**
	TOM0_5	O1		**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_REF1_15			**IOM reference input**
	—	O2		**Reserved**
	QSPI2_SLSO1	O3		**QSPI2 output (aka: SLSO21)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-40 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
121	P14.3	I	A1 / PU / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	SCU_REQ10			**SCU input**
	SCU_HWCFG3_BMI			**SCU input**
	P14.3	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_REF2_4			**IOM reference input**
	—	O2		**Reserved**
	QSPI2_SLSO3	O3		**QSPI2 output (aka: SLSO23)**
	ASCLIN1_SLSO	O4		**ASCLIN1 output (aka: ASLSO1)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
122	P14.4	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	P14.4	O0		**General-purpose output**
	TOM0_7	O1		**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_REF2_8			**IOM reference input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-40 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
123	P14.5	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	P14.5	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	IOM_REF2_11			**IOM reference input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
124	P14.6	I	A1+ / PU / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI0_MRSTD			**QSPI0 input (aka: MRST0D)**
	P14.6	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	IOM_REF2_14			**IOM reference input**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**QSPI2 output (aka: SLSO22)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
125	P14.7	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	P14.7	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	IOM_REF2_15			**IOM reference input**
	ASCLIN0_RTS	O2		**ASCLIN0 output (aka: ARTS0)**
	QSPI2_SLSO4	O3		**QSPI2 output (aka: SLSO24)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-40 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
127	P14.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXD			**ASCLIN1 input (aka: ARX1D)**
	CAN2_RXDD			**CAN node 2 input (aka: RXDCAN2D)**
	P14.8	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-41 Port 15 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
109	P15.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	P15.0	O0		**General-purpose output**
	TOM1_3	O1		**GTM_TOUT**
	TOM0_11			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI0_SLSO13	O3		**QSPI0 output (aka: SLSO013)**
	—	O4		**Reserved**
	CAN2_TXD	O5		**CAN node 2 output (aka: TXDCAN2)**
	IOM_MON2_7			**IOM monitor input**
	IOM_REF2_7			**IOM reference input**
	ASCLIN1_SCLK	O6		**ASCLIN1 output (aka: ASCLK1)**
	—	O7		**Reserved**

Table 2-41 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
110	P15.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXA			**ASCLIN1 input (aka: ARX1A)**
	QSPI2_SLSIB			**QSPI2 input (aka: SLSI2B)**
	CAN2_RXDA			**CAN node 2 input (aka: RXDCAN2A)**
	SCU_REQ16			**SCU input**
	SCU_EVRWUPB	AI		**SCU input**
	P15.1	O0		**General-purpose output**
	TOM1_4	O1		**GTM_TOUT (= DTM5_OUT4)**
	TOM0_12			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI2_SLSO5	O3		**QSPI2 output (aka: SLSO25)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
111	P15.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI2_MRSTE			**QSPI2 input (aka: MRST2E)**
	QSPI2_SLSIA			**QSPI2 input (aka: SLSI2A)**
	QSPI2_HSICINA			**QSPI2 input (aka: HSIC2INA)**
	P15.2	O0		**General-purpose output**
	TOM1_5	O1		**GTM_TOUT (= DTM5_OUT5)**
	TOM0_13			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	QSPI2_SLSO0	O3		**QSPI2 output (aka: SLSO20)**
	—	O4		**Reserved**
	CAN1_TXD	O5		**CAN node 1 output (aka: TXDCAN1)**
	IOM_MON2_6			**IOM monitor input**
	IOM_REF2_6			**IOM reference input**
	ASCLIN0_SCLK	O6		**ASCLIN0 output (aka: ASCLK0)**
	—	O7		**Reserved**

Table 2-41 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
112	P15.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN0_RXB			**ASCLIN0 input (aka: ARX0B)**
	QSPI2_SCLKA			**QSPI2 input (aka: SCLK2A)**
	QSPI2_HSICINB			**QSPI2 input (aka: HSIC2INB)**
	CAN1_RXDA			**CAN node 1 input (aka: RXDCAN1A)**
	P15.3	O0		**General-purpose output**
	TOM1_6	O1		**GTM_TOUT (= DTM5_OUT6)**
	TOM0_14			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	QSPI2_SCLK	O3		**QSPI2 output (aka: SCLK2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
113	P15.4	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI2_MRSTA			**QSPI2 input (aka: MRST2A)**
	SCU_REQ0			**SCU input**
	P15.4	O0		**General-purpose output**
	TOM1_7	O1		**GTM_TOUT (= DTM5_OUT7)**
	TOM0_15			**GTM_TOUT**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI2_MRST	O3		**QSPI2 output (aka: MRST2)**
	IOM_MON2_2			**IOM monitor input**
	IOM_REF2_2			**IOM reference input**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**CCU60 output**
	IOM_MON1_0			**IOM monitor input**
	IOM_REF1_4			**IOM reference input**

Table 2-41 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
114	P15.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXB			**ASCLIN1 input (aka: ARX1B)**
	QSPI2_MTSRA			**QSPI2 input (aka: MTSR2A)**
	SCU_REQ13			**SCU input**
	P15.5	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI2_MTSR	O3		**QSPI2 output (aka: MTSR2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC61	O7		**CCU60 output**
	IOM_MON1_1			**IOM monitor input**
	IOM_REF1_5			**IOM reference input**
115	P15.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	QSPI2_MTSRB			**QSPI2 input (aka: MTSR2B)**
	P15.6	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	—	O2		**Reserved**
	QSPI2_MTSR	O3		**QSPI2 output (aka: MTSR2)**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**QSPI2 output (aka: SCLK2)**
	—	O6		**Reserved**
	CCU60_CC60	O7		**CCU60 output**
	IOM_MON1_2			**IOM monitor input**
	IOM_REF1_6			**IOM reference input**

Table 2-41 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
116	P15.7	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI2_MRSTB			**QSPI2 input (aka: MRST2B)**
	P15.7	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	—	O2		**Reserved**
	QSPI2_MRST	O3		**QSPI2 output (aka: MRST2)**
	IOM_MON2_2			**IOM monitor input**
	IOM_REF2_2			**IOM reference input**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**CCU60 output**
	IOM_MON1_3			**IOM monitor input**
	IOM_REF1_3			**IOM reference input**
117	P15.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	QSPI2_SCLKB			**QSPI2 input (aka: SCLK2B)**
	SCU_REQ1			**SCU input**
	P15.8	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**QSPI2 output (aka: SCLK2)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**CCU60 output**
	IOM_MON1_4			**IOM monitor input**
	IOM_REF1_2			**IOM reference input**

Table 2-42 Port 20 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
93	P20.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	SCU_REQ9			**SCU input**
	$\overline{\text{OCDS\_TGI0}}$			**OCDS input**
	GPT120_T6EUDA			**GPT120 input**
	P20.0	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	$\overline{\text{OCDS\_TGO0}}$	O		**OCDS**
94	P20.2	I	Input Only / PU / VDDP3	**General-purpose input**
	$\overline{\text{TESTMODE}}$			**Factory Test Mode Enable**
95	P20.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	GPT120_T6INA			**GPT120 input**
	P20.3	O0		**General-purpose output**
	TOM1_12	O1		**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	IOM_MON1_14			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SLSO9	O3		**QSPI0 output (aka: SLSO09)**
	QSPI2_SLSO9	O4		**QSPI2 output (aka: SLSO29)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-42 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
100	P20.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	P20.6	O0		**General-purpose output**
	TOM1_10	O1		**GTM_TOUT**
	TOM0_10			**GTM_TOUT**
	IOM_MON1_15			**IOM monitor input**
	ASCLIN1_RTS	O2		**ASCLIN1 output (aka: ARTS1)**
	QSPI0_SLSO8	O3		**QSPI0 output (aka: SLSO08)**
	QSPI2_SLSO8	O4		**QSPI2 output (aka: SLSO28)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
101	P20.7	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	ASCLIN1_CTSA			**ASCLIN1 input (aka: ACTS1A)**
	CAN0_RXDB			**CAN node 0 input (aka: RXDCAN0B)**
	P20.7	O0		**General-purpose output**
	TOM1_11	O1		**GTM_TOUT**
	TOM0_11			**GTM_TOUT**
	IOM_MON2_4			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**CCU61 output**
	IOM_MON1_7			**IOM monitor input**
	IOM_REF1_7			**IOM reference input**

Table 2-42 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
102	P20.8	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	P20.8	O0		**General-purpose output**
	TOM1_7	O1		**GTM_TOUT (= DTM5_OUT7)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_MON2_8			**IOM monitor input**
	ASCLIN1_SLSO	O2		**ASCLIN1 output (aka: ASLSO1)**
	QSPI0_SLSO0	O3		**QSPI0 output (aka: SLSO00)**
	QSPI1_SLSO0	O4		**QSPI1 output (aka: SLSO10)**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	SCU_WDT0LCK	O6		**SCU output**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**
103	P20.9	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_RXC			**ASCLIN1 input (aka: ARX1C)**
	QSPI0_SLSIB			**QSPI0 input (aka: SLSI0B)**
	SCU_REQ11			**SCU input**
	P20.9	O0		**General-purpose output**
	TOM1_13	O1		**GTM_TOUT**
	TOM0_13			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	IOM_MON2_11			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**QSPI0 output (aka: SLSO01)**
	QSPI1_SLSO1	O4		**QSPI1 output (aka: SLSO11)**
	—	O5		**Reserved**
	SCU_WDTSLCK	O6		**SCU output**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**

Table 2-42 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
104	P20.10	I	A1 / HighZ / VDDP3	**General-purpose input**
	P20.10	O0		**General-purpose output**
	TOM1_14	O1		**GTM_TOUT**
	TOM0_14			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_MON2_14			**IOM monitor input**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI0_SLSO6	O3		**QSPI0 output (aka: SLSO06)**
	QSPI2_SLSO7	O4		**QSPI2 output (aka: SLSO27)**
	—	O5		**Reserved**
	ASCLIN1_SCLK	O6		**ASCLIN1 output (aka: ASCLK1)**
	CCU61_CC62	O7		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**
105	P20.11	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_SCLKA			**QSPI0 input (aka: SCLK0A)**
	P20.11	O0		**General-purpose output**
	TOM1_15	O1		**GTM_TOUT**
	TOM0_15			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_MON2_15			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**QSPI0 output (aka: SCLK0)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**

Table 2-42 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
106	P20.12	I	A1 / HighZ / VDDP3	**General-purpose input**
	QSPI0_MRSTA			**QSPI0 input (aka: MRST0A)**
	IOM_PIN13			**IOM pad input**
	P20.12	O0		**General-purpose output**
	TOM1_0	O1		**GTM_TOUT**
	TOM0_8			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_MON0_13			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**QSPI0 output (aka: MRST0)**
	IOM_MON2_0			**IOM monitor input**
	IOM_REF2_0			**IOM reference input**
	QSPI0_MTSR	O4		**QSPI0 output (aka: MTSR0)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**
107	P20.13	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_SLSIA			**QSPI0 input (aka: SLSI0A)**
	IOM_PIN14			**IOM pad input**
	P20.13	O0		**General-purpose output**
	TOM1_1	O1		**GTM_TOUT**
	TOM0_9			**GTM_TOUT**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_MON0_14			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**QSPI0 output (aka: SLSO02)**
	QSPI1_SLSO2	O4		**QSPI1 output (aka: SLSO12)**
	QSPI0_SCLK	O5		**QSPI0 output (aka: SCLK0)**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**

Table 2-42 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
108	P20.14	I	A1+ / HighZ / VDDP3	**General-purpose input**
	QSPI0_MTSRA			**QSPI0 input (aka: MTSR0A)**
	IOM_PIN15			**IOM pad input**
	P20.14	O0		**General-purpose output**
	TOM1_2	O1		**GTM_TOUT**
	TOM0_10			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_MON0_15			**IOM monitor input**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**QSPI0 output (aka: MTSR0)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-43 Port 21 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
84	P21.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	SCU_EMGSTOPB			**SCU input**
	P21.2	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_4			**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-43 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
85	P21.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	P21.3	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_4N			**GTM_TOUT (= DTM1_OUT4_N)**
	TOM1_4N			**GTM_TOUT (= DTM5_OUT4_N)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
86	P21.4	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	P21.4	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-43 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
87	P21.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	P21.5	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
88	P21.6	I	A1 / PU / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	TDI			**OCDS input**
	$\overline{\text{OCDS\_TGI2}}$			**OCDS input**
	GPT120_T5EUDA			**GPT120 input**
	P21.6	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**GPT120 output**
	$\overline{\text{OCDS\_TGO2}}$	O		**OCDS**

Table 2-43 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
90	P21.7	I	A1+ / PU / VDDP3	**General-purpose input**
	TIM0_5			**GTM_TIN**
	OCDS_DAP2			**OCDS input**
	$\overline{\text{OCDS\_TGI3}}$			**OCDS input**
	GPT120_T5INA			**GPT120 input**
	P21.7	O0		**General-purpose output**
	TOM0_5	O1		**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**GPT120 output**
	$\overline{\text{OCDS\_TGO3}}$	O		**OCDS**
	OCDS_DAP2	O		**OCDS Output**
	TDO	O		**JTAG Output**

Table 2-44 Port 22 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P22.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI3_MTSRE			**QSPI3 input (aka: MTSR3E)**
	P22.0	O0		**General-purpose output**
	TOM0_9	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**QSPI3 output (aka: MTSR3)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-44 Port 22 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
75	P22.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	QSPI3_MRSTE			**QSPI3 input (aka: MRST3E)**
	P22.1	O0		**General-purpose output**
	TOM0_8	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	—	O2		**Reserved**
	QSPI3_MRST	O3		**QSPI3 output (aka: MRST3)**
	IOM_MON2_3			**IOM monitor input**
	IOM_REF2_3			**IOM reference input**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
76	P22.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	QSPI3_SLSID			**QSPI3 input (aka: SLSI3D)**
	P22.2	O0		**General-purpose output**
	TOM0_11	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	—	O2		**Reserved**
	QSPI3_SLSO12	O3		**QSPI3 output (aka: SLSO312)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-44 Port 22 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
77	P22.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	QSPI3_SCLKE			**QSPI3 input (aka: SCLK3E)**
	P22.3	O0		**General-purpose output**
	TOM0_12	O1		**GTM_TOUT**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**QSPI3 output (aka: SCLK3)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
78	P22.4	I	A1 / HighZ / VDDP3	**General-purpose input**
	P22.4	O0		**General-purpose output**
	TOM0_7N	O1		**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_SLSO12	O4		**QSPI0 output (aka: SLSO012)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-45 Port 23 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P23.1	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	P23.1	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM0_15			**GTM_TOUT**
	ASCLIN1_RTS	O2		**ASCLIN1 output (aka: ARTS1)**
	QSPI3_SLSO13	O3		**QSPI3 output (aka: SLSO313)**
	GTM_CLK0	O4		**GTM output**
	SCU_EXTCLK1	O5		**SCU output**
	SCU_EXTCLK0	O6		**SCU output**
	—	O7		**Reserved**

Table 2-46 Port 33 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
56	P33.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	IOM_PIN0			**IOM pad input**
	P33.0	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	IOM_MON0_0			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	VADC_G1BFL0	O6		**VADC output**
	—	O7		**Reserved**

Table 2-46 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
57	P33.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_5			**GTM_TIN**
	IOM_PIN1			**IOM pad input**
	P33.1	O0		**General-purpose output**
	TOM0_5	O1		**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_MON0_1			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_EMUX02	O5		**VADC output**
	VADC_G1BFL1	O6		**VADC output**
	—	O7		**Reserved**
58	P33.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_6			**GTM_TIN**
	IOM_PIN2			**IOM pad input**
	P33.2	O0		**General-purpose output**
	TOM0_6	O1		**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_MON0_2			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_EMUX01	O5		**VADC output**
	VADC_G1BFL2	O6		**VADC output**
	CCU61_COUT63	O7		**CCU61 output**
	IOM_MON1_7			**IOM monitor input**
	IOM_REF1_7			**IOM reference input**

Table 2-46 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
59	P33.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_7			**GTM_TIN**
	IOM_PIN3			**IOM pad input**
	P33.3	O0		**General-purpose output**
	TOM0_7	O1		**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_MON0_3			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_EMUX00	O5		**VADC output**
	VADC_G1BFL3	O6		**VADC output**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**
60	P33.4	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	CCU61_CTRAPC			**CCU61 input**
	IOM_PIN4			**IOM pad input**
	P33.4	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	IOM_MON0_4			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	VADC_EMUX12	O5		**VADC output**
	VADC_G0BFL0	O6		**VADC output**
	—	O7		**Reserved**

Table 2-46 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
61	P33.5	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	CCU61_CCPOS2C			**CCU61 input**
	GPT120_T4EUDB			**GPT120 input**
	IOM_PIN5			**IOM pad input**
	P33.5	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_5			**GTM_TOUT (= DTM1_OUT5)**
	TOM1_5			**GTM_TOUT (= DTM5_OUT5)**
	IOM_MON0_5			**IOM monitor input**
	QSPI0_SLSO7	O2		**QSPI0 output (aka: SLSO07)**
	QSPI1_SLSO7	O3		**QSPI1 output (aka: SLSO17)**
	—	O4		**Reserved**
	VADC_EMUX11	O5		**VADC output**
	VADC_G0BFL1	O6		**VADC output**
	CCU61_CC60	O7		**CCU61 output**
	IOM_MON1_8			**IOM monitor input**
	IOM_REF1_13			**IOM reference input**

Table 2-46 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
62	P33.6	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	ASCLIN1_RXF			**ASCLIN1 input (aka: ARX1F)**
	CCU61_CCPOS1C			**CCU61 input**
	GPT120_T2EUDB			**GPT120 input**
	IOM_PIN6			**IOM pad input**
	P33.6	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	TOM0_5N			**GTM_TOUT (= DTM1_OUT5_N)**
	TOM1_5N			**GTM_TOUT (= DTM5_OUT5_N)**
	IOM_MON0_6			**IOM monitor input**
	—	O2		**Reserved**
	—	O3		**Reserved**
	ASCLIN1_TX	O4		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	VADC_EMUX10	O5		**VADC output**
	VADC_G0BFL2	O6		**VADC output**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**

Table 2-46 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
63	P33.7	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_3			**GTM_TIN**
	CAN0_RXDE			**CAN node 0 input (aka: RXDCAN0E)**
	SCU_REQ8			**SCU input**
	CCU61_CCPOS0C			**CCU61 input**
	GPT120_T2INB			**GPT120 input**
	IOM_PIN7			**IOM pad input**
	P33.7	O0		**General-purpose output**
	TOM0_3	O1		**GTM_TOUT**
	TOM1_3			**GTM_TOUT**
	TOM0_6			**GTM_TOUT (= DTM1_OUT6)**
	TOM1_6			**GTM_TOUT (= DTM5_OUT6)**
	IOM_MON0_7			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO7	O3		**QSPI3 output (aka: SLSO37)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	VADC_G0BFL3	O6		**VADC output**
	CCU61_COUT60	O7		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**

Table 2-46 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
64	P33.8	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_4			**GTM_TIN**
	SCU_EMGSTOPA			**SCU input**
	IOM_PIN8			**IOM pad input**
	P33.8	O0		**General-purpose output**
	TOM0_4	O1		**GTM_TOUT (= DTM1_OUT4)**
	TOM1_4			**GTM_TOUT (= DTM5_OUT4)**
	TOM0_6N			**GTM_TOUT (= DTM1_OUT6_N)**
	TOM1_6N			**GTM_TOUT (= DTM5_OUT6_N)**
	IOM_MON0_8			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**QSPI3 output (aka: SLSO32)**
	—	O4		**Reserved**
	CAN0_TXD	O5		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**CCU61 output**
	IOM_MON1_13			**IOM monitor input**
	IOM_REF1_8			**IOM reference input**
	SMU_FSP	O		**SMU**

Table 2-46 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
65	P33.9	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_1			**GTM_TIN**
	QSPI3_HSICINA			**QSPI3 input (aka: HSIC3INA)**
	IOM_PIN9			**IOM pad input**
	P33.9	O0		**General-purpose output**
	TOM0_1	O1		**GTM_TOUT**
	TOM1_1			**GTM_TOUT**
	TOM0_7			**GTM_TOUT (= DTM1_OUT7)**
	TOM1_7			**GTM_TOUT (= DTM5_OUT7)**
	IOM_MON0_9			**IOM monitor input**
	—	O2		**Reserved**
	QSPI3_SLSO1	O3		**QSPI3 output (aka: SLSO31)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC62	O7		**CCU61 output**
	IOM_MON1_10			**IOM monitor input**
	IOM_REF1_11			**IOM reference input**
66	P33.10	I	A1+ / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	QSPI3_SLSIC			**QSPI3 input (aka: SLSI3C)**
	QSPI3_HSICINB			**QSPI3 input (aka: HSIC3INB)**
	IOM_PIN10			**IOM pad input**
	P33.10	O0		**General-purpose output**
	TOM0_0	O1		**GTM_TOUT**
	TOM1_0			**GTM_TOUT**
	TOM0_7N			**GTM_TOUT (= DTM1_OUT7_N)**
	TOM1_7N			**GTM_TOUT (= DTM5_OUT7_N)**
	IOM_MON0_10			**IOM monitor input**
	QSPI1_SLSO6	O2		**QSPI1 output (aka: SLSO16)**
	QSPI3_SLSO11	O3		**QSPI3 output (aka: SLSO311)**
	ASCLIN1_SLSO	O4		**ASCLIN1 output (aka: ASLSO1)**
	GTM_CLK1	O5		**GTM output**
	SCU_EXTCLK1	O6		**SCU output**
	CCU61_COUT61	O7		**CCU61 output**
	IOM_MON1_12			**IOM monitor input**
	IOM_REF1_9			**IOM reference input**

Table 2-46 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
67	P33.11	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_2			**GTM_TIN**
	QSPI3_SCLKD			**QSPI3 input (aka: SCLK3D)**
	SCU_REQ17			**SCU input**
	IOM_PIN11			**IOM pad input**
	P33.11	O0		**General-purpose output**
	TOM0_2	O1		**GTM_TOUT**
	TOM1_2			**GTM_TOUT**
	IOM_MON0_11			**IOM monitor input**
	ASCLIN1_SCLK	O2		**ASCLIN1 output (aka: ASCLK1)**
	QSPI3_SCLK	O3		**QSPI3 output (aka: SCLK3)**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**CCU61 output**
	IOM_MON1_9			**IOM monitor input**
	IOM_REF1_12			**IOM reference input**
68	P33.12	I	A1 / HighZ / VDDP3	**General-purpose input**
	TIM0_0			**GTM_TIN**
	QSPI3_MTSRD			**QSPI3 input (aka: MTSR3D)**
	IOM_PIN12			**IOM pad input**
	P33.12	O0		**General-purpose output**
	TOM1_12	O1		**GTM_TOUT**
	TOM0_12			**GTM_TOUT**
	IOM_MON0_12			**IOM monitor input**
	ASCLIN1_TX	O2		**ASCLIN1 output (aka: ATX1)**
	IOM_MON2_13			**IOM monitor input**
	IOM_REF2_13			**IOM reference input**
	QSPI3_MTSR	O3		**QSPI3 output (aka: MTSR3)**
	ASCLIN1_SCLK	O4		**ASCLIN1 output (aka: ASCLK1)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**CCU61 output**
	IOM_MON1_11			**IOM monitor input**
	IOM_REF1_10			**IOM reference input**

Table 2-47 Port 34 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
52	P34.0	I	A1 / HighZ / VDDP3	**General-purpose input**
	P34.0	O0		**General-purpose output**
	TOM1_12	O1		**GTM_TOUT**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
53	P34.1	I	A1 / HighZ / VDDP3	**General-purpose input**
	P34.1	O0		**General-purpose output**
	TOM1_13	O1		**GTM_TOUT**
	ASCLIN0_TX	O2		**ASCLIN0 output (aka: ATX0)**
	IOM_MON2_12			**IOM monitor input**
	IOM_REF2_12			**IOM reference input**
	—	O3		**Reserved**
	CAN0_TXD	O4		**CAN node 0 output (aka: TXDCAN0)**
	IOM_MON2_5			**IOM monitor input**
	IOM_REF2_5			**IOM reference input**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
54	P34.2	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN0_RXD			**ASCLIN0 input (aka: ARX0D)**
	CAN0_RXDG			**CAN node 0 input (aka: RXDCAN0G)**
	P34.2	O0		**General-purpose output**
	TOM1_14	O1		**GTM_TOUT**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-47 Port 34 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
55	P34.3	I	A1 / HighZ / VDDP3	**General-purpose input**
	ASCLIN1_CTSB			**ASCLIN1 input (aka: ACTS1B)**
	P34.3	O0		**General-purpose output**
	TOM1_15	O1		**GTM_TOUT**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI2_SLSO10	O4		**QSPI2 output (aka: SLSO210)**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-48 Port 40 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
51	P40.0	I	S / VDDM	**General-purpose input**
	VADCG0_0	AI		**VADC input channel 0 of group 0**
50	P40.1	I	S / VDDM	**General-purpose input**
	VADCG0_1	AI		**VADC input channel 1 of group 0** (with multiplexer diagnostics)
49	P40.2	I	S / VDDM	**General-purpose input**
	VADCG0_2	AI		**VADC input channel 2 of group 0** (with multiplexer diagnostics)
48	P40.3	I	S / VDDM	**General-purpose input**
	VADCG0_3	AI		**VADC input channel 3 of group 0**
47	P40.4	I	S / VDDM	**General-purpose input**
	VADCG0_4	AI		**VADC input channel 4 of group 0**
46	P40.5	I	S / VDDM	**General-purpose input**
	VADCG0_5	AI		**VADC input channel 5 of group 0**
45	P40.6	I	S / VDDM	**General-purpose input**
	VADCG0_6	AI		**VADC input channel 6 of group 0**
40	P40.7	I	S / VDDM	**General-purpose input**
	VADCG0_7	AI		**VADC input channel 7 of group 0** (with pull down diagnostics)
39	P40.8	I	S / VDDM	**General-purpose input**
	VADCG0_8	AI		**VADC input channel 8 of group 0**
38	P40.9	I	S / VDDM	**General-purpose input**
	VADCG0_9	AI		**VADC input channel 9 of group 0** (with multiplexer diagnostics)

Table 2-48 Port 40 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
37	P40.10	I	S / VDDM	**General-purpose input**
	VADCG0_10	AI		**VADC input channel 10 of group 0** (with multiplexer diagnostics)
36	P40.11	I	S / VDDM	**General-purpose input**
	SENT_SENT0A			**SENT input**
	CCU60_CCPOS0D			**CCU60 input**
	VADCG0_11	AI		**VADC input channel 11 of group 0**

Table 2-49 Port 41 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
35	P41.0	I	S / VDDM	**General-purpose input**
	SENT_SENT1A			**SENT input**
	CCU60_CCPOS1B			**CCU60 input**
	VADCG1_0	AI		**VADC input channel 0 of group 1**
34	P41.1	I	S / VDDM	**General-purpose input**
	VADCG1_1	AI		**VADC input channel 1 of group 1** (with multiplexer diagnostics)
33	P41.2	I	S / VDDM	**General-purpose input**
	SENT_SENT2A			**SENT input**
	CCU61_CCPOS1B			**CCU61 input**
	VADCG1_2	AI		**VADC input channel 2 of group 1** (with multiplexer diagnostics)
32	P41.3	I	S / VDDM	**General-purpose input**
	SENT_SENT3A			**SENT input**
	CCU61_CCPOS1D			**CCU61 input**
	VADCG1_3	AI		**VADC input channel 3 of group 1** (with pull down diagnostics)
31	P41.4	I	S / VDDM	**General-purpose input**
	VADCG1_4	AI		**VADC input channel 4 of group 1**
30	P41.5	I	S / VDDM	**General-purpose input**
	VADCG1_5	AI		**VADC input channel 5 of group 1**
29	P41.6	I	S / VDDM	**General-purpose input**
	VADCG1_6	AI		**VADC input channel 6 of group 1**
28	P41.7	I	S / VDDM	**General-purpose input**
	VADCG1_7	AI		**VADC input channel 7 of group 1**
27	P41.8	I	S / VDDM	**General-purpose input**
	VADCG1_8	AI		**VADC input channel 8 of group 1**

Table 2-49 Port 41 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
26	P41.9	I	S / VDDM	**General-purpose input**
	VADCG1_9	AI		**VADC input channel 9 of group 1** (with multiplexer diagnostics)
25	P41.10	I	S / VDDM	**General-purpose input**
	VADCG1_10	AI		**VADC input channel 10 of group 1** (with multiplexer diagnostics)
24	P41.11	I	S / VDDM	**General-purpose input**
	VADCG1_11	AI		**VADC input channel 11 of group 1**

Table 2-50 System I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
81	XTAL1	I	VDDP3	**Main Oscillator/PLL/Clock Generator Input**
82	XTAL2	O	VDDP3	**Main Oscillator/PLL/Clock Generator Output**
89	TMS/DAP1	I	A1+ / PD / VDDP3	**Debug Interface**
	DAP1	I/O		**Device Access Port LIne 1**
91	$\overline{\text{TRST}}$	I	Input Only / PD / VDDP3	**JTAG Module Reset/Enable Input**
92	TCK/DAP0	I	Input Only / PD / VDDP3	**OCDS input**
	DAP0	I		**Device Access Port LIne 0**
96	$\overline{\text{ESR1}}$	I/O	A1+ / PU / VDDP3	**SCU input**
	EVRWUP	I		**EVR Wakeup Pin**
97	$\overline{\text{PORST}}$	I	Input Only / PD / VDDP3	**Power On Reset** Additional strong PD in case of power fail.
98	$\overline{\text{ESR0}}$	I/O	A1+ / OD / VDDP3	**SCU input/output**
	EVRWUP	I		**EVR Wakeup Pin**

Table 2-51 Supply

Pin	Symbol	Ctrl.	Buffer Type	Function
41	V_{AGND}	I	—	**Negative Analog Reference Voltage 0**
42	V_{AREF}	I	—	**Positive Analog Reference Voltage 0**
126	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)** This pin supplies also the Flash 3.3V.
69	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)**

Table 2-51 Supply (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
79	V_{DD}	I	—	**Digital Core Power Supply (1.3V)** This pin supplies also the main XTAL Oscillator/PLL (1.3V). A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity.
83	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)** This pin supplies also the main XTAL Oscillator/PLL (3.3V). A higher decoupling capacitor is therefore recommended to the VSS pin for better noise immunity.
44	V_{DDM}	I	—	**ADC Power Supply (5.0V)**
23	V_{DDP3}	I	—	**Digital I/O Power Supply (3.3V)**
10	V_{DD}	I	—	**Digital Core Power Supply (1.3V)**
22	V_{DD}	I	—	**Digital Core Power Supply (1.3V)**
99	V_{DD}	I	—	**Digital Core Power Supply (1.3V)**
43	V_{SSM}	I	—	**Analog Ground for VDDM**
80	V_{SS}	I	—	**Digital Ground**

2.3.2 Pull-Up/Pull-Down Reset Behavior of the Pins

Table 2-52 List of Pull-Up/Pull-Down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
all GPIOs	High-Z	
TDI, TESTMODE	Pull-up	
PORST[1)]	Pull-down with I_{PORST} relevant	Pull-down with I_{PDLI} relevant
TRST, TCK, TMS	Pull-down	
ESR0	The open-drain driver is used to drive low.[2)]	Pull-up[3)]
ESR1	Pull-up[3)]	
P14.2, P14.3, P14.6	Pull-up	
P21.7 / TDO	Pull-up	High-Z/Pull-up[4)]

1) Pull-down with I_{PORST} relevant is always activated when a primary supply monitor detects a violation.
2) Valid additionally after deactivation of PORST until the internal reset phase has finished. See the SCU chapter for details.
3) See the SCU_IOCR register description.
4) Depends on JTAG/DAP selection with TRST.

3 Electrical Specification

3.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC212 / TC213 / TC214 / TC222 / TC223 / TC224 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC212 / TC213 / TC214 / TC222 / TC223 / TC224 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC212 / TC213 / TC214 / TC222 / TC223 / TC224 designed in.

3.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the Operational Conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} SR	-65	-	170	°C	upto 65h @ T_J = 150°C; upto 15h @ T_J = 170°C
Voltage at V_{DD} power supply pins with respect to V_{SS} 1)	V_{DD} SR	-	-	1.9	V	
Voltage at V_{DDP3} power supply pins with respect to V_{SS}	V_{DDP3} SR	-	-	4.43	V	
Voltage at V_{DDM} power supply pin with respect to V_{SS}	V_{DDM} SR	-	-	7.0	V	
Voltage on all analog and class S input pins with respect to V_{SS} 2)	V_{IN} SR	-0.5	-	7.0	V	
Voltage on all other input pins with respect to V_{SS} 1)2)	V_{IN} SR	-0.5	-	min(V_{DDP3} + 0.6 , 4.23)	V	Whatever is lower
Input current on any pin during overload condition 3)	I_{IN} SR	-10	-	10	mA	
Absolute maximum sum of all input circuit currents during overload condition 3)	ΣI_{IN} SR	-100	-	100	mA	

1) Valid for cumulated for up to 2.8h and pulse forms following a power supply switch on phase, where the rise and fall times are releated to the system capacities and coils.

2) Voltages below V_{INmin} have no Impact to the device reliabiltiy as Long as the times and currents defined in section Pin Reliability in Overload for the affected pad(s) are not violated.

3) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device.

3.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels
  - temperature
- Parameters defined in **Absolute Maximum Ratings** are not violated

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Table 3-2 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	
Input current on analog input pin during overload condition	I_{INANA}	-1	-	3	mA	
		-5	-	5	mA	limited to 60h over lifetime
Absolute sum of all ADC inputs during overload condition	I_{INSCA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{INS}	-100	-	100	mA	
Inactive device pin current during overload condtion [1]	I_{ID}	-1	-	1	mA	All power supply voltages V_{DDx} = 0
Sum of all inactive device pin currents [1]	I_{IDS}	-100	-	100	mA	
Overload coupling factor for digital inputs, negative [2]	K_{OVDN} CC	-	-	$2*10^{-3}$		Overload injected on GPIO pad and affecting neighbor GPIO pad
Overload coupling factor for digital inputs, positive [2]	K_{OVDP} CC	-	-	$1*10^{-5}$		Overload injected on GPIO pad and affecting neighbor GPIO pad
Overload coupling factor for analog inputs, negative	K_{OVAN} CC	-	-	$1*10^{-3}$		Analog Inputs overlaid with pull down diagnostics
		-	-	$1*10^{-4}$		else

Table 3-2 Overload Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, positive	K_{OVAP} CC	-	-	$1*10^{-4}$		Analog Inputs overlaid with pull down diagnostics
		-	-	$1*10^{-5}$		else

1) Limitations for time and supply levels specified in this section are not valid for this parameter.
2) Overload is measured as increase of pad leakage caused by injection on neighbor pad.

Table 3-3 PN-Junction Characteristics for positive Overload

Pad Type	I_{IN} = 3 mA	I_{IN} = 5 mA
A1 / A1+	$U_{IN} = V_{DDP3}$ + 0.5 V	$U_{IN} = V_{DDP3}$ + 0.6 V
D	$U_{IN} = V_{DDM}$ + 0.75 V	-

Table 3-4 PN-Junction Characteristics for negative Overload

Pad Type	I_{IN} = -3 mA	I_{IN} = -5 mA
A1 / A1+	$U_{IN} = V_{SS}$ - 0.5 V	$U_{IN} = V_{SS}$ - 0.6 V
D	$U_{IN} = V_{SS}$ - 0.75 V	-

3.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC212 / TC213 / TC214 / TC222 / TC223 / TC224. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC212 / TC213 / TC214 / TC222 / TC223 / TC224 must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise noticed in the Note / Test Condition column.

Table 3-5 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SRI frequency	f_{SRI} SR	-	-	133	MHz	
Max System Frequency	f_{MAX} SR	-	-	133	MHz	
CPU0 Frequency	f_{CPU0} SR	-	-	133	MHz	
PLL output frequency	f_{PLL} SR	20	-	200	MHz	
SPB frequency	f_{SPB} SR	-	-	100	MHz	
ASCLIN fast frequency	$f_{ASCLINF}$ SR	-	-	133	MHz	
ASCLIN slow frequency	$f_{ASCLINS}$ SR	-	-	100	MHz	
Baud2 frequency	f_{BAUD2} SR	-	-	133	MHz	
FSI2 frequency	f_{FSI2} SR	-	-	133	MHz	
FSI frequency	f_{FSI} SR	-	-	100	MHz	
GTM frequency	f_{GTM} SR	-	-	100	MHz	
STM frequency	f_{STM} SR	-	-	100	MHz	
MultiCAN frequency	f_{CAN} SR	-	-	100	MHz	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	-	-	100	mA	
Ambient Temperature	T_A SR	-40	-	125	°C	valid for all SAK products
		-40	-	150	°C	valid for all SAL products
Junction Temperature	T_J SR	-40	-	150	°C	valid for all SAK products
		-40	-	165	°C	valid for all SAL products
Core Supply Voltage [1]	V_{DD} SR	1.17	1.3	1.43 [2]	V	Only required if externally supplied
ADC analog supply voltage	V_{DDM} SR	2.97	5.0	5.5 [3]	V	
Digital ground voltage	V_{SS} SR	0	-	-	V	
Analog ground voltage for V_{DDM}	V_{SSM} CC	-0.1	0	0.1	V	

Table 3-5 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage to ensure defined pad states [4]	V_{DDPPA} CC	0.72	-	-	V	
Digital supply voltage for GPIO pads and EVR [5]	V_{DDP3} SR	2.97	3.3	3.63	V	

1) No external inductive load permissible if EVR is used. All V_{DD} pins shall be connected together externally on the PCB.
2) Voltage overshoot to 1.69V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
3) Voltage overshoot to 6.5V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
4) This parameter is valid under the assumption the PORST signal is constantly at low level during the power-up/power-down of V_{DDP3}.
5) All V_{DDP3} pins shall be connected together externally on the PCB.

3.5 3.3 V Pads

Table 3-6 Standard_Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	-	6	10	pF	
Spike filter always blocked pulse duration	t_{SF1} CC	-	-	80	ns	PORST only
Spike filter pass-through pulse duration	t_{SF2} CC	220	-	-	ns	PORST only
PORST pad output current [1]	I_{PORST} CC	10.1	-	-	mA	V_{DDP3} = 3.0V; V_{PORST} = 0.9V; T_J = 150°C;

1) Pull-down with I_{PORST} relevant is always activated when a primary supply monitor detects a violation.

Table 3-7 Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} SR	-	-	100	MHz	
Input Hysteresis A1	$HYSA1$ CC	0.1 * V_{DDP3}	-	-	V	
Input Leakage Current Class A1	I_{OZA1} CC	-400	-	400	nA	(0.1*V_{DDP3}) < V_{IN} < (0.9*V_{DDP3})
		-475	-	475	nA	(0.1*V_{DDP3}) < V_{IN} < (0.9*V_{DDP3}); only vaild for P0.0
		-800	-	800	nA	else
Pull-down current class A1 pads	I_{PDLA1} CC	-	-	|120|	µA	V_{IHmin}
		|15|	-	-	µA	V_{ILmax}
Pull-up current class A1 pads	I_{PUHA1} CC	|15|	-	-	µA	V_{IHmin}
		-	-	|120|	µA	V_{ILmax}
On-Resistance of the A1 pad, medium driver	$R_{DSONA1M}$ CC	50	125	200	Ohm	I_{OH}=2mA; I_{OL}=2mA
On-Resistance of the class A1 pad, weak driver	$R_{DSONA1W}$ CC	250	500	800	Ohm	I_{OH}=0.5mA; I_{OL}=0.5mA
Input high voltage class A1 pads	V_{IHA1} CC	0.7 * V_{DDP3}	-	-	V	CMOS
Input low voltage, class A1 pads	V_{ILA1} CC	-	-	0.3 * V_{DDP3}	V	CMOS

Table 3-7 Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise/fall time [1]	t_{A1} CC	-	-	10+0.4 * C_L	ns	C_L≤100pF; pin out driver=medium
		-	-	30+2.0 * C_L	ns	C_L≤100pF; pin out driver=weak

1) Rise / fall times are defined 10% - 90% of V_{DDP3}.

Table 3-8 Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} SR	-	-	75	MHz	
Input Leakage Current Class A1+	I_{OZA1+} CC	-1	-	1	µA	(0.1*V_{DDP3}) < V_{IN} < (0.9*V_{DDP3})
		-2	-	2	µA	else
Pull-down current class A1+ pads	I_{PDLA1+} CC	-	-	|120|	µA	V_{IHmin}
		|15|	-	-	µA	V_{ILmax}
Pull-up current class A1+ pads	I_{PUHA1+} CC	|15|	-	-	µA	V_{IHmin}
		-	-	|120|	µA	V_{ILmax}
On-Resistance of the A1+ pad, medium driver	$R_{DSONA1+M}$ CC	50	125	200	Ohm	I_{OH}=2mA; I_{OL}=2mA
On-Resistance of the A1+ pad, strong driver	$R_{DSONA1+S}$ CC	10	40	65	Ohm	I_{OH}=6mA; I_{OL}=6mA
On-Resistance of the A1+ pad, weak driver	$R_{DSONA1+W}$ CC	250	500	800	Ohm	I_{OH}=0.5mA; I_{OL}=0.5mA
Input high voltage, Class A1+ pads	V_{IHA1+} CC	0.7 * V_{DDP3}	-	-	V	CMOS
Input low voltage Class A1+ pads	V_{ILA1+} CC	-	-	0.3 * V_{DDP3}	V	CMOS
Rise/fall time [1]	t_{A1+} CC	-	-	8+0.14 * C_L	ns	C_L≤100pF; edge=slow ; pin out driver=strong (sw)
		-	-	1+0.14 * C_L	ns	C_L≤100pF; edge=soft ; pin out driver=strong (sf)
		-	-	10+0.4 * C_L	ns	C_L≤100pF; pin out driver=medium
		-	-	30+2.0 * C_L	ns	C_L≤100pF; pin out driver=weak
Input Hysteresis A1+	HYSA1+ CC	0.1 * V_{DDP3}	-	-	V	

1) Rise / fall times are defined 10% - 90% of V_{DDP3}.

Table 3-9 Class_S

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} SR	-	-	75	MHz	
Input Hysteresis for S pad [1]	$HYSS$ CC	0.3	-	-	V	
Pull-up current for S pad	I_{PUHS} CC	|11|	-	-	µA	V_{IHmin}
		-	-	|120|	µA	V_{ILmax}
Pull-down current for S pad	I_{PDLS} CC	-	-	|120|	µA	V_{IHmin}
		|30|	-	-	µA	V_{ILmax}
Input Leakage current Class S	I_{OZS} CC	-350	-	350	nA	Analog Inputs overlaid with pull down diagnosis
		-150	-	150	nA	else
Input voltage high for S pad	V_{IHS} SR	-	-	3.8 [2]	V	
Input voltage low for S pad	V_{ILS} SR	1.39 [3]	-	-	V	
Input low threshold variation for S pad [4]	V_{ILSD} SR	-50	-	50	mV	max. variation of 1ms; V_{DDM}=constant
Input capacitance for S pad	C_{INS} CC	-	-	10	pF	
Pad set-up time for S pad	t_{SETS} CC	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) V_{ILx} = 0.65 * V_{DDM}
3) V_{ILx} = 0.41 * V_{DDM}
4) VILSD is implemented to ensure J2716 specification. For details of dedicated pins please see AP32286 for details.

Table 3-10 Class I

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} SR	-	-	100	MHz	
Input Hysteresis for I pad [1]	$HYSI$ CC	0.1 * V_{DDP3}	-	-	V	
Pull-up current for I pad	I_{PUHI} CC	|15|	-	-	µA	V_{IHImin}
		-	-	|120|	µA	V_{ILImax}
Pull-down current for I pad	I_{PDLI} CC	-	-	|120|	µA	V_{IHImin}
		|15|	-	-	µA	V_{ILImax}
Input Leakage Current for I pad	I_{OZI} CC	-150	-	150	nA	$(0.1*V_{DDP3}) < V_{IN} < (0.9*V_{DDP3})$
		-500	-	350	nA	else
Input high voltage for I pad	V_{IHI} SR	0.7 * V_{DDP3}	-	-	V	CMOS

Table 3-10 Class I (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage for I pad	V_{ILI} SR	-	-	0.3 * V_{DDP3}	V	CMOS
Pad set-up time for I pad	t_{SETI} CC	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

Table 3-11 Driver Mode Selection for A1 Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	X	0	Speed grade 1	medium (A1m)
X	X	1	Speed grade 2	weak (A1w)

Table 3-12 Driver Mode Selection for A1+ Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong soft edge (A1+sf)
X	0	1	Speed grade 2	Strong slow edge (A1+sw)
X	1	0	Speed grade 3	medium (A1+m)
X	1	1	Speed grade 4	weak (A1+w)

3.6 VADC Parameters

VADC parameter are valid for V_{DDM} = 4.5 V to 5.5 V.

This table also covers the parameters for Class D pads.

Table 3-13 VADC

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage [1]	V_{AREF} SR	V_{AGND} + 1.0	-	V_{DDM} + 0.05	V	
Analog reference ground	V_{AGND} SR	V_{SSM} - 0.05	-	V_{SSM} + 0.05	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	-	V_{AREF}	V	
Converter reference clock	f_{ADCI} SR	2	-	20	MHz	
Charge consumption per conversion [2] [3]	Q_{CONV} CC	-	50	75	pC	V_{AIN} = 5 V, charge consumed from reference pin, precharging disabled
		-	10	22	pC	V_{AIN} = 5 V, charge consumed from reference pin, precharging enabled
Conversion time for 12-bit result	t_{C12} CC	-	(16 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time and post calibration
Conversion time for 10-bit result	t_{C10} CC	-	(14 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time
Conversion time for 8-bit result	t_{C8} CC	-	(12 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time
Conversion time for fast compare mode	t_{CF} CC	-	(4 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time
Broken wire detection delay against V_{AGND} [4]	t_{BWG} CC	-	-	120	cycles	Result below 10%
Broken wire detection delay against V_{AREF} [5]	t_{BWR} CC	-	-	60	cycles	Result above 80%
Input leakage at analog inputs	I_{OZ1} CC	-350	-	350	nA	Analog Inputs overlaid with pull down diagnosis
		-150	-	150	nA	else
Total Unadjusted Error [1]	TUE CC	-4 [6]	-	4 [6]	LSB	12-bit resolution

Table 3-13 VADC (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
INL Error	EA_{INL} CC	-3	-	3	LSB	12-bit resolution
Gain Error [1]	EA_{GAIN} CC	-3.5	-	3.5	LSB	12-bit resolution
DNL error [1]	EA_{DNL} CC	-3	-	3	LSB	12-bit resolution
Offset Error [1]	EA_{OFF} CC	-4	-	4	LSB	12-bit resolution
Total capacitance of an analog input	C_{AINT} CC	-	-	30	pF	
Switched capacitance of an analog input	C_{AINS} CC	2	-	7	pF	
Resistance of the analog input path	R_{AIN} CC	-	-	1.5	kOhm	
		-	-	1.8	kOhm	valid for analog inputs mapped to GPIOs
Switched capacitance of a reference input	C_{AREFS} CC	-	-	30	pF	
RMS Noise [7]	EN_{RMS} CC	-	0.5	0.8 [6][8]	LSB	
Positive reference V_{AREFx} pin leakage	I_{OZ2} CC	-2	-	2	µA	$V_{AREFx} = V_{AREF}$; T_J>150°C
		-1	-	1	µA	$V_{AREFx} = V_{AREF}$; T_J≤150°C
Negative reference V_{AGNDx} pin leakage	I_{OZ3} CC	-2.5	-	2.5	µA	$V_{AGNDx} = V_{AGND}$; T_J>150°C
		-1.5	-	1.5	µA	$V_{AGNDx} = V_{AGND}$; T_J≤150°C
Resistance of the reference input path	R_{AREF} CC	-	-	1	kOhm	
CSD resistance [9]	R_{CSD} CC	-	-	28	kOhm	
Resistance of the multiplexer diagnostics pull-down device	R_{MDD} CC	25 + 1*V_{IN}	-	35 - 8*V_{IN}	kOhm	0 V ≤ V_{IN} ≤ 2.5 V
		-5 + 13*V_{IN}	-	15 + 16*V_{IN}	kOhm	2.5 V ≤ V_{IN} ≤ V_{DDM}
Resistance of the multiplexer diagnostics pull-up device	R_{MDU} CC	45 - 6*V_{IN}	-	90 - 16*V_{IN}	kOhm	0 V ≥ V_{IN} ≤ 2.5 V
		40 - 4*V_{IN}	-	65 - 6*V_{IN}	kOhm	2.5 V ≤ V_{IN} ≤ V_{DDM}
Resistance of the pull-down test device [10]	R_{PDD} CC	-	-	0.3	kOhm	
CSD voltage accuracy [11][12]	$dVCSD$ CC	-	-	10	%	
Wakeup time	t_{WU} CC	-	-	12	µs	

1) If the reference voltage is reduced by the factor k (k < 1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k. V_{AREF} must be decoupled with an external capacitor.

2) For QCONV = X pC and a conversion time of 1 µs a rms value of X µA results for I_{AREFx}.

3) For the details of the mapping for a VADC group to pin V_{AREFx} please see the User's Manual.

4) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 500 ms.

5) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 10 ms. This function is influenced by leakage current, in particular at high temperature.
6) Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS}.
7) This parameter is valid for soldered devices and requires careful analog board design.
8) Value is defined for one sigma Gauss distribution.
9) In order to avoid an additional error due to incomplete sampling, the sampling time shall be set greater than 5 * R_{CSD} * C_{AINS}.
10) The pull-down resistor R_{PDD} is connected between the input pad and the analog multiplexer. The input pad itself adds another 200-Ohm series resistance, when measuring through the pin.
11) CSD: Converter Self Diagnostics, for details please consult the User's Manual.
12) Note, that in case CSD voltage is chosen to nom. 1/3 or 2/3 of V_{AREF} voltage, the reference voltage is loaded with a current of max. V_{AREF} / 45 kOhm.

VADC parameter are valid for V_{DDM} = 2.97 V to 4.5 V.

Table 3-14 VADC_33

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage [1]	V_{AREF} SR	V_{AGND} + 1.0	-	V_{DDM} + 0.05	V	
Analog reference ground	V_{AGND} SR	V_{SSM} - 0.05	-	V_{SSM} + 0.05	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	-	V_{AREF}	V	
Converter reference clock	f_{ADCI} SR	2	-	20	MHz	
Charge consumption per conversion [2] [3]	Q_{CONV} CC	-	35	50	pC	V_{AIN} = 3.3 V, charge consumed from reference pin, precharging disabled
		-	8	17	pC	V_{AIN} = 3.3 V, charge consumed from reference pin, precharging enabled
Conversion time for 12-bit result	t_{C12} CC	-	(16 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time and post calibration
Conversion time for 10-bit result	t_{C10} CC	-	(14 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time
Conversion time for 8-bit result	t_{C8} CC	-	(12 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time
Conversion time for fast compare mode	t_{CF} CC	-	(4 + STC) x t_{ADCI} + 2 x t_{VADC}	-		Includes sample time
Broken wire detection delay against V_{AGND} [4]	t_{BWG} CC	-	-	120	cycles	Result below 10%

Table 3-14 VADC_33 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against V_{AREF} [5]	t_{BWR} CC	-	-	60	cycles	Result above 80%
Input leakage at analog inputs	I_{OZ1} CC	-350	-	350	nA	Analog Inputs overlaid with pull down diagnostics
		-150	-	150	nA	else
Total Unadjusted Error [1]	TUE CC	-12	-	12	LSB	12-bit Resolution; T_J > 150 °C
		-6	-	6	LSB	12-bit Resolution; T_J ≤ 150 °C
INL Error	EA_{INL} CC	-12	-	12	LSB	12-bit Resolution; T_J > 150 °C
		-5	-	5	LSB	12-bit Resolution; T_J ≤ 150 °C
Gain Error [1]	EA_{GAIN} CC	-6	-	6	LSB	12-bit Resolution; T_J > 150 °C
		-5.5	-	5.5	LSB	12-bit Resolution; T_J ≤ 150 °C
DNL error [1]	EA_{DNL} CC	-4	-	4	LSB	12-bit resolution
Offset Error [1]	EA_{OFF} CC	-6	-	6	LSB	12-bit Resolution; T_J > 150 °C
		-5	-	5	LSB	12-bit Resolution; T_J ≤ 150 °C
Total capacitance of an analog input	C_{AINT} CC	-	-	30	pF	
Switched capacitance of an analog input	C_{AINS} CC	2	4	7	pF	
Resistance of the analog input path	R_{AIN} CC	-	-	4.5	kOhm	
Switched capacitance of a reference input	C_{AREFS} CC	-	-	30	pF	
RMS Noise [6]	EN_{RMS} CC	-	-	1.7	LSB	
Positive reference V_{AREFx} pin leakage	I_{OZ2} CC	-2	-	2	µA	V_{AREFx} = V_{AREF}; T_J>150°C
		-1	-	1	µA	V_{AREFx} = V_{AREF}; T_J≤150°C
Negative reference V_{AGNDx} pin leakage	I_{OZ3} CC	-2.5	-	2.5	µA	V_{AGNDx} = V_{AGND}; T_J>150°C
		-1	-	1	µA	V_{AGNDx} = V_{AGND}; T_J≤150°C
Resistance of the reference input path	R_{AREF} CC	-	-	3	kOhm	

Table 3-14 VADC_33 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSD resistance [7]	R_{CSD} CC	-	-	28	kOhm	
Resistance of the multiplexer diagnostics pull-down device	R_{MDD} CC	$25 + 3*V_{IN}$	-	$40 + 12*V_{IN}$	kOhm	0 V ≤ V_{IN} ≤ 1.667 V
		$0 + 18*V_{IN}$	-	$0 + 18*V_{IN}$	kOhm	1.667 V ≤ V_{IN} ≤ V_{DDM}
Resistance of the multiplexer diagnostics pull-up device	R_{MDU} CC	$60 - 12*V_{IN}$	-	$120 - 30*V_{IN}$	kOhm	0 V ≤ V_{IN} ≤ 1.667 V
		$55 - 9*V_{IN}$	-	$95 - 15*V_{IN}$	kOhm	1.667 V ≤ V_{IN} ≤ V_{DDM}
Resistance of the pull-down test device [8]	R_{PDD} CC	-	-	0.9	kOhm	
CSD voltage accuracy [9] [10]	$dVCSD$ CC	-	-	10	%	
Wakeup time	t_{WU} CC	-	-	12	µs	

1) If the reference voltage is reduced by the factor k (k < 1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k. V_{AREF} must be decoupled with an external capacitor.
2) For QCONV = X pC and a conversion time of 1 µs a rms value of X µA results for I_{AREFx}.
3) For the details of the mapping for a VADC group to pin V_{AREFx} please see the User's Manual.
4) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 500 ms.
5) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate higher than 1 conversion per 10 ms. This function is influenced by leakage current, in particular at high temperature.
6) This parameter is valid for soldered devices and requires careful analog board design.
7) In order to avoid an additional error due to incomplete sampling, the sampling time shall be set greater than 5 * R_{CSD} * C_{AINS}.
8) The pull-down resistor R_{PDD} is connected between the input pad and the analog multiplexer. The input pad itself adds another 200-Ohm series resistance, when measuring through the pin.
9) CSD: Converter Self Diagnostics, for details please consult the User's Manual.
10) Note, that in case CSD voltage is chosen to nom. 1/3 or 2/3 of V_{AREF} voltage, the reference voltage is loaded with a current of max. V_{AREF} / 45 kOhm.

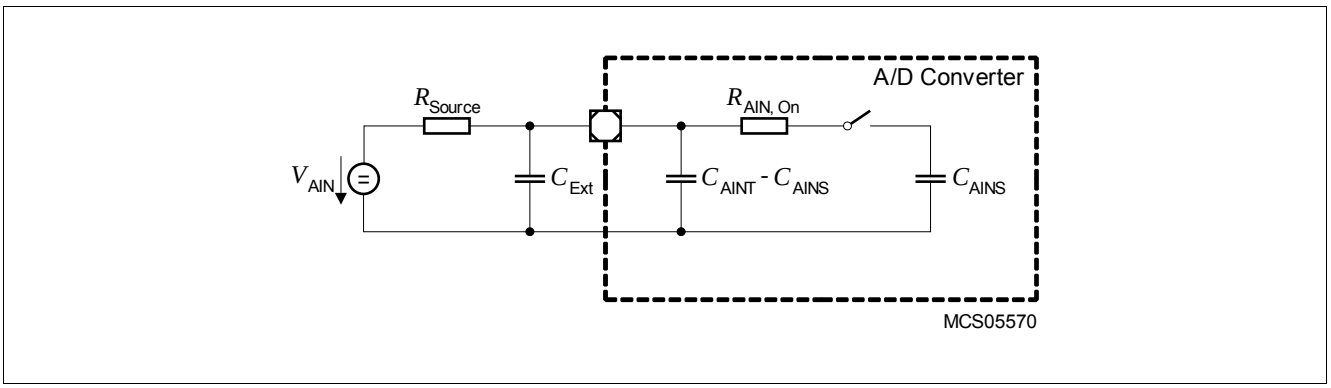


Figure 3-1 Equivalent Circuitry for Analog Inputs

3.7 MHz Oscillator

OSC_XTAL is used as accurate and exact clock source. OSC_XTAL supports 8 MHz to 40 MHz crystals external outside of the device. Support of ceramic resonators is also provided.

Table 3-15 OSC_XTAL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-25	-	25	µA	V_{IN}>0V; V_{IN}<V_{DDP3}V
Oscillator frequency	f_{OSC} SR	4	-	40	MHz	Direct Input Mode selected
		8	-	40	MHz	External Crystal Mode selected
Oscillator start-up time [1]	t_{OSCS} CC	-	-	5 [2]	ms	
Input high voltage at XTAL1	V_{IHBX} SR	0.8	-	V_{DDP3} + 0.5	V	If shaper is bypassed
Input low voltage at XTAL1	V_{ILBX} SR	-0.5	-	0.4	V	If shaper is bypassed
Input voltage at XTAL1	V_{IX} SR	-0.5	-	V_{DDP3} + 0.5	V	If shaper is not bypassed
Input amplitude (peak to peak) at XTAL1	V_{PPX} SR	0.3 * V_{DDP3}	-	V_{DDP3} + 1.0	V	If shaper is not bypassed; f_{OSC} > 25MHz
		0.4 * V_{DDP3}	-	V_{DDP3} + 1.0	V	If shaper is not bypassed; f_{OSC} ≤ 25MHz

1) t_{OSCS} is defined from the moment when V_{DDP3} = 3.13V until the oscillations reach an amplitude at XTAL1 of 0.3 * V_{DDP3}. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

2) This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decrease.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

3.8 Back-up Clock

The back-up clock provides an alternative clock source.

Table 3-16 Back-up Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Back-up clock before trimming	f_{BACKUT} CC	75	100	125	MHz	
Slow speed Back-up clock	f_{BACKSS} CC	75	100	125	kHz	
Back-up clock after trimming	f_{BACKT} CC	97.5	100	102.5	MHz	

3.9 Temperature Sensor

Table 3-17 DTS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	-	-	100	µs	
Calibration reference accuracy	T_{CALACC} CC	-1	-	1	°C	calibration points @ T_J=-40°C and T_J=127°C
Non-linearity accuracy over temperature range	T_{NL} CC	-2	-	2	°C	
Temperature sensor range	T_{SR} SR	-40	-	170	°C	
Start-up time after resets inactive	t_{TSST} SR	-	-	20	µs	

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

(3.1)

$$Tj = \frac{DTSSTATRESULT - (607)}{2,13}$$

3.10 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following table and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:

The real (realisic) power pattern defines the following conditions:

- T_J = 150 °C
- f_{SRI} = f_{MAX} = f_{CPU0} = 200 MHz
- f_{SPB} = f_{STM} = f_{GTM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLIN} = 40 MHz
- V_{DD} = 1.326 V
- V_{DDP3} = 3.366 V
- V_{DDM} = 5.1 V
- core is active
- the following peripherals are inactive: HSM, Ethernet, and MTU

The max power pattern defines the following conditions:

- T_J = 150 °C
- f_{SRI} = f_{MAX} = f_{CPU0} = 200 MHz
- f_{SPB} = f_{STM} = f_{GTM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLIN} = 100 MHz
- V_{DD} = 1.43 V
- V_{DDP3} = 3.63 V
- V_{DDM} = 5.5 V
- core is active
- all peripherals are active

Table 3-18 Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of I_{DD} 1.3 V core and peripheral supply currents	I_{DD} CC	-	-	99	mA	max power pattern
		-	-	75	mA	real power pattern
I_{DD} core current during active power-on reset (PORST held low)	$I_{DDPORST}$ CC	-	-	15	mA	T_J=125°C
		-	-	26	mA	T_J=150°C
		-	-	44	mA	T_J=165°C
I_{DD} core current of CPU0 lockstep core active	I_{DDC01} CC	-	-	20	mA	real power pattern
∑ Sum of 3.3 V supply currents without pad activity	$I_{DDx3RAIL}$ CC	-	-	36 [1]	mA	real power pattern; incl. OSC, EVR and Pflash programming current.
		-	-	38	mA	real power pattern; incl. OSC, EVR and Pflash rerad current.

Table 3-18 Power Supply (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DDM} supply current	I_{DDM} CC	-	-	6	mA	max pattern; current for VADC only
∑ Sum of all currents (incl. $I_{DDP3RAIL}$+I_{DD}+I_{DDM})	I_{DDTOTL} CC	-	-	117	mA	real power pattern
∑ Sum of all currents (STANDBY mode)	I_{EVRSB} CC	-	-	150 [2]	µA	Standby RAM is active. Power to remaining domains switched off. T_J = 25°C; V_{EVRSB} = 5V
∑ Sum of all currents (SLEEP mode)	I_{SLEEP} CC	-	-	10	mA	CPU is in idle, All peripherals in sleep, $f_{SRI/SPB}$ = 1 MHz; T_J = 55°C
Maximum power dissipation	PD CC	-	-	370 [3]	mW	max power pattern
		-	-	290 [3]	mW	real power pattern

1) Realistic Pflash read pattern with 50% Pflash bandwidth utlilization and a code mix of 50% 0s and 50% 1s. Dynamic Flash Idle via FCON.IDLE is activated bringing a benefit of 4 mA. A decoupling capacitor of atleast 100nF is used. Dflash read current is also included.

2) The current during STANDBY mode is drawn at V_{DDP3} supply pin. During RUN-STANDBY mode transition the current drawn at V_{DDP3} supply pin is less than 6mA.

3) SC DC DC losses is included in the power consumption estimate.

3.10.1 Calculating the 1.3 V Current Consumption

The current consumption of the 1.3 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature T_J and the dynamic current consumption depends of the configured clocking frequencies and the software application executed. These two parts needs to be added in order to get the rail current consumption.

(3.2)

$$I_0 = 0,0228\left[\frac{mA}{C}\right] \times e^{0,02266 \times T_J[C]}$$

(3.3)

$$I_0 = 0,868\left[\frac{mA}{C}\right] \times e^{0,02266 \times T_J[C]}$$

Function 2 defines the typical static current consumption and Function 3 defines the maximum static current consumption. Both functions are valid for V_{DD} = 1.326 V.

3.11 Power-up and Power-down

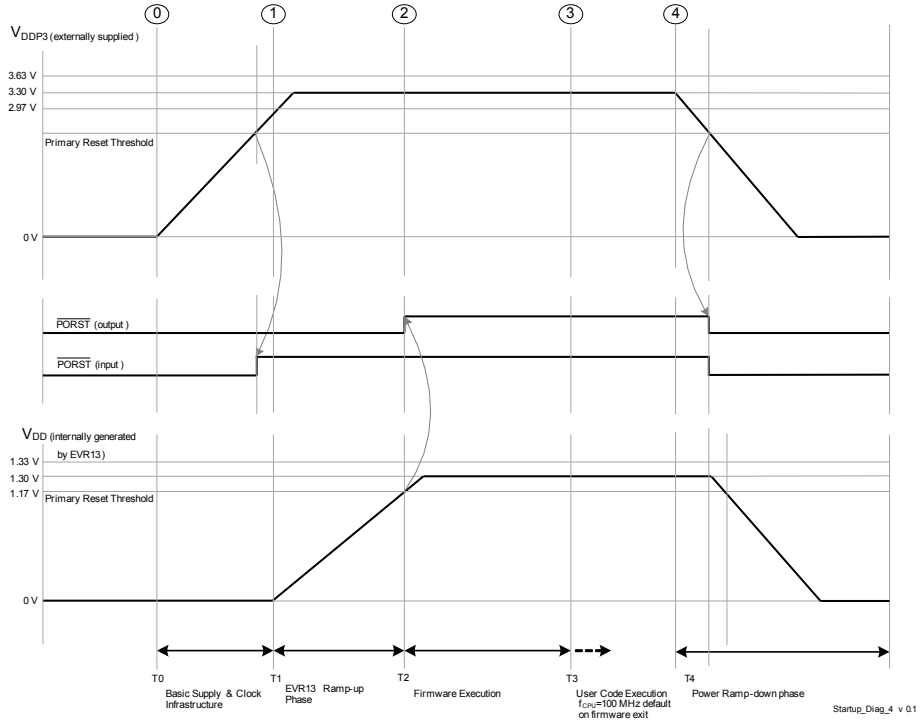


Figure 3-2 Single Supply mode - 3.3 V single supply

3.11.1 Single Supply mode

3.3 V single supply mode. 1.3 V is generated internally by the EVR13 regulator.

- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited during the basic infrastructure and EVR13 regulator start-up phase (T0 upto T2) to a maximum of 100 mA/100 us. EVR13 is also robust against a voltage ramp-up starting from a residual voltage between 0 - 1 V. Start-up slew rates for supply rails should comply to datasheet values.
- Furthermore it is also ensured that the current drawn from the external regulator (dIEXT /dt) is limited during the Firmware start-up phase (T2 upto T3) to a maximum of 100 mA/100 us.
- PORST is active/ asserted when either PORST (input) or PORST (output) is active/ asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when atleast one among the two supply domains (1.3 V or 3.3 V) violate their primary under-voltage reset thresholds.The PORST (output) is deasserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available.
- The power sequence as shown in **Figure 3-2** is enumerated below
  - T1 refers to the point in time when basic supply and clock infrastructure is available as the external supply ramps up. The supply mode is evaluated based on the HWCFG[0,2] pins and consequently a soft start of EVR13 regulator is initiated.
  - T2 refers to the point in time when all supplies are above their primary reset thresholds. EVR13 regulator has ramped up. PORST (output) is deasserted and HWCFG[3:5] pins are latched on PORST rising edge. Firmware execution is initiated.
  - T3 refers to the point in time when Firmware execution is completed. User code execution starts with a default frequency of 100 MHz.
  - T4 refers to the point in time during the Ramp-down phase when atleast one of the externally provided or generated supplies (1.3 V or 3.3 V) drop below their respective primary under-voltage reset thresholds.

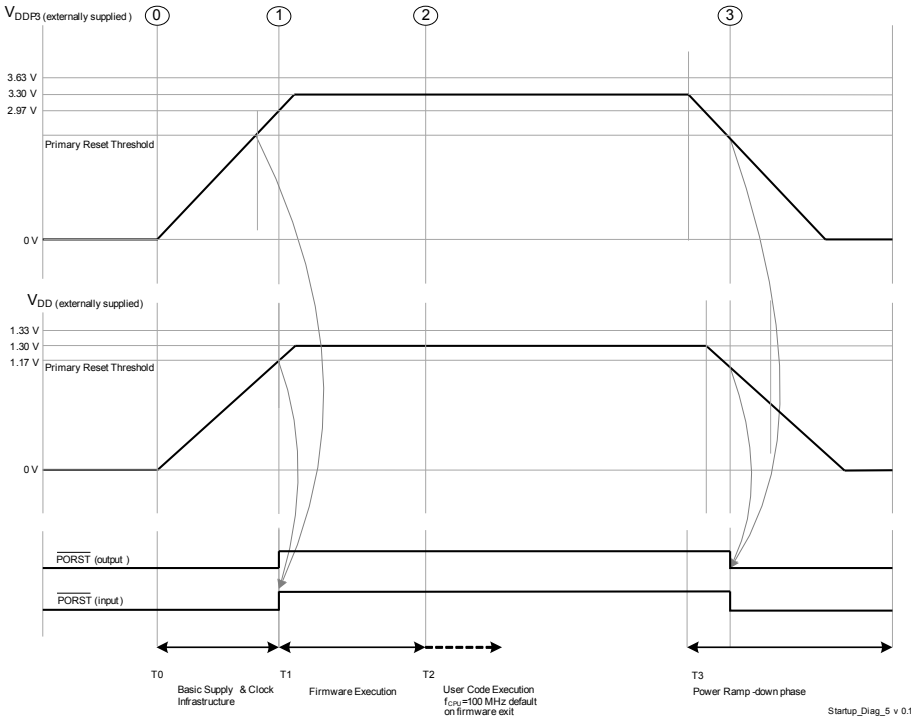


Figure 3-3 External Supply mode - 3.3 V and 1.3 V external supply

3.11.2 External Supply mode

All supplies, namely 3.3 V & 1.3 V, are externally supplied.

- External supplies VDDP3 & VDD may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). The supply system is also robust against a voltage ramp-up starting from a residual voltage between 0 - 1 V. Start-up slew rates for supply rails should comply to datasheet values.
- The rate at which current is drawn from the external regulator (dIEXT /dt, dIDD /dt) is limited in the Start-up phase to a maximum of 50 mA/100 us.
- PORST is active/ asserted when either PORST (input) or PORST (output) is active/ asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when atleast one among the two supply domains (1.3 V or 3.3 V) violate their primary under-voltage reset thresholds.The PORST (output) is deasserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available.
- The power sequence as shown in **Figure 3-3** is enumerated below
  - T1 refers to the point in time when all supplies are above their primary reset thresholds and basic clock infrastructure is available. The supply mode is evaluated based on the HWCFG[0,2] pins. PORST (output) is deasserted and HWCFG[3:5] pins are latched on PORST rising edge. Firmware execution is initiated.
  - T2 refers to the point in time when Firmware execution is completed. User code execution starts with a default frequency of 100 MHz.
  - T3 refers to the point in time during the Ramp-down phase when atleast one of the externally provided supplies (1.3 V or 3.3 V) drop below their respective primary under-voltage reset thresholds.

3.12 Reset Timing

Table 3-19 Reset Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time [1]	t_B CC	-	-	350	µs	operating with max. frequencies
System Reset Boot Time	t_{BS} CC	-	-	1	ms	
Power on Reset Boot Time [2]	t_{BP} CC	-	-	2.5	ms	dV/dT=1V/ms. including EVR ramp-up and Firmware execution time
		-	-	1.1	ms	Firmware execution time; without EVR operation (external supply only)
EVR start-up or ramp-up time	$t_{EVRstartup}$ CC	-	-	1	ms	dV/dT=1V/ms
Minimum PORST active hold time after power supplies are stable at operating levels [3]	t_{POA} CC	1	-	-	ms	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} CC	16 / f_{SPB}	-	-	ns	
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	-	-	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	-	-	8/f_{SPB}	ns	
Ports inactive after PORST reset active [4]	t_{PIP} CC	-	-	150	ns	
Hold time from PORST rising edge	t_{POH} SR	150	-	-	ns	
Setup time to PORST rising edge	t_{POS} SR	0	-	-	ns	

1) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

2) The duration of the boot time is defined by all external supply voltages are inside there operation condictions and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

3) The regulator that supplies V_{EXT} should ensure that V_{EXT} is in the operational region before PORST is externally released by the regulator. Incase of 5V nominal supply, it should be ensured that V_{EXT} > 4V before PORST is released. Incase of 3.3V nominal supply , it should be ensured that V_{EXT} > 3V before PORST is released. The additional minimum PORST hold time is required as an additional mechanism to avoid consecutive PORST toggling owing to slow supply slopes or residual supply ramp-ups. It is also required to activate external PORST atleast 100us before power-fail is recognised to avoid consecutive PORST toggling on a power fail event.

4) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.

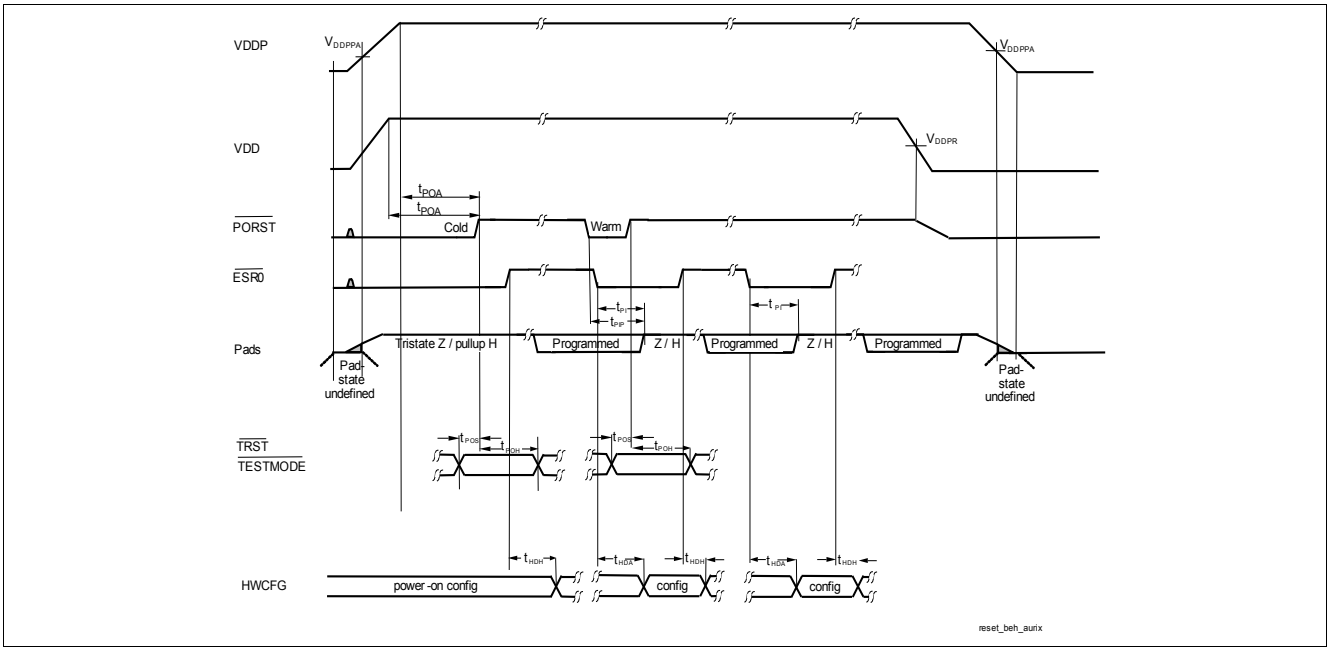


Figure 3-4 Power, Pad and Reset Timing

3.13 EVR

Table 3-20 LDO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range [1]	V_{IN} SR	2.97	-	3.63	V	V_{IN}≥; pass device=on chip
Output voltage operational range including load/line regulation and aging incase of LDO regulator	V_{OUT} CC	1.17	1.3	1.43	V	V_{IN}≥; pass device=on chip
Output V_{DD} static voltage accuracy after trimming without dynamic load/line regulation with aging incase of LDO regulator.	V_{OUTT} CC	1.275	1.3	1.325	V	load equal to I_{DD} of max power pattern; V_{IN}≥; pass device=on chip
Output buffer capacitance on V_{OUT} [2]	C_{OUT} CC	1.4	2.2	3	µF	On chip pass device usage restricted to IDD < 150mA.; V_{IN}≥; pass device=on chip
Primary undervoltage reset threshold for V_{DD} [3]	V_{RST13} CC	-	-	1.17 [4]	V	V_{IN}≥; pass device=on chip
Startup time	t_{STR} CC	-	-	1000	µs	V_{IN}≥; pass device=on chip
External V_{IN} supply ramp [5]	$dVin/dT$ SR	-	1	50	V/ms	V_{IN}≥; pass device=on chip
Load step response	$dVout/dIout$ CC	-	-	100	mV	dI=-100mA; $Tsettle$=20μs; V_{IN}≥; pass device=on chip
		-100	-	-	mV	dI=75mA; $Tsettle$=20μs; V_{IN}≥; pass device=on chip
Line step response	$dVout/dVin$ CC	-10	-	10	mV	dV/dT=1V/ms; V_{IN}≥; pass device=on chip

1) A maximum pass device dropout voltage of 700mV is included in the minimum input voltage to ensure optimal pass device operation.

2) It is recommended to select a capacitor with ESR less than 50 mOhm (0.5MHz - 10 MHz). It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm.

3) The reset release on supply ramp-up is delayed by a time duration 30-60 µs after reaching undervoltage reset threshold. This serves as a time hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released.The reset limit of 1,17V at pin is for the case with 1.3V generated internally from EVR13. In case the 1.3V supply is provided externally, the bondwire drop will cause a reset at a higher voltage of 1.18V at the VDD pin.

4) In TQFP-80 and TQFP-100 pin package, only VDDPRIUV is tested instead of VRST13 as HWCFG2 pin is absent.

5) EVR robust against residual voltage ramp-up starting between 0-1 V.

Table 3-21 Supply Monitoring

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP3} primary undervoltage monitor accuracy after trimming [1]	$V_{DDP3PRIUV}$ SR	2.86	2.92	2.97	V	
V_{DD} primary undervoltage monitor accuracy after trimming [1]	$V_{DDPRIUV}$ SR	1.13	1.15	1.17	V	
V_{DDP3} secondary supply monitor accuracy	$V_{DDP3MON}$ CC	3.23	3.30	3.37	V	SWDxxVAL V_{DDP3} monitoring threshold=3.3V=91h
V_{DD} secondary supply monitor accuracy	V_{DDMON} CC	1.27	1.30	1.33	V	EVR13xxVAL V_{DD} monitoring threshold=1.3V=E3h
EVR primary and secondary monitor measurement latency for a new supply value	t_{EVRMON} CC	-	-	1.8	µs	after trimming

1) The monitor tolerances constitute the inherent variation of the bandgap and ADC over process, voltage and temperature operational ranges. The xxxPRIUV parameters are device individually tested in production with ±1% tolerance about the min and max xxxPRIUV limits. In TQFP100 and QFP80 pin packages, VDDPRIUV is not tested as HWCFG2 pin is absent.

3.14 Phase Locked Loop (PLL)

Table 3-22 PLL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PLL base frequency	$f_{PLLBASE}$ CC	80	150	360	MHz	
VCO frequency range	f_{VCO} SR	400	-	800	MHz	
VCO Input frequency range	f_{REF} CC	8	-	24	MHz	
Modulation Amplitude	MA CC	0	-	2	%	
Peak Period jitter	DP CC	-200	-	200	ps	
Peak Accumulated Jitter	D_{PP} CC	-5	-	5	ns	without modulation
Total long term jitter	J_{TOT} CC	-	-	12.2	ns	including modulation; MA ≤ 1%
		-	-	11.5	ns	including modulation; MA≤0.9%
System frequency deviation	f_{SYSD} CC	-	-	0.01	%	with active modulation
Modulation variation frequency	f_{MV} CC	2	3.6	5.4	MHz	
PLL lock-in time	t_L CC	11.5	-	200	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and soft edge (speed grade 1).

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

3.15 AC Specifications

All AC parameters are specified for the complette operating range defined in **Chapter 3.4** unless otherwise noted in colum Note / test Condition.

Unless otherwise noted in the figures the timings are defined with the following guidelines:

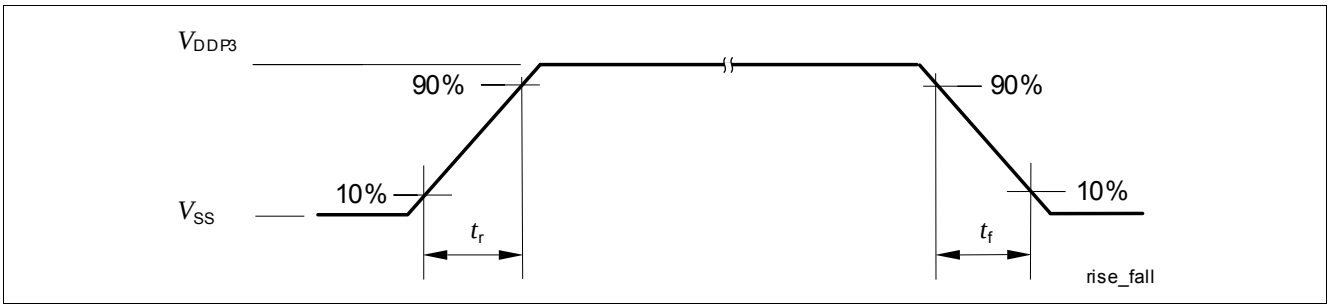


Figure 3-5 Definition of rise / fall times

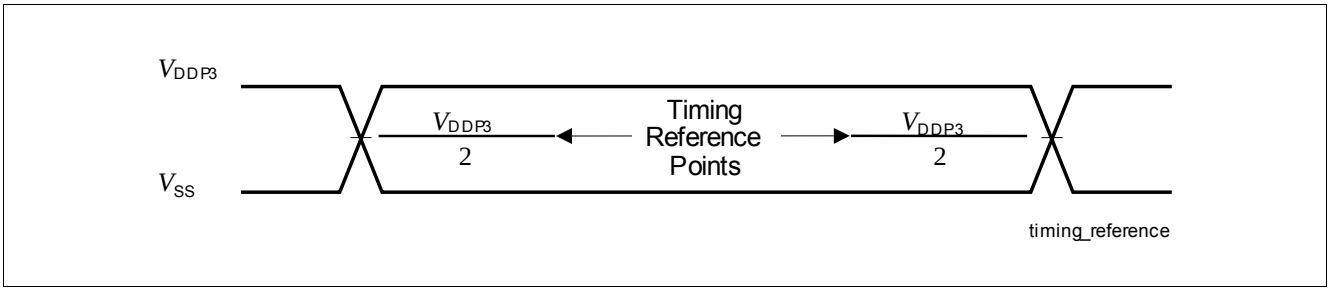


Figure 3-6 Time Reference Point Definition

3.16 JTAG Parameters

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Table 3-23 JTAG

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	-	-	ns	
TCK high time	t_2 SR	10	-	-	ns	
TCK low time	t_3 SR	10	-	-	ns	
TCK clock rise time	t_4 SR	-	-	4	ns	
TCK clock fall time	t_5 SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay) [1]	t_8 CC	3.0	-	-	ns	C_L≤20pF
		-	-	16	ns	C_L≤50pF
TDO hold after TCK falling edge [1]	t_{18} CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge [1][2]	t_9 CC	-	-	17.5	ns	C_L≤50pF
TDO valid output to high impedance from TCK falling edge [1]	t_{10} CC	-	-	17	ns	C_L≤50pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

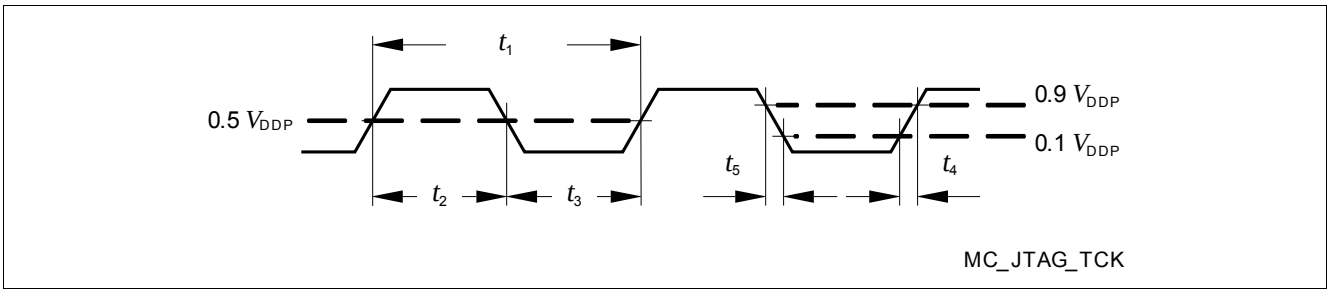


Figure 3-7 Test Clock Timing (TCK)

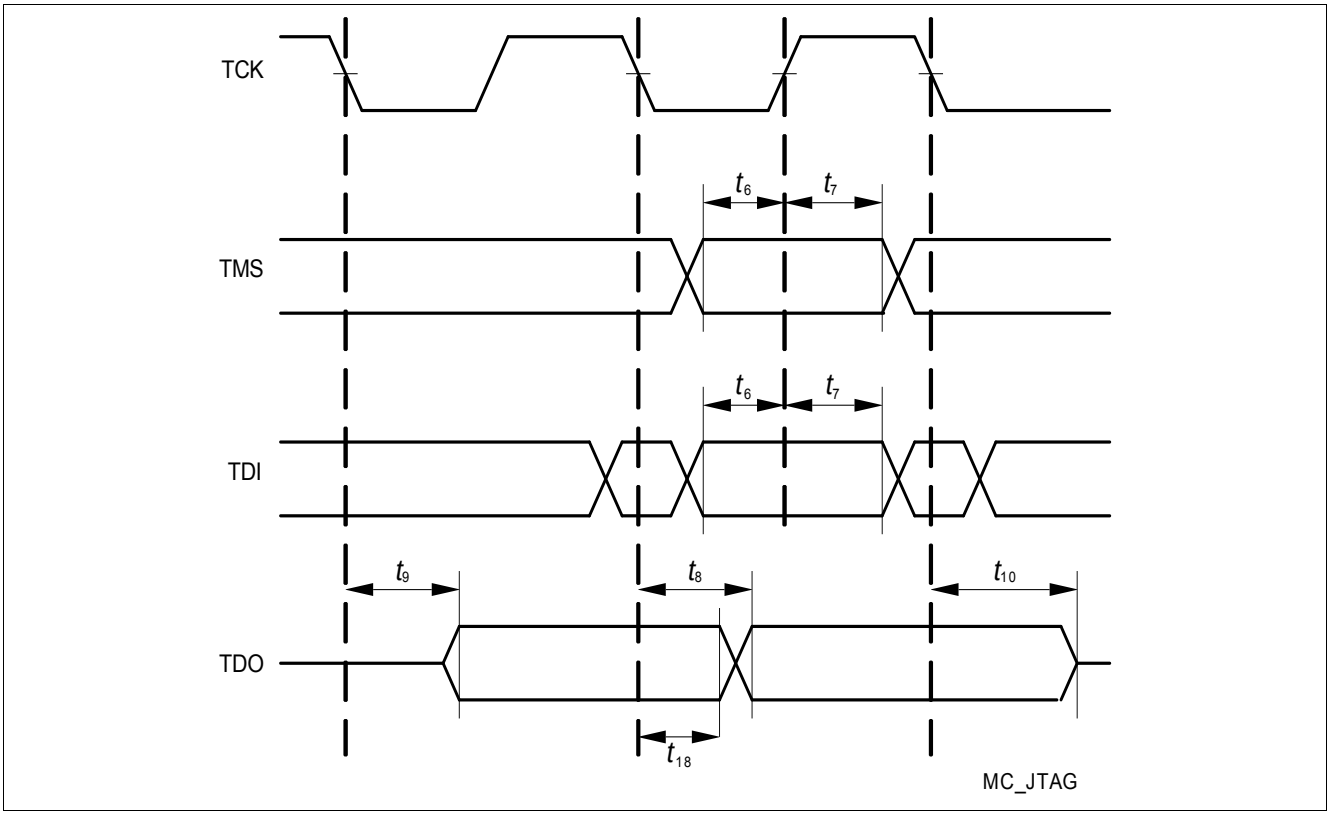


Figure 3-8 JTAG Timing

3.17 DAP Parameters

The following parameters are applicable for communication through the DAP debug interface.

Table 3-24 DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	7.51	-	-	ns	
DAP0 high time	t_{12} SR	2	-	-	ns	
DAP0 low time	t_{13} SR	2	-	-	ns	
DAP0 clock rise time	t_{14} SR	-	-	1	ns	f=133MHz
		-	-	2	ns	f=80MHz
DAP0 clock fall time	t_{15} SR	-	-	1	ns	f=133MHz
		-	-	2	ns	f=80MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	4	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	2	-	-	ns	
DAP1 valid per DAP0 clock period [1]	t_{19} CC	3	-	-	ns	C_L=20pF; f=133MHz
		8	-	-	ns	C_L=20pF; f=80MHz
		10	-	-	ns	C_L=50pF; f=40MHz

1) The Host has to find a suitable sampling point by analyzing the sync telegram response.

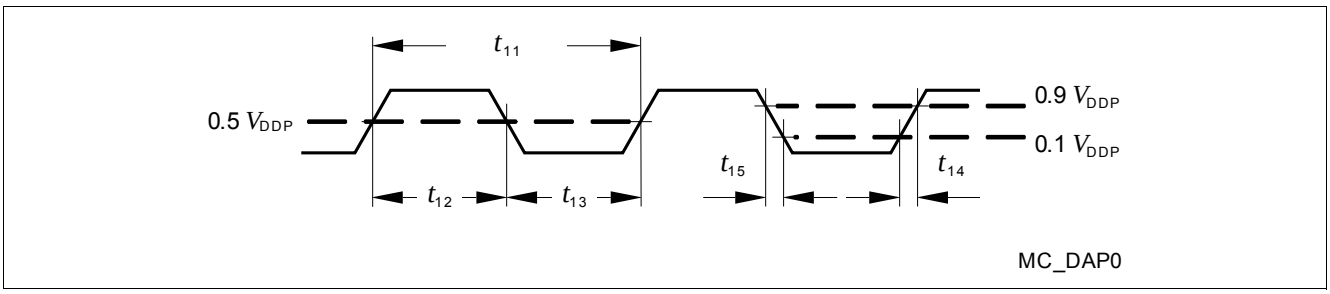


Figure 3-9 Test Clock Timing (DAP0)

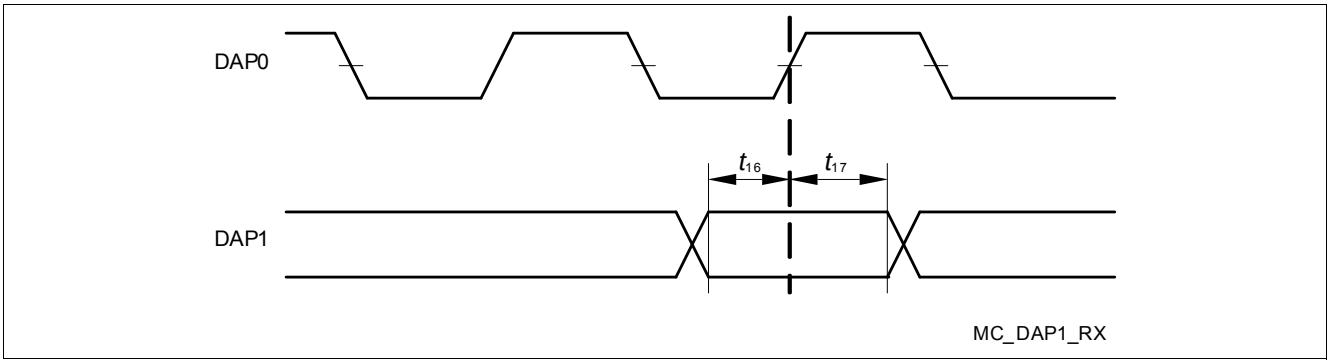


Figure 3-10 DAP Timing Host to Device

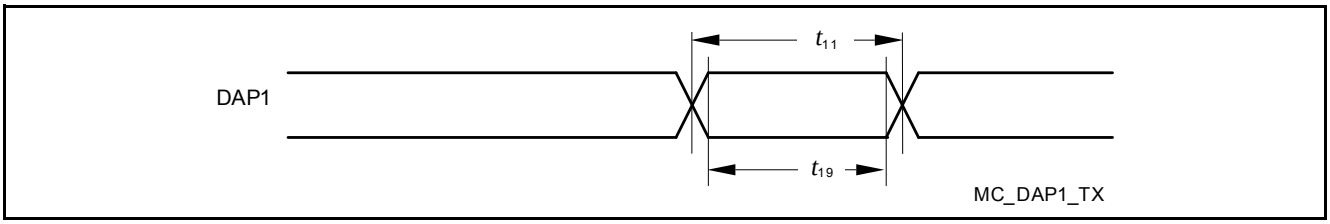


Figure 3-11 DAP Timing Device to Host (DAP1 and DAP2 pins)

Note: The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.

3.18 ASCLIN SPI Master Timing

This section defines the timings for the ASCLIN in the TC212 / TC213 / TC214 / TC222 / TC223 / TC224.

Table 3-25 Master Mode A1+strong soft (sf) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period [1]	t_{50} CC	20	-	-	ns	C_L=25pF
Deviation from ideal duty cycle [2]	t_{500} CC	-3	-	3	ns	C_L=25pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-4	-	4	ns	C_L=25pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-4	-	4	ns	C_L=25pF
MRST setup to ASCLKO latching edge	t_{52} SR	20	-	-	ns	C_L=25pF
MRST hold from ASCLKO latching edge	t_{53} SR	-3	-	-	ns	C_L=25pF

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of T_{MAX} = 1 / f_{MAX}.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

Table 3-26 Master Mode A1+strong slow (sw) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period [1]	t_{50} CC	80	-	-	ns	C_L=50pF
Deviation from ideal duty cycle [2]	t_{500} CC	-8	-	8	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-12	-	12	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-12	-	12	ns	C_L=50pF
MRST setup to ASCLKO latching edge	t_{52} SR	40	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-3	-	-	ns	C_L=50pF

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of T_{MAX} = 1 / f_{MAX}.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

Table 3-27 Master Mode medium output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period [1]	t_{50} CC	100	-	-	ns	C_L=50pF
Deviation from ideal duty cycle [2]	t_{500} CC	-10	-	10	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-15	-	15	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-15	-	15	ns	C_L=50pF
MRST setup to ASCLKO latching edge	t_{52} SR	50	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-5	-	-	ns	C_L=50pF

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of T_{MAX} = 1 / f_{MAX}.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

Table 3-28 Master Mode weak output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period [1]	t_{50} CC	1000	-	-	ns	C_L=50pF
Deviation from ideal duty cycle [2]	t_{500} CC	-25	-	25	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-65	-	65	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-65	-	65	ns	C_L=50pF
MRST setup to ASCLKO latching edge	t_{52} SR	150	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-10	-	-	ns	C_L=50pF

1) PLL Jitter not included. Should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the BITCON.SAMPLEPOINT bitfield with the finest granularity of T_{MAX} = 1 / f_{MAX}.

2) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.

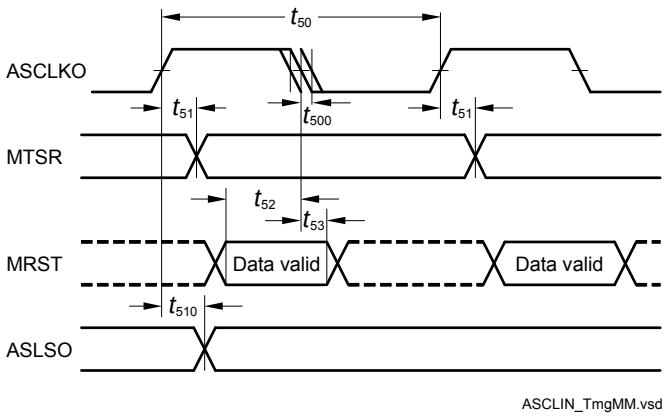


Figure 3-12 ASCLIN SPI Master Timing

3.19 QSPI Timings, Master and Slave Mode

This section defines the timings for the QSPI in the TC212 / TC213 / TC214 / TC222 / TC223 / TC224.
It is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings:

Table 3-29 Master Mode timing A1+ strong soft (sf) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	20	-	-	ns	C_L=25pF
Deviation from the ideal duty cycle [2] [3]	t_{500} CC	-3	-	3	ns	C_L=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-4	-	4	ns	C_L=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4	-	4	ns	C_L=25pF
MRST setup to SCLK latching edge [4]	t_{52} SR	20 [4]	-	-	ns	C_L=25pF
MRST hold from SCLK latching edge	t_{53} SR	-3 [4]	-	-	ns	C_L=25pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of T_{MAX} = 1 / f_{MAX}.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

Table 3-30 Master Mode timing A1+ strong slow (sw) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	80	-	-	ns	C_L=50pF
Deviation from the ideal duty cycle [2] [3]	t_{500} CC	-8	-	8	ns	C_L=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-12	-	12	ns	C_L=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-12	-	12	ns	C_L=50pF
MRST setup to SCLK latching edge [4]	t_{52} SR	40 [4]	-	-	ns	C_L=50pF
MRST hold from SCLK latching edge	t_{53} SR	-3	-	-	ns	C_L=50pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of T_{MAX} = 1 / f_{MAX}.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

Table 3-31 Master Mode timing A1+m/A1m output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	100	-	-	ns	C_L=50pF
Deviation from the ideal duty cycle [2] [3]	t_{500} CC	-3	-	3	ns	C_L=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-8	-	8	ns	C_L=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-15	-	15	ns	C_L=50pF
MRST setup to SCLK latching edge [4]	t_{52} SR	50 [4]	-	-	ns	C_L=50pF
MRST hold from SCLK latching edge	t_{53} SR	-5 [4]	-	-	ns	C_L=50pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of T_{MAX} = 1 / f_{MAX}.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

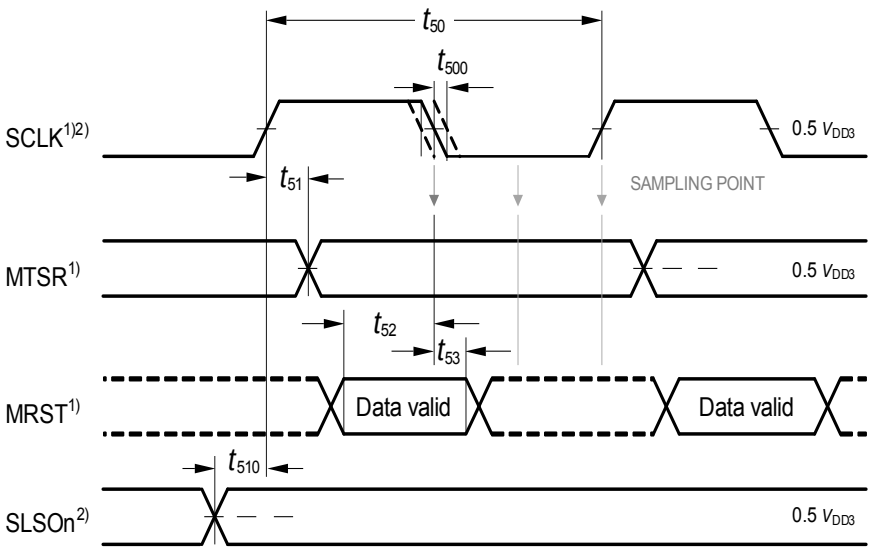
Table 3-32 Master Mode Weak output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period [1]	t_{50} CC	1000	-	-	ns	C_L=50pF
Deviation from the ideal duty cycle [2] [3]	t_{500} CC	-25	-	25	ns	C_L=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-65	-	65	ns	C_L=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-65	-	65	ns	C_L=50pF
MRST setup to SCLK latching edge [4]	t_{52} SR	150 [4]	-	-	ns	C_L=50pF
MRST hold from SCLK latching edge	t_{53} SR	-10 [4]	-	-	ns	C_L=50pF

1) Documented value is valid for master transmit or slave receive only. For full duplex the external SPI counterpart timing has to be taken into account.
2) The PLL jitter is not included. It should be considered additionally, corresponding to the used baudrate. The duty cycle can be adjusted using the bit fields ECONz.A, B and C with the finest granularity of T_{MAX} = 1 / f_{MAX}.
3) Positive deviation lenghtens the high time and shortens the low time of a clock period. Negative deviation does the opposite.
4) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

Table 3-33 Slave mode timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	t_{54} SR	4 x T_{MAX}	-	-	ns	
SCLK duty cycle	$t_{55/t54}$ SR	40	-	60	%	
MTSR setup to SCLK latching edge	t_{56} SR	3	-	-	ns	
MTSR hold from SCLK latching edge	t_{57} SR	3	-	-	ns	
SLSI setup to first SCLK shift edge	t_{58} SR	3	-	-	ns	
SLSI hold from last SCLK latching edge	t_{59} SR	3	-	-	ns	
MRST delay from SCLK shift edge	t_{60} CC	5	-	50	ns	A1+m/A1m; C_L=50pF
		3	-	20	ns	A1+sf; C_L=25pF
		5	-	40	ns	A1+sw; C_L=50pF
		10	-	150	ns	A1+w/A1w; C_L=50pF
SLSI to valid data on MRST	t_{61} SR	-	-	9	ns	

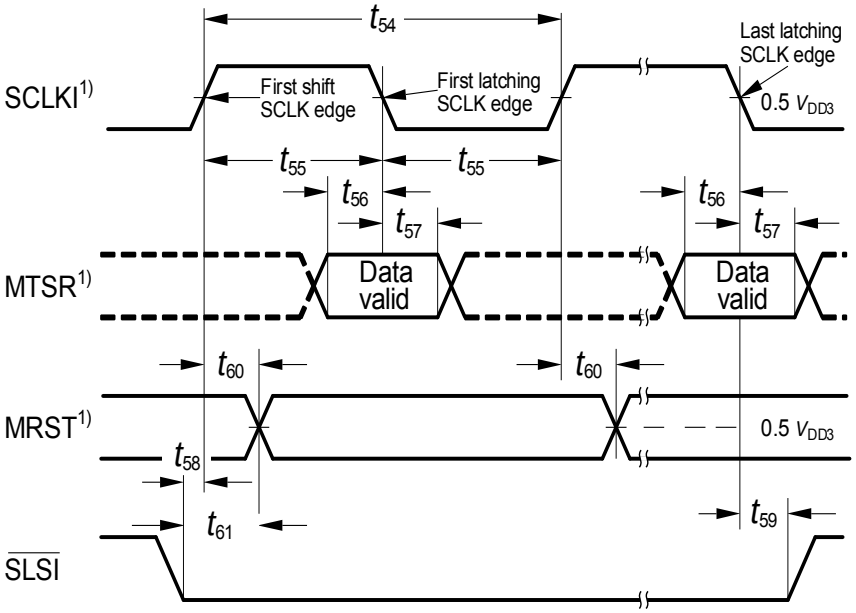


1) This timing is based on the following setup : ECON.CPH = 1, ECON.CPOL = 0, ECON.B=0 (no sampling point delay).

2) t510 is the deviation from the ideal position configured with the leading delay , BACON.LPRE and BACON.LEAD > 0.

QSPI_TmgMM_EP.vsd

Figure 3-13 Master Mode Timing



1) This timing is based on the following setup : ECON.CPH = 1, ECON.CPOL = 0.

QSPI_TmgSM_EP.vsd

Figure 3-14 Slave Mode Timing

3.20 Flash Parameters

Program Flash program and erase operation is only allowed up the T_J = 150°C.

Table 3-34 FLASH

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector	t_{ERP} CC	-	-	1	s	cycle count < 1000
		-	0.207 + 0.003 * (S [KByte]) / (f_{FSI} [MHz])[1)]	-	s	cycle count < 1000, for sector of size S
Program Flash Erase Time per Multi-Sector Command	t_{MERP} CC	-	-	1	s	For consecutive logical sectors in a physical sector, cycle count < 1000
		-	0.207 + 0.003 * (S [KByte]) / (f_{FSI} [MHz])[1)]	-	s	For consecutive logical sector range of size S in a physical sector, cycle count < 1000
Program Flash program time per page in 3.3 V mode	t_{PRP3} CC	-	-	81 + 3400/(f_{FSI} [MHz])	µs	32 Byte
Program Flash program time per burst in 3.3 V mode	t_{PRPB3} CC	-	-	410 + 12000/(f_{FSI} [MHz])	µs	256 Byte
Program Flash program time for 1 MByte with burst programming in 3 V mode excluding communication	t_{PRPB3_1MB} CC	-	-	2.2	s	Derived value for documentation purpose, valid for f_{FSI} = 100MHz
Write Page Once adder	t_{ADD} CC	-	-	15 + 500/(f_{FSI} [MHz])	µs	Adder to Program Time when using Write Page Once
Program Flash suspend to read latency	t_{SPNDP} CC	-	-	12000/(f_{FSI} [MHz])	µs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Erase Time per Sector [2)]	t_{ERD} CC	-	0.12 + 0.08/(f_{FSI} [MHz])[1)]	-	s	cycle count < 1000
		-	0.57 + 0.15/(f_{FSI} [MHz])[1)]	0.928 + 0.15/(f_{FSI} [MHz])	s	cycle count < 125000

Table 3-34 FLASH (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Multi-Sector Command [2]	t_{MERD} CC	-	0.12 + 0.01 * (S [KByte]) / (f_{FSI} [MHz])[1]	-	s	For consecutive logical sector range of size S, cycle count < 1000
		-	0.57 + 0.019 * (S [KByte]) / (f_{FSI} [MHz])[1]	0.928 + 0.019 * (S [KByte]) / (f_{FSI} [MHz])	s	For consecutive logical sector range of size S, cycle count < 125000
Data Flash erase disturb limit	N_{DFD} CC	-	-	50	cycles	
Program time data flash per page [3]	t_{PRD} CC	-	-	50 + 2500/(f_{FSI} [MHz]) [3]	µs	8 Byte
Data Flash program time per burst [3]	t_{PRDB} CC	-	-	96 + 4400/(f_{FSI} [MHz]) [3]	µs	32 Bytes
Data Flash suspend to read latency	t_{SPNDD} CC	-	-	12000/(f_{FSI} [MHz])	µs	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	-	-	10	µs	
Program Flash Retention Time, Sector	t_{RET} CC	20	-	-	years	Max. 1000 erase/program cycles
Data Flash Endurance per EEPROMx sector [4]	N_{E_EEP10} CC	125000	-	-	cycles	Max. data retention time 10 years
UCB Retention Time	t_{RTU} CC	20	-	-	years	Max. 100 erase/program cycles per UCB, max 400 erase/program cycles in total
Data Flash access delay	t_{DF} CC	-	-	100	ns	see PMU_FCON.WSDFLASH
Data Flash ECC Delay	t_{DFECC} CC	-	-	20	ns	see PMU_FCON.WSECDF
Program Flash access delay	t_{PF} CC	-	-	30	ns	see PMU_FCON.WSPFLASH
Program Flash ECC delay	t_{PFECC} CC	-	-	10	ns	see PMU_FCON.WSECPF

Table 3-34 FLASH (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase operations on DF0 over lifetime	N_{ERD0} CC	-	-	750000	cycles	
Junction temperature limit for PFlash program/erase operations	$T_{JPFlash}$ SR	-	-	150	°C	

1) All typical values were characterised, but are not tested. Typical values are safe median values at room temperature
2) Under out-of-spec conditions (e.g. over-cycling) or in case of activation of WL oriented defects, the duration of erase processes may be increased by up to 50%.
3) Time is not dependent on program mode (5V or 3.3V).
4) Only valid when a robust EEPROM emulation algorithm is used. For more details see the Users Manual.

3.21 Package Outline

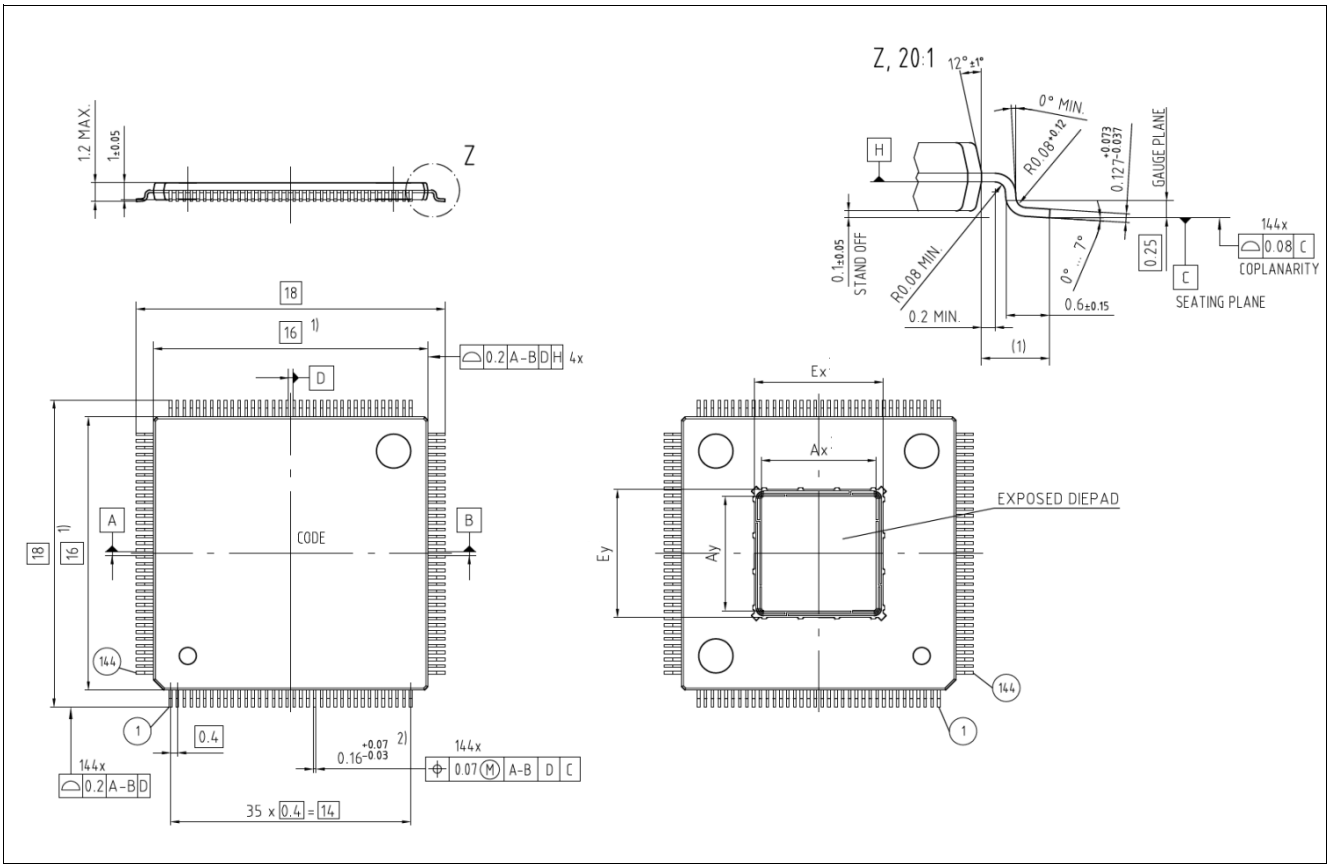


Figure 3-15 Package Outlines PG-TQFP-144-27

Table 3-35 Exposed Pad Dimensions

Ex; (nominal EPad size)	**5.7 mm ± 50 µm**
Ey; (nominal EPad size)	**5.7 mm ± 50 µm**
Ax; (solder able EPad size)	**4.9 mm ± 50 µm**
Ay; (solder able EPad size)	**4.9 mm ± 50 µm**

Note: It is recommended to use dimensions Ex and Ey for board layout considerations. Solder wetting between Ex / Ey and Ax / Ay and lead between Ex / Ey and Ax / Ay will not case any harm.

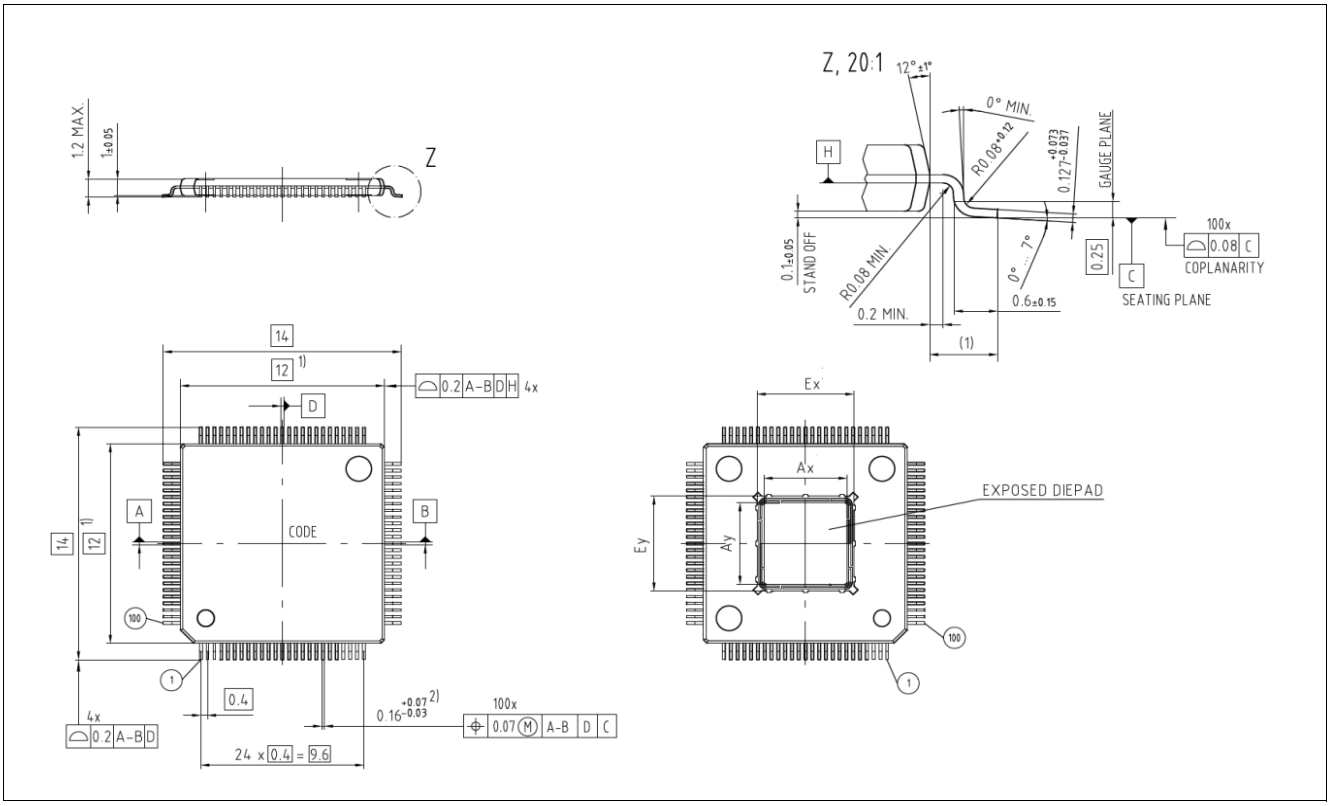


Figure 3-16 Package Outlines PG-TQFP-100-23

Table 3-36 Exposed Pad Dimensions

Ex; (nominal EPad size)	**5.7 mm ± 50 µm**
Ey; (nominal EPad size)	**5.7 mm ± 50 µm**
Ax; (solder able EPad size)	**4.9 mm ± 50 µm**
Ay; (solder able EPad size)	**4.9 mm ± 50 µm**

Note: It is recommended to use dimensions Ex and Ey for board layout considerations. Solder wetting between Ex / Ey and Ax / Ay and lead between Ex / Ey and Ax / Ay will not case any harm.

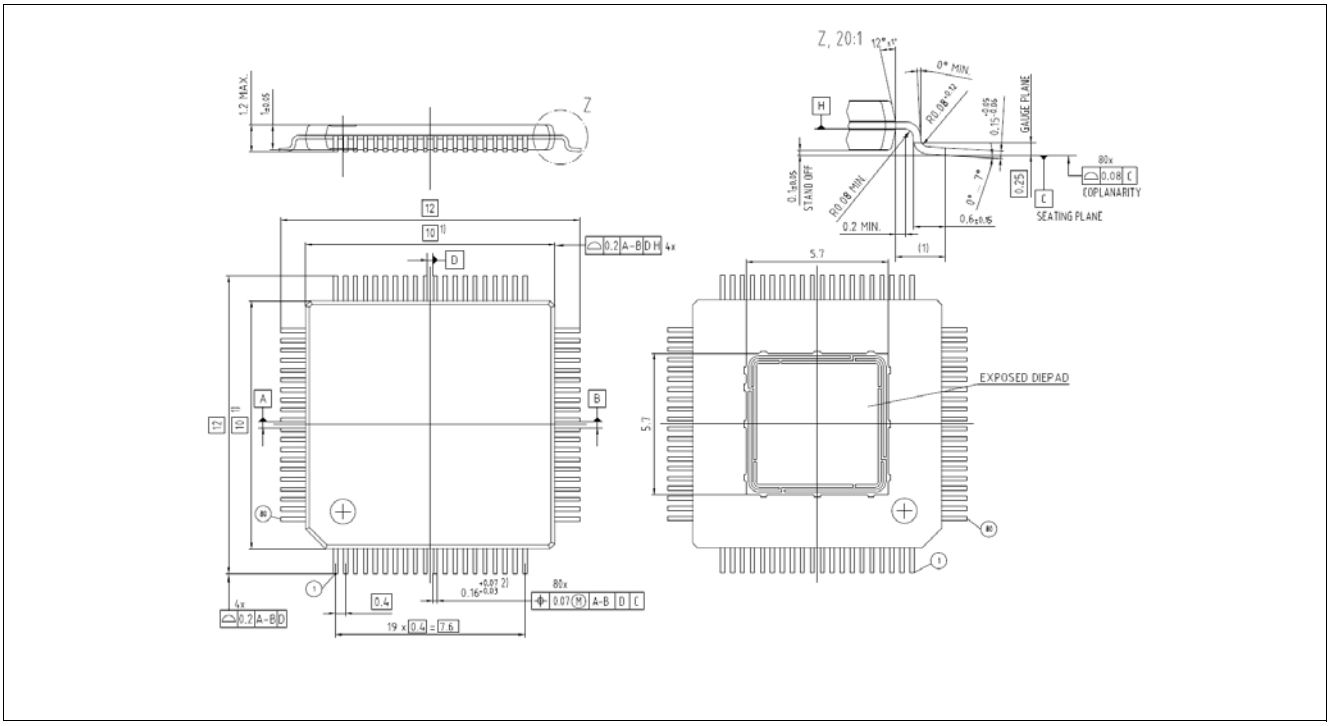


Figure 3-17 Package Outlines PG-TQFP-80-7

Table 3-37 Exposed Pad Dimensions

Ex; (nominal EPad size)	**5.7 mm ± 50 µm**
Ey; (nominal EPad size)	**5.7 mm ± 50 µm**
Ax; (solder able EPad size)	**4.9 mm ± 50 µm**
Ay; (solder able EPad size)	**4.9 mm ± 50 µm**

Note: It is recommended to use dimensions Ex and Ey for board layout considerations. Solder wetting between Ex / Ey and Ax / Ay and lead between Ex / Ey and Ax / Ay will not case any harm.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

3.21.1 Package Parameters

Table 3-38 Thermal Characteristics of the Package

Device	Package	RQJCT[1)]	RQJCB[1)]	RQJA	Unit	Note
TC212 / TC222	PG-TQFP-80-7	23.9	12.9	31.2[2)]	K/W	with soldered exposed pad and internal pass device
TC213 / TC223	PG-TQFP-100-23	23.8	13.0	31.1[2)]	K/W	with soldered exposed pad and internal pass device
TC214 / TC224	PG-TQFP-144-27	22.4	12.9	30.6[2)]	K/W	with soldered exposed pad and internal pass device

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT}, R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
   The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} * P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.
   Thermal resistances as measured by the ’cold plate method’ (MIL SPEC-883 Method 1012.1).
2) Value is defined in accordance with JEDEC JESD51-3, JESD51-5, and JESD51-7.

3.22 Quality Declarations

Table 3-39 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime	t_{OP}	-	-	24500	hour	
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	-	2000	V	Conforming to JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM}	-	-	500	V	for all other balls/pins; conforming to JESD22-C101-C
		-	-	750	V	for corner balls/pins; conforming to JESD22-C101-C
Moisture Sensitivity Level	MSL	-	-	3		Conforming to Jedec J-STD--020C for 240C

4 History

Version 0.6 is the first version of this document.

4.1 Changes from Version TC21x22x_DS_V1.0 to Version TC21x22x_AC_DS_V1.0

- Overload
  - Remove parameter I_{ING}
- changes in table' Class_S' of Standard_Pads
  - add footenote ' V_{ILx} = 0.65 * V_{DDM}' to V_{IHS}
  - add footenote ' V_{ILx} = 0.41 * V_{DDM}' to V_{ILS}
- Back-up Clock
  - Add parameter f_{BACKSS}
- VADC
  - Add parameter t_{WU}
  - Add parameter R_{MDU}
  - Add parameter R_{MDD}
- VADC_33
  - Add parameter t_{WU}
  - Add parameter R_{MDU}
  - Add parameter R_{MDD}
- Power Supply
  - Change max value of I_{EVRSB} from 650 µA to 150 µA
  - Change note of I_{EVRSB} from 'Standby RAM is active. Power to remaining domains switched off. T_J =25°C' to 'Standby RAM is active. Power to remaining domains switched off. T_J = 25°C; V_{EVRSB} = 5V'
  - Update formulas 3.2 and 3.3
- Package Outlne
  - Improve information in table 3-35
  - Improve information in table 3-36
  - Improve information in table 3-37

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