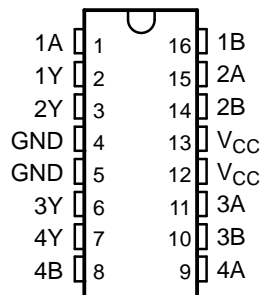


## FEATURES

- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typ Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (N)

**D OR N PACKAGE  
(TOP VIEW)**



## DESCRIPTION

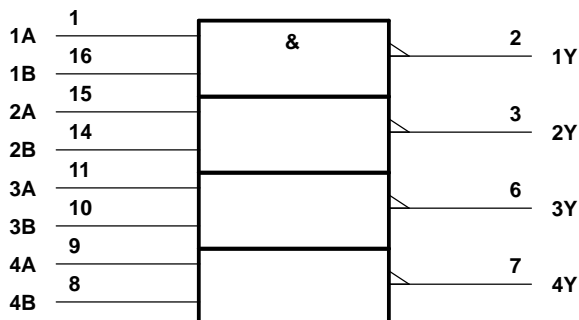
This device contains four independent 2-input NAND gates. It performs the Boolean function  $Y = \overline{A \bullet B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

The 74AC11000 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE  
(EACH GATE)**

INPUTS		OUTPUT Y
A	B	
H	H	L
L	X	H
X	L	H

**LOGIC SYMBOL<sup>(1)</sup>**



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

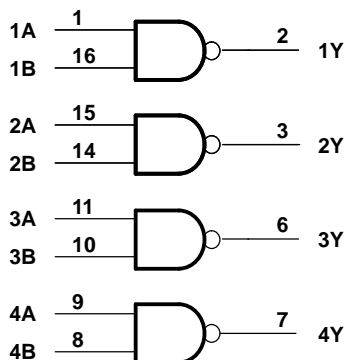
EPIC is a trademark of Texas Instruments.

# 74AC11000

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS054B–APRIL 1987–REVISED JUNE 2005

### LOGIC DIAGRAM (POSITIVE LOGIC)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		−0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		−0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>		−0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	±20		mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±50		mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±50		mA
Continuous current through V <sub>CC</sub> or GND			±100		mA
Maximum power dissipation at T <sub>A</sub> = 55°C (in still air) <sup>(3)</sup>		D package	1.3		W
		N package	1.1		
T <sub>stg</sub>	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1			V
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 5.5\text{ V}$	3.85			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$			0.9	V
		$V_{CC} = 4.5\text{ V}$			1.35	
		$V_{CC} = 5.5\text{ V}$			1.65	
$V_I$	Input voltage		0		$V_{CC}$	V
$V_O$	Output voltage		0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$			–4	mA
		$V_{CC} = 4.5\text{ V}$			–24	
		$V_{CC} = 5.5\text{ V}$			–24	
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$			12	mA
		$V_{CC} = 4.5\text{ V}$			24	
		$V_{CC} = 5.5\text{ V}$			24	
$\Delta t/\Delta v$	Input transition rise fall rate		0		10	ns/V
$T_A$	Operating free-air temperature		–40		85	°C

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
$V_{OL}$	$I_{OL} = 50\text{ }\mu\text{A}$	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	$I_{OL} = 12\text{ mA}$	3 V			0.36		0.44	
		4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
					4		40	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V						$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		3.5				pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

# 74AC11000

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS054B–APRIL 1987–REVISED JUNE 2005

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	1.5	7.2	9.8	1.5	11.1	ns
$t_{PHL}$			1.5	5.8	8.6	1.5	9.6	

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

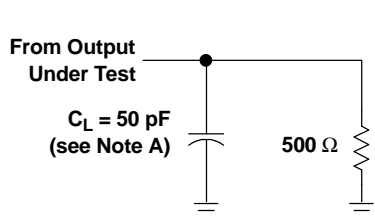
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	1.5	5	6.5	1.5	7.4	ns
$t_{PHL}$			1.5	4.4	6.1	1.5	6.8	

### Operating Characteristics

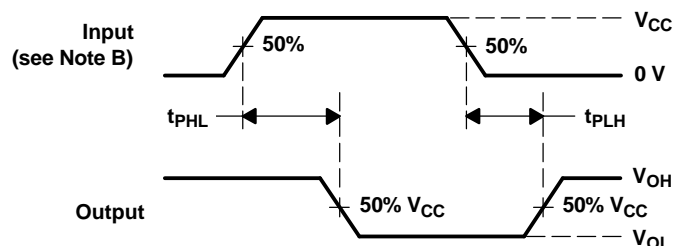
$V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per gate	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$	33	pF

### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AC11000D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11000	<a href="#">Samples</a>
74AC11000DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11000	<a href="#">Samples</a>
74AC11000N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	74AC11000N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

---

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AC11000DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AC11000DR	SOIC	D	16	2500	340.5	336.1	32.0



## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74AC11000D	D	SOIC	16	40	507	8	3940	4.32
74AC11000N	N	PDIP	16	25	506	13.97	11230	4.32
74AC11000N	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated