37V / 1.5A Stepping Motor Driver

FEATURES

- 4-phase input control
  → 2-phase, half step, 1-2 phase, W1-2 phase excitation enabled
- PWM can be driven by built-in CR (3-value can be selected during PWM OFF period.)
  → The selection of PWM OFF period enables the best PWM drive.
- Mix Decay control (4-value can be selected for Fast Decay ratio)
  → Mix Decay control can improve accuracy of motor current waveform.
- Built-in over-current protection (OCP)
  → If the current flows to motor output more than the setup value due to ground-fault etc., the OCP operates and all motor outputs are turned OFF
- Built-in under voltage lockout (UVLO)
  → If supply voltage falls to less than the operating supply voltage range, the UVLO operates and all motor outputs are turned OFF.
- Built-in thermal protection (TSD)
  → If chip junction temperature rises and reaches to the setup temperature, all motor outputs are turned OFF.
- Built-in abnormal detection output function (NFAULT)
  → If OCP or TSD operates, an abnormal detection signal is output.
- Built-in standby function
  → The operation of standby function can lower current consumption of this LSI.
- Built-in 3.3 V power supply (accuracy : ±3%)
- Built-in EMI reduction function
- Built-in malfunction prevention function when it don't input supply voltage
  → it prevents from malfunction and destruction when it input voltage to IF (ENABLEA/ENABLEB, IN0～3, PHA, PHB, STBY, VREFA, VREFB) and it don't supply voltage to VM.
- 32 pin Plastic Small Outline Package (SOP Type)

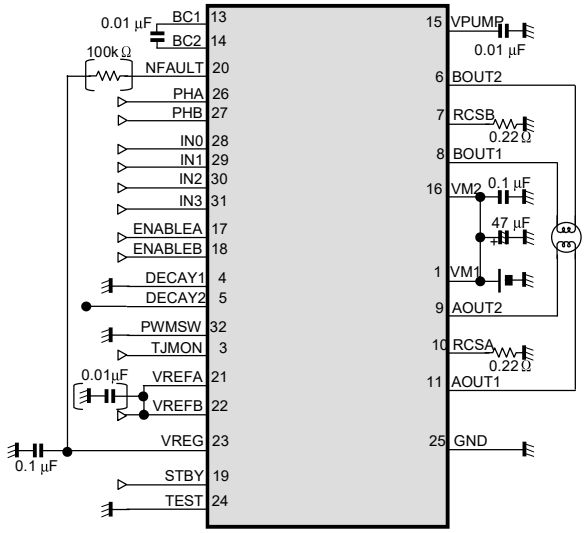
APPLICATIONS

- LSI for stepping motor drives

DESCRIPTION

AN44180A is a two channel H-bridge driver LSI. Bipolar stepping motor can be controlled by a single driver LSI. Interface is "parallel control IF" and 2 phase excitation, half-step, 1-2 phase excitation, W1-2 phase excitation can be selected.

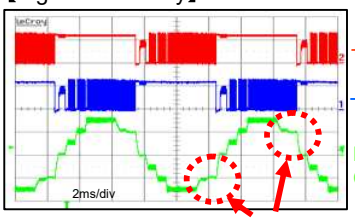
TYPICAL APPLICATION



Notes : This application circuit is an example. The operation of the mass production set is not guaranteed. Customers shall perform enough evaluation and verification on the design of mass production set. Customers shall be fully responsible for the incorporation of the above application circuit and information in the design of the equipment.

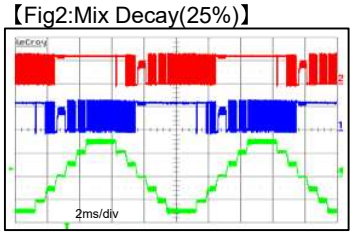
Mix Decay effect for Motor current

【Fig1:Slow Decay】



distortion

【Fig2:Mix Decay(25%)】



distortionless

Condition:
excitation mode :W1-2 phase drive
fig1 DECAY1=L DECAY2=L
fig2 DECAY1=L DECAY2=H

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_M	37	V	*1
Power dissipation	P_D	0.347	W	*2
Operating ambient temperature	T_{opr}	–20 ～ +85	°C	*3
Operating junction temperature	T_j	–20 ～ +150	°C	*3
Storage temperature	T_{stg}	–55 ～ +150	°C	*3
Output pin voltage (AOUT1～BOUT2)	V_{OUT}	37	V	*4
Motor drive current (AOUT1～BOUT2)	I_{OUT}	±1.5	A	*5
Flywheel diode current (AOUT1～BOUT2)	I_f	±1.5	A	*5
Input Voltage Range	V_{RCSA},V_{RCSB}	2.5	V	—
	V_{VPUMP}	43	V	*6
	V_{BC2}	43	V	*6
	V_{VREFA},V_{VREFB}	-0.3 to 6	V	—
	V_{STBY}	-0.3 to 6	V	—
	V_{PHA},V_{PHB}	-0.3 to 6	V	—
	$V_{ENABLEA}$,$V_{ENABLEB}$	-0.3 to 6	V	—
	V_{PWMSW}	-0.3 to 6	V	—
	V_{DECAY1},V_{DECAY2}	-0.3 to 6	V	—
	$V_{IN0\sim IN3}$	-0.3 to 6	V	—
	V_{TEST}	-0.3 to 6	V	—
Input Current Range	I_{VREG}	-1 to 0	mA	—
	I_{NFAULT}	0 to 2	mA	*7
ESD	HBM (Human Body Model)	± 2	kV	—
	CDM (Charge Device Model)	± 1	kV	—

Notes). This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) LSI package without a heat sink. When using this LSI, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, operating junction temperature,and storage temperature, all ratings are for T_a = 25°C.

*4 : This is output voltage rating and do not apply input voltage from outside to these pins. Set not to exceed allowable range at any time.

*5 : Do not apply external currents to any pin specially mentioned. For circuit currents, (+) denotes current flowing into the LSI and (–) denotes current flowing out of the LSI.

*6 : External voltage must not be applied to this pin. Do not exceed the rated value at any time.

*7 : This pin is connected to open drain circuit inside. Connect a resistor in series with power supply. Do not exceed the rated value at any time.

POWER DISSIPATION RATING

Package	θ_{JA}	PD(Ta=25℃)	PD(Ta=85℃)
SSOP032-P-0300D	68.4 °C/W *1	1827mW *1	950mW *1
	96.9 °C/W *2	1290mW *2	671mW *2
	187.1 °C/W *3	668mW *3	347mW *3

Note). For the actual usage, please refer to the P_D-T_a characteristics diagram in the package specification, supply voltage, load and ambient temperature conditions to ensure that there is enough margin follow the power and the thermal design does not exceed the allowable value.

*1: Mount On PWB(4Layers)[50X50X0.8t(mm)]

*2: Mount On PWB(1Layers)[Glass-Epoxy:50X50X0.8t(mm)]

*3: Without PWB

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VM1,VM2	8	24	34	V	*1
Input Voltage Range	V_{VREFA},V_{VREFB}	0.1	-	3.5	V	—
	V_{STBY}	0	-	5.5	V	—
	V_{PHA},V_{PHB}	0	-	5.5	V	—
	$V_{ENABLEA}$,$V_{ENABLEB}$	0	-	5.5	V	—
	V_{PWMSW}	0	-	5.5	V	—
	V_{DECAY1},V_{DECAY2}	0	-	5.5	V	—
	$V_{IN0\sim IN3}$	0	-	5.5	V	—
	V_{TEST}	-	GND	-	V	*2
External Constants	RCSA,RCSB	-	0.22	-	Ω	—
	C_{BC}	-	0.01	-	μF	—
	C_{VPUMP}	-	0.01	-	μF	—
	C_{VREG}	-	0.1	-	μF	—
Operating ambient temperature	Ta^{opr}	-20	-	85	°C	—
Operating junction temperature	Tj^{opr}	-	-	120	°C	—

Note) *1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2:Be sure to connect TEST pin to GND.

ELECTRICAL CHARACTERISTICS

VM=24V,Ta = 25°C±2°C unless otherwise specified.

Parameter	Symbol	Conditions	Limits			Unit	Note
			Min	Typ	Max		
Output Drivers							
Upper-side output ON Resistance	R_{ONH}	I = –0.8 A	—	0.38	0.57	Ω	—
Lower-side output ON Resistance	R_{ONL}	I = 0.8 A	—	0.57	0.855	Ω	—
Flywheel diode forward voltage	V_{DI}	I = 0.8A	0.5	1	1.5	V	—
Output leakage current	I_{LEAK}	V_M = 37 V, V_{RCS} = 0 V	—	—	10	μA	—
Supply current							
Supply current (Active)	I_M	ENABLE = Low, STBY = High	—	7.5	12.5	mA	—
Supply current (STBY)	I_{MSTBY}	STBY = Low	—	25	40	μA	—
I/O Block							
STBY High-level input voltage	V_{STBYH}	—	2.1	—	5.5	V	—
STBY Low-level input voltage	V_{STBYL}	—	0	—	0.8	V	—
STBY High-level input current	I_{STBYH}	STBY = 5 V	6	12.5	25	μA	—
STBY Low-level input current	I_{STBYL}	STBY = 0 V	-2	—	2	μA	—
PWMSW High-level input voltage	V_{PWMSWH}	—	2.3	—	5.5	V	—
PWMSW Middle-level input voltage	V_{PWMSWM}	—	1.2	—	1.7	V	—
PWMSW Low-level input voltage	V_{PWMSWL}	—	0	—	0.6	V	—
PWMSW High-level input current	I_{PWMSWH}	PWMSW = 5 V	36	73	146	μA	—
PWMSW Low-level input current	I_{PWMSWL}	PWMSW = 0 V	-60	-30	-15	μA	—
PWMSW open voltage	V_{PWMSWO}	—	1.2	1.45	1.7	V	—
Logic input High-level input voltage	V_{LOGICH}	—	2.1	—	5.5	V	*1
Logic input Low-level input voltage	V_{LOGICL}	—	0	—	0.8	V	*1
Logic input High-level input current	I_{LOCIGH}	Logic input pin = 5 V	25	50	100	μA	*1
Logic input Low-level input current	I_{LOGICL}	Logic input pin = 0 V	-2	—	2	μA	*1
DECAY High-level input voltage	V_{DECAYH}	—	2.1	—	5.5	V	*2
DECAY Low-level input voltage	V_{DECAYL}	—	0	—	0.8	V	*2
DECAY High-level input current	I_{DECAYH}	DECAY = 5 V	12.5	25	50	μA	*2
DECAY Low-level input current	I_{DECAYL}	DECAY = 0 V	-2	—	2	μA	*2

Notes) *1 : Logic input pin represents PHA, PHB, ENABLEA, ENABLEB, IN0～3.
*2 : DECAY represents DECAY1 and DECAY2.

ELECTRICAL CHARACTERISTICS（continued）

VM=24V,Ta = 25°C±2°C unless otherwise specified.

Parameter	Symbol	Conditions	Limits			Unit	Note
			Min	Typ	Max		
Torque control block							
VREF input bias current	I_{VREF}	—	-1	—	1	μA	*3
VREF input voltage range	V_{VREF}	—	0.1	—	3.5	V	*3
PWM OFF time 1	T_{OFF1}	PWMSW = Low	16.8	28	39.2	μs	—
PWM OFF time 2	T_{OFF2}	PWMSW = High	9.1	15.2	21.3	μs	—
PWM OFF time 3	T_{OFF3}	PWMSW = Middle	4.9	8.1	11.3	μs	—
Pulse blanking time	T_B	VREF = 0 V	0.4	0.75	1.0	μs	—
Comp threshold H (100%)	VT_{CMP1}	VREF = 3.3 V	321	330	339	mV	*3 *4
Comp threshold M (70.7%)	VT_{CMP2}	VREF = 3.3 V	224	233	242	mV	*3 *5
Comp threshold L (38.4%)	VT_{CMP3}	VREF = 3.3 V	118	127	136	mV	*3 *6

Notes) *3 : VREF represents VREFA and VREFB.

*4 : $VT_{CMP1} = VREF \times 0.1 \times 100\%$

*5 : $VT_{CMP2} = VREF \times 0.1 \times 70.7\%$

*6 : $VT_{CMP3} = VREF \times 0.1 \times 38.4\%$

ELECTRICAL CHARACTERISTICS（continued）

VM=24V,Ta = 25°C±2°C unless otherwise specified.

Parameter	Symbol	Conditions	Limits			Unit	Note
			Min	Typ	Max		
Reference voltage block							
Reference voltage	V_{VREG}	I_{VREG} = 0 mA	3.21	3.3	3.39	V	—
Output impedance	Z_{VREG}	I_{VREG} = –1 mA	—	—	10	Ω	—
Test input block							
TEST High-level input voltage	V_{TESTH}	—	2.1	—	5.5	V	—
TEST Low-level input voltage	V_{TESTL}	—	0	—	0.8	V	—
TEST High-level input current	I_{TESTH}	TEST = 5 V	25	50	100	μA	—
TEST Low-level input current	I_{TESTL}	TEST = 0 V	-2	—	2	μA	—
Abnormal detection output block							
NFAULT pin output Low-level voltage	$V_{NFAULTL}$	I_{NFAULT} = 1mA	—	—	0.2	V	—
NFAULT pin output leak current	$I_{NFAULT(leak)}$	V_{NFAULT} = 3.3V	—	—	5	μA	—

ELECTRICAL CHARACTERISTICS（continued）

VM=24V,Ta = 25°C±2°C unless otherwise specified.

Parameter	Symbol	Conditions	Limits			Unit	Note
			Min	Typ	Max		
Output block							
Output slew rate 1	VT_r	At the rising edge of output voltage, sink side of motor current	—	300	—	V/μs	*7 *10
Output slew rate 2	VT_f	At the falling edge of output voltage, sink side of motor current	—	300	—	V/μs	*7 *10
Thermal shutdown protection							
Thermal shutdown protection operating temperature	TSD_{on}	—	—	150	—	°C	*8 *10
Under voltage lockout							
Protection start voltage	V_{UVLO1}	—	—	6.0	—	V	*10
Protection stop voltage	V_{UVLO2}	—	—	7.0	—	V	*10
Over current protection							
Protection start current	I_{OCP}	—	—	5	—	A	*9 *10

Notes) *7 : It represent the characteristics of AOUT1, AOUT2,BOUT1,BOUT2 .

*8 : TSD is a latch type protection

→ The protection operation starts at 150°C. (All motor outputs are turned off , and latched.)
/ The latch is released by Standby or UVLO.

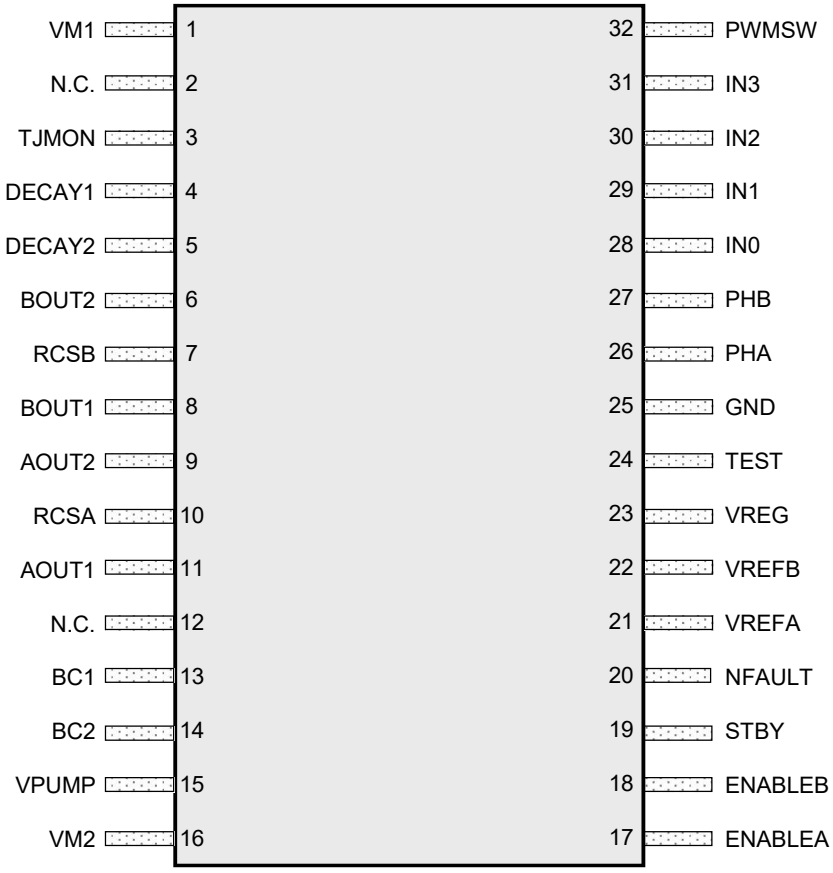
*9 : OCP is a latch type protection

→ All motor outputs are turned off by over-current detection, and be latched. / The latch is released by Standby or UVLO.
In addition, All motor outputs are turned off at under UVLO.

*10 :Typical Value checked by design.

PIN CONFIGURATION

Top View

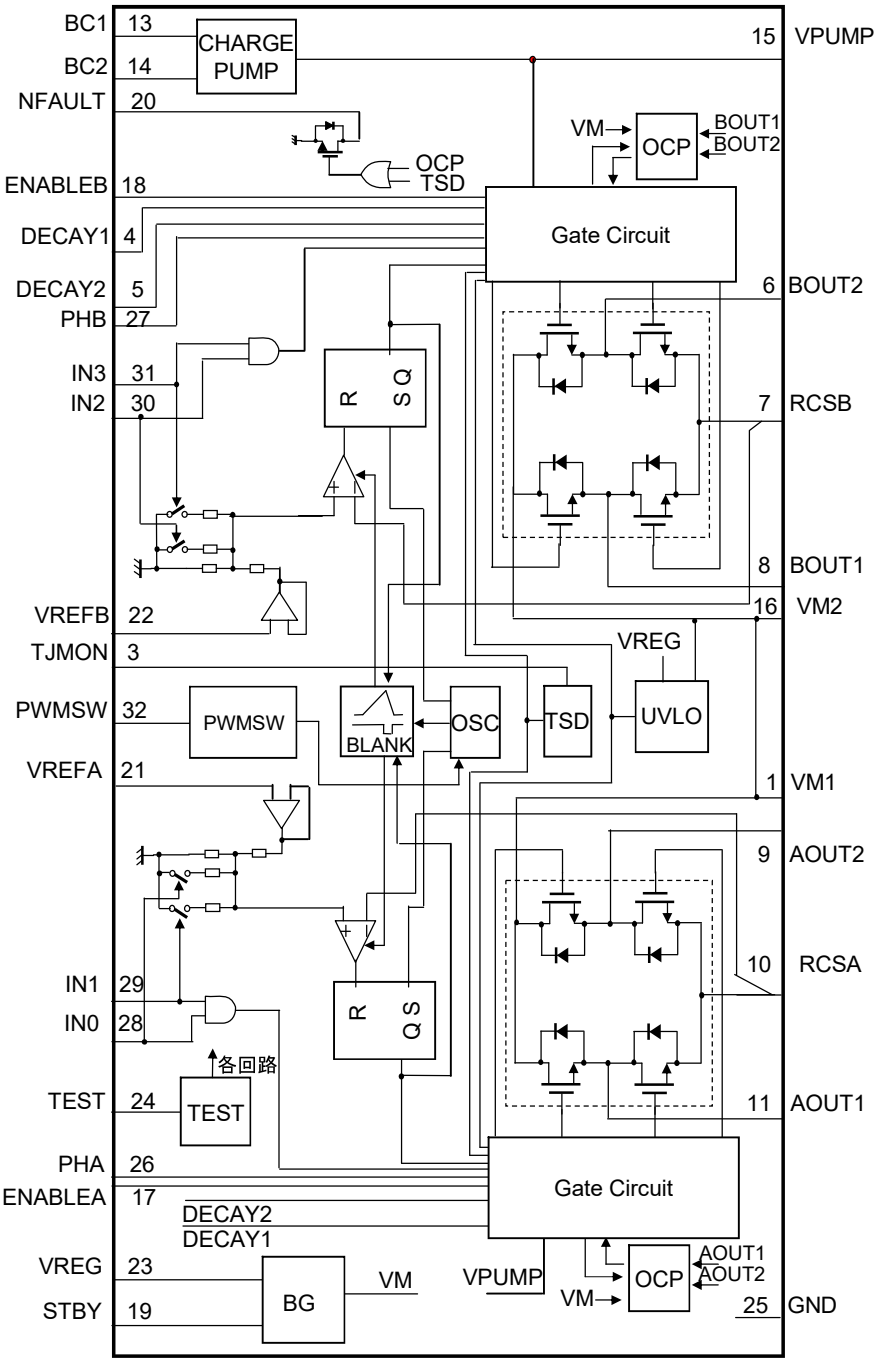


PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	VM1	Power supply	Power supply 1 for motor
2	N.C.	—	N.C.
3	TJMON	Output	VBE monitor
4	DECAY1	Input	Mix Decay setup 1
5	DECAY2	Input	Mix Decay setup 2
6	BOUT2	Output	Phase B motor drive output 2
7	RCSB	Input/Output	Phase B motor current detection
8	BOUT1	Output	Phase B motor drive output 1
9	AOUT2	Output	Phase A motor drive output 2
10	RCSA	Input/Output	Phase A motor current detection
11	AOUT1	Output	Phase A motor drive output 1
12	N.C.	—	N.C.
13	BC1	Output	Capacitor connection 1 for charge pump
14	BC2	Output	Capacitor connection 2 for charge pump
15	VPUMP	Output	Charge pump circuit output
16	VM2	Power supply	Power supply 2 for motor
17	ENABLEA	Input	Phase A Enable/Disable CTL
18	ENABLEB	Input	Phase B Enable/Disable CTL
19	STBY	Input	Standby
20	NFAULT	Output	Abnormal detection output
21	VREFA	Input	Phase A Torque reference voltage input
22	VREFB	Input	Phase B Torque reference voltage input
23	VREG	Output	Internal reference voltage (output 3.3 V)
24	TEST	Input	Test mode setup
25	GND	Ground	Ground
26	PHA	Input	Phase A phase selection input
27	PHB	Input	Phase B phase selection input
28	IN0	Input	Phase A output torque control 1
29	IN1	Input	Phase A output torque control 2
30	IN2	Input	Phase B output torque control 1
31	IN3	Input	Phase B output torque control 2
32	PWMSW	Input	PWM OFF period selection input

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

1. Control mode

1) Truth table (output control)

STBY	ENABLEA	ENABLEB	Control / Charge pump circuit	Ach output transistor	Bch output transistor
Low	-	-	OFF	OFF	OFF
High	Low	High	ON	OFF	ON
High	High	Low	ON	ON	OFF
High	High	High	ON	ON	ON

Note) Input external signals to STBY pin in order to set STBY signal to High-level.
Because, STBY pin cannot be set to High-level when it is connected to VREG.
Note) Low : 0V～0.8V 、High : 2.1V～5.5V

2) Truth table (PHA/PHB input)

PHA/PHB	AOUT1/BOUT1	AOUT2/BOUT2
High	High	Low
Low	Low	High

Note) Low : 0V～0.8V 、High : 2.1V～5.5V

3) Truth table (PWM OFF period selection)

PWMSW	PWM OFF period
Low	28.0 μ sec
Middle or OPEN	8.1 μ sec
High	15.2 μ sec

Note) Low : 0V～0.6V, Middle : 1.2V～1.7V ,High : 2.3V～5.5V
Note) PWMSW can be set to Middle by setting PWMSW to Open. However, it might occur the error of operation due to the noise. In case, connect the capacity of 0.01 μ F or more between PWMSW and GND .

4) Truth table (Decay selection)

DECAY1	DECAY2	Decay control
Low	Low	Slow Decay
Low	High	25%
High	Low	50%
High	High	100%

Note) The above rate is applied to Fast Decay every PWM OFF period.
Note) Low : 0V～0.8V 、High : 2.1V～5.5V
Note) DECAY1 and DECAY2 can be set to Low by setting DECAY1 and DECAY2 to Open.
However, it might change to High setting due to the noise. In case, DECAY1 pin and DECAY2 pin is shorted to GND.

5) Truth table (IN0～IN3 control)

IN0/IN2	IN1/IN3	output current
Low	Low	$(VREF / 10) \times (1 / Rs) \times 100\% = I_{OUT}$
High	Low	$(VREF / 10) \times (1 / Rs) \times 70.7\% = I_{OUT}$
Low	High	$(VREF / 10) \times (1 / Rs) \times 38.4\% = I_{OUT}$
High	High	0

Note) Rs : current detection resistance
Note) IN0 = IN1 = High / IN2 = IN3 = High, all outputs transistors turn off.
Note) Low : 0V～0.8V 、High : 2.1V～5.5V

6) Truth table (NFAULT output)

TSD	OCP	NFAULT	Output transistor
Thermal shutdown protection start	—	Low	All channel output : OFF
—	Over-current detection start	Low	All channel output : OFF
Thermal shutdown protection stop	Over-current detection stop	Hi-Z	ON

Notes)
・TSD is a latch type protection→ The protection operation starts at 150°C. (All motor outputs are turned off , and latched.)
The latch is released by Standby or UVLO.
・OCP is a latch type protection → All motor outputs are turned off by over-current detection, and be latched.
The latch is release by Standby or UVLO. In addition, All motor outputs are turned off at under UVLO.
・NFAULT is an open drain output → If it uses NFAULT pin ,connect the resistance between VREG and NFAULT pin.
The recommended value of resistance is 100kΩ. If it don't use NFAULT, it recommends open pins.

OPERATION (continued)

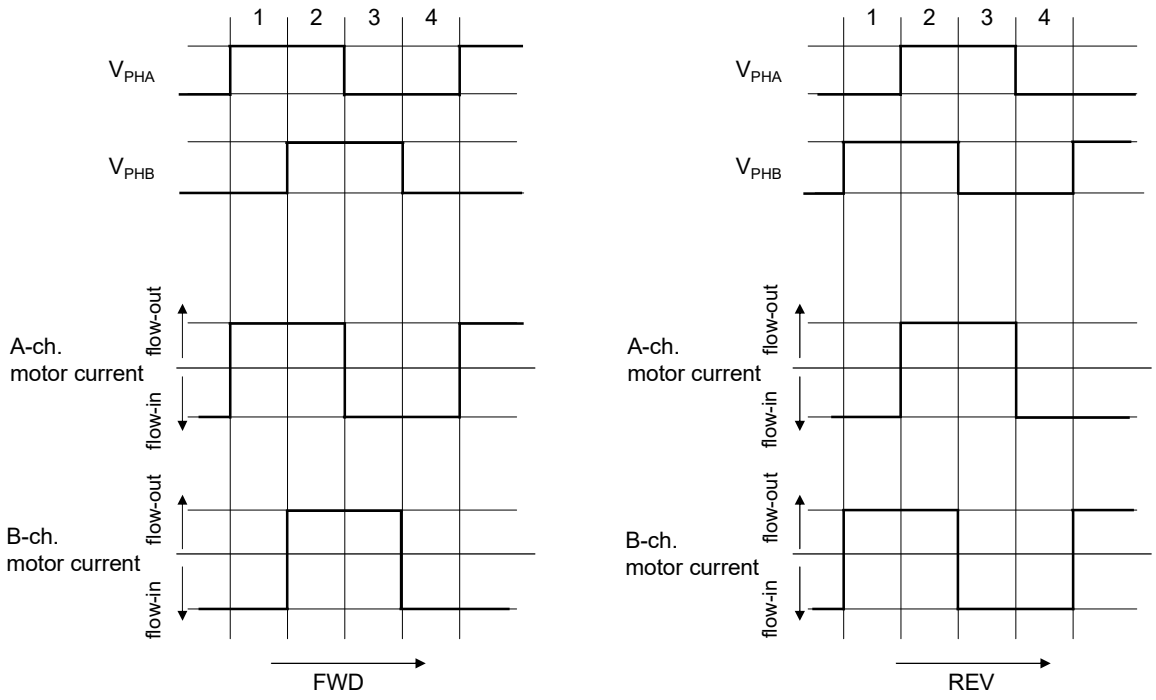
2. About motor current setup

Motor current is represented by the following formula.

- motor current :Imotor = (VREF × 0.1) / RCS (current detection resistance)

3. Each phase current value (Timing chart)

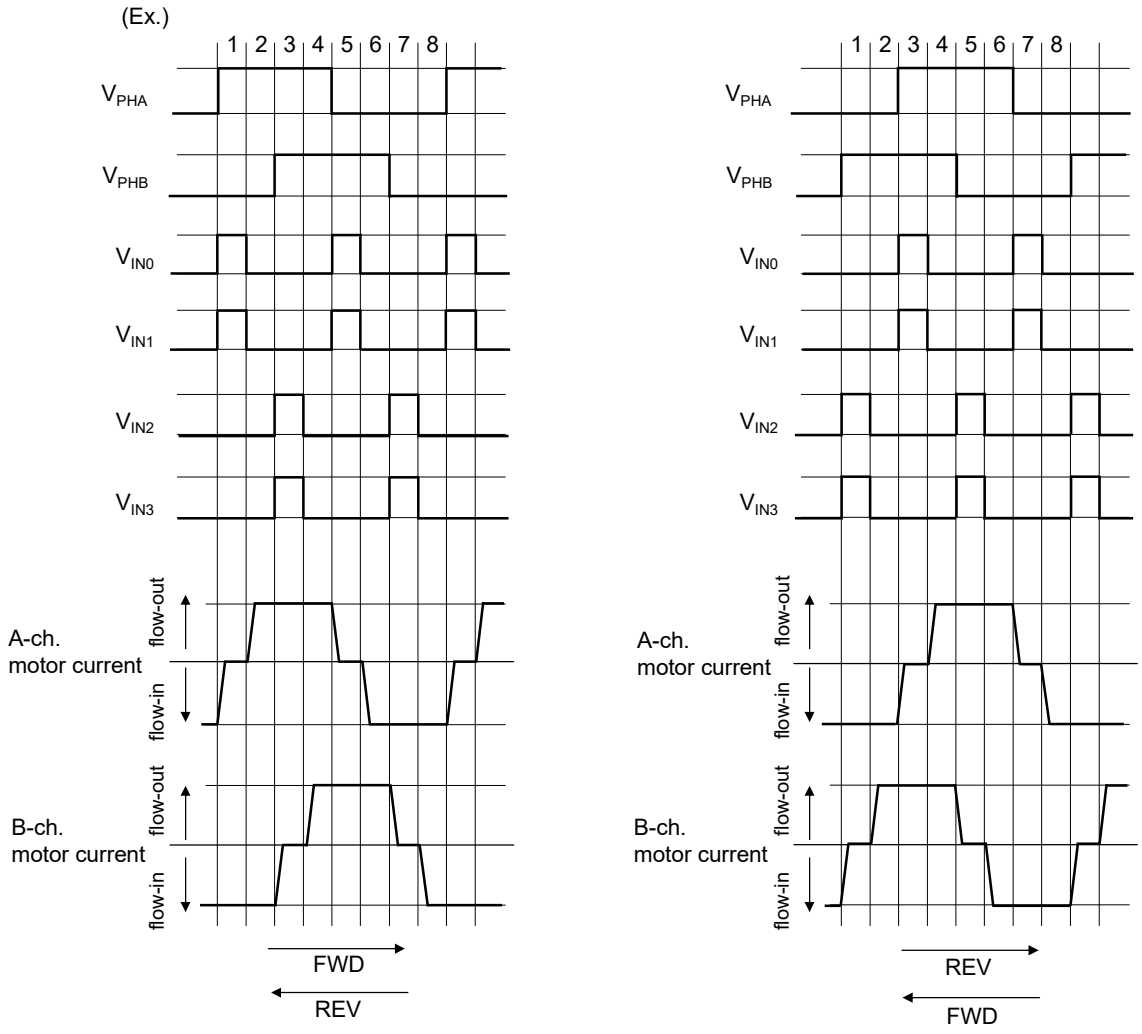
1) 2-phase excitation drive (4-step sequence)
(IN0～IN3 = const.)



OPERATION (continued)

3. Each phase current value (Timing chart) (continued)

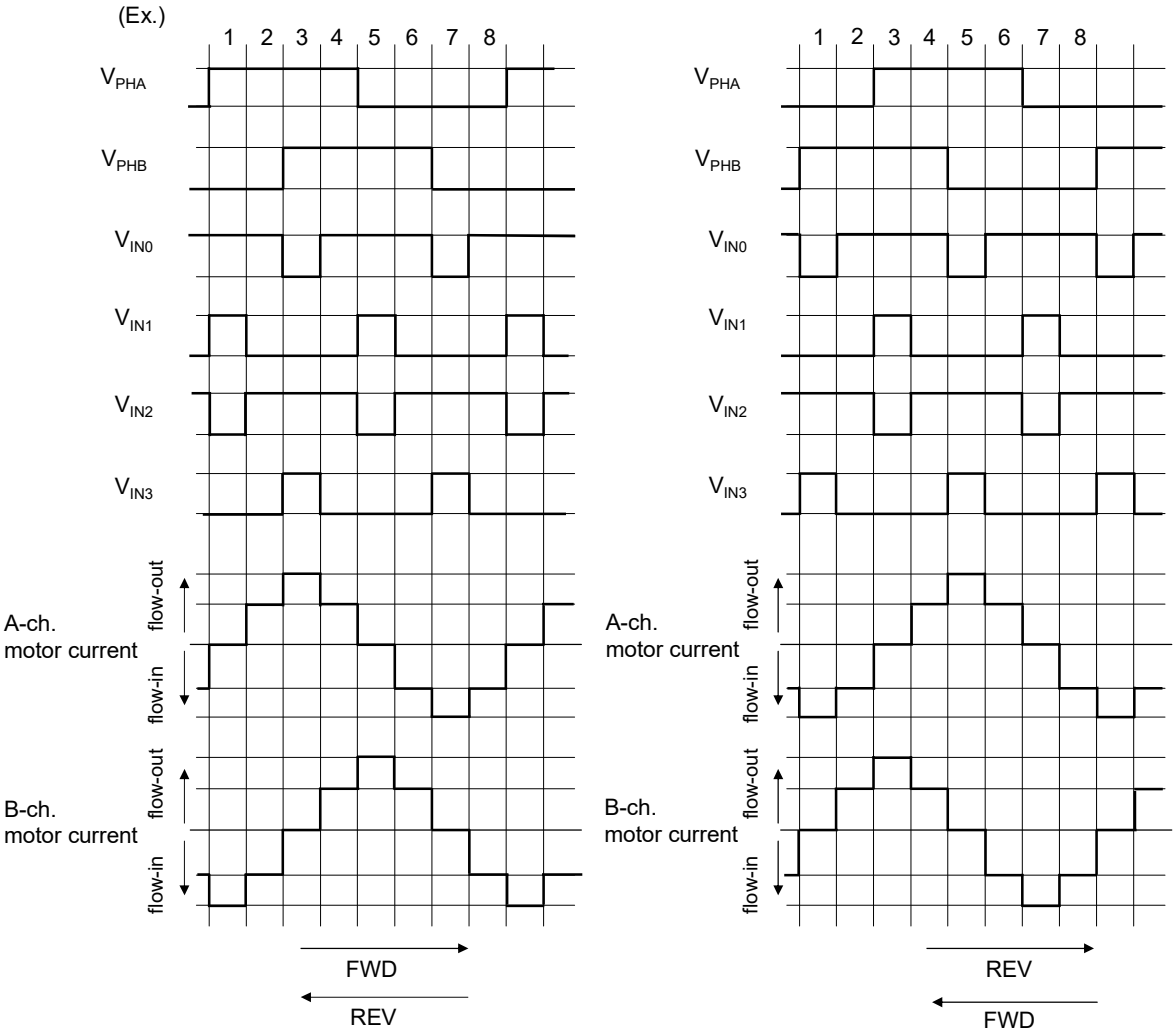
2) Half-step drive (8-step sequence)



OPERATION (continued)

3. Each phase current value (Timing chart) (continued)

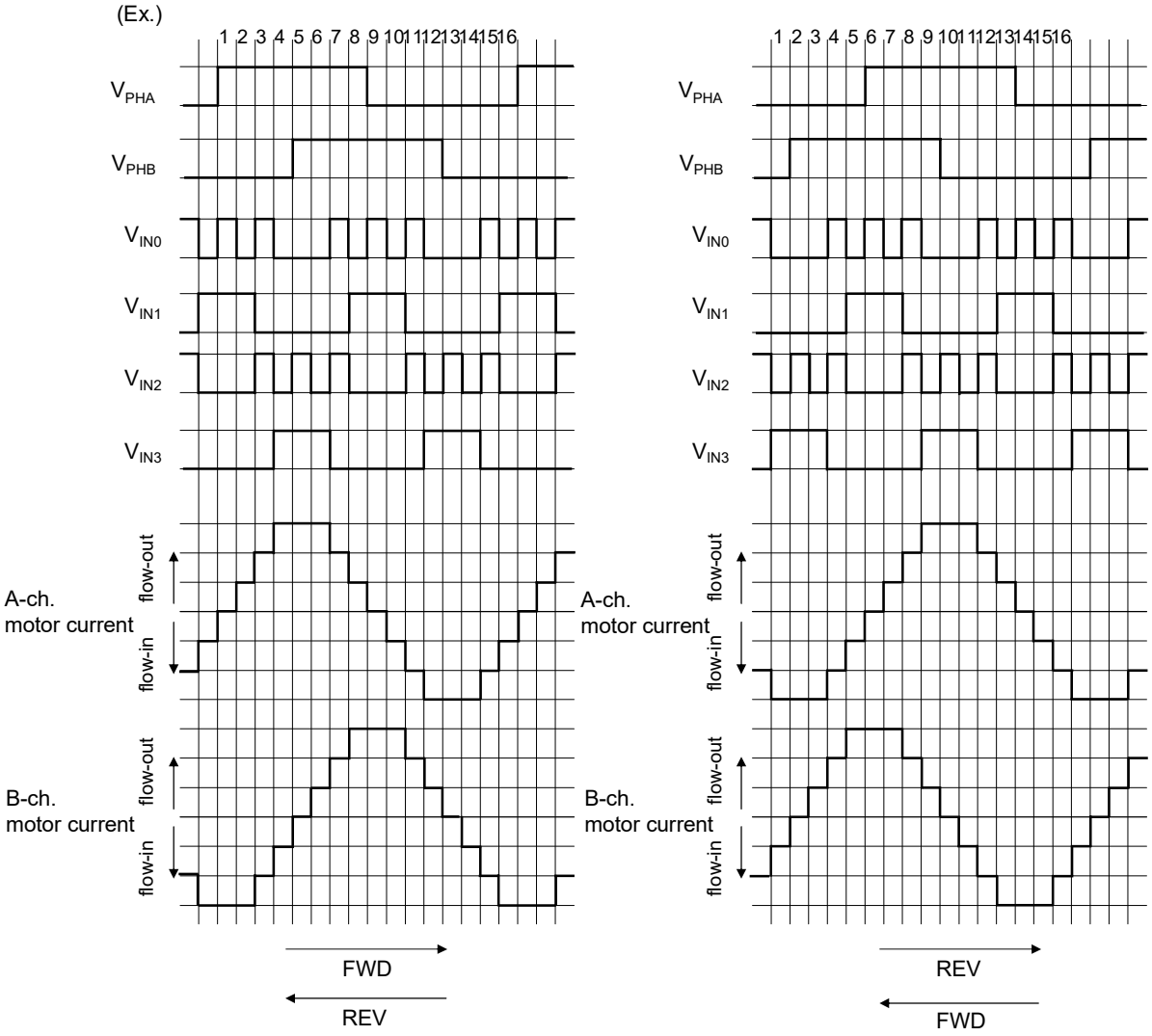
3) 1-2-phase excitation drive (8-step sequence)



OPERATION (continued)

3. Each phase current value (Timing chart) (continued)

4) W1-2-phase excitation drive (16-step sequence)



APPLICATIONS INFORMATION

1. Notes

1) Pulse blanking time

This LSI has pulse blanking time (0.75 µs/Typ. value) to prevent erroneous current detection caused by noise. Therefore, the motor current value will not be less than current determined by pulse blanking time. Pay attention at the time of low current control. The relation between pulse blanking time and minimum current value is shown as Figure1. In addition, increase-decrease of motor current value is determined by L value, wire wound resistance, induced voltage and PWM on Duty inside a motor.

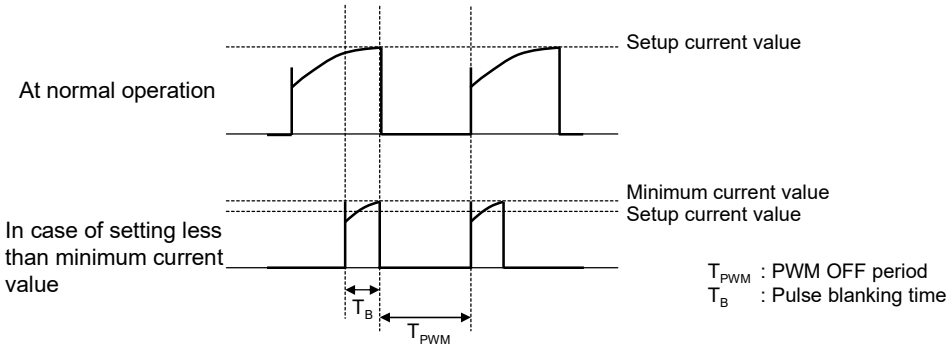


Figure1. RCS current waveform

2) VREF voltage

When VREF* voltage is set to Low-level, erroneous detection of current might be caused by noise because threshold of motor current detection comparator becomes low (= VREF/10 × motor current ratio [%]).
Use this LSI after confirming no misdetection with setup VREF* voltage.
Measures such as adding capacity are recommended, if the VREF* voltage is not stabilized due to the noise.
The recommended value of capacity is 0.01µF. (* : A or B)

3) Notes on interface, DECAY1,DECAY2,PWMSW,TEST

Absolute maximum of Pin 4 to 5, Pin 17 to 19, Pin 21 to 22, Pin 24 and Pin 26 to 32 is –0.3 V to 6 V. When the setup current for a motor is large and lead line of GND is long, GND pin potential might rise. Take notice that above-mentioned pin potential is negative to difference in potential between GND pin reference and above-mentioned pin in spite of inputting 0 V to the above-mentioned pin. At that time, pay attention allowable voltage range must not be exceeded.(*Interface pin: ENABLEA, ENABLEB, IN0~3, PHA, PHB, STBY,VREFA,VREFB)

4) Notes on ENABLE and IN0~3

In case it set ENABLEA,ENABLEB,IN0~3 pin to High -level, short above-mentioned pins to VREG or input external High-level signal. In case it set ENABLEA,ENABLEB,IN0~3 pin to Low -level, short above-mentioned pins to GND.

5) Notes on DECAY1 and DECAY2 and PWMSW

DECAY1 and DECAY2 and PWMSW are not IF pin. As for the High/Low setting of DECAY1, DECAY2, PWMSW, it is recommended to short to GND or VREG. If the above pins are high-impedance such as open, note that this LSI might not operate normally because it easily influences the noise.
PWMSW can be set to Middle by setting PWMSW to Open. However, it might occur the error of operation due to the noise. In case, connect the capacity of 0.01µF or more between PWMSW and GND .

6) Notes on test mode

When inputting voltage of above 0.8 V to TEST (Pin 24), this LSI might become test mode.
When disturbance noise etc. makes this LSI test mode, motor might not operate normally. Therefore, use this LSI on condition that TEST pin is shorted to GND at normal motor operation.

7) Notes on N.C. pin

It recommends connecting N.C. pin to GND.

APPLICATIONS INFORMATION (continued)

1. Notes (continued)

8) Notes on Standby mode release / Under-voltage lockout release

This LSI has all motor outputs OFF period of about 400 µs (typ) owing to release of Standby and UVLO (Refer to the below figure).

This is why restart from Standby and UVLO after charge pump voltage rises sufficiently because charge pump operation stops at Standby and UVLO.

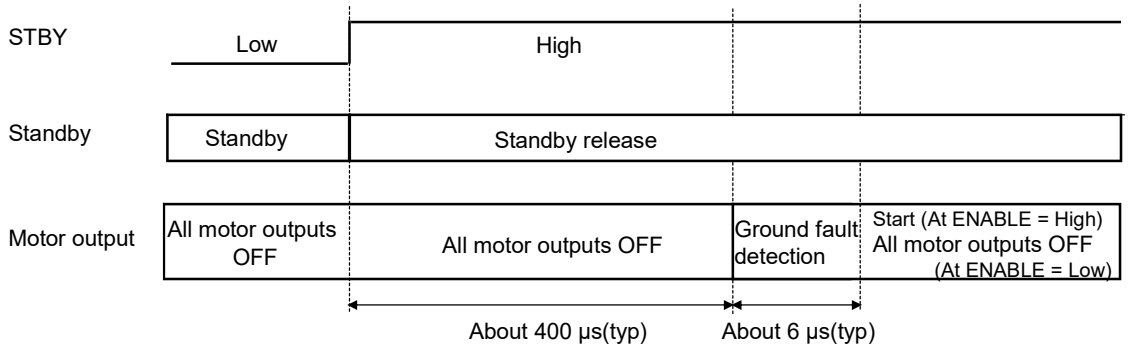
When the charge pump voltage does not rise sufficiently during all motor outputs OFF period due to that capacitance between VPUMP and GND becomes large etc., the LSI might overheat and it might not operate normally. In this case, release Standby and UVLO at ENABLE = Low-level, and restart at ENABLE = High-level after the charge pump voltage rises sufficiently.

After all motor outputs OFF period, the ground-fault detection period is set to about 6 µs in order to detect the ground-fault of motor output before motor is turned on.

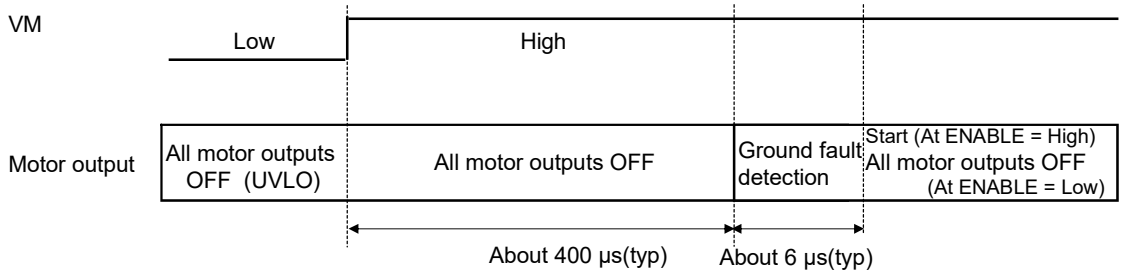
All the upper side power MOS are turned on during the above ground fault detection period, and then whether the ground-fault occurs or not is checked. (Refer to the following contents.)

If the ground-fault is detected at that time, all motor outputs are turned off, and motor drive stops.

[At Standby release]



[At under-voltage lockout release]



APPLICATIONS INFORMATION (continued)

1. Notes (continued)

9) Notes on RCS line

Take consideration in the below figure and the points and design PCB pattern.

(1) Point 1

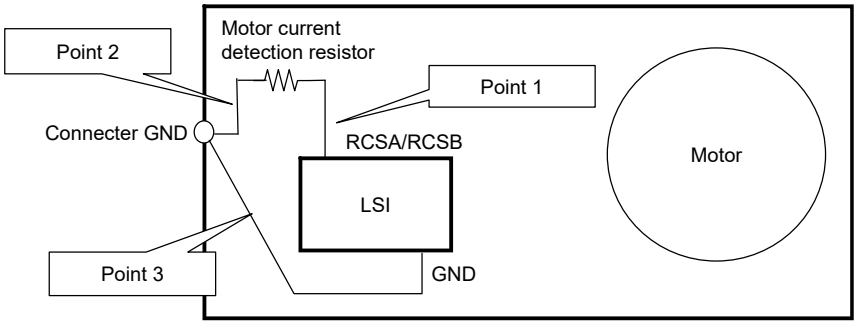
Design so that the wiring to the current detection pin (RCSA/RCSB pin) of this LSI is thick and short to lower impedance. This is why current can not be detected correctly owing to wiring impedance and current might not be supplied to a motor sufficiently.

(2) Point 2

Design so that the wiring between current detection resister and connecter GND (the below figure Point 2) is thick and short to lower impedance. As the same as Point 1, sufficient current might not be supplied due to wiring impedance. In addition, if there is a common impedance on the side of GND of RCSA/RCSB, peak detection might be erroneous detection. Therefore, install the wiring on the side of GND of RCSA/RCSB independently.

(3) Point 3

Connect GND pin of this LSI to the connecter on PCB independently. Separate the wiring removed current detection resister of large current line (Point 2) from GND wiring and make these wirings one-point shorted at the connecter as the below figure. That can make fluctuation of GND minimum.



10)Note of a substrate pattern design

A high current flows into the LSI. Therefore, the common impedance of PCB can not be ignored. Take the following points into consideration and design the PCB pattern for a motor. Because the wiring connecting to VM1 (Pin 1) and VM2 (Pin 16)of this LSI is high-current, it is easy to generate noise at time of switching by wiring L. That might cause malfunction and destruction (Figure 2). As Figure 3, the escape way of the noise is secured by connecting a capacitor to the connector close to the VM pin of the LSI. This makes it possible to suppress the fluctuation of direct VM pin voltage of the LSI. Make the setting as shown in Figure 3 as much as possible.

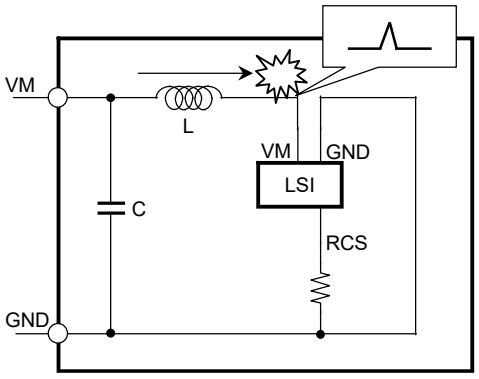


Figure 2. No recommended pattern

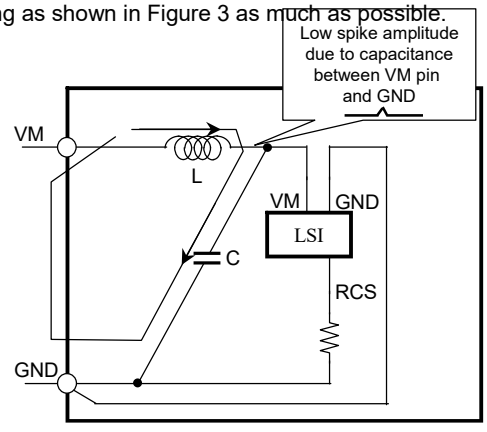


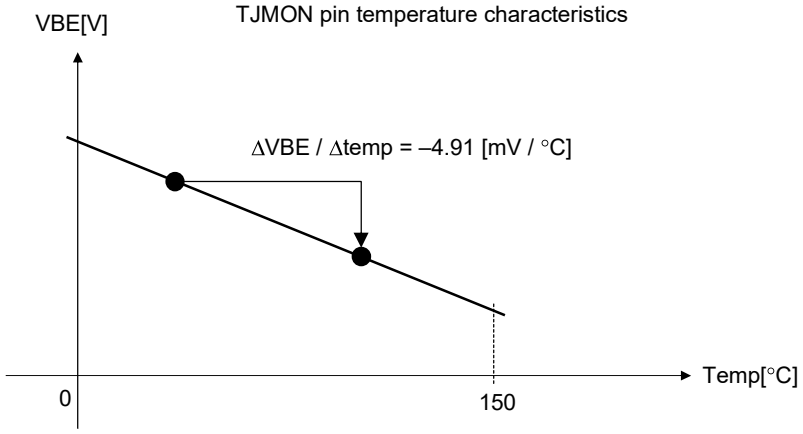
Figure 3. Recommended pattern

APPLICATIONS INFORMATION (continued)

1. Notes (continued)

11) LSI junction temperature

In case of measuring chip temperature of this LSI, measure the voltage of TJMON pin (Pin 3) and estimate the chip temperature from the data below. However, because this data is technical reference data, conduct a sufficient reliability test of the LSI and evaluate the product with the LSI incorporated.



12) Power-on and Supply voltage change

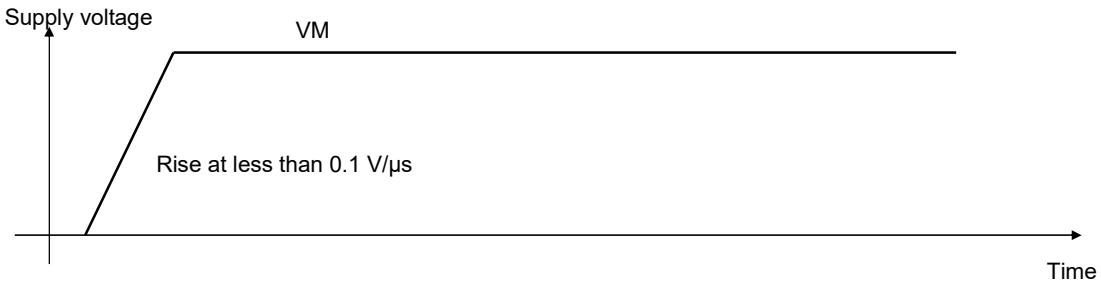
When supplying to VM pin (Pin 1, 16) or raising supply voltage, set the rise speed of VM voltage to less than 0.1 V/µs . If the rise speed of supply voltage is too rapid, it might cause error of operation and destruction of the LSI. If the rise speed of VM voltage is more rapid than 0.1V/µs, conduct a sufficient reliability test and also check a sufficient evaluation for a product.

In addition, rise the VM supply voltage in an ENABLE = Low state when change VM supply voltage from low voltage to high voltage within the operating supply voltage range.

Since there is not the all motor outputs OFF period shown in P17. APPLICATION INFORMATION 8) for the supply voltage change within the operating supply voltage range, the VPUMP voltage is in a low voltage state due to not following to VM supply voltage change enough, and this LSI might not operate normally.

Therefore, restart this LSI by setting ENABLE to High after the VPUMP voltage rises enough.

In addition, it is recommended to fall VM voltage in motor stop state (ENABLEA/B = Low or STBY = Low) for the stable fall of supply voltage.



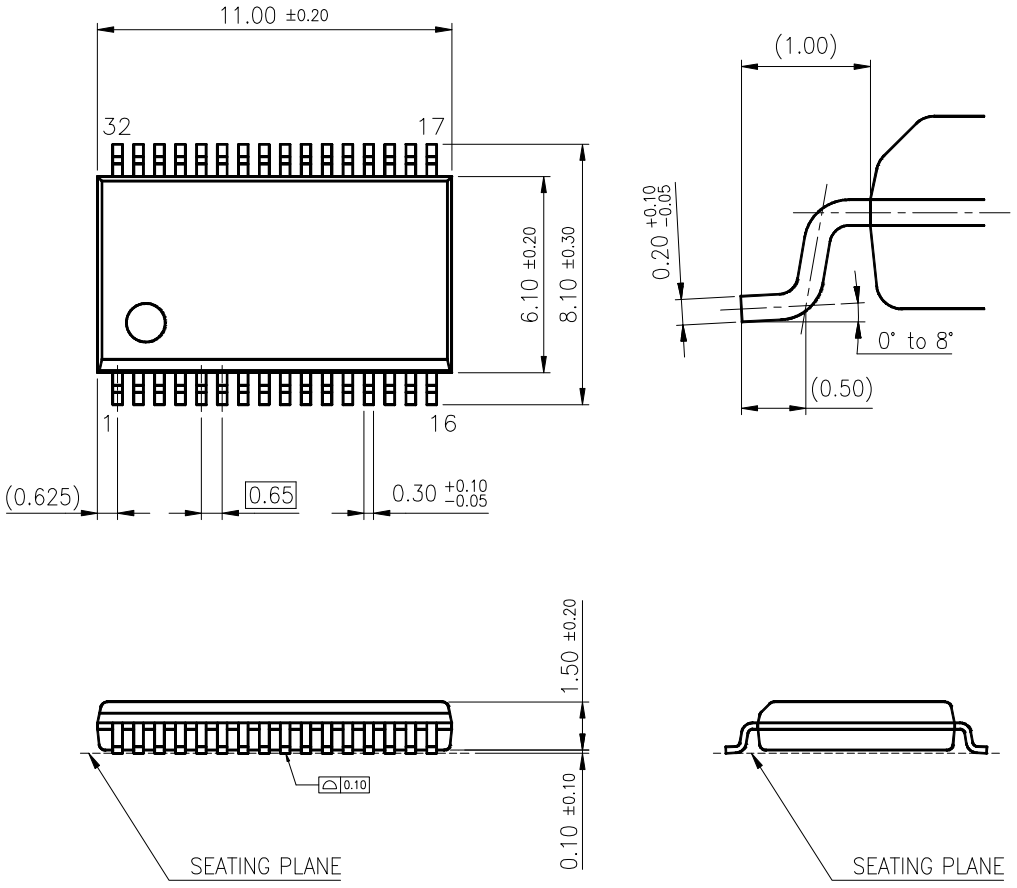
13) Over-current protection function

This LSI has over-current protection (OCP) circuit to protect from the ground-fault etc. of the motor output. When motor current more than setting value flows to power MOS for about 5 µs (Typ.) due to the ground-fault, all motor outputs are turned OFF by latch operation. OCP is canceled by STBY = Low or UVLO (Under-voltage lockout) operation. However, the OCP circuit do not guaranteed the protection circuit of set. Therefore, do not use the OCP function of this LSI to protect a set. Note that this LSI might break before the protection function operates when it instantaneously exceeds the safe operation area and the maximum rating. When the inductor element is large due to the length of wiring at ground-fault, note that this LSI might break. Because the motor output voltage falls on a negative voltage or excessively rises after motor current excessively flows to motor outputs.

PACKAGE INFORMATION (Reference Data)

Package Code :SSOP032-P-0300D

unit : mm



Body Material	:	Br/Sb Free Epoxy resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	SnBi Plating

■ IMPORTANT NOTICE

1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this LSI, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our LSI being used by our customers, not complying with the applicable laws and regulations.
4. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
5. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
6. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
7. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VM short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short).

   Especially, for the pins below, take notice Power supply fault, Ground fault, short to motor current detection pin, load short and short between the pin.
   - Motor drive output pin (Pin 6, 8, 9, 11)
   - Motor current detection pin (Pin 7, 10)
   - Charge pump circuit pin (Pin 13, 14, 15)
   - Power supply (Pin 1, 16)

   Safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply..
8. This LSI is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the LSI being used for any special application, unless our company agrees to the use of such special application.
9. This LSI is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the LSI being used in automotive application, unless our company agrees to such application in this book.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VM short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Product which has specified ASO (Area of Safe Operation) should be operated in ASO
13. Verify the risks which might be caused by the malfunctions of external components.

■ IMPORTANT NOTICE (continued)

14. Confirm characteristics fully when using the LSI. Secure adequate margin after considering variation of external part and this LSI including not only static characteristics but transient characteristics. Especially, Pay attention that abnormal current or voltage must not be applied to external parts because the pins (Pin 6, 8, 9, 11, 13, 14, 15) output high current or voltage.
15. Design the heat radiation with sufficient margin so that Power dissipation must not be exceeded base on the conditions of power supply voltage, load and ambient temperature.
    (It is recommended to design to set connective parts to 70% to 80% of maximum rating)
16. Set capacitance value between VPUMP and GND so that VPUMP (Pin 15) must not exceed 43 V transiently at the time of motor standby to motor start.
17. This LSI employs a PWM drive method that switches the high-current output of the output transistor. Therefore, the LSI is apt to generate noise that may cause the LSI to malfunction or have fatal damage. To prevent these problems, the power supply must be stable enough. Therefore, the capacitance between the VREG and GND pins must be a minimum of 0.1 μF and the one between the VM and GND pins must be a minimum of 47 μF and as close as possible to the LSI so that PWM noise will not cause the LSI to malfunction or have fatal damage.

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(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information de-scribed in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Please consult with our sales staff in advance for information on the following applications, moreover please exchange documents separately on terms of use etc.: Special applications (such as for in-vehicle equipment, airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, medical equipment and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
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(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Other-wise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. We do not guarantee quality for disassembled products or the product re-mounted after removing from the mounting board.
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