

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN65558, SN75558 ELECTROLUMINESCENT ROW DRIVERS

SLDS018B – D2999, DECEMBER 195 – REVISED APRIL 1993

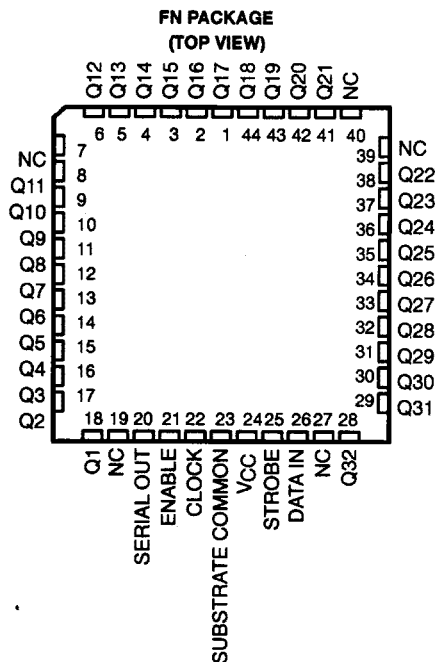
- Each Device Drives 32 Electrodes
- High-Voltage Open-Collector NPN Outputs Using Ramped Supply
- 300-mA Output Current Capability
- CMOS-Compatible Inputs
- Very Low Steady-State Power Consumption

description

These devices are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible, and all outputs are high-voltage open-collector npn transistors.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to SUBSTRATE COMMON. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The serial data output (SERIAL OUT) from the shift register can be used to cascade additional devices. This output is not affected by the ENABLE or STROBE inputs.

The SN65558 is characterized for operation from –40°C to 85°C. The SN75558 is characterized for operation from 0°C to 70°C.



NC – No internal connection

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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SN75558, SN75558S

CMOS/EL DISP
[Emitter Supply]

Pin 23: SUBSTRATE COMMON
Pin 25: COMMON
Pin 21: ENABLE
Pin 22: CLOCK
Pin 26: DATA IN

Internal Components:
V3
Q2
SRG 32
C1

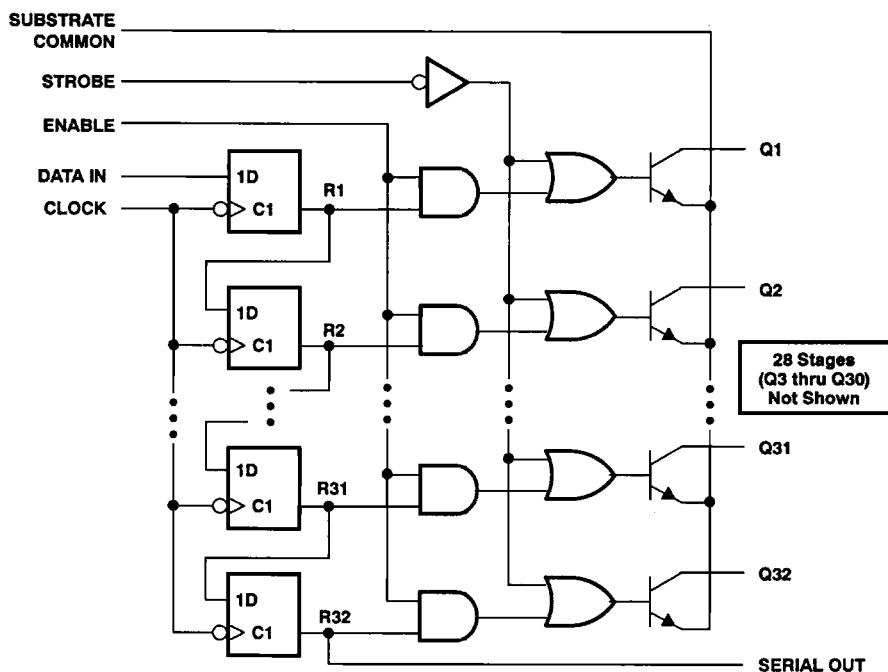
Outputs (Right Side):
Pin 18: Q1
Pin 17: Q2
Pin 8: Q11
Pin 6: Q12
Pin 1: Q15
Pin 44: Q16
Pin 41: Q21
Pin 38: Q22
Pin 29: Q31
Pin 28: Q32
Pin 20: SERIAL OUT

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
Load	↓ No ↓	X X	X X	Load and shift† No change	R32 R32	Determined by ENABLE and STROBE Determined by ENABLE and STROBE
Enable	X X	L H	H H	As determined above As determined above	R32 R32	All Q outputs off Determined by R1 through R32
Strobe	X	X	L	As determined above	R32	All Q outputs on

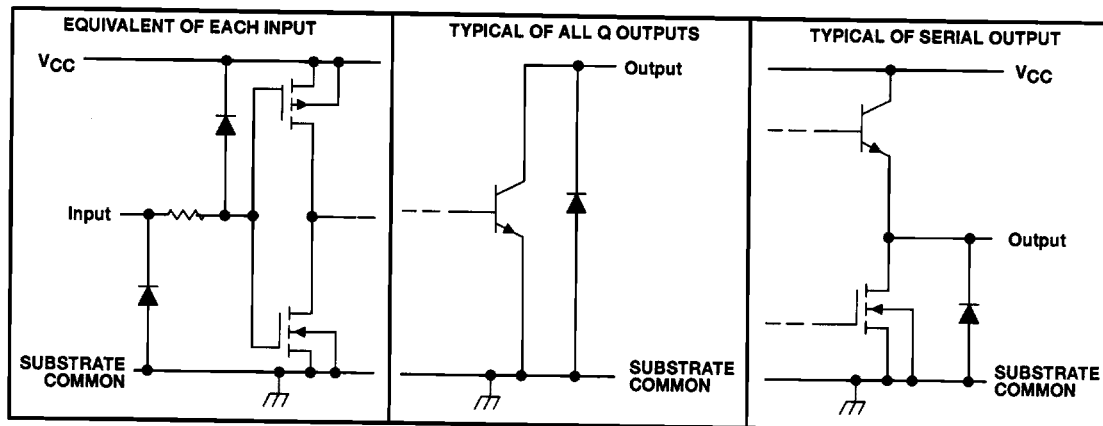
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

† Register R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

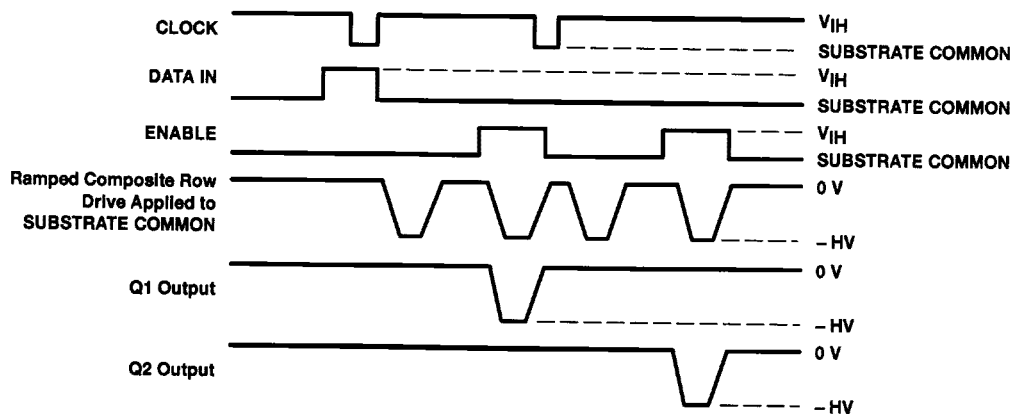
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schematic of inputs and outputs



typical operating sequence



HV = High voltage

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Off-state output voltage, $V_{O(off)}$ (see Note 2)	110 V
Input voltage, V_I	$V_{CC} + 0.3$ V
Substrate common terminal current (see Note 3)	750 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 4)	1700 mW
Operating free-air temperature range: SN65558	– 40°C to 85°C
SN75558	0°C to 70°C
Storage temperature range	– 65°C to 150°C
Case temperature for 10 seconds	260°C

NOTE 1: Voltage values are with respect to SUBSTRATE COMMON.

- Data must be clocked into the shift register and Q outputs enabled prior to ramping SUBSTRATE COMMON to –HV (see typical operating sequence).
- Duty cycle is limited by package dissipation.
- For operation above 25°C free-air temperature, derate linearly to 1088 mW at 70°C, and 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	10.8	12	15	V
High-level input voltage, V_{IH} (see Figure 1)	$V_{CC} = 10.8$ V		8.1	11.1
	$V_{CC} = 15$ V		11.25	15.3
Low-level input voltage, V_{IL} (see Figure 1)	$V_{CC} = 10.8$ V		–0.3	2.7
	$V_{CC} = 15$ V		–0.3	3.75
Off-state Q output voltage, $V_{O(off)}$			–0.3	100
On-state Q output current, $I_{O(on)}$, duty cycle $\leq 1\%$, $V_{CC} = 15$ V				300
Rate of rise for SUBSTRATE COMMON, dv/dt				100
Clock frequency, f_{clock}			0	4
Pulse duration, CLOCK high or low, t_w			125	ns
Setup time, t_{su}	DATA IN before CLOCK↓ (see Figure 2)		50	ns
	ENABLE before SUBSTRATE COMMON ↓ (see Figure 4)		500	
Hold time, DATA IN after CLOCK↓, t_h (see Figure 2)			100	ns
Operating free-air temperature, T_A	SN65558		–40	85
	SN75558		0	70

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 12$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN65558		SN75558		UNIT
				MIN	MAX	MIN	MAX	
I _{O(off)}	Off-state Q output current		V _O = 100 V	20		10		μA
V _{OH}	High-level output voltage	SERIAL OUT	I _O = −100 μA	10.5		10.5		V
V _{OL}	Low-level output voltage	Q outputs	I _{OL} = 300 mA	20		10		V
		SERIAL OUT	I _{OL} = 100 μA	1		1		
I _{IH}	High-level input current		V _I = 12 V	1		1		μA
I _{IL}	Low-level input current		V _I = 0	−1		−1		μA
I _{CC}	Supply current from V _{CC}			250		250		μA

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switching characteristics, $V_{CC} = 12\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level, SERIAL OUT from CLOCK	$C_L = 20\text{ pF}$ to SUBSTRATE COMMON, (see Figure 3)		200	ns
t_{PLH} Propagation delay time, low-to-high-level, SERIAL OUT from CLOCK			200	ns
$t_{d(on)}$ Turn-on delay time, Q outputs from ENABLE	$dv/dt = 100\text{ V}/\mu\text{s}$, STROBE at V_{CC} , $R_L = 2\text{ k}\Omega$ to 60 V (see Figure 4)		500	ns

RECOMMENDED OPERATING CONDITIONS

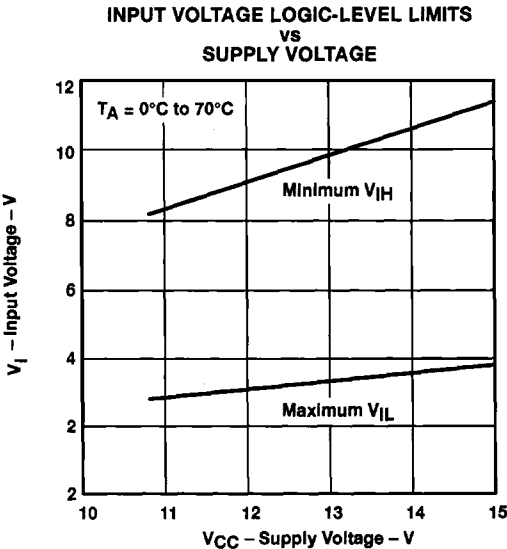


Figure 1

PARAMETER MEASUREMENT INFORMATION

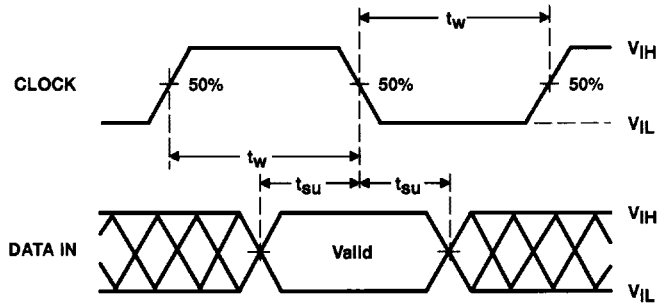


Figure 2. Input-Timing Voltage Waveforms

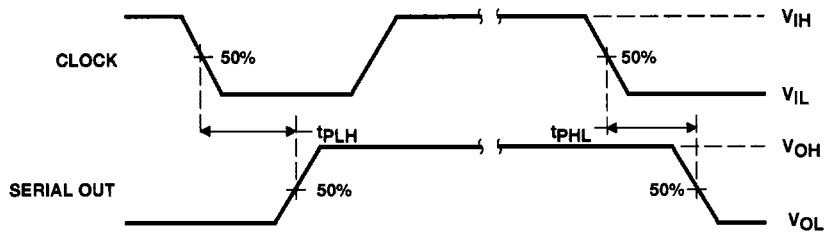


Figure 3. Voltage Waveforms for Propagation Delay Time, CLOCK to SERIAL OUT

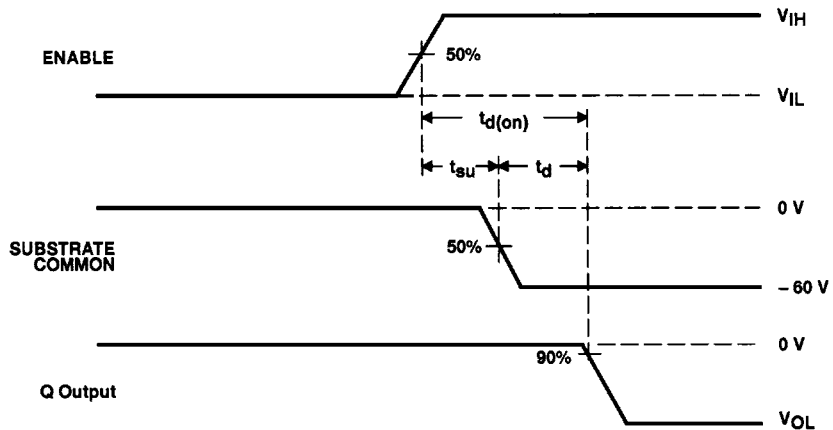


Figure 4. Voltage Waveforms for Turn-On Delay Time, SUBSTRATE COMMON to Q Output

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TYPICAL CHARACTERISTICS

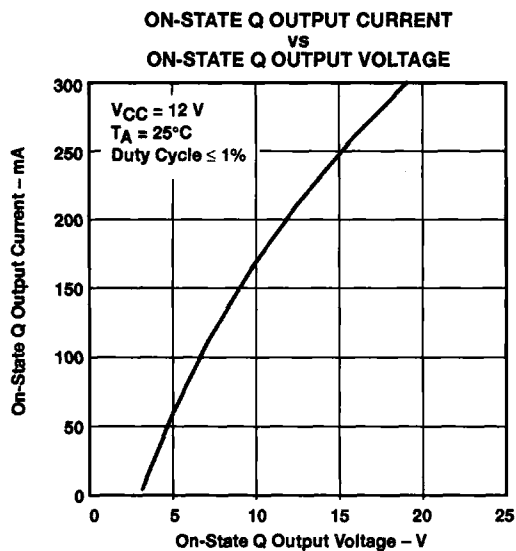


Figure 5