NCT6776F / NCT6776D

Nuvoton LPC I/O

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1. GENERAL DESCRIPTION

The NCT6776F / NCT6776D is a member of Nuvoton's Super I/O product line. The NCT6776F / NCT6776D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the NCT6776F / NCT6776D adopts the Current Mode (dual current source) and thermistor sensor approach. The NCT6776F / NCT6776D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ IV, which makes the system more stable and user-friendly.

The NCT6776F / NCT6776D supports four – 360K, 720K, 1.2M, 1.44M, or 2.88M – disk drive types and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s, 1 Mb/s, and 2 Mb/s. The disk drive adapter supports the functions of floppy disk drive controller (compatible with the industry standard 82077/ 765), data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. Such a wide range of functions integrated into one NCT6776F / NCT6776D greatly reduce the number of required components to interface with floppy disk drives.

The NCT6776F / NCT6776D provides two high-speed serial communication port (UART), which includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The NCT6776F / NCT6776D supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP). The NCT6776F / NCT6776D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT6776F / NCT6776D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT6776F / NCT6776D supports the Intel® PECI (Platform Environment Control Interface) and AMD® SB-TSI interface. The NCT6776F / NCT6776D supports separated VID input and output pins for Vcore voltage adjustment. It also supports AMD® CPU power on sequence, and it also supports Intel® Deep Sleep Well glue logic to help customers to reduce the external circuits needed while using Deep Sleep Well function.

The NCT6776F / NCT6776D supports to decode port 80 diagnostic messages on the LPC bus. This could help on system power on debugging. It also supports two-color LED control to indicate system power states. The NCT6776F / NCT6776D supports Consumer IR function for remote control purpose. It also supports Advanced Power Saving function to further reduce the power consumption while the system is at S5 state.

The configuration registers inside the NCT6776F / NCT6776D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

Meet LPC Specification 1.1
Support AMD power on sequence
Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
Integrated hardware monitor functions
Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
Programmable configuration settings
Single 24-MHz or 48-MHz clock input
Support selective pins of 5 V tolerance

FDC

Variable write pre-compensation with track-selection capability
Support vertical recording format
DMA-enable logic
16-byte data FIFO
Support floppy disk drives and tape drives
Detect all overrun and underrun conditions
Built-in address mark detection circuit to simplify the read electronics
FDD anti-virus functions with software write protect and FDD-write enable signal (write data signal forced to be inactive)
Support 3.5-inch or 5.25-inch floppy disk drives
Compatible with industry standard 82077
360K / 720K / 1.2M / 1.44M / 2.88M formats
250K, 300K, 500K, 1M, 2M bps data transfer rate
Support 3-mode FDD and its Windows driver

UART

Two high-speed, 16550-compatible UART with 16-byte send / receive FIFO
Support RS485
--- Supports auto flow control
Fully programmable serial-interface characteristics:
--- 5, 6, 7 or 8-bit characters
--- Even, odd or no parity bit generation / detection
--- 1, 1.5 or 2 stop-bit generation
Internal diagnostic capabilities:
--- Loop-back controls for communications link fault isolation
--- Break, parity, overrun, framing error simulation
Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16}-1)
Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Parallel Port

Compatible with IBM® parallel port
Support PS/2-compatible bi-directional parallel port
Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
Enhanced printer port back-drive current protection

Keyboard Controller

8042-based keyboard controller
Asynchronous access to two data registers and one status register
Software-compatible with 8042
Support PS/2 mouse
Support Port 92
Support both interrupt and polling modes
Fast Gate A20 and Hardware Keyboard Reset
12MHz operating frequency

Hardware Monitor Functions

Smart Fan control system
Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
Support Current Mode (dual current source) temperature sensing method
Nine voltage inputs (CPUVCORE, VIN[0..3], 3VCC, AVCC, 3VSB and VBAT)
Five fan-speed monitoring inputs
Three fan-speed controls
Dual mode for fan control (PWM and DC) for SYSFANOUT
Built-in case-open and CPU socket occupied detection circuit
Programmable hysteresis and setting points for all monitored items
Issue SMI#, OVT# (Over-temperature) to activate system protection
Nuvoton Health Manager support
Provide I^2C master / slave interface to read / write registers

CIR and IR (Infrared)

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR, including CIRTX, CIRRX, CIRRXWB, CIR LED, CIR SENSE

VCORE Voltage Adjustment

Support INTEL® VRM11.1 VID input to VID output
Watch Dog Timer for VID over-voltage failure recovery
Support AMD® Parallel VID input to VID output
Support Intel® VR12 SVID
Support AMD® Serial VID input to Serial VID output

General Purpose I/O Ports

GPIO0 ~ GPIOA programmable general purpose I/O ports
Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

ACPI Configuration

Support Glue Logic functions
Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys
Mouse Wake-Up by programmable buttons
OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 1.1, 2.0 and 3.0 specification
Support 2 CPU addresses and 2 domains per CPU address

AMD SB-TSI Interface

Support AMD® SB-TSI specification

SMBus Interface

Support SMBus Slave interface to report Hardware Monitor device data
Support SMBus Master interface to get thermal data from PCH
Support SMBus Master interface to get thermal data from MXM module

Power Measurement

Support Power Consumption measurement
Fading LED driver control for power status and diagnostic indications

Intel Deep Sleep Well (DSW) Glue Logic

Support Deep Sleep Well (DSW) Glue Logic

AMD® CPU Power on Sequence

Support AMD® CPU power on sequence

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Operation voltage

- 3.3 voltage

Package

NCT6776F 128-pin QFP
NCT6776D 128-pin LQFP
Green

3. BLOCK DIAGRAM

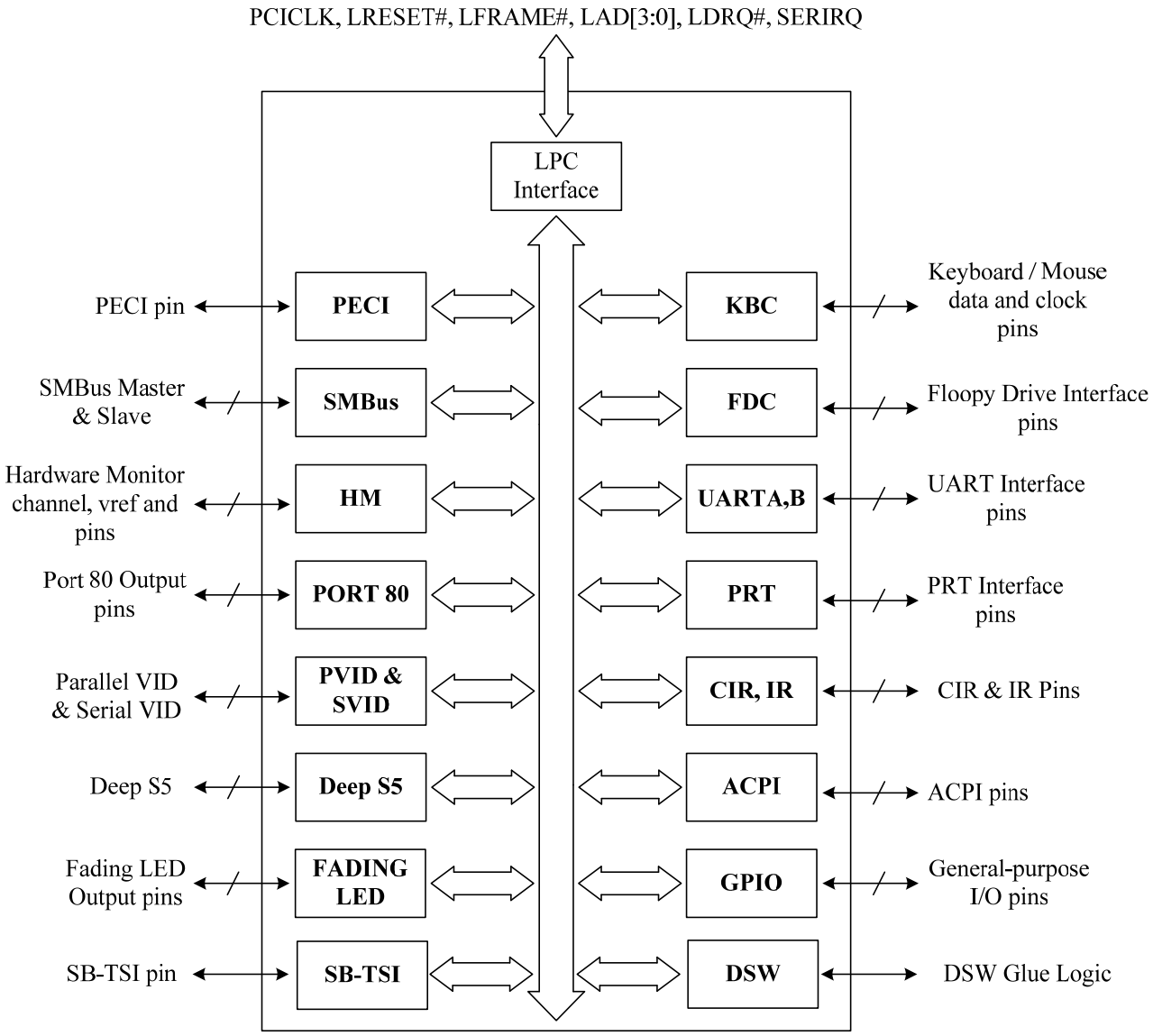


Figure 3-1 NCT6776F / NCT6776D Block Diagram

4. PIN LAYOUT

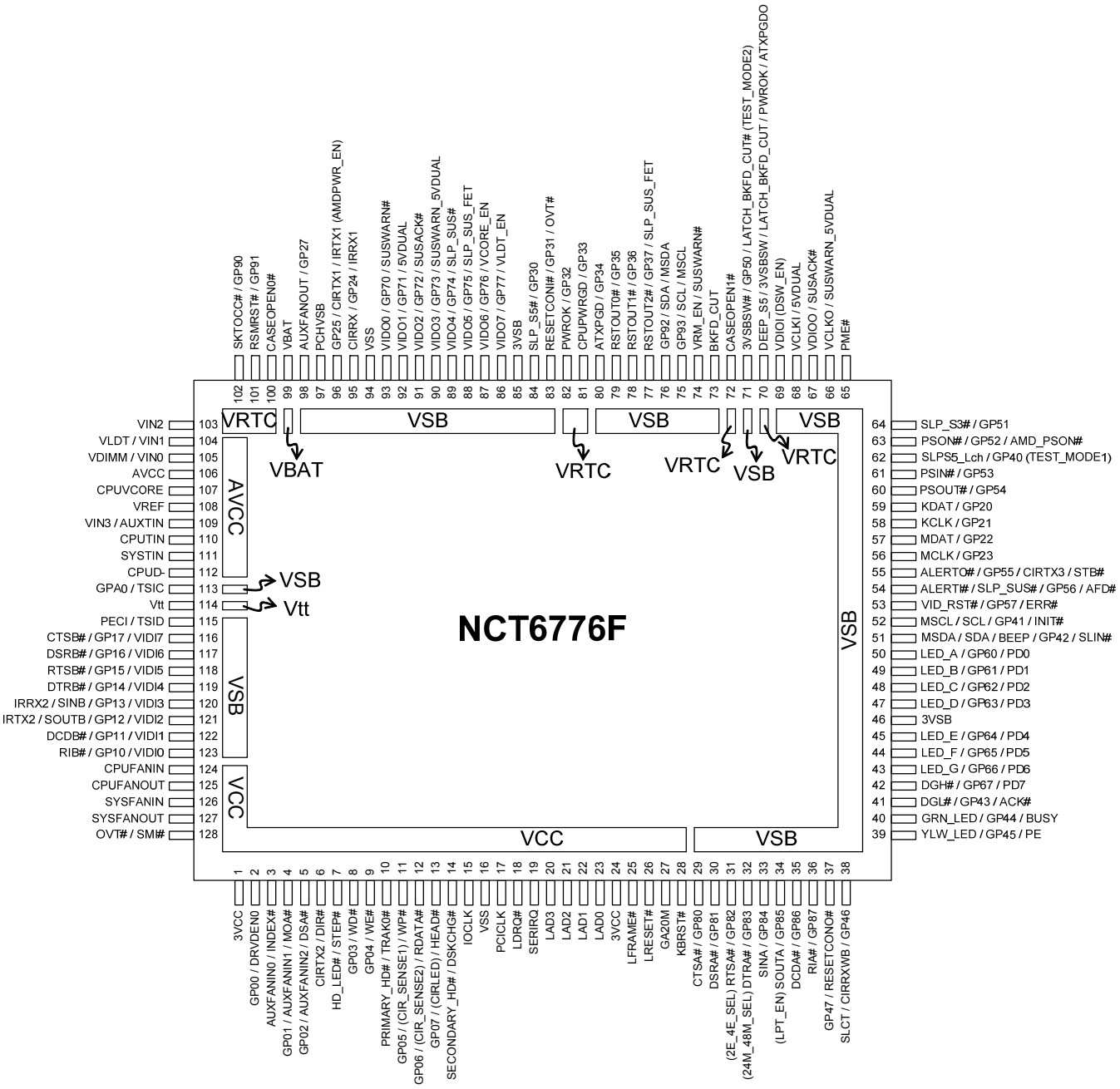


Figure 4-1 NCT6776F Pin Layout

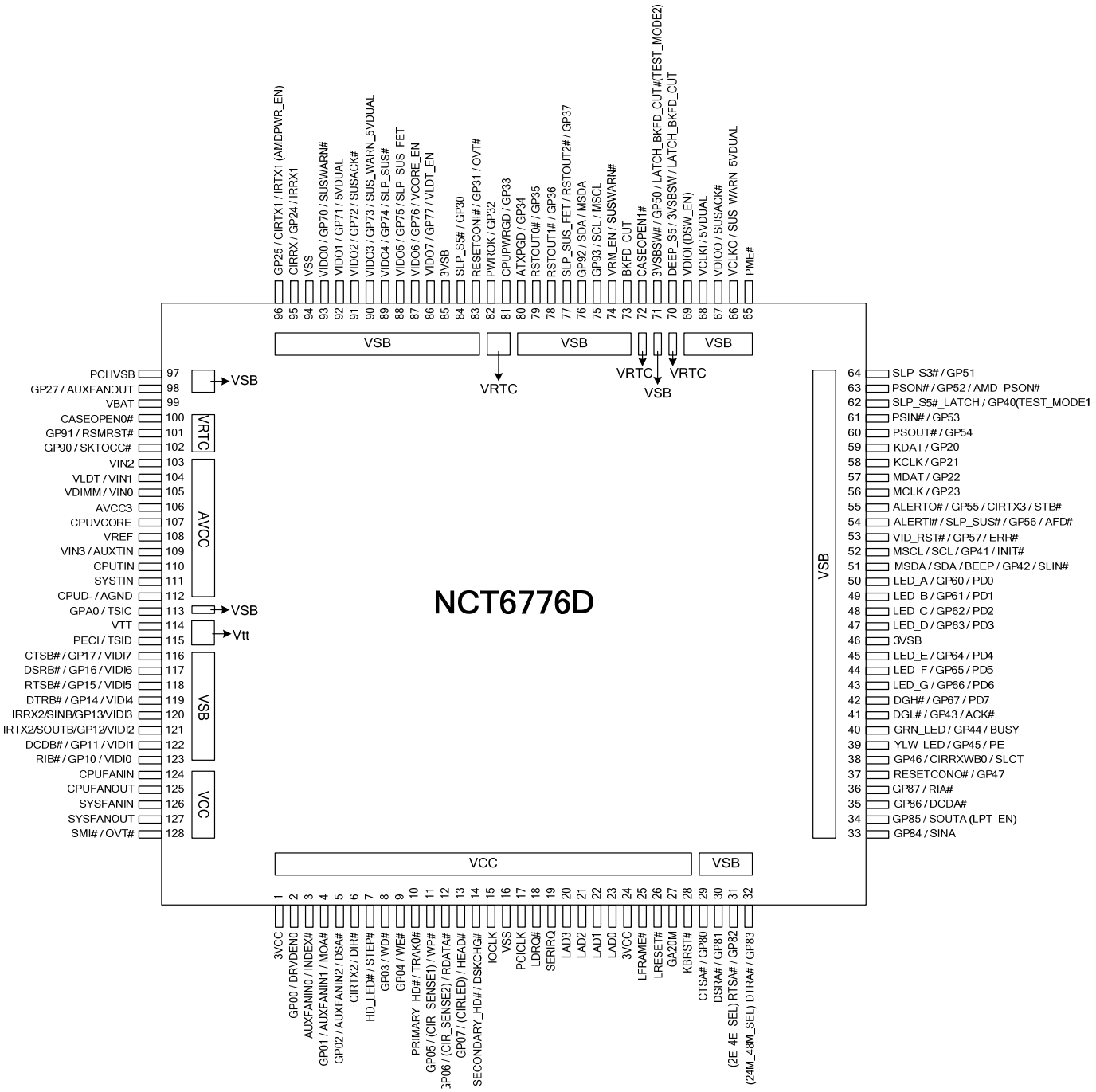


Figure 4-2 NCT6776D Pin Layout

5. PIN DESCRIPTION

Note: Please refer to 25.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{tp3} - 3.3V TTL-level input pin
IN_{tsp3} - 3.3V TTL-level, Schmitt-trigger input pin
IN_{gp5} - 5V GTL-level input pin
IN_{tp5} - 5V TTL-level input pin
IN_{tscup5} - 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN_{tsp5} - 5V TTL-level, Schmitt-trigger input pin
IN_{tdp5} - 5V TTL-level input pin with internal pull-down resistor
O_8 - output pin with 8-mA source-sink capability
OD_8 - open-drain output pin with 8-mA sink capability
O_{12} - output pin with 12-mA source-sink capability
OD_{12} - open-drain output pin with 12-mA sink capability
O_{24} - output pin with 24-mA source-sink capability
OD_{24} - open-drain output pin with 24-mA sink capability
O_{48} - output pin with 48-mA source-sink capability
OD_{48} - open-drain output pin with 48-mA sink capability
I/O_{v3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4} - Bi-direction pin with source capability of 6 mA
O_{12cu} - output pin 12-mA source-sink capability with controllable pull-up
OD_{12cu} - open-drain 12-mA sink capability output pin with controllable pull-up

5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
15	IOCLK	I	IN_{tp5}	VCC	System clock input, either 24MHz or 48MHz. The actual frequency must be specified by 24M_48M_SEL strapping.
65	PME#	O	OD_{12}	VSB	Generated PME event.
17	PCICLK	I	IN_{tp3}	VCC	PCI-clock 33-MHz input.
18	LDRQ#	O	O_{12}	VCC	Encoded DMA Request signal.
19	SERIRQ	I/O	IN_{tp3} O_{12} OD_{12}	VCC	Serialized IRQ input / output.
20-23	LAD[3:0]	I/O	IN_{tp3} OD_{12}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
25	LFRAME#	I	IN_{tp3}	VCC	Indicates the start of a new cycle or the termination of a broken cycle.
26	LRESET#	I	IN_{tp3}	VCC	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 FDC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
2	DRVDEN0	O	OD_{24}	VCC	Drive Density Select bit 0.
3	INDEX#	I	IN_{tscup5}	VCC	This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the beginning of a track marked by an index hole. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
4	MOA#	O	OD_{24}	VCC	Motor A On. When set to 0, this pin activates disk drive A. This is an open-drain output.
5	DSA#	O	OD_{24}	VCC	Drive Select A. When set to 0, this pin activates disk drive A. This is an open-drain output.
6	DIR#	O	OD_{24}	VCC	Direction of the head step motor. An open-drain output. Logic 1 = outward motion Logic 0 = inward motion
7	STEP#	O	OD_{24}	VCC	Step output pulses. This active-low open-drain output produces a pulse to move the head to another track.
8	WD#	O	OD_{24}	VCC	Write data. This logic-low open-drain writes pre-compensation serial data to the selected FDD. An open-drain output.
9	WE#	O	OD_{24}	VCC	Write enable. An open-drain output.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
10	TRAK0#	I	IN_{tscup5}	VCC	Track 0. This Schmitt-trigger input from the disk drive is active-low when the head is positioned over the outermost track. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
11	WP#	I	IN_{tscup5}	VCC	Write protected. This active-low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
12	RDATA#	I	IN_{tscup5}	VCC	The read-data input signal from the FDD. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.
13	HEAD#	O	OD_{24}	VCC	Head selection. This open-rain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
14	DSKCHG#	I	IN_{tscup5}	VCC	Diskette change. This signal is active-low at power-on and whenever the diskette is removed. This input pin needs to connect a pulled-up 1-KΩ resistor to 5V for Floppy Drive compatibility.

5.3 Multi-Mode Parallel Port

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
38	SLCT	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
39	PE	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
40	BUSY	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
41	ACK#	I	IN_{tsp5}	VSB	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.
53	ERR#	I	IN_{tsp5}	VSB	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
51	SLIN#	O	O_{12}	VSB	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
52	INIT#	O	O_{12}	VSB	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
54	AFD#	O	O_{12}	VSB	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
55	STB#	O	O_{12}	VSB	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
50	PD0	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
49	PD1	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
48	PD2	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
47	PD3	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
45	PD4	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
44	PD5	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
43	PD6	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
42	PD7	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

5.4 Serial Port Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
36	RIA#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
35	DCDA#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
34	SOUTA	O	O_{12}	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
33	SINA	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
32	DTRA#	O	O_{12}	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
31	RTSA#	O	O_{12}	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
30	DSRA#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
29	CTSA#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
123	RIB#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
122	DCDB#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
121	SOUTB	O	O_{12}	VSB	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
120	SINB	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
119	DTRB#	O	O_{12}	VSB	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
118	RTSB#	O	O_{12}	VSB	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
117	DSRB#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
116	CTSB#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.

5.5 KBC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
27	GA20M	O	O_{12}	VCC	Gate A20 output. This pin is high after system reset. (KBC P21)
28	KBRST#	O	O_{12}	VCC	Keyboard reset. This pin is high after system reset. (KBC P20)
58	KCLK	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Clock.
59	KDAT	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Data.
56	MCLK	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Clock.
57	MDAT	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Data.

5.6 CIR Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
95	CIRRX	I	IN_{tsp5}	VSB	CIR input for long length
96	CIRTX1	O	O_{12}	VSB	CIR transmission output
6	CIRTX2	O	O_{24}	VCC	CIR transmission output
55	CIRTX3	O	O_{12}	VSB	CIR transmission output
38	CIRRXWB	I	IN_{tsp5}	VSB	CIR input for wide band.
11	CIR_SENSE1	I	IN_{tsp5}	VCC	It could be CIR function by Nuvoton CIR driver.
12	CIR_SENSE2	I	IN_{tsp5}	VCC	It could be CIR function by Nuvoton CIR driver.
13	CIRLED	O	OD_{24}	VCC	It could be CIR function by Nuvoton CIR driver.

5.7 Hardware Monitor Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
102	SKTOCC#	I	IN_{tp5}	VRTC	CPU socket occupied detection
100	CASEOPEN0#	I	IN_{tp5}	VRTC	CASE OPEN 0 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
72	CASEOPEN1#	I	IN_{tp5}	VRTC	CASE OPEN 1 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
103	VIN2	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
104	VIN1	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
105	VIN0	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
107	CPUVCORE	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048 V)
108	VREF	O	AOUT	AVCC	Reference Voltage (around 2.048 V).
109	VIN3 / AUXTIN	I	AIN	AVCC	Analog input for voltage measurement (Range: 0 to 2.048V)
110	CPUTIN	I	AIN	AVCC	The input of temperature sensor 2. It is used for CPU temperature sensing.
111	SYSTIN	I	AIN	AVCC	The input of temperature sensor 1. It is used for system temperature sensing.
128	OVT#	O	OD_{12}	VCC	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#	O	OD_{12}	VCC	System Management Interrupt channel output.
83	OVT#	O	OD_{12}	VSB	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
3	AUXFANIN0	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
4	AUXFANIN1	I	IN_{tp5}	VCC	0 to +5 V amplitude fan tachometer input.
5	AUXFANIN2	I	IN_{tp5}	VCC	0 to +5 V amplitude fan tachometer input.
98	AUXFANOUT	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
124	CPUFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
125	CPUFANOUT	O	O_{12} OD_{12}	VCC	PWM duty-cycle signal for fan speed control.
126	SYSFANIN	I	IN_{tsp5}	VCC	0 to +5 V amplitude fan tachometer input.
127	SYSFANOUT	O	O_{12} OD_{12} AOUT	VCC	PWM duty-cycle signal for fan speed control. DC voltage output for fan speed control.
51	BEEP	O	OD_{12}	VSB	Beep function for hardware monitor.

5.8 VID Input/Output

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
116 117 118 119 120 121 122 123	VIDI7 VIDI6 VIDI5 VIDI4 VIDI3 VIDI2 VIDI1 VIDI0	I	IN_{gp5}	VSB	VID input detection, also with output control.
86 87 88 89 90 91 92 93	VIDO7 VIDO6 VIDO5 VIDO4 VIDO3 VIDO2 VIDO1 VIDO0	O	OD_{12}	VSB	VID Output. These pins could be connected to VCORE voltage regulator's VID input pins.
53	VID_RST#	I	IN_{gp5}	VSB	VID external reset.

5.9 Intel® PECI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
115	PECI	I/O	I/O_{V3}	Vtt	INTEL® CPU PECI interface. Connect to CPU.
114	Vtt	I	Power	Vtt	INTEL® CPU Vtt Power.

5.10 Advanced Configuration & Power Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
61	PSIN#	I	IN_{tp5}	VSB	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
60	PSOUT#	O	OD_{12}	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
101	RSMRST#	O	OD_{12}	VRTC	Resume reset signal output.
64	SLP_S3#	I	IN_{tp5}	VSB	SLP_S3# input.
84	SLP_S5#	I	IN_{tp5}	VSB	SLP_S5# input.
80	ATXPGD	I	IN_{tp5}	VSB	ATX power good signal.
63	PSON#	O	OD_{12}	VSB	Power supply on-off output.
82	PWROK	O	O_{12} OD_{12}	VRTC	3VCC PWROK signal.
81	CPUPWRGD	O	O_{12} OD_{12}	VRTC	3VCC PWROK signal.
83	RESETCONI#	I	IN_{tp5}	VSB	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
37	RESETCONO#	O	OD_{12}	VSB	RESETCON output.
70	3VSBSW	O	OD_{12}	VRTC	Switch 3VSB power to memory when in S3 state.
71	3VSBSW#	O	O_{24}	VSB	Switch 3VSB power to memory when in S3 state.
79	RSTOUT0#	O	OD_{24}	VSB	PCI Reset Buffer 0. (from pin26)
78	RSTOUT1#	O	O_{24} OD_{24}	VSB	PCI Reset Buffer 1. (from pin26) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit6.
77	RSTOUT2#	O	O_{24} OD_{24}	VSB	PCI Reset Buffer 2. (from pin26) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit7.

5.11 Advanced Sleep State Control Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
62	SLP_S5#_LATCH	O	O_{12}	VSB	This pin has the same signal output as SLP_S5#, but keeps the output signal high while in deep S3
70	DEEP_S5	O	OD_{12}	VSB	This pin is to control system power for entering “more power saving mode”.

5.12 Port 80 Message Display & LED Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
42	DGH#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
41	DGL#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
50 49 48 47 45 44 43	LED_A LED_B LED_C LED_D LED_E LED_F LED_G	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
39	YLW_LED	O	O_{12}	VSB	Yellow LED output control. This pin could indicate the power status.
40	GRN_LED	O	O_{12}	VSB	Green LED output control. This pin could indicate the power status.

5.13 SMBus Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
75	SCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave clock.
76	SDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave bi-directional Data.
52	SCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave clock.
51	SDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus slave bi-directional Data.
75	MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master clock. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
76	MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master bi-directional Data. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
52	MSCL	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master clock. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.
51	MSDA	I/O	IN_{tsp5} OD_{12}	VSB	SMBus master bi-directional Data. The SMBus master function could be performed through either pin#51, pin#52 or pin#75, pin#76.

5.14 Hard Disk Message Display & LED Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
7	HD_LED#	O	O_{24}	VCC	Hard disk operation message output for LED.
10	PRIMARY_HD#	I	IN_{tsp5}	VCC	LED control. The primary HD control the LED.
14	SECONDARY_HD#	I	IN_{tsp5}	VCC	LED control. The secondary HD control the LED.

5.15 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
46, 85	3VSB	I		3VSB	+3.3 V stand-by power supply for the digital circuits.
99	VBAT	I		VBAT	+3 V on-board battery for the digital circuits.
1,24	VCC	I		VCC	+3.3 V power supply for driving 3 V on host interface.
106	AVCC	I		AVCC3	Analog +3.3 V power input. Internally supply power to all analog circuits.
112	CPUD- / AGND	I		CPUD- / AGND	Analog ground. The ground reference for all analog input. Internally connected to all analog circuits. This pin should be connected to ground.
16, 94	VSS	I		VSS	Ground.
114	VTT	I		VTT	INTEL® CPU Vtt power.

5.16 AMD Power-On Sequence

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
107	CPUVCORE	I	AIN	AVCC	Power sequence group B signal
104	VLDT	I	AIN	AVCC	Power sequence group C signal
105	VDIMM	I	AIN	AVCC	Memory power enable
87	VCORE_EN	O	OD_{12}	VSB	CPU Vcore power enable
86	VLDT_EN	O	OD_{12}	VSB	Hyper transport I/O power enable
81	CPUPWRGD	O	OD_{12}	VSB	AMD power on sequence ok signal
63	AMD_PSON#	O	OD_{12}	VSB	Power supply on/off output to enable ATX

5.17 Intel Serial VID

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
68	VCLKI	I	IN_{gp5}	VSB	Intel Serial VID input clock signal from CPU
69	VDIOI	I	IN_{gp5}	VSB	Intel Serial VID input data signal from CPU

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
54	ALERTI#	I	IN_{gp5}	VSB	Intel Serial VID input alert signal from Regulator
66	VCLKO	O	OD_{12}	VSB	Intel Serial VID output clock signal to Regulator
67	VDIOO	O	OD_{12}	VSB	Intel Serial VID output data signal to Regulator
55	ALERTO#	O	OD_{12}	VSB	Intel Serial VID output alert signal to CPU

5.18 AMD Serial VID

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
74	VRM_EN	I	IN_{tp5}	VSB	Active high signal generated by system to enable Regulator
68	VCLKI	I	IN_{gp5}	VSB	AMD Serial VID input clock signal from CPU
69	VDIOI	I	IN_{gp5}	VSB	AMD Serial VID input data signal from CPU
66	VCLKO	O	OD_{12}	VSB	AMD Serial VID output clock signal to Regulator
67	VDIOO	O	OD_{12}	VSB	AMD Serial VID output data signal to Regulator

5.19 AMD SB-TSI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
113	TSIC	O	OD_{12}	VCC	AMD SB-TSI clock output.
115	TSID	I/O	IN_{tsp3} OD_{12}	VCC	AMD SB-TSI data input / output.

5.20 Dual Voltage Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
73	BKFD_CUT	O	OD_{12}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S3 sleep state.
71	LATCH_BKFD_CUT#	O	O_{24}	VSB	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.
70	LATCH_BKFD_CUT	O	O_{12}	VRTC	Power distribution control (When switching between main and standby regulators) for system transition into and out of the S5 sleep state.

5.21 DSW

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
54	SLP_SUS#	I	IN_{tp5}	VSB	This pin connects to SLP_SUS# in CPT PCH

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
66	SUS_WARN_5 VDUAL	O	OD_{12}	VSB	This pin links to external 5VDUAL control circuits
67	SUSACK#	O	OD_{12}	VSB	This pin connects to SUSACK# in CPT PCH
68	5VDUAL	I	AIN	VSB	Analog input to monitor 5VDUAL voltage
74	SUSWARN#	I	IN_{tp5}	VSB	This pin connects to SUSWARN# in CPT PCH
77	SLP_SUS_FET	O	OD_{12}	VSB	This pin connects to VSB power switch
89	SLP_SUS#	I	IN_{tp5}	VSB	This pin connects to SLP_SUS# in CPT PCH
90	SUS_WARN_5 VDUAL	O	OD_{12}	VSB	This pin links to external 5VDUAL control circuits
91	SUSACK#	O	OD_{12}	VSB	This pin connects to SUSACK# in CPT PCH
92	5VDUAL	I	AIN	VSB	Analog input to monitor 5VDUAL voltage
93	SUSWARN#	I	IN_{tp5}	VSB	This pin connects to SUSWARN# in CPT PCH
88	SLP_SUS_FET	O	OD_{12}	VSB	This pin connects to VSB power switch
97	PCHVSB	I	AIN	VSB	PCHVSB function

5.22 IR

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
95	IRRX1	I	IN_{tsp5}	VSB	IR Receiver input.
96	IRTX1	O	O_{12}	VSB	IR Transmitter output.
120	IRRX2	I	IN_{tp5}	VSB	IR Receiver input.
121	IRTX2	O	O_{12}	VSB	IR Transmitter output.

5.23 General Purpose I/O Port

5.23.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
2	GP00	I/O	IN_{tp5} O_{24} OD_{24}	VCC	General-purpose I/O port 0 bit 0.
4	GP01	I/O	IN_{tp5} O_{24} OD_{24}	VCC	General-purpose I/O port 0 bit 1.
5	GP02	I/O	IN_{tp5} O_{24} OD_{24}	VCC	General-purpose I/O port 0 bit 2.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
8	GP03	I/O	IN_{tp5} O_{24} OD_{24}	VCC	General-purpose I/O port 0 bit 3.
9	GP04	I/O	IN_{tp5} O_{24} OD_{24}	VCC	General-purpose I/O port 0 bit 4.
11	GP05	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 5.
12	GP06	I/O	IN_{tsp5} O_{12} OD_{12}	VCC	General-purpose I/O port 0 bit 6.
13	GP07	I/O	IN_{tp5} O_{24} OD_{24}	VCC	General-purpose I/O port 0 bit 7.

5.23.2 GPIO-1 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
123	GP10	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 0.
122	GP11	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 1.
121	GP12	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 2.
120	GP13	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 3.
119	GP14	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 4.
118	GP15	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 5.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
117	GP16	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 6.
116	GP17	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 7.

5.23.3 GPIO-2 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
59	GP20	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 0.
58	GP21	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 1.
57	GP22	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 2.
56	GP23	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 3.
95	GP24	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 4.
96	GP25	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 5.
98	GP27	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 7.

5.23.4 GPIO-3 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
84	GP30	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 0.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
83	GP31	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 1.
82	GP32	I/O	IN_{tp5} O_{12} OD_{12}	VRTC	General-purpose I/O port 3 bit 2.
81	GP33	I/O	IN_{tp5} O_{12} OD_{12}	VRTC	General-purpose I/O port 3 bit 3.
80	GP34	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 4.
79	GP35	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 5.
78	GP36	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 6.
77	GP37	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 7.

5.23.5 GPIO-4 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
62	GP40	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 0.
52	GP41	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 1.
51	GP42	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 2.
41	GP43	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 4 bit 3.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
40	GP44	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 4.
39	GP45	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 5.
38	GP46	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 6.
37	GP47	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 7.

5.23.6 GPIO-5 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
71	GP50	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 5 bit 0.
64	GP51	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 1.
63	GP52	I/O	IN_{tp5} O_{8} OD_{8}	VSB	General-purpose I/O port 5 bit 2.
61	GP53	I/O	IN_{tp5} O_{8} OD_{8}	VSB	General-purpose I/O port 5 bit 3.
60	GP54	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 4.
55	GP55	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 5.
54	GP56	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 6.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
53	GP57	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 7.

5.23.7 GPIO-6 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
50	GP60	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 0.
49	GP61	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 1.
48	GP62	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 2.
47	GP63	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 3.
45	GP64	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 4.
44	GP65	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 5.
43	GP66	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 6.
42	GP67	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 6 bit 7.

5.23.8 GPIO-7 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
93	GP70	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 0.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
92	GP71	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 1.
91	GP72	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 2.
90	GP73	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 3.
89	GP74	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 4.
88	GP75	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 5.
87	GP76	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 6.
86	GP77	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 7.

5.23.9 GPIO-8 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
29	GP80	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 0.
30	GP81	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 1.
31	GP82	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 2.
32	GP83	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 3.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
33	GP84	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 4.
34	GP85	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 5.
35	GP86	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 6.
36	GP87	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 7.

5.23.10GPIO-9 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
102	GP90	I/O	IN_{tp5} O_{12} OD_{12}	VRTC	General-purpose I/O port 9 bit 0.
101	GP91	I/O	IN_{tp5} O_{12} OD_{12}	VRTC	General-purpose I/O port 9 bit 1.
76	GP92	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 2.
75	GP93	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 9 bit 3.

5.23.11GPIO-A Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
113	GPA0	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port A bit 0.

5.24 Strapping Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	2E_4E_SEL	I	IN_{tdp5}	VSB	SIO I/O address selection. (Strapped by LRESET#) Strapped to high: SIO I/O address is 4Eh/4Fh. Strapped to low: SIO I/O address is 2Eh/2Fh.
32	24M_48M_SEL	I	IN_{tdp5}	VSB	Input clock rate selection (Strapped by **VCC**: internal Power OK signal without any delay.) Strapped to high: The clock input on pin 15 is 48MHz. Strapped to low: The clock input on pin 15 is 24MHz.
34	LPT_EN	I	IN_{tdp5}	VSB	PRT function selection. (Strapped by **VCC**: internal Power OK signal without any delay.) Strapped to high: PRT function. Strapped to low: non-PRT function
62	TEST_MODE1	I	IN_{tdp5}	VSB	Test Mode1. (Strapped by **VSB** power: internal RSMRST# signal.) Please strap this pin to low
69	DSW_EN	I	IN_{tp5}	VSB	DSW position selection. (Strapped by **VSB** power: internal RSMRST# signal]) Strapped to high: Pin 54, 66~68, 74, 77 Strapped to low: Pin 88~93
71	TEST_MODE2	I	IN_{tdp5}	VSB	Test Mode2. (Strapped by **VSB** power: internal RSMRST# signal.) Please strap this pin to low
96	AMDPWR_EN	I	IN_{tdp5}	VSB	Enable AMD power sequence function. (Strapped by **VSB** power: internal RSMRST# signal.) Strapped to high: Enable AMD power sequence Strapped to low: Disable AMD power sequence

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
2) VCC Strapping result can be programming by LPC, and reset by PWROK.
3) LRESET# strapping (2E_4E_SEL) can be programming by LPC, and reset by LRESET#.

5.25 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
FDC					
FDC internal pull-up resistors could be controlled by Logic Device 0, CRF0 bit7. (=1, has pull-up (default); =0, no pull-up)					
INDEX#	3	3VCC	Pull-up	1.006K	1
TRAK0#	10	3VCC	Pull-up	1.006K	1
WP#	11	3VCC	Pull-up	1.006K	1
RDATA#	12	3VCC	Pull-up	1.006K	1
DSKCHG#	14	3VCC	Pull-up	1.006K	1
Strapping Pins					
2E_4E_SEL	31	3VSB	Pull-down	47.4K	2
24M_48M_SEL	32	3VSB	Pull-down	47.4K	2
LPT_EN	34	3VSB	Pull-down	47.4K	2
TEST_MODE1	62	3VSB	Pull-down	47.4K	3
TEST_MODE2	71	3VSB	Pull-down	47.4K	3
AMDPWR_EN	96	3VSB	Pull-down	47.4K	3
Advanced Configuration & Power Interface					
PSIN#	61	3VSB	Pull-up	47.03K	

Note1. FDC internal pull-up resistors could be controlled by Logic Device 0, CRF0 bit7. (=1, has pull-up; =0, no pull-up (default))

Note2. Active only during VCC Power-up reset

Note3. Active only during VSB Power-up reset

6. GLUE LOGIC

6.1 ACPI Glue Logic

Table 6-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SLP_S5#	84	SLP_S5# input.
RESETCONI#	83	RESETCON# input signal. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
RESETCONO#	37	RESETCON# output signal.
PWROK	82	This pin generates the PWROK signals while 3VCC is present.
ATXPGD	80	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWRGD generation. The default is enabled.
RSMRST#	101	The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge. When the NCT6776F / NCT6776D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

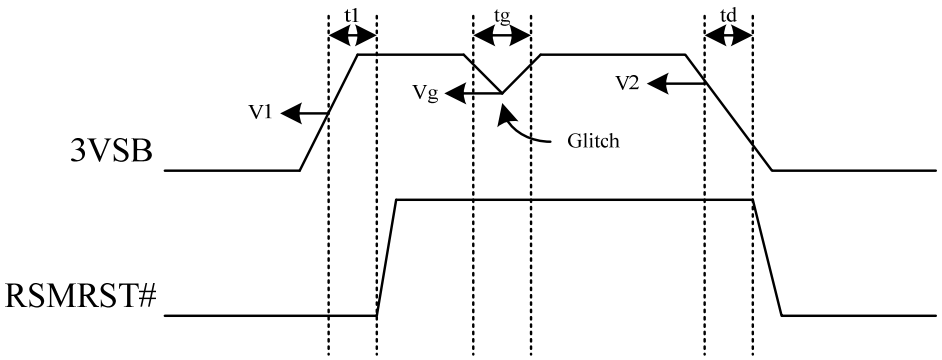


Figure 6-1 RSMRST#

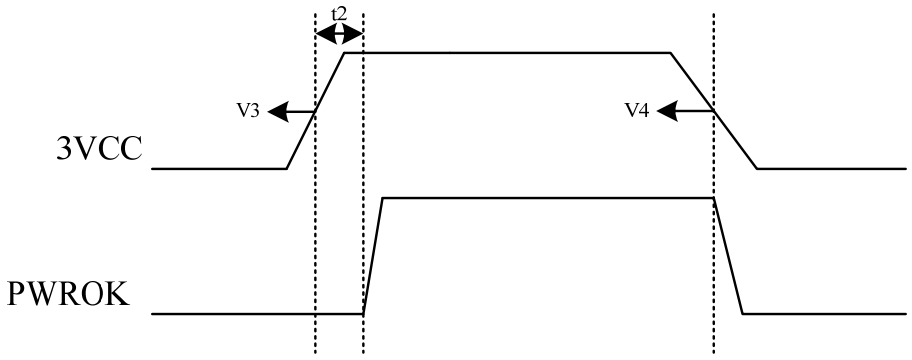


Figure 6-2 PWROK

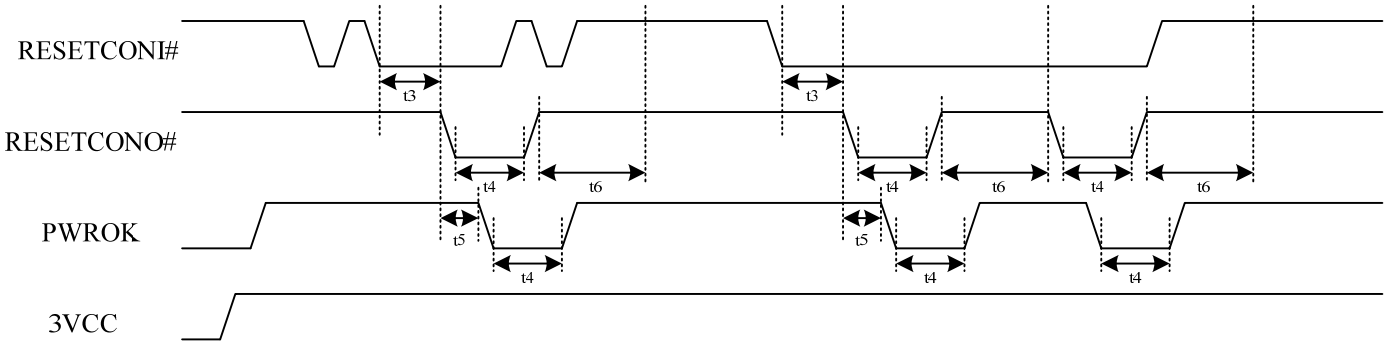


Figure 6-3 RESETCONI# and PWROK

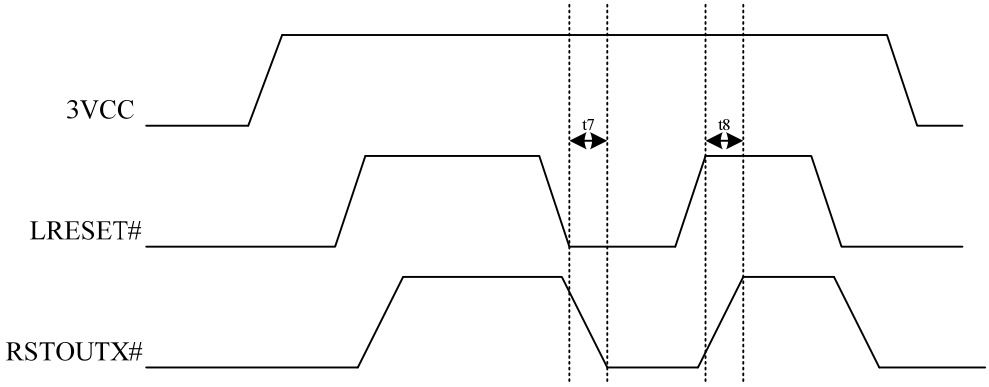


Figure 6-4 RSTOUTX# and LRESET#

TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	200	300	mS
tg	3VSB Glitch allowance		1	uS
td	Falling 3VSB supply Delay		1	uS
t2	Valid 3VCC to PWROK active	300	500	mS

TIMING	PARAMETER	MIN	MAX	UNIT
t3	RESETCONI# de-bounce	15	20	mS
t4	RESETCONO# and PWROK active	See LDB CRFA		
t5	RESETCONO# active to PWROK active	1	2	uS
t6	RESETCONO# inactive to RESETCONI# detect	2	3	S
t7	LRESET# active to RSTOUTx# active	0	80	nS
t8	LRESET# inactive to RSTOUTx# inactive	0	80	nS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage	-	3.033	Volt
V2	3VSB Ineffective Voltage	2.882	-	Volt
V3	3VCC Valid Voltage	-	2.83	Volt
V4	3VCC Ineffective Voltage	2.68	-	Volt
Vg	3VSB drops by Power noise	2	-	Volt

Note： 1. The values above are the worst-case results of R&D simulation.

6.2 BKFD_CUT & LATCH_BKFD_CUT

NCT6776F / NCT6776D supports BKFD_CUT & LATCH_BKFD_CUT functions, please refer the timing diagram below:

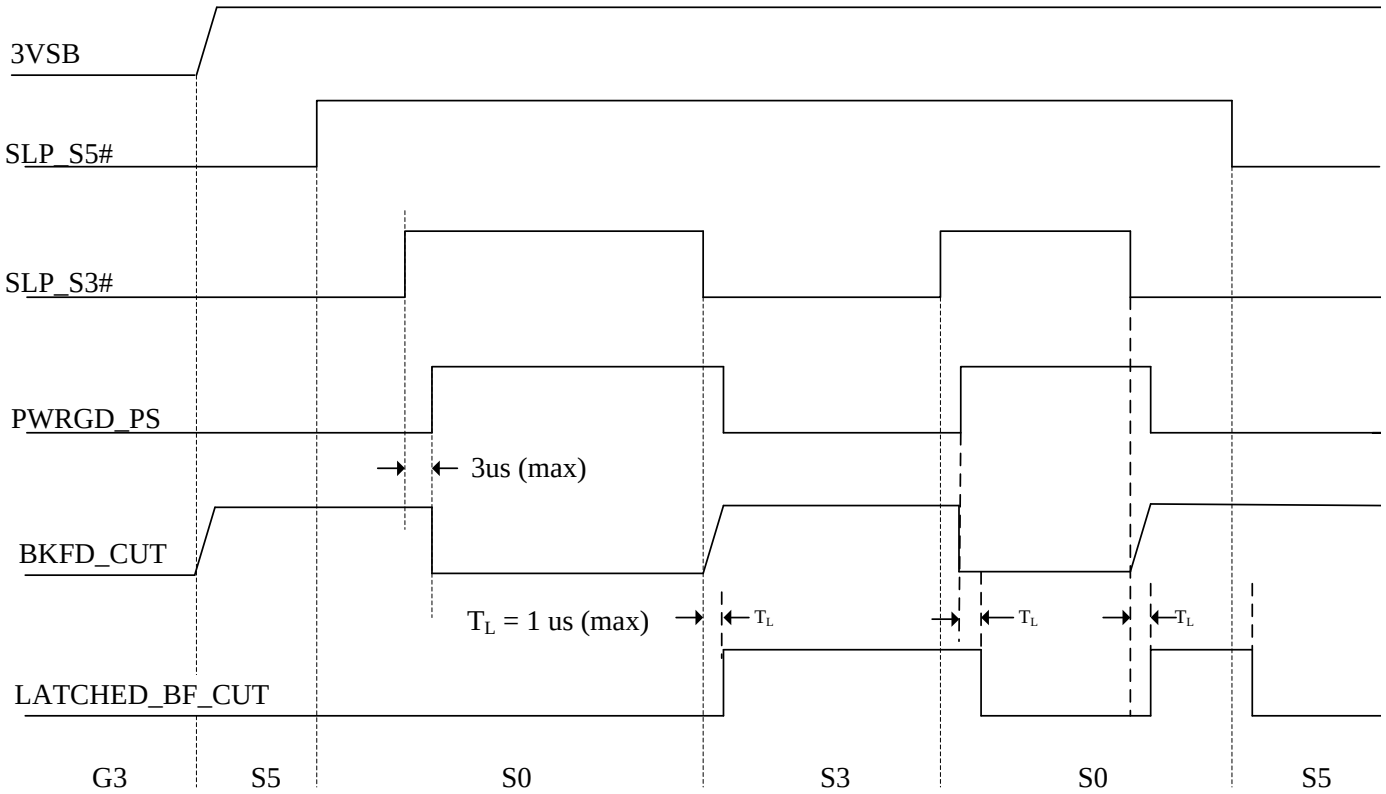


Figure 6-5 BKFD_CUT and LATCH_BKFD_CUT

BKFD_CUT (Backfeed_Cut) – When high, switches dual rails to standby power.

LATCH_BKFD_CUT (Latched_Backfeed_Cut) – When high, switches dual rails to standby power.

6.3 3VSBSW#

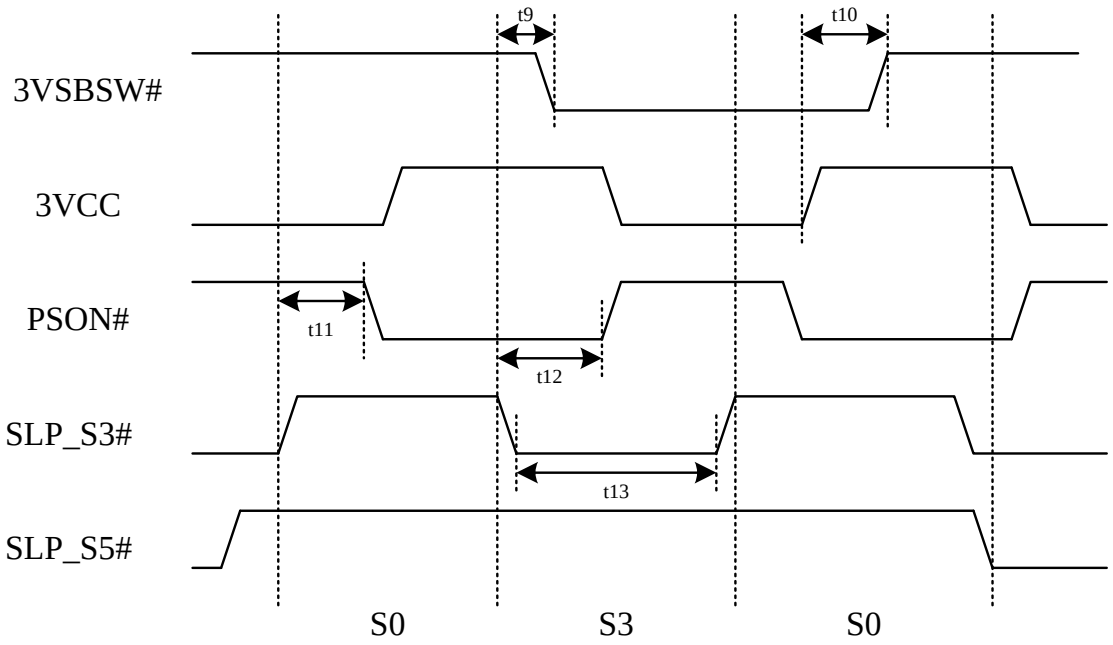


Figure 6-6 3VSBSW#

TIMING	PARAMETER	MIN	MAX	UNIT
t9	SLP_S3# active to 3VSBSW# active	0	30	mS
t10	3VCC active to 3VSBSW# inactive	90	142	mS
t11	SLP_S3# inactive to PSON# active	0	80	nS
t12	SLP_S3# active to PSON# inactive	15	45	mS
t13	SLP_S3# minimal Low Time	40	-	mS

6.4 PSON# Block Diagram

The PSON# function controls the main power on/off. The main power is turned on when PSON# is low. Please refer to the figure below.

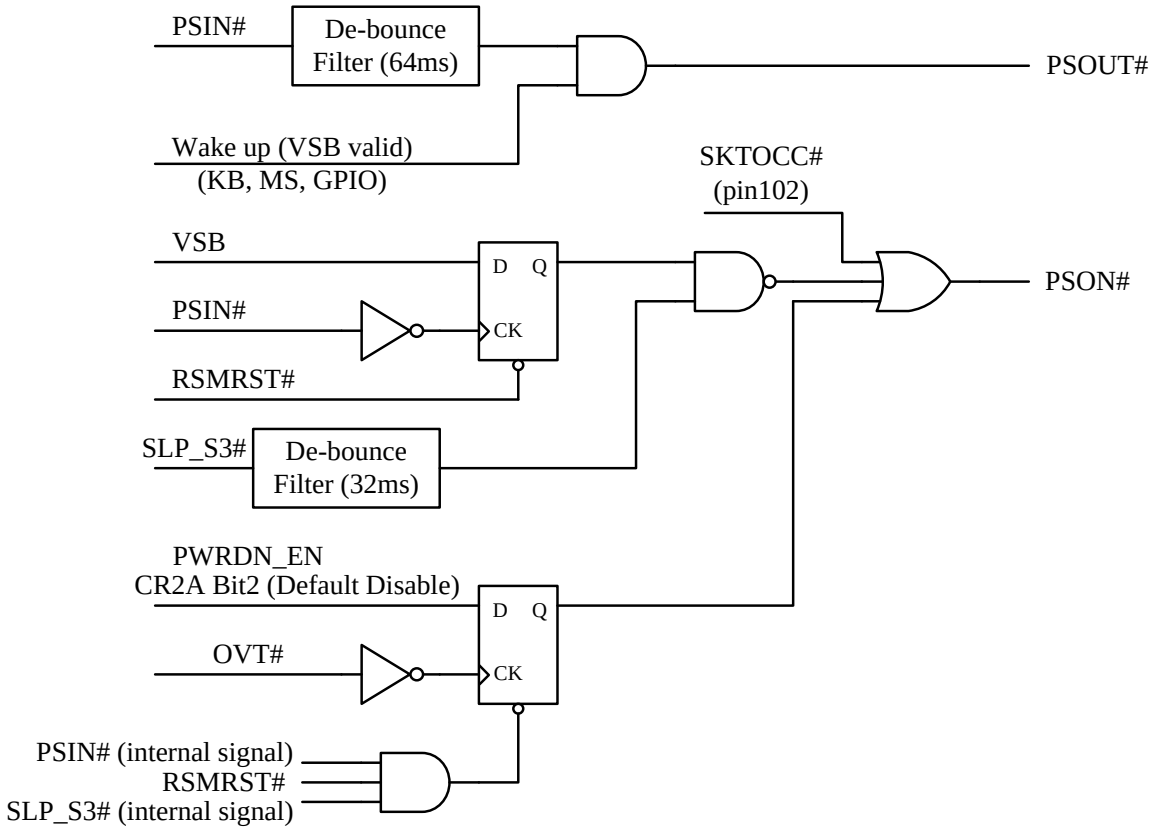


Figure 6-7 PSON# Block Diagram

6.5 PWROK

PWROK Signal indicates the main power (VCC Power) is valid. Besides, valid PWROK signal also requires the following conditions, as shown in the figure below.

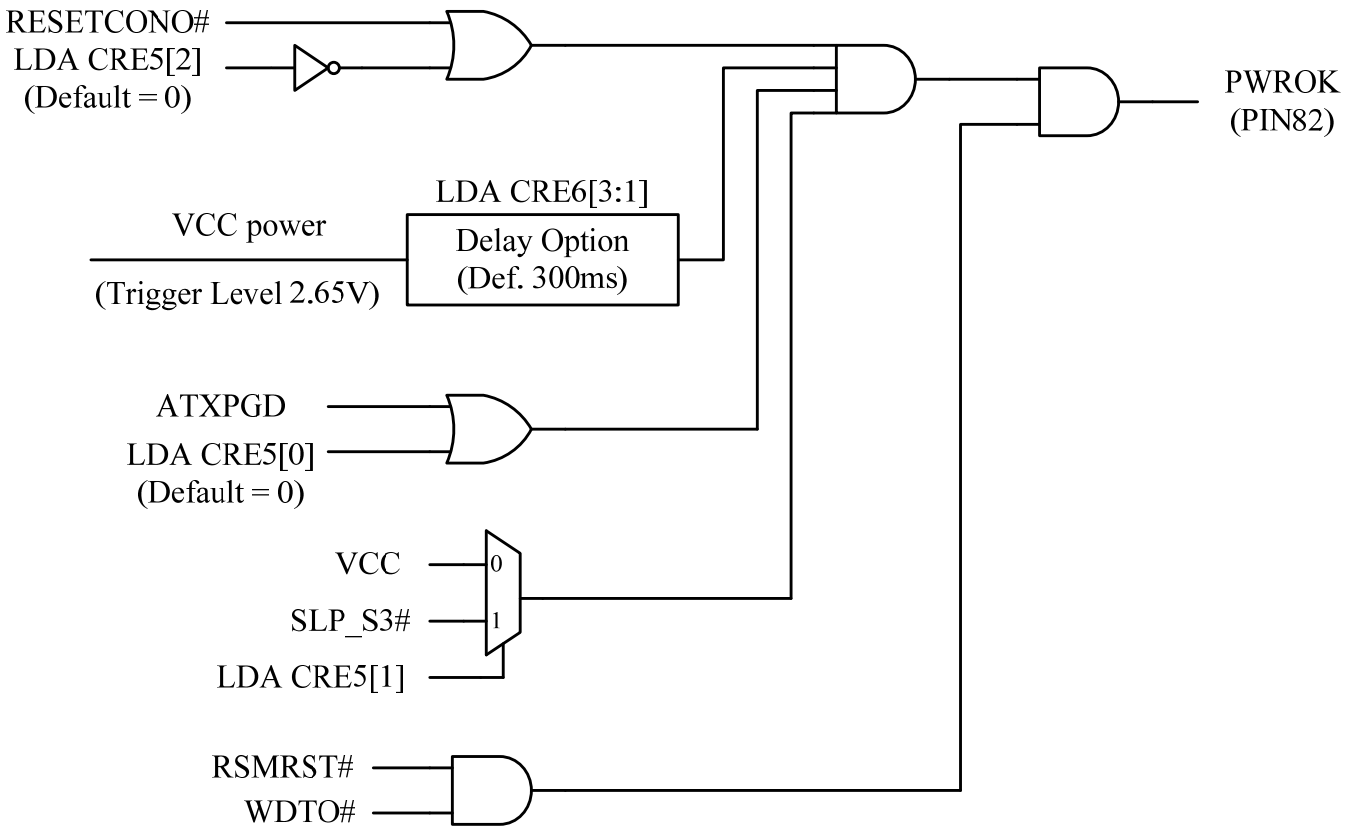


Figure 6-8 PWROK Block Diagram

6.6 Front Panel LEDs

NCT6776F / NCT6776D supports two LED control pins – GRN_LED and YLW_LED.

For dual-color LED application:

(1)GRN_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the green LED and the anode of the yellow LED.

(2)YLW_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the yellow LED and the anode of the green LED.

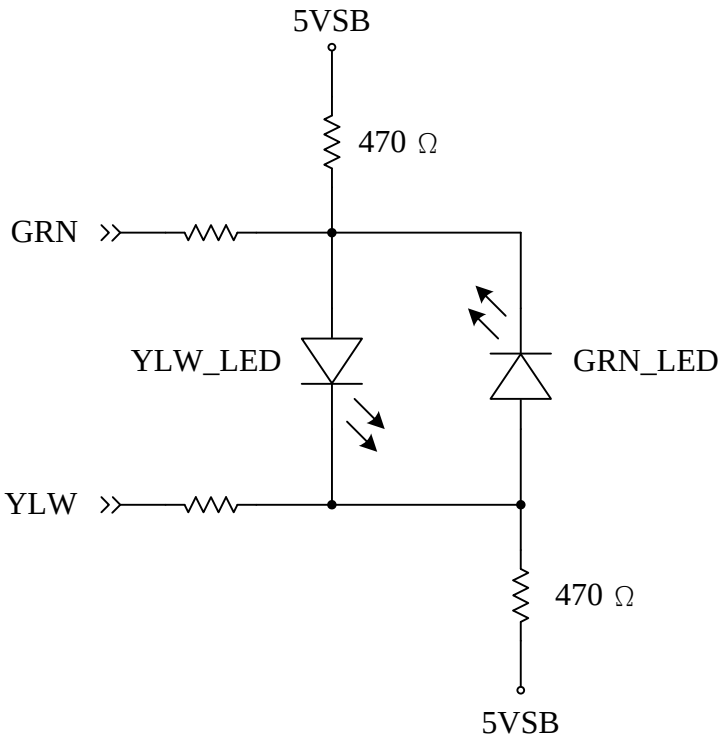


Figure 6-9 Illustration of Dual Color LED application

GRN_LED and YLW_LED pins are designed to show currently power states. There are Manual Mode and Automatic Mode:

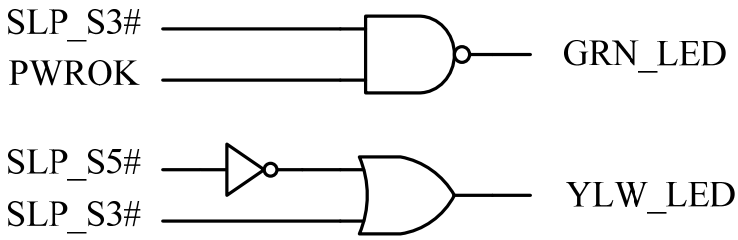
6.6.1 Automatic Mode

Power state is S0 or S1: GRN_LED will be asserted by default.

Power state is S3: YLW_LED will be asserted by default.

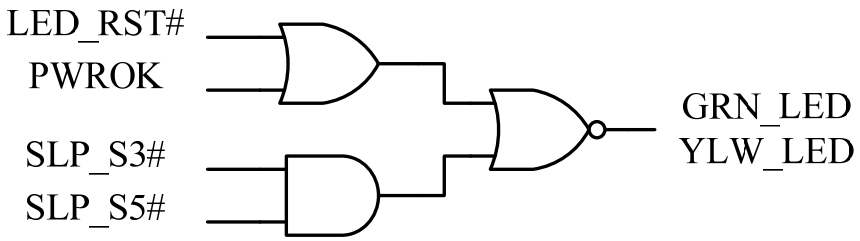
Power state is S4 or S5: Both GRN_LED and YLW_LED will be de-asserted by default.

AUTO_EN	GRN_LED_RST (YLW_LED_RST)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
1	X	S0,S1	1	1	GRN_BLK_FREQ	HIGH-Z
1	X	S3	0	1	HIGH-Z	YLW_BLK_FREQ
1	X	S4,S5	X	0	HIGH-Z	HIGH-Z



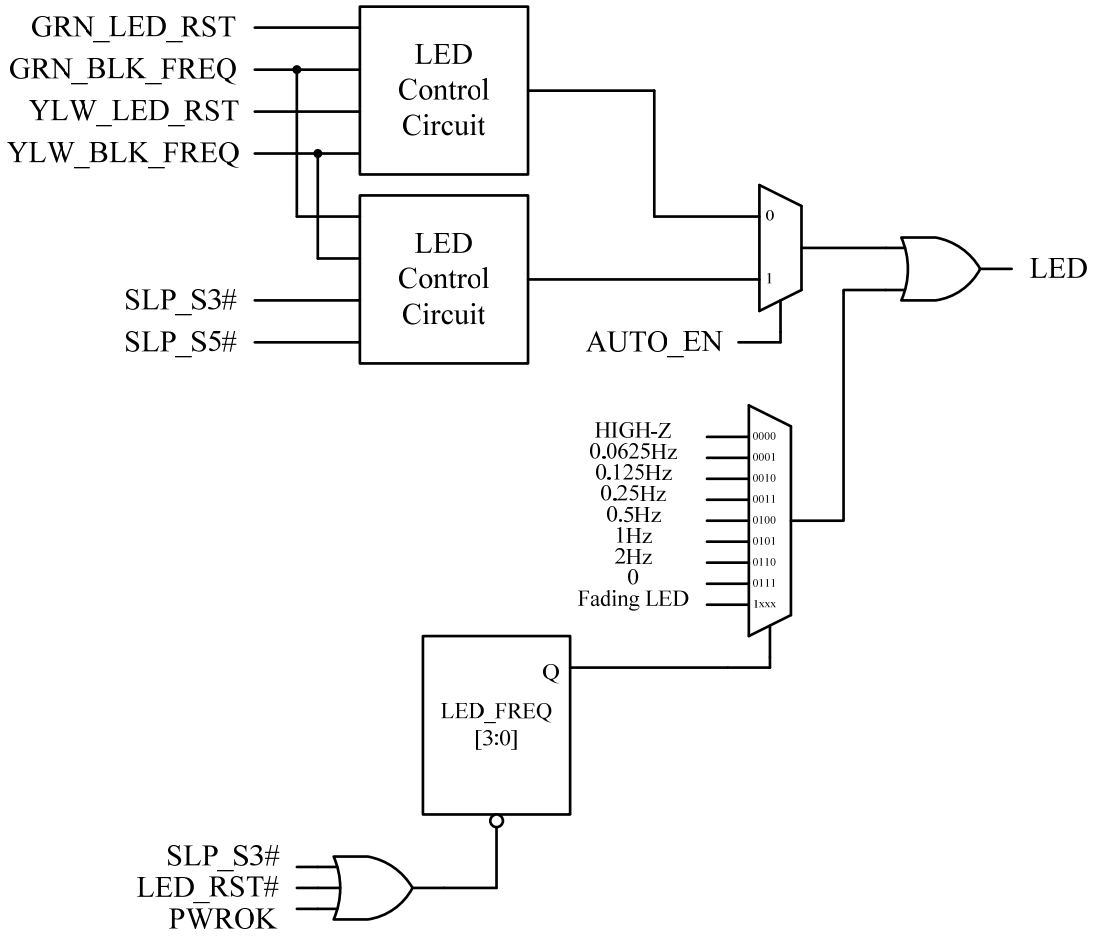
6.6.2 Manual Mode

AUTO_EN	GRN_LED_RST# (YLW_LED_RST)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
0	0	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	0	S3	0	1	HIGH-Z	HIGH-Z
0	0	S4,S5	X	0	HIGH-Z	HIGH-Z
0	1	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S3	0	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S4,S5	X	0	GRN_BLK_FREQ	YLW_BLK_FREQ



Register Neme	Register Location
AUTO_EN	Logic Device B, CRF7h, bit7
GRN_BLK_FREQ	Logic Device B, CRF7h, bit3~0
YLW_BLK_FREQ	Logic Device B, CRF8h, bit3~0
GRN_LED_RST#	Logic Device B, CRF7h, bit6
YLW_LED_RST#	Logic Device B, CRF8h, bit6

6.6.3 S0~S5 LED Blink Block Diagram



6.6.4 LED Pole (LED_POL)

Set to 0b, GRN_LED output is active low, as the following Figure(a)

Set to 1b, GRN_LED output is active high, as the following Figure(b)

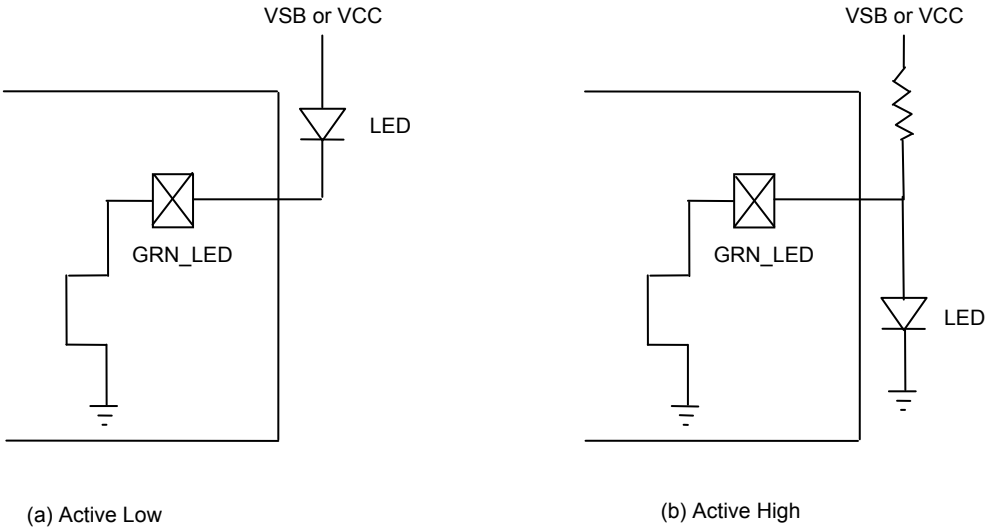


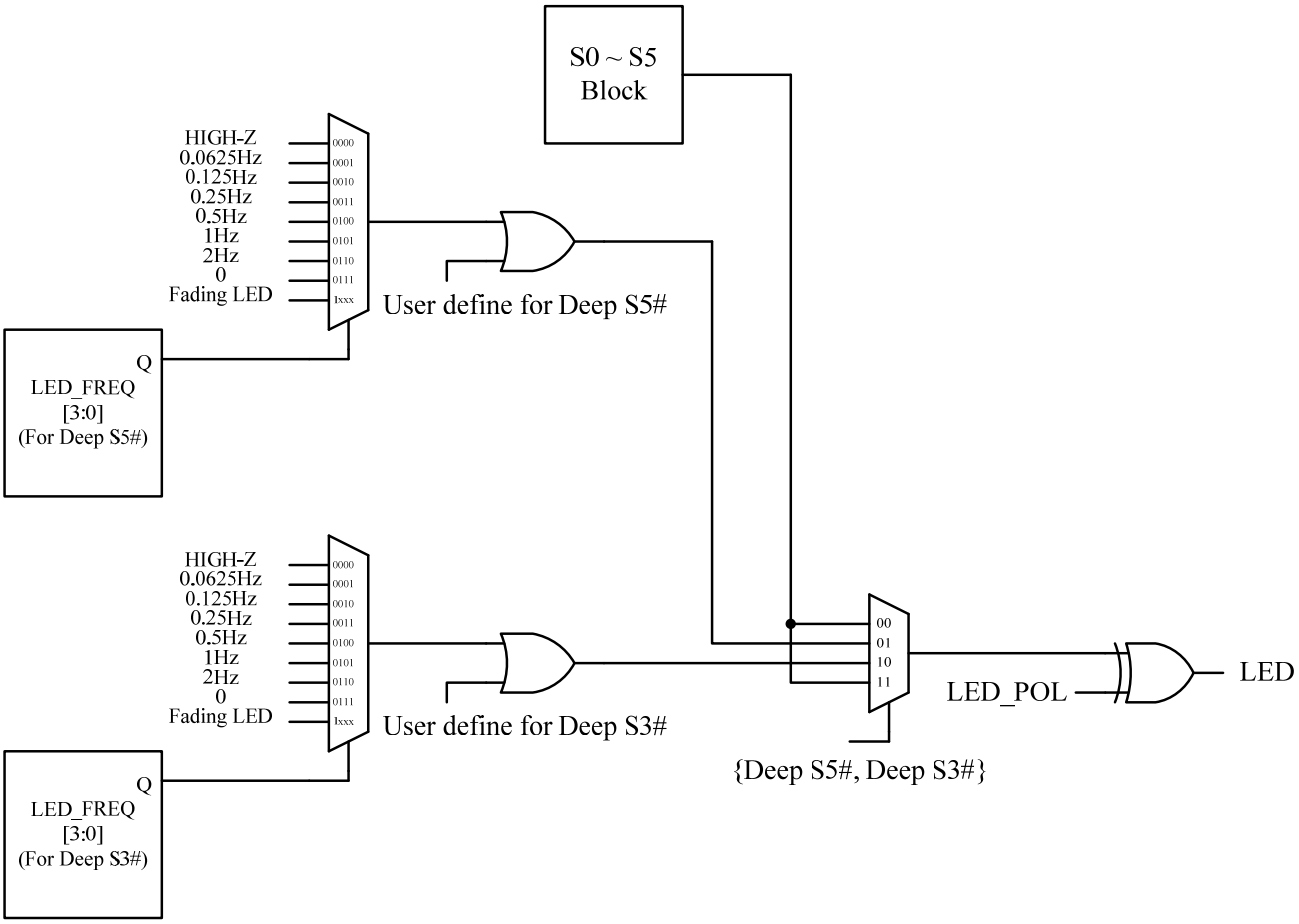
Figure 6-10 Illustration of LED polarity

6.6.5 Deeper Sleeping State Detect Function

These two LED pins could also be used to indicate if the system is in Deeper Sleeping State. For more detail, please refer to the section of Advanced Sleep State Control Function.

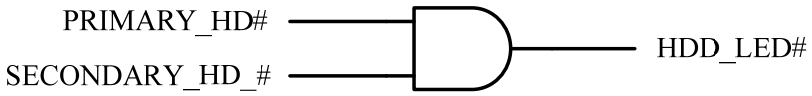
Enable_DEEP_S5	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S5	DeepS5_GRN_BLK_FREQ	DeepS5_YLW_BLK_FREQ
1	1	DEEP_S5	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior

Enable_DEEP_S3	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S3	DeepS3_GRN_BLK_FREQ	DeepS3_YLW_BLK_FREQ
1	1	DEEP_S3	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior


S0 ~ S5
Block
HIGH-Z
0.0625Hz
0.125Hz
0.25Hz
0.5Hz
1Hz
2Hz
0
Fading LED
0000
0001
0010
0011
0100
0101
0110
0111
1xxx
User define for Deep S5#
Q
LED_FREQ
[3:0]
(For Deep S5#)
HIGH-Z
0.0625Hz
0.125Hz
0.25Hz
0.5Hz
1Hz
2Hz
0
Fading LED
User define for Deep S3#
Q
LED_FREQ
[3:0]
(For Deep S3#)
00
01
10
11
LED_POL
LED
{Deep S5#, Deep S3#}

6.7 HDD LED

HDD LED is used for Hard Drive Disk, red LED indicator, and it will drive low when PRIMARY_HDD# = 0 or SECONDARY_HDD# = 0. Below shows the simplified diagram of the circuit that generates the HDD LED signal.



6.8 Advanced Sleep State Control (ASSC) Function

Advanced Sleep State Control (ASSC) Function is used to control the system power at S3 or S5 state. The purpose of this function is to provide a method to reduce power consumption at S3 or S5 state. This function is disabled by default. When VCC power is first supplied, BIOS can program the register to enable ASSC Function. The register is powered by 3VSB_IO and some is powered by VBAT. The related registers are located at Logic Device 16 CRE0h ~ CRE3h.

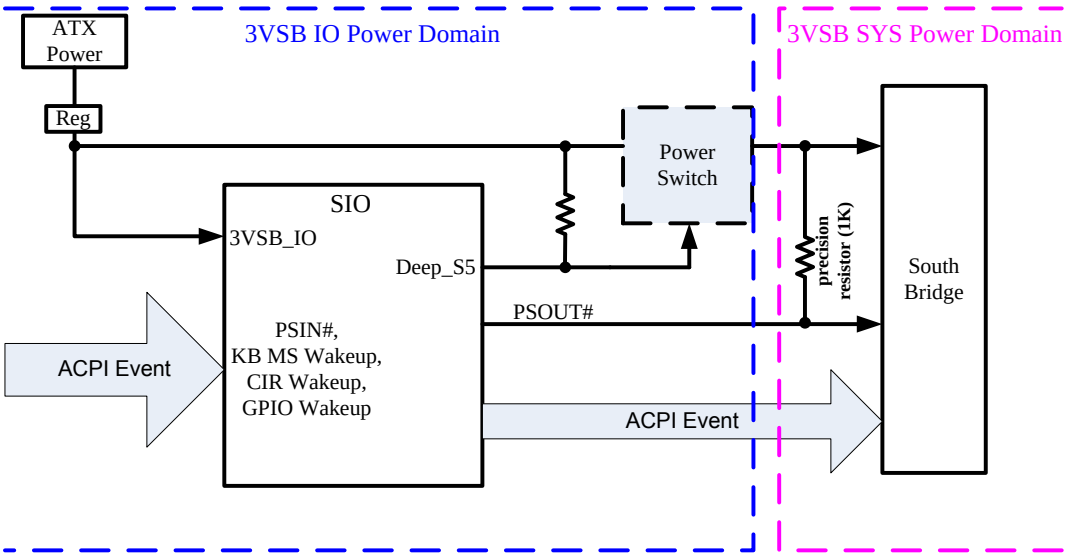
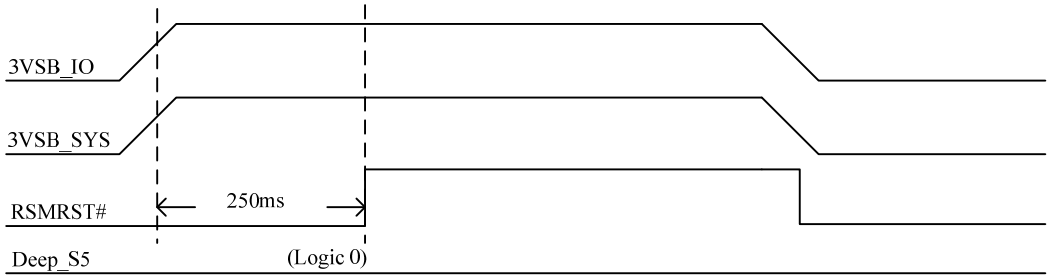


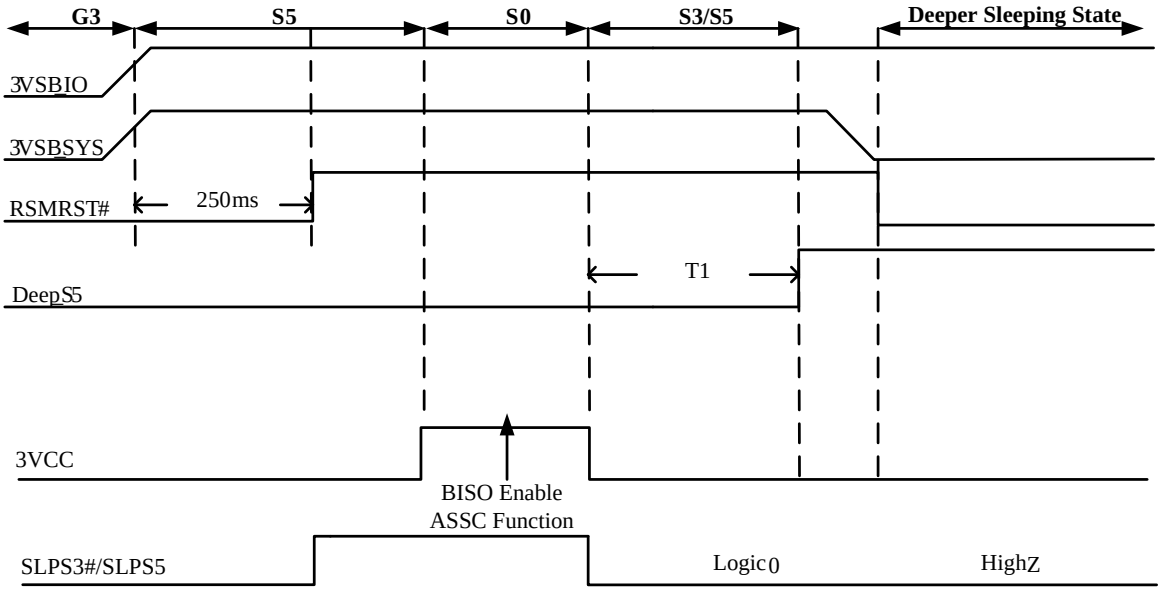
Figure 6-11 ASSC Application Diagram

6.8.1 When ASSC is disabled



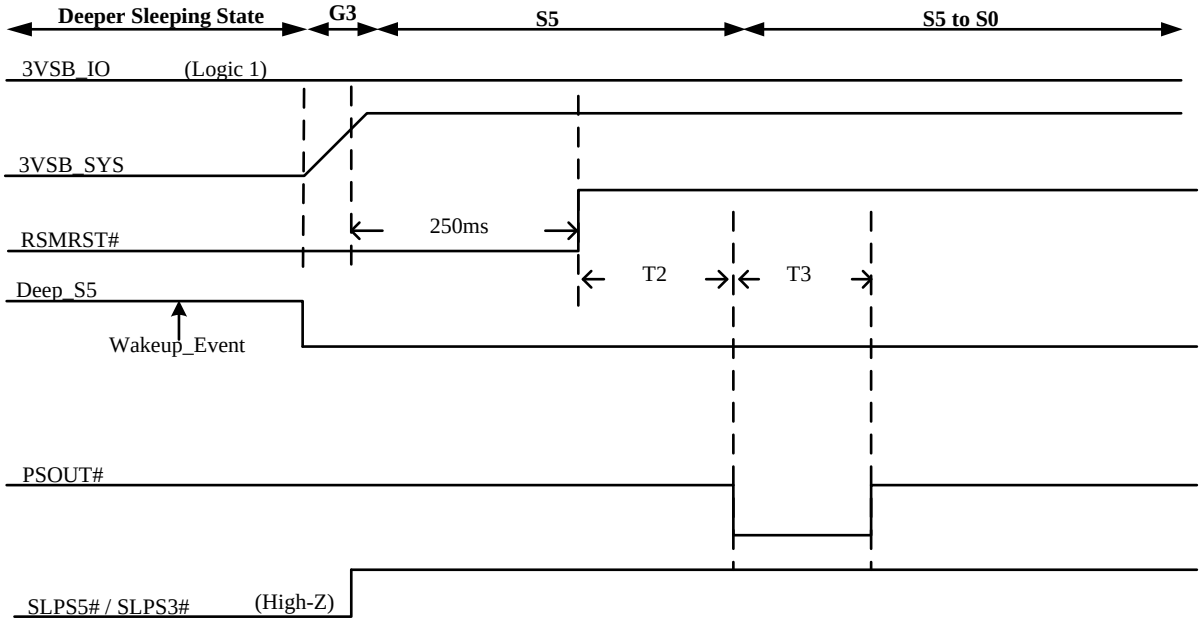
When ASSC is disabled, ACPI function is as same as the normal ACPI behavior.

6.8.2 When ASSC is enabled (Enter into Deeper Sleeping State)



When the first time AC plug in and enter into S0 State, BIOS can enable ASSC Function (DeepS3 or DeepS5), when the system enters S3/S5 state, the pin DEEP_S5 will be asserted after pre configuration delay time (power_off_dly_time, LD16 CRE2) to make the system entering the "Deeper Sleeping State (DSS)" where system's VSB power is cut off. When pin DEEP_S5 asserts, the pin RSMRST# will de-assert by detecting PSOUT# signal (monitor 3VSB SYS Power).

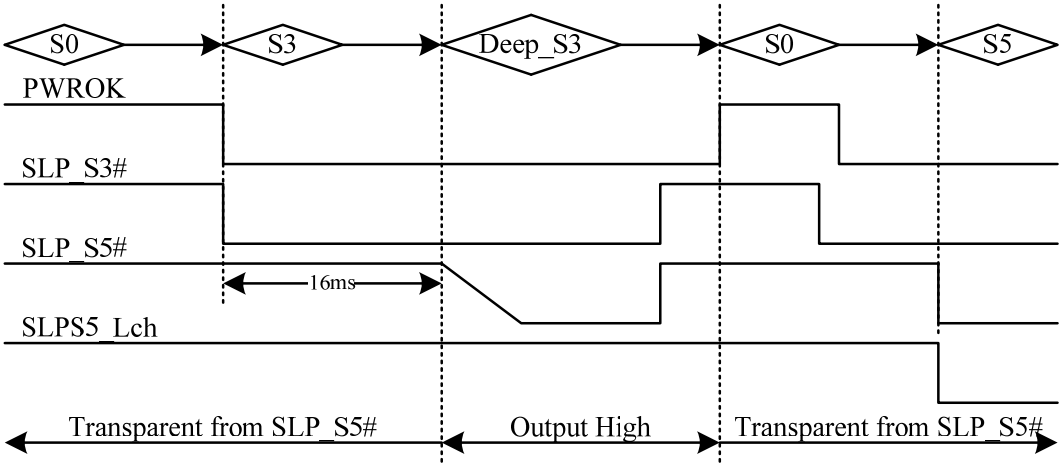
6.8.3 When ASSC is enabled (Exit Deeper Sleeping State)



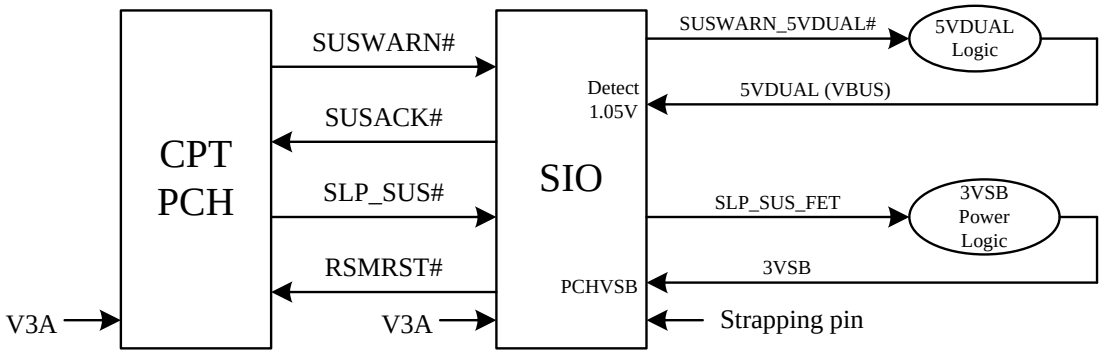
When any Wakeup Event (PSIN#, KB MS Wakeup, CIR wakeup, GPIO Wakeup) happened, pin DEEP_S5 will be de-asserted to turn on the VSB power to the system. The pin RSMRST# will de-assert when 3VSB_SYS power reach valid voltage. And then the pin PSOUT# will issue a low pulse (T3) turn on the system after T2 time (wakeup delay time, LD16 CRE0). The PSOUT# low pulse is also programmable (LD16 CRE1). The T4 time is the delay from Deep_S5 ds-assert to Deeo_S5#_DELAY de-assert.

6.8.4 SLP_S5#_LATCH Control Function

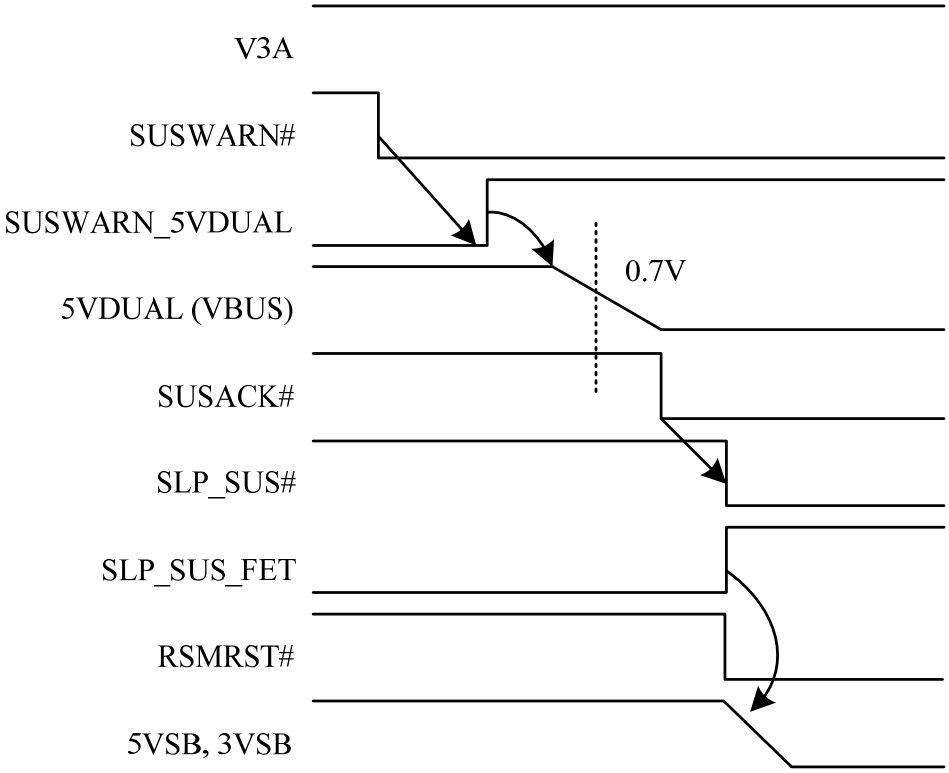
SLP_S5#_LATCH control signal is similar to SLPS5# signal. When System is at S0 ~ S5 state, SLP_S5#_LATCH follows the SLPS5# signal. When system is at DeepS5 State, SLP_S5#_LATCH will keep low state till system returns to S0 state. When system is at DeepS3 State, SLP_S5#_LATCH will keep high till system returns to S0 state. Please see the following timing diagram:



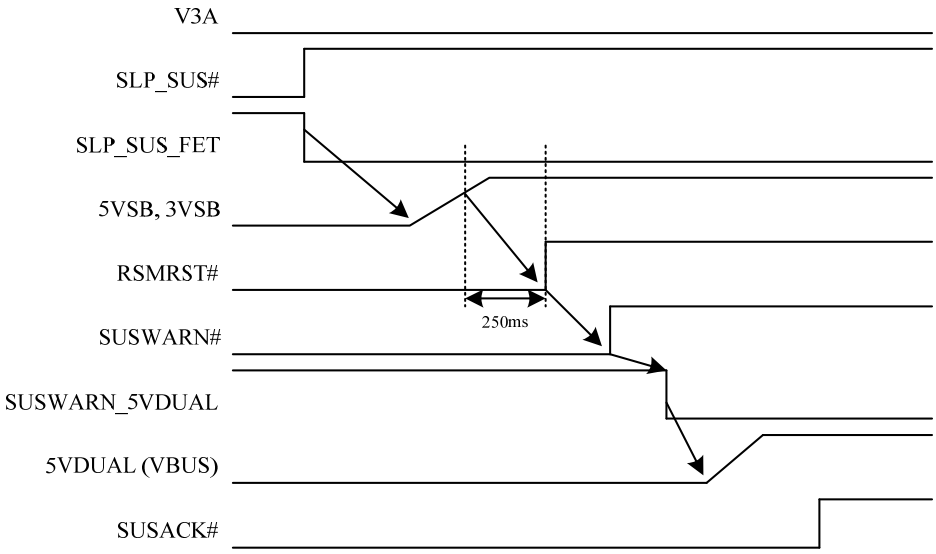
6.9 Intel DSW Function



6.9.1 Enter DSW State timing diagram

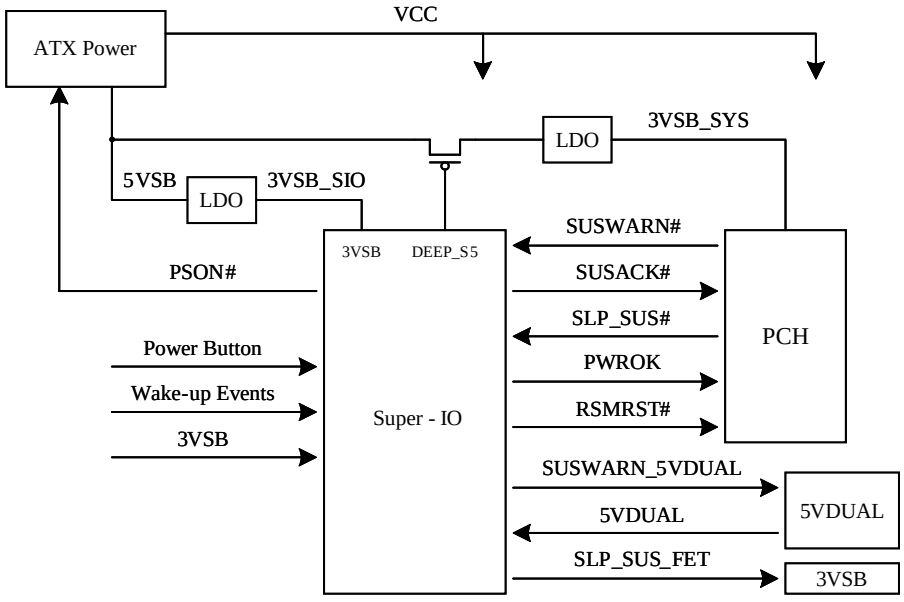


6.9.2 Exit DSW State timing diagram

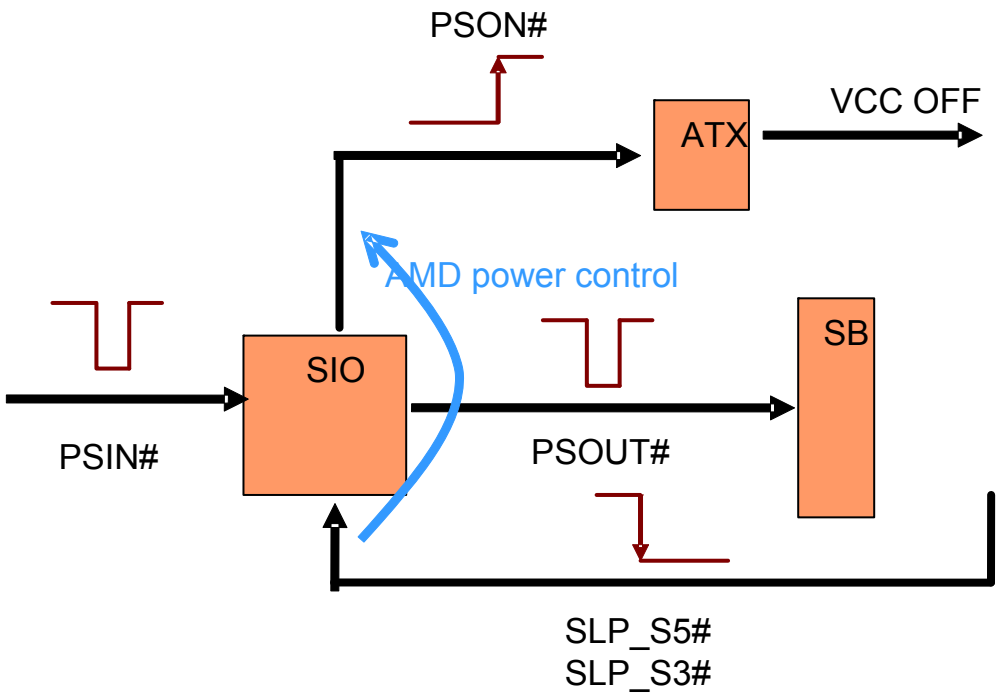


6.9.3 Application Circuit

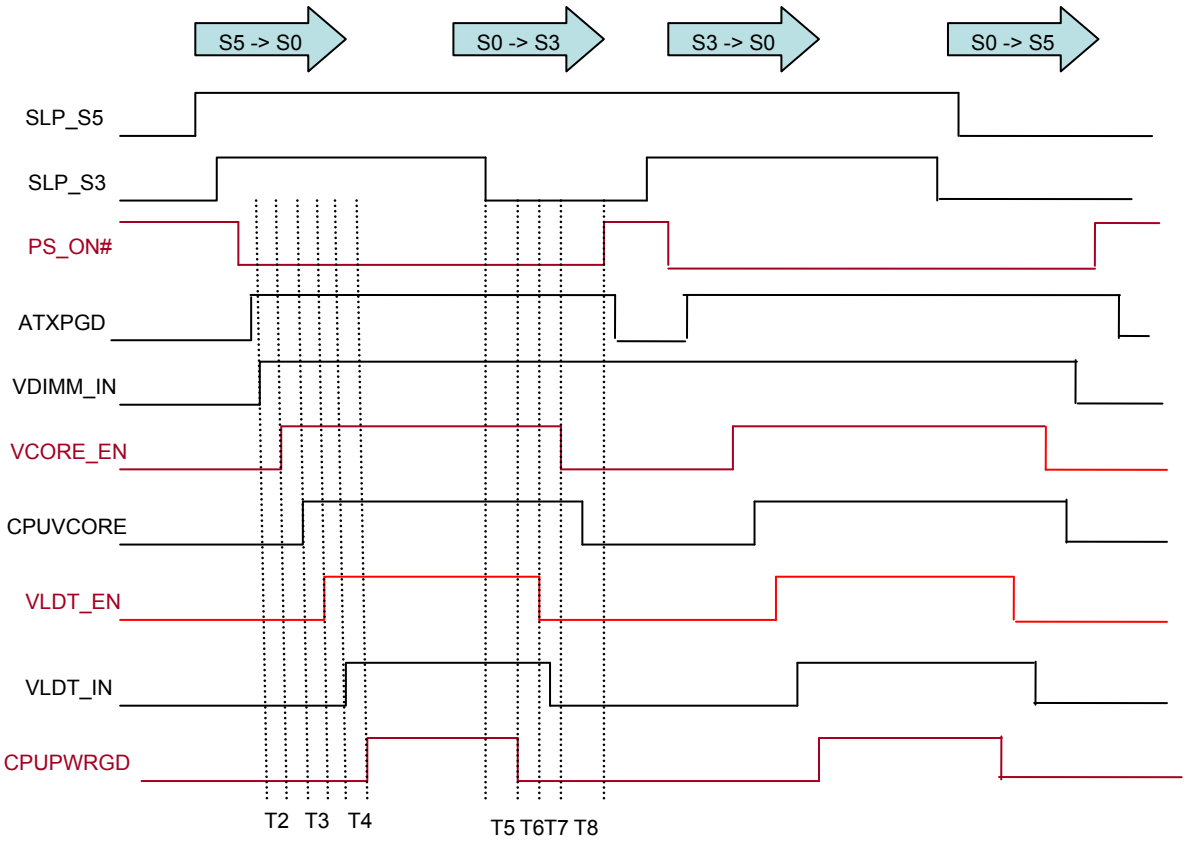
The NCT6776 can not only provide SIO Deep S5/S3 function, but Intel DSW function. The application circuit should follow the guide below:



6.10 AMD Power-On Sequence



We support new AMD power on sequence bace on ACPI power on sequence，therefore，user can choose which architecture by set the strapping pin GP25。If GP25 is 0, only ACPI power on sequence is set，otherwise, AMD power on sequence is combined with ACPI, user can set CR2F[5] to get the same condition. To make sure CR2B[4]:GP34_SEL and CR2B[0]:GP30_SEL are “0” before running the sequence, because they are ATXPGD and SLP_S5 pin select.



When S0->S3 or S0->S5, we support two kinds of power off sequence. One is non_level detect: it means VCORE_EN will pull low as long as about 10~15ms after VLDT_EN pull low and PSON will pull high as long as about 10~15ms after VCORE_EN pull low. Two, level detect, means VCORE_EN will pull low depend on delay time and pre-power group VLDT_IN, and PSON will pull high depend on pre-power group (VDIMM_IN, ATXPGD), too. User can set CR27[1] to choose two condition and its default is “0” (level detect).

Timing Parameters

Parameter	Description	Min.	Typ.	Max.	Unit
T2	Period of VDIMM rises to 0.7V to VCORE_EN assertion	10		15	ms
T3	Period of CPUVCORE rises to 0.7V to VLDT_EN assertion	10		15	ms
T4	Period of VLDT_IN rises to 0.7V to CPUPWRGD assertion	10		15	ms
T5	Period of SLP_S3# deassertion to CPUPWRGD deassertion	10		50	ms
T6	Period of CPUPWRGD deassertion to VLDT_EN deassertion	10		15	ms
T7	Period of VLDT_EN deassertion to VCORE_EN deassertion	10		15	ms
T8	Period of VCORE_EN deassertion to PS_ON# deassertion	10		15	ms

VDDA: 2.5V (not controlled by SIO)
VDIMM: DDR 1.8V, DDR3 1.5V (not controlled by SIO)
VLDT: 1.2V
VCORE: 0.8V ~ 1.55V

To support AMD power on sequence，we add some Pinout as VLDT_EN ，VCORE_EN，VLDT_12，VDIMM_18。The sequence is follow the figure above。CPU and NB must conform to the SPEC or else the SIO will suspend at the sequence。

7. CONFIGURATION REGISTER ACCESS PROTOCOL

The NCT6776F / NCT6776D uses a special protocol to access configuration registers to set up different types of configurations. The NCT6776F / NCT6776D has a total of 17 Logical Devices (from Logical Device 0 to Logical Device 17 with the exception of Logical Device 4, C, 10, 11, 12, 13 & 15 for backward compatibility) corresponding to fourteen individual functions: FDC (Logical Device 0), Parallel Port (Logical Device 1), UART A (Logical Device 2), UART B & IR (Logical Device 3), Keyboard Controller (Logical Device 5), CIR (Logical Device 6), GPIO6, 7, 8 & 9 (Logical Device 7), WDT1 & GPIO0, 1 & A (Logical Device 8), GPIO1, 2, 3, 4, 5, 6 & 7 (Logical Device 9), ACPI (Logical Device A), Hardware Monitor & Front Panel LED (Logical Device B), VID (Logical Device D), CIRWAKEUP (Logical Device E), GPIO (Logical Device F), SVID (Logical Device 14), Deep Sleep (Logical Device 16), and GPIOA (Logical Device 17).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The NCT6776F / NCT6776D, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin 2E_4E_SEL. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

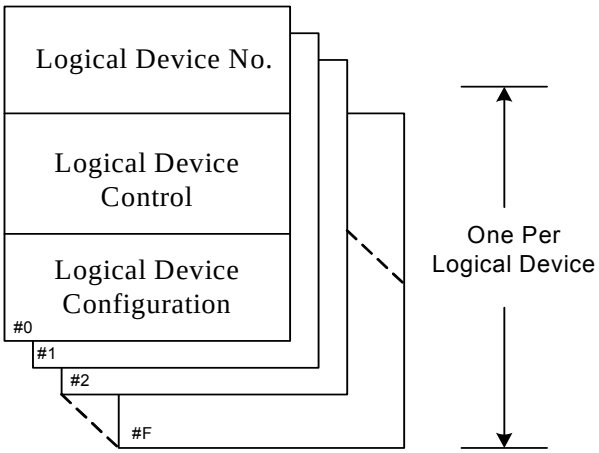


Figure 7-1 Structure of the Configuration Register

Table 7-1 Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	FDC	100h ~ FF8h
1	Parallel Port	100h ~ FF8h
2	UART A	100h ~ FF8h
3	UART B & IR	100h ~ FF8h
4	Reserved	
5	Keyboard Controller	100h ~ FFFh
6	CIR	100h ~ FF8h
7	GPIO 6, 7, 8 & 9	Reserved
8	WDT1 ,GPIO 0, 1 & A	Reserved
9	GPIO 1, 2, 3, 4, 5, 6 & 7	Reserved
A	ACPI	Reserved
B	Hardware Monitor & Front Panel LED	100h ~ FFEh
C	Reserved	
D	VID	Reserved
E	CIRWAKEUP	100h ~ FF8h
F	GPIO	Reserved
10	Reserved	
11	Reserved	
12	Reserved	
13	Reserved	
14	SVID	Reserved
15	Reserved	
16	Deep Sleep	Reserved
17	GPIO A	Reserved

7.1 Configuration Sequence

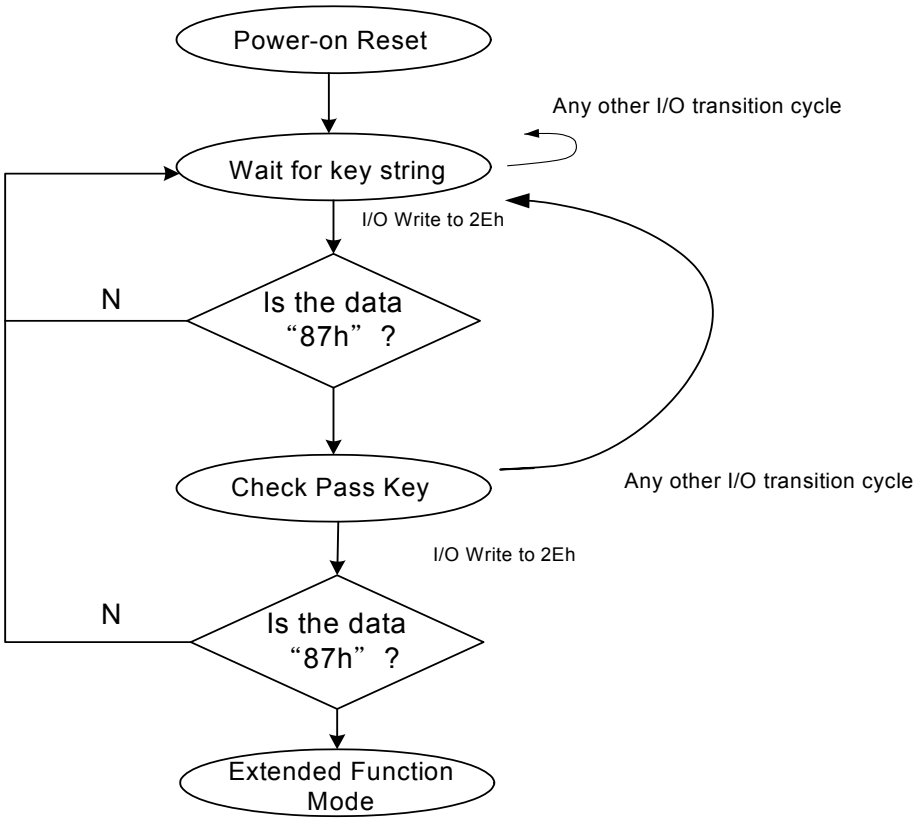


Figure 7-2 Configuration Register

To program the NCT6776F / NCT6776D configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR[26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```
;-------------------------------------------------
; Enter the Extended Function Mode
;-------------------------------------------------
MOV    DX, 2EH
MOV    AL, 87H
OUT    DX, AL
OUT    DX, AL
;-------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;-------------------------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 07H
OUT    DX, AL          ; point to Logical Device Number Reg.
MOV    DX, 2FH
MOV    AL, 01H
OUT    DX, AL          ; select Logical Device 1
;
MOV    DX, 2EH
MOV    AL, F0H
OUT    DX, AL          ; select CRF0
MOV    DX, 2FH
MOV    AL, 3CH
OUT    DX, AL          ; update CRF0 with value 3CH
;-----------------------------------------------
; Exit the Extended Function Mode
;-----------------------------------------------
MOV    DX, 2EH
MOV    AL, AAH
OUT    DX, AL
```

8. HARDWARE MONITOR

8.1 General Description

The NCT6776F / NCT6776D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The NCT6776F / NCT6776D can simultaneously monitor all of the following inputs:

- Nine analog voltage inputs (five internal voltages CPUVCORE, VBAT, 3VSB, 3VCC and AVCC; four external voltage inputs)
- Five fan tachometer inputs
- Three remote temperatures, using either a thermistor or from the CPU thermal diode (voltage or Current Mode measurement method)
- Two case-open detection signal.

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the NCT6776F / NCT6776D can generate the following outputs:

- Three PWM (pulse width modulation) and one DC fan outputs for the fan speed control
- SMI#
- OVT# signals for system protection events

The NCT6776F / NCT6776D provides hardware access to all monitored parameters through the LPC or I^2C interface and software access through application software, such as Nuvoton's Hardware Doctor™, or BIOS.

The rest of this section introduces the various features of the NCT6776F / NCT6776D hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interfaces

The NCT6776F / NCT6776D provides two interfaces, LPC and I^2C, for the microprocessor to read or write the internal registers of the hardware monitor.

8.3 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 7 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed form an index/data pair of CPU I/O addresses. The

standard locations are usually 295h/296h and are set by CR[60h]&CR[61h] accessed using the Super I/O protocol as described in Chapter 7.

Due to the number of internal register, it is necessary to separate the register sets into “banks” specified by register 4Eh. The structure of the internal registers is shown in the following figure.

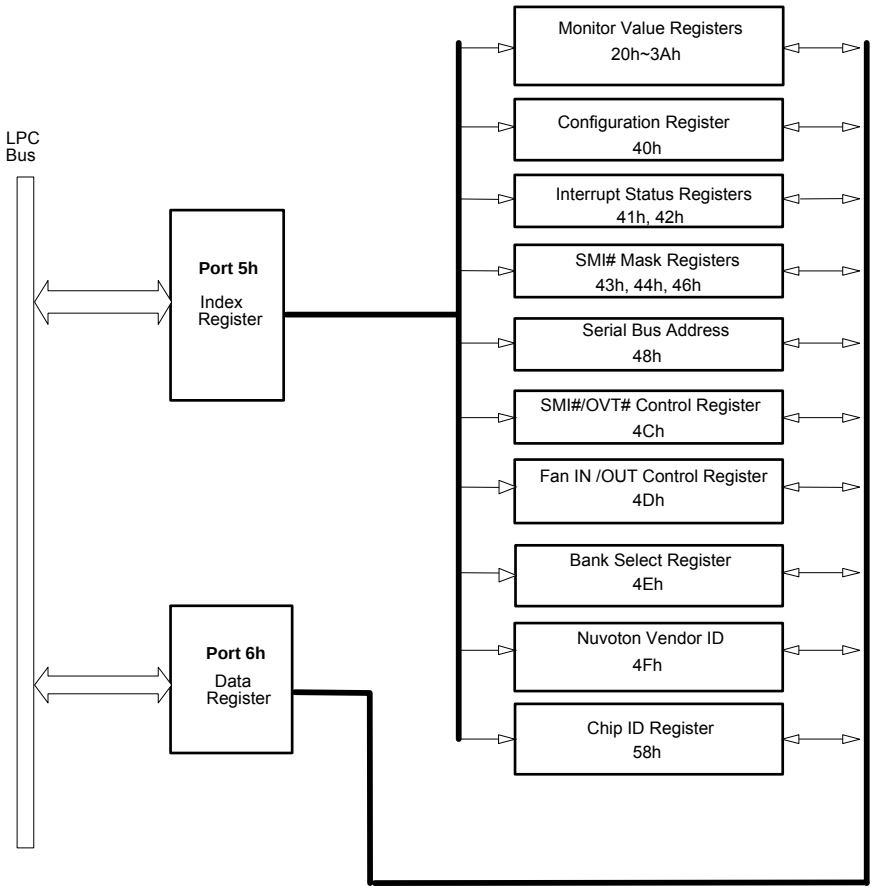


Figure 8-1 LPC Bus’ Reads from / Write to Internal Registers

8.4 I²C interface

The I²C interface is a second, serial port into the internal registers of the hardware monitor function block. The interface is totally compatible with the industry-standard I²C specification, allowing external components that are also compatible to read the internal registers of the NCT6776F / NCT6776D hardware monitor and control fan speeds. The address of the I²C peripheral is set by the register located at index 48h (which is accessed by the index/data pair at I/O address typically at 295h/296h)

The two timing diagrams below illustrate how to use the I²C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

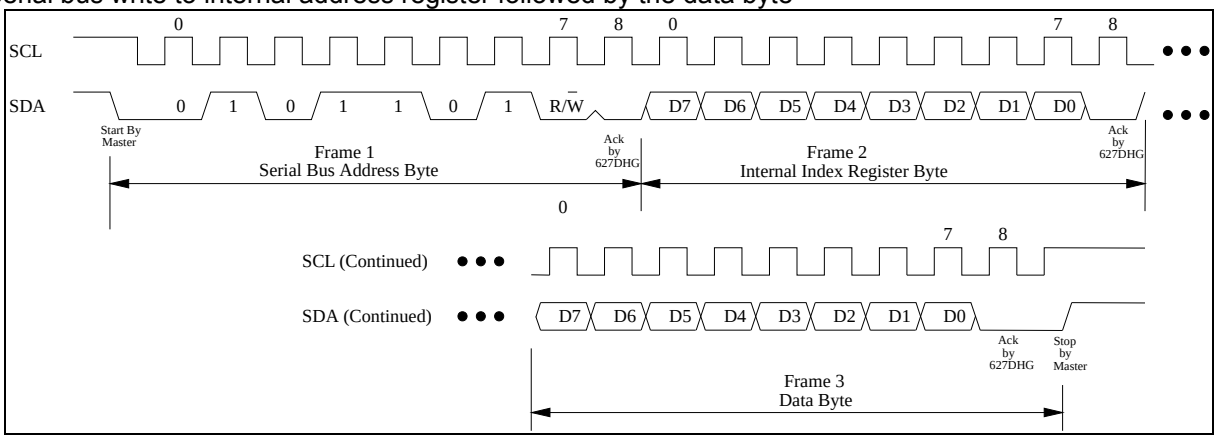


Figure 8-2 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

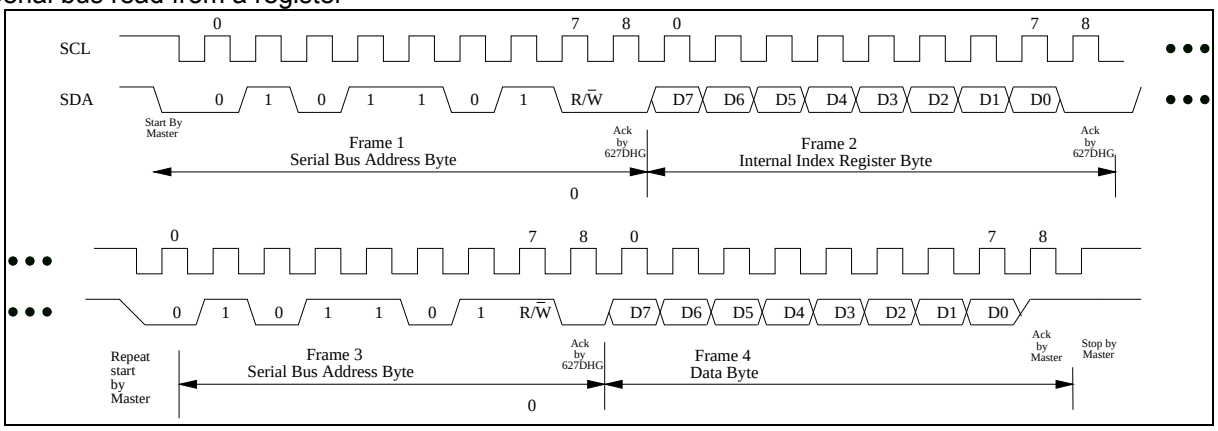


Figure 8-3 Serial Bus Read from Internal Address Register

8.5 Analog Inputs

The nine analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of 4 general-purpose inputs connected to external device pins (VIN0 – VIN3) and five internal signals connected to the power supplies (CPUVCORE, AVCC, VBAT, 3VSB and 3VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

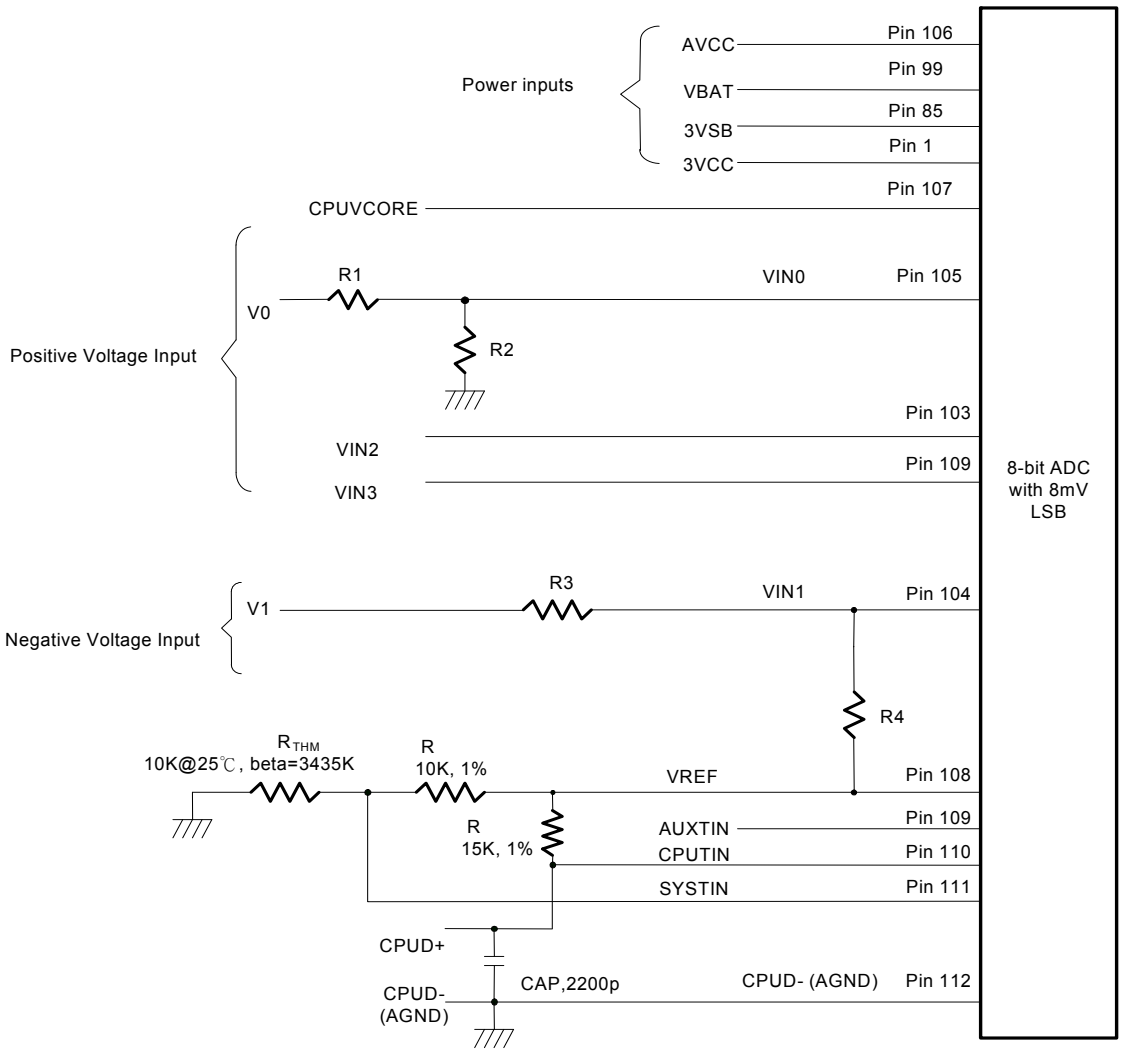


Figure 8-4 Analog Inputs and Application Circuit of the NCT6776F / NCT6776D

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing.

8.5.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVCC, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34KΩ, yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

R3 and R4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from –12 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

8.5.2 Voltage Data Format

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

Detected Voltage = Reading * 0.008 V

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled accordingly.

8.5.2.1. Voltage Reading

NCT6776F / NCT6776D has 9 voltage reading:

	3VCC	**AVCC**	**3VSB**	**VBAT**	
Voltage reading	Bank0, index23	Bank0, index22	Bank5, Index50	Bank5, Index51	
	CPUVCORE	**VIN0**	**VIN1**	**VIN2**	**VIN3**
Voltage reading	Bank0, index20	Bank0, index21	Bank0, index24	Bank0, index25	Bank0, index26

8.5.3 Temperature Data Format

The data format for sensors SYSTIN, CPUTIN and AUXTIN is 9-bit, two's-complement. This is illustrated in the table below. There are two sources of temperature data: external thermistors or thermal diodes.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1Ceh
-55°C	1100,1001	C9h	1,1001,0010	192h

8.5.3.1. Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF (pin 108). The configuration registers to select a thermistor temperature sensor and the measurement method are found at Bank 0, index 59h, 5Dh, and 5Eh.

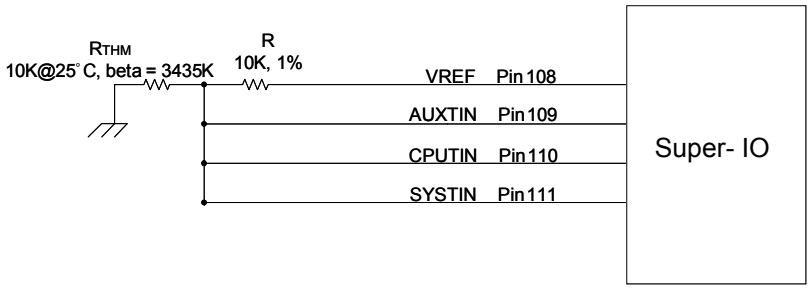


Figure 8-5 Monitoring Temperature from Thermistor

8.5.3.2. Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to AGND (pin 112), and the D+ pin is connected to the temperature sensor pin in the NCT6776F / NCT6776D. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh, and 5Eh.

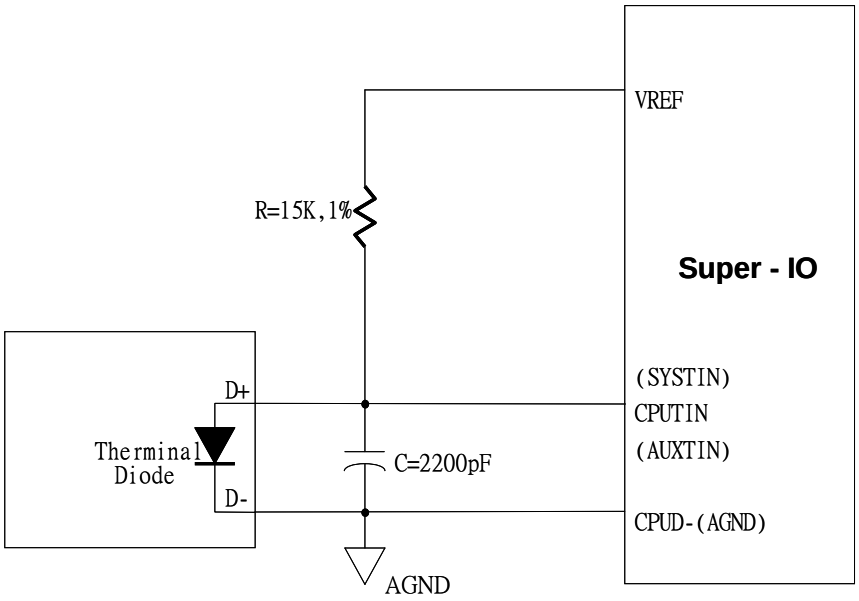


Figure 8-6 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.5.3.3. Monitor Temperature from Thermal Diode (Current Mode)

The NCT6776F / NCT6776D can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

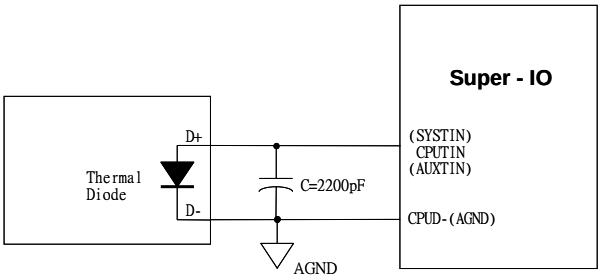


Figure 8-7 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- (pin 112) and the pin D+ is connected to temperature sensor pin in the NCT6776F / NCT6776D. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh and 5Eh.

8.5.3.4. Temperature Reading

NCT6776F / NCT6776D has 6 temperature reading can monitor different temperature sources (ex. SYSTIN, CPUTIN, AUXTIN, PECI…etc).

	SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4	SMIOVT5	SMIOVT6
Temperature source select	Bank6, index21 bit[4:0] default:	Bank6, index22 bit[4:0] default:	Bank6, index23 bit[4:0] default:	Bank6, index24 bit[4:0] default:	Bank6, index25 bit[4:0] default:	Bank6, index26 bit[4:0] default:

	SYSTIN	CPUTIN	AUXTIN	SYSTIN	SYSTIN	SYSTIN
Temperature reading (2's complement)	Bank0, index27	Bank1, index50 & index51 bit7	Bank2, index50 & index51 bit7	Bank6, index2B & index2E bit0	Bank6, index2C & index2E bit1	Bank6, index2D & index2E bit2

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

8.6 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the NCT6776F / NCT6776D supports. The NCT6776F / NCT6776D contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-8 PECI Temperature shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

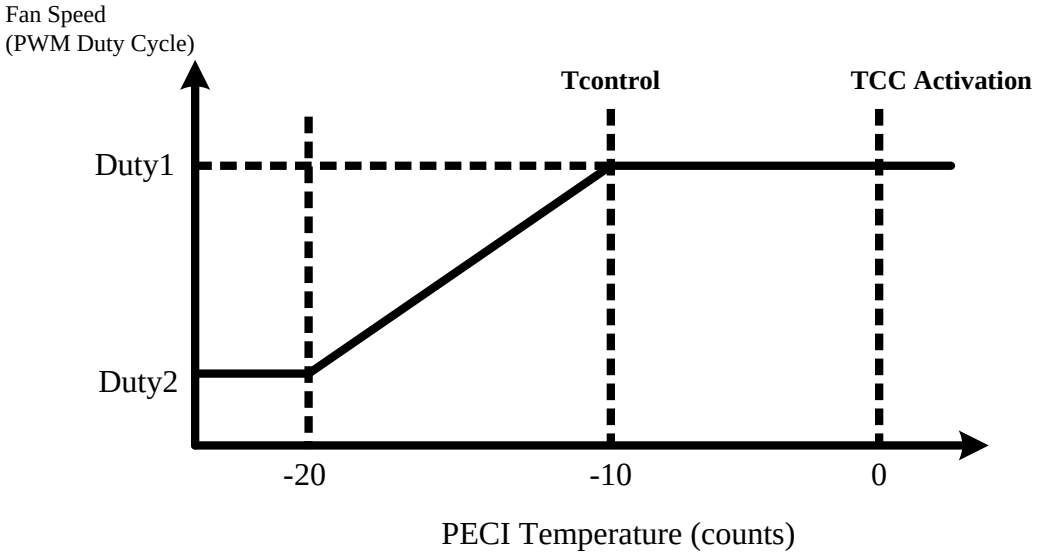


Figure 8-8 PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

The device also provides an offset register to 'shift' the negative PECI readings to positive values. The offset registers are called "Tbase", which are located at Bank7 Index 09h for Agent0 and Bank7 Index 0Ah for Agent1. All default values of these Tbase registers are 8'h00. The unit of the Tbase register contents is "count" to match that of PECI values. The resultant value (Tbase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

The Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets, shows the temperature and fan-speed relationship after Tbase offset is applied (based on Figure 8-8 PECI Temperature). This view is from the perspective of the NCT6776F / NCT6776D fan control circuit.

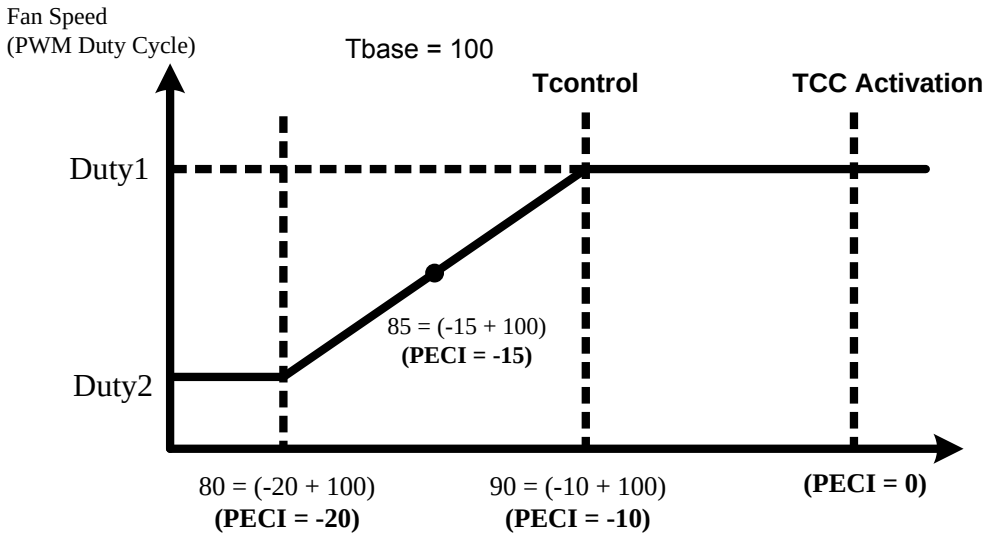


Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets

Assuming Tbase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of NCT6776F / NCT6776D, BIOS/software can include Tbase in determining the thresholds (limits). In this example, assuming Tcontrol is -10 and Tbase is set to 100 (1), the threshold temperature value corresponding to the "100% fan duty-cycle" event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

Tcontrol is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of Tcontrol to match the specific application.

8.7 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.7.1 Fan Speed Reading

The fan speed reading at:

	FAN COUNT READING 13-bit		FAN RPM READING NOTE 16-bit	
	[12:5]	[4:0]	[15:8]	[7:0]
SYSFANIN	Bank6, index30	Bank6, index31	Bank6, index56	Bank6, index57
CPUFANIN	Bank6, index32	Bank6, index33	Bank6, index58	Bank6, index59
AUXFANIN0	Bank6, index34	Bank6, index35	Bank6, index5A	Bank6, index5B
AUXFANIN1	Bank6, index36	Bank6, index37	Bank6, index5C	Bank6, index5D
AUXFANIN2	Bank6, index38	Bank6, index39	Bank6, index5E	Bank6, index5F

Note. The default value of the “16-bit RPM reading” is 0x00A4h.

8.7.2 Fan Speed Calculation by Fan Count Reading

In 16-bit fan count reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by the following equation, fan count could be 8-bit or 16-bit:

$$RPM = \frac{1.35 \times 10^6}{Count}$$

8.7.3 Fan Speed Calculation by Fan RPM Reading

In 16-bit fan RPM reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by translating 16-bit RPM reading from hexadecimal to decimal.

Register reading 0x09C4h = 2500 RPM

8.7.4 Fan Speed Control

The NCT6776F / NCT6776D has three output pins for fan control, only SYSFANOUT offers PWM duty cycle and DC voltage to control the fan speed. The output type (PWM or DC) of each pin is configured by Bank0 index 04h, bits 0 for SYSFANOUT, bits 1 for CPUFANOUT, and Bank0 index 12h, bit 0 for AUXFANOUT.

		SYSFANOUT	CPUFANOUT	AUXFANOUT
Output Type Select		Bank0, index04 bit0 **0: PWM output** **1: DC output (default)**	Bank0, index04 bit1 **Only PWM output**	Bank0, index12 bit0 **Only PWM output**
Output Type Select (in PWM output)		CR24 bit4 0: open-drain (default) 1: push-pull	CR24 bit3 0: open-drain (default) 1: push-pull	CR24 bit5 0: push-pull (default) 1: open-drain
PWM Output Freqency		Bank0, Index00	Bank0, Index02	Bank0, Index10
Fan Control Mode Select		Bank1, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank3, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
Output Value (write)	**PWM output (Duty)**	Bank1, index09 bit[7:0]	Bank2, index09 bit[7:0]	Bank3, index09 bit[7:0]
	DC output (Voltage)	Bank1, index09 bit[7:2]		
Current Output Value (read only)		Bank0, index01	Bank0, index03	Bank0, index11

For PWM, the duty cycle is programmed by eight-bit registers at Bank1 Index 09h for SYSFANOUT, Bank2 Index 09h for CPUFANOUT and Bank3 Index 09h for AUXFANOUT. The duty cycle can be calculated using the following equation:

$$\text{Dutycycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The default duty cycle is FFh, or 100%. The PWM clock frequency is programmed at Bank0 Index 00h, Index 02h, and Index 10h.

For DC, the NCT6776F / NCT6776D has a six bit digital-to-analog converter (DAC) that produces 0 to 2.048 Volts DC. The analog output is programmed at Bank1 Index 09h bit[7:2] for SYSFANOUT. The analog output can be calculated using the following equation:

$$\text{OUTPUT Voltage (V)} = Vref \times \frac{\text{Programmed 6 - bit Register Value}}{64}$$

The default value is 111111YY, or nearly 2.048 V, and Y is a reserved bit.

8.7.5 SMART FAN™ Control

The NCT6776F / NCT6776D supports various different fan control features:

- SMART FAN™ I (Thermal Cruise & Speed Cruise)
- SMART FAN™ IV
- Close-Loop Fan Control RPM mode

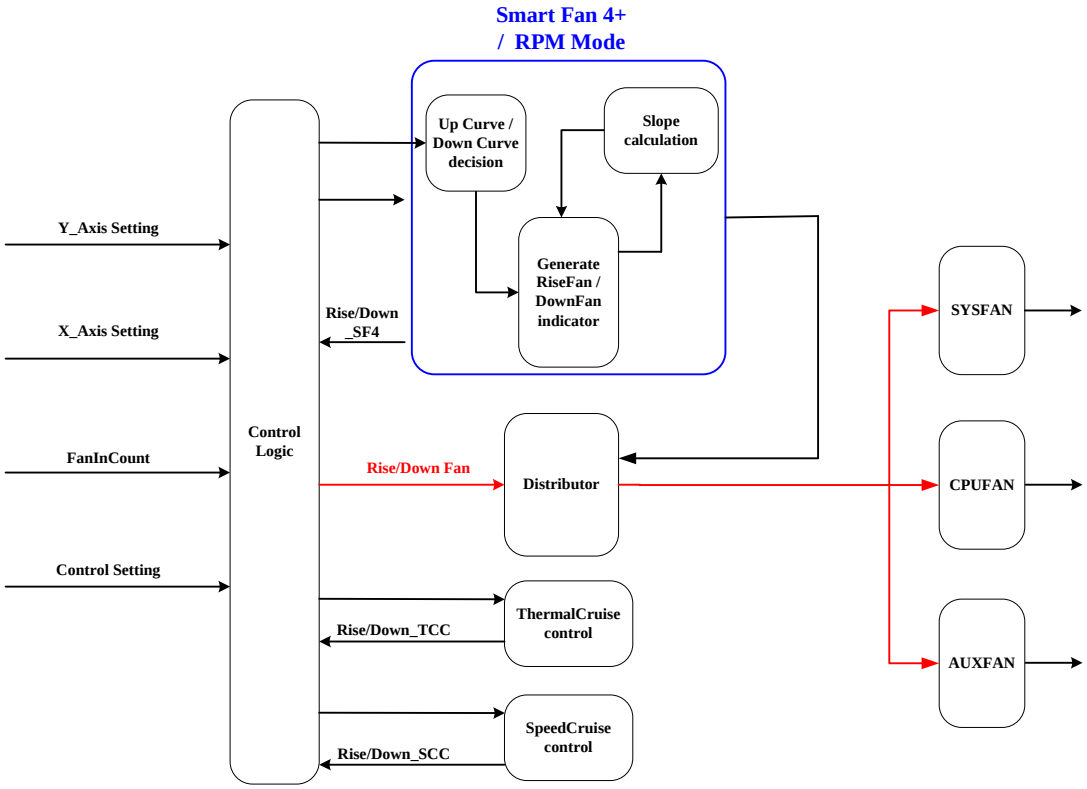
	SYSFANOUT	CPUFANOUT	AUXFANOUT
Fan Control Mode Select	Bank1, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank3, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV

8.7.6 Temperature Source & Reading for Fan Control

Select temperature source for each fan control output:

	SYSFANOUT	CPUFANOUT	AUXFANOUT
Fan Control Temperature Source Select	Bank1, index00 bit[4:0] Default: SYSTIN	Bank2, index00 bit[4:0] Default: CPUTIN	Bank3, index00 bit[4:0] Default: AUXTIN
Fan Control Temperature Reading	Bank0, index73 & Bank0, index74 bit7	Bank0, index75 & Bank0, index76 bit7	Bank0, index77 & Bank0, index78 bit7

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.



SMART FAN™ Function Block Diagram

8.8 SMART FAN™ I

8.8.1 Thermal Cruise Mode

Thermal Cruise mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (e.g., 58°C) but remains above the low end (e.g., 52 °C), fan output remains the same.

(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified "stop value". This "stop value" is enabled by the Bank1, Index00h, Bit7 for SYSFANOUT; Bank2, Index00h, Bit7 for CPUFANOUT and Bank3, Index00h, Bit7 for AUXFANOUT. The stop value itself is separately specified in Bank1 Index05h, Bank2 Index05h and Bank3 Index05h. The fan remains at the stop value for the period of time also separately defined in Bank1 Index07h, Bank2 Index07h and Bank3 Index07h.

In general, Thermal Cruise mode means

- If the current temperature is higher than the high end, increase the fan speed.
- If the current temperature is lower than the low end, decrease the fan speed.
- Otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise mode.

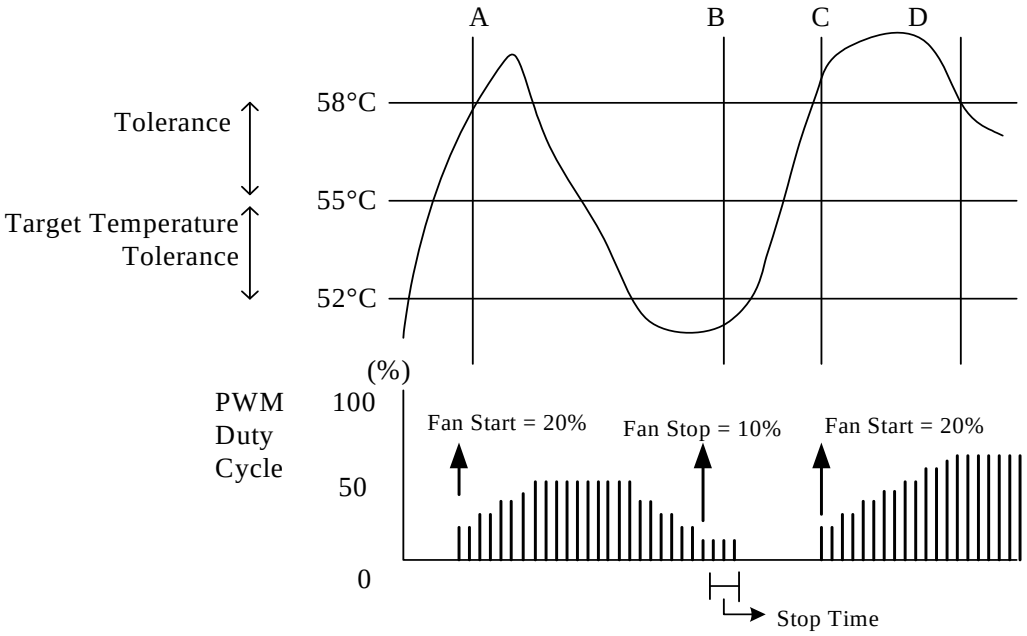


Figure 8-10 Mechanism of Thermal Cruise™ Mode (PWN Duty Cycle)

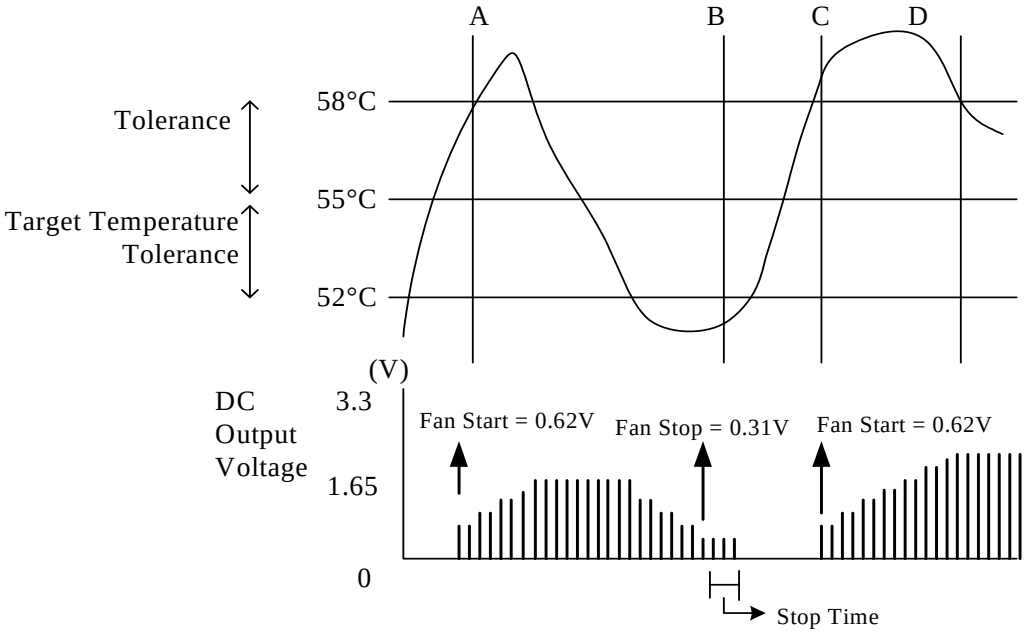


Figure 8-11 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

8.8.2 Speed Cruise Mode

Speed Cruise mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

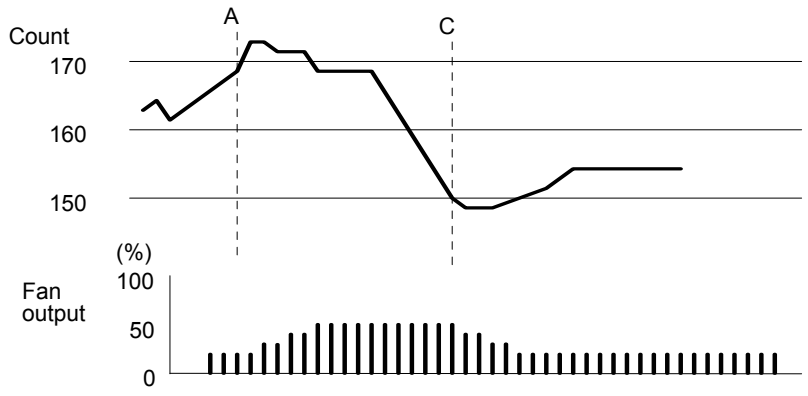


Figure 8-12 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise and Fan Speed mode.

Table 8-2 Relative Registers – at Thermal CruiseTM Mode

THERMAL CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP- UP TIME	STEP-DOWN TIME
SYSFANOUT	Bank 1, index 01h bit[7:0]	Bank 1, index 02h Bit[2:0]	Bank 1, index 06h	Bank 1, index 05h	Bank 1, Index 00h, bit7	Bank 1, index 07h	Bank 1, index 03h	Bank 1, index 04h
CPUFANOUT	Bank 2, index 01h bit[7:0]	Bank 2, index 02h Bit[2:0]	Bank 2, index 06h	Bank 2, index 05h	Bank 2, Index 00h, bit7	Bank 2, index 07h	Bank 2, index 03h	Bank 2, index 04h
AUXFANOUT	Bank 3, index 01h bit[7:0]	Bank 3, index 02h Bit[2:0]	Bank 3, index 06h	Bank 3, index 05h	Bank 3, Index 00h, bit7	Bank 3, index 07h	Bank 3, index 03h	Bank 3, index 04h

THERMAL CRUISE MODE	CRITICAL TEMPERATURE	ENABLE THERMAL CRUISE MODE
SYSFANOUT	Bank 1, index 35h	Bank 1, Index 02h, bit[7:4] = 01h
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 02h, bit[7:4] = 01h
AUXFANOUT	Bank 3, Index 35h	Bank 3, Index 02h, bit[7:4] = 01h

Table 8-3 Relative Registers – at Speed CruiseTM Mode

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE2_H	STEP- UP TIME	STEP-DOWN TIME	ENABLE SPEED CRUISE MODE
SYSFANOUT	Bank 1, Index 01h	Bank 1, Index 0C bit[3:0]	Bank 1, Index 02 bit[2:0]	Bank 1, Index 0C bit[6:4]	Bank 1, Index 03h	Bank 1, Index 04h	Bank 1, Index 02h bit[7:4] = 02h
CPUFANOUT	Bank 2, Index 01h	Bank 2, Index 0C bit[3:0]	Bank 2, Index 02 bit[2:0]	Bank 2, Index 0C bit[6:4]	Bank 2, Index 03h	Bank 2, Index 04h	Bank 2, Index 02h bit[7:4] = 02h
AUXFANOUT	Bank 3, Index 01h	Bank 3, Index 0C bit[3:0]	Bank 3, Index 02 bit[2:0]	Bank 3, Index 0C bit[6:4]	Bank 3, Index 03h	Bank 3, Index 04h	Bank 3, Index 02h bit[7:4] = 02h

8.9 SMART FAN™ IV & Close Loop Fan Control Mode

SMART FAN™ IV and Close Loop Fan Control Mode offer 3 slopes to control the fan speed.

Set **Critical Temperature, Bank1 Index 35_{HEX} , Bank2 Index 35_{HEX} , Bank3 Index 35_{HEX}**

- Set the **Relative Register-at SMART FAN™ IV Control Mode Table**
  If fan control mode is set as Close Loop Fan Control, the unit step is 50RPM. So the maximum controllable RPM is 50*255=12,750RPM.
- Set Tolerance **of Target Temperature, Bank1 Index 02_{HEX} bit[2:0] . Bank2 Index 02_{HEX} bit[2:0]. Bank3 Index 02_{HEX} bit[2:0]**.

The 3 slopes can be obtained by setting FanDuty1/RPM1~FanDuty4/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target FanDuty/RPM based on the current slope. For example, assuming Tx is the current temperature and Ty is the target, then

The slope:

$$X2 = \frac{(FanDuty3/RPM3) - (FanDuty2/RPM2)}{(T3 - T2)}$$

Fan Output:

$$Target\ FanDuty\ or\ RPM = (FanDuty2\ or\ RPM2) + (Tx - T2) \cdot X2$$

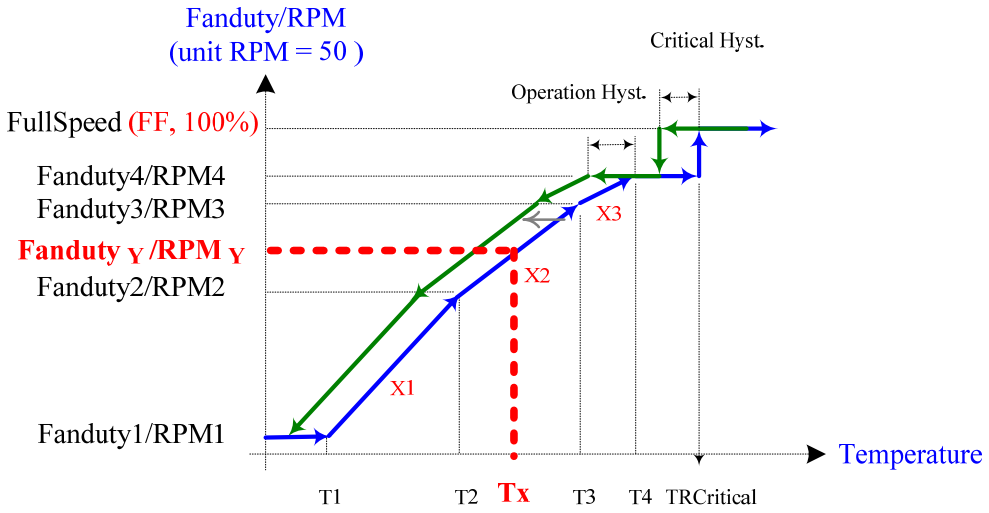


Figure 8-13 SMART FAN™ IV & Close Loop Fan Control Mechanism

Table 8-4 Relative Register-at SMART FANTM IV Control Mode

DESCRIPTION	T1	T2	T3	T4
SYSFANOUT	Bank 1, Index 21h	Bank 1, Index 22h	Bank 1, Index 23h	Bank 1, Index 24h
CPUFANOUT	Bank 2, Index 21h	Bank 2, Index 22h	Bank 2, Index 23h	Bank 2, Index 24h
AUXFANOUT	Bank 3, Index 21h	Bank 3, Index 22h	Bank 3, Index 23h	Bank 3, Index 24h

DESCRIPTION	T1	T2	T3	T4
DESCRIPTION	**DC/PWM1**	**DC/PWM2**	**DC/PWM3**	**DC/PWM4**
SYSFANOUT	Bank 1, Index 27h	Bank 1, Index 28h	Bank 1, Index 29h	Bank 1, Index 2Ah
CPUFANOUT	Bank 2, Index 27h	Bank 2, Index 28h	Bank 2, Index 29h	Bank 2, Index 2Ah
AUXFANOUT	Bank 3, Index 27h	Bank 3, Index 28h	Bank 3, Index 29h	Bank 3, Index 2Ah

DESCRIPTION	CRITICAL TEMPERATURE	Critical Tolerance	Monitored temperature tolerance	ENABLE SMART FAN IV
SYSFANOUT	Bank 1, Index 35h	Bank 1, Index 38h, bit[2:0]	Bank1, Index 02h, bit[2:0]	Bank 1, Index 02h bit[7:4] = 04h
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 38h, bit[2:0]	Bank2, Index 02h, bit[2:0]	Bank 2, Index 02h bit[7:4] = 04h
AUXFANOUT	Bank 3, Index 35h	Bank 3, Index 38h, bit[2:0]	Bank3, Index 02h, bit[2:0]	Bank 3, Index 02h bit[7:4] = 04h

DESCRIPTION	ENABLE KEEP MIN	STEP-UP TIME	STEP-DOWN TIME	STOP VALUE	START-UP VALUE	STOP TIME	FANOUT STEP
SYSFANOUT	Bank 1, Index 00h, bit7	Bank 1, index 03h	Bank 1, index 04h	Bank 1, index 05h	Bank 1, index 06h	Bank 1, index 07h	Bank 1, Index 20h, Bit0
CPUFANOUT	Bank 2, Index 00h, bit7	Bank 2, index 03h	Bank 2, index 04h	Bank 2, index 05h	Bank 2, index 06h	Bank 2, index 07h	Bank 2, Index 20h, Bit0
AUXFANOUT	Bank 3, Index 00h, bit7	Bank 3, index 03h	Bank 3, index 04h	Bank 3, index 05h	Bank 3, index 06h	Bank 3, index 07h	Bank 3, Index 20h, Bit0

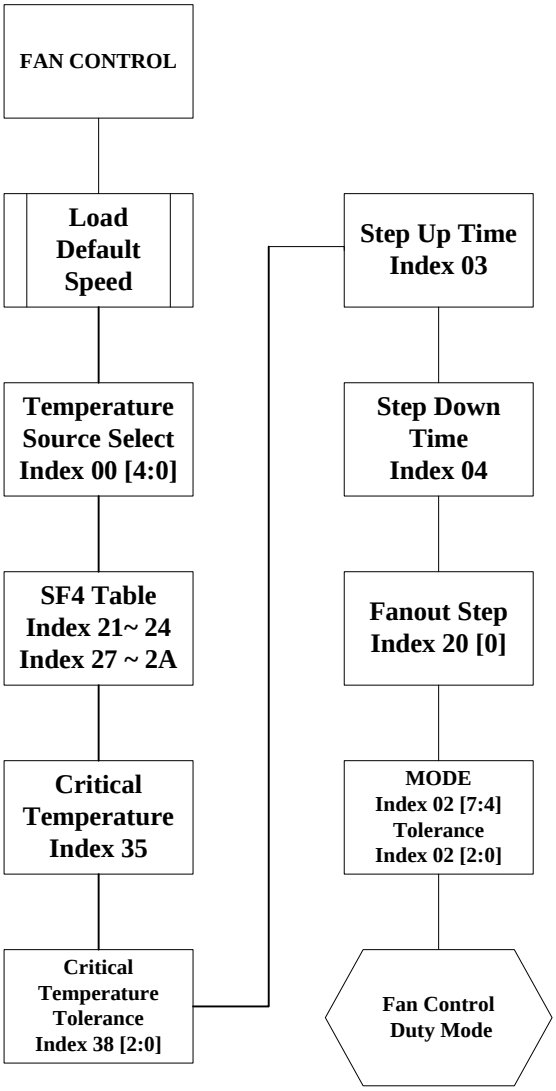


Figure 8-14 Fan Control Duty Mode Programming Flow

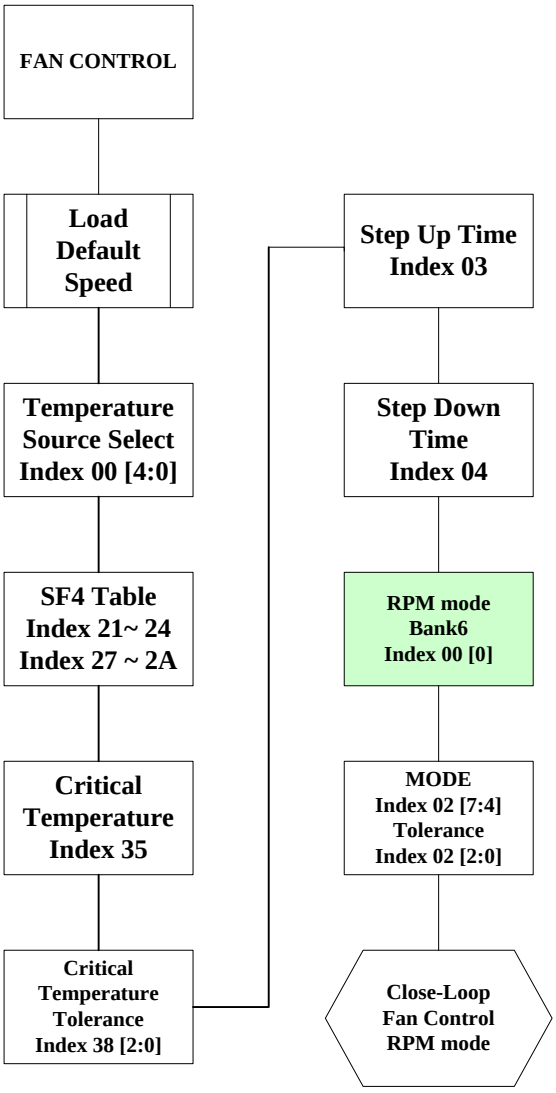


Figure 8-15 Close-Loop Fan Control RPM mode Programming Flow

8.9.1 Step Up Time / Step Down Time

SMART FAN™ IV is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat. This register should never be set to 0, otherwise, the fan duty will be abnormal.

8.9.2 Fan Output Start-up Value

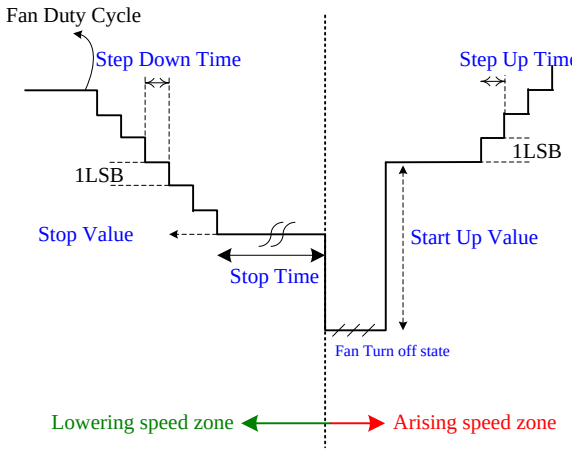
From still to rotate, the fan usually needs a higher fan output value to generate enough torque to conquer the restriction force. Thus the Fan Output Start-up Value is used to turn on the fan with the specified output value.

8.9.3 Fan Output Stop Value

It takes some time to bring a fan from still to working state. Therefore, Stop value are designed with a minimum fan output to keep the fan working when the system does not require the fan to help reduce heat but still want to keep the fast response time to speed up the fan.

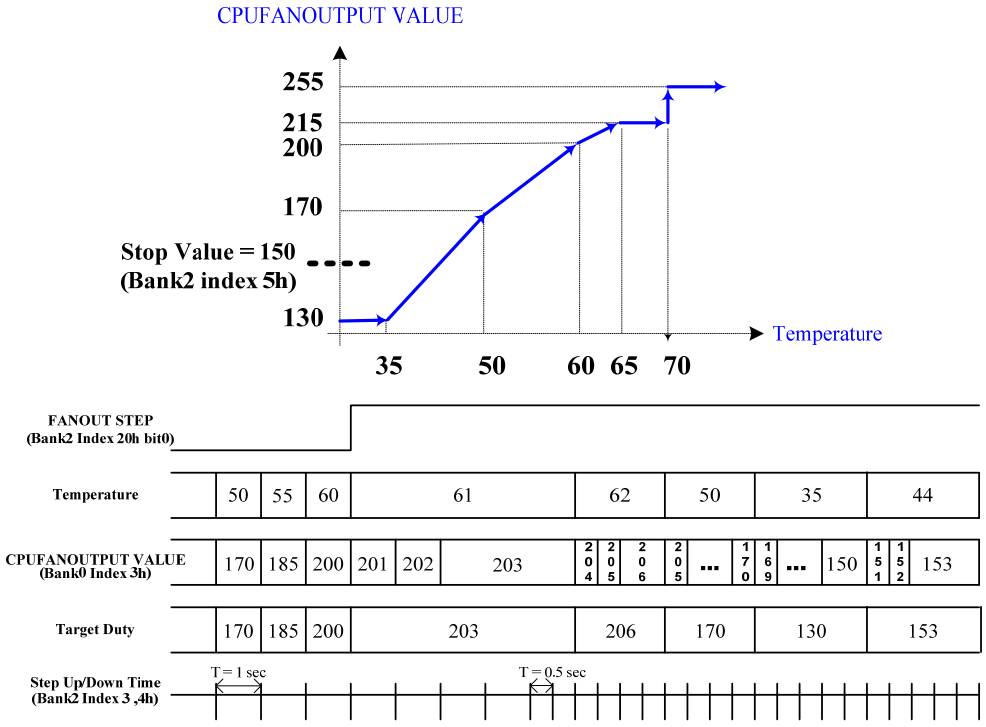
8.9.4 Fan Output Stop Time

A time interval is specified to turn off the fan if SmartFan continuously requests to slow down the fan which has already reached the Stop time.



Smart Fan Control Parameters Figure

8.9.5 Fan Output Step



8.9.6 Revolution Pulse Selection

The NCT6776F / NCT6776D supports four RPM output of the pulses selection function for different type of FAN which has the character of different pulses per revolution.The others could be set by HM register at Bank6, Index44, Bit1-0 for SYSFANIN; Bank6, Index45, Bit1-0 for CPUFANIN and Bank6, Index46, Bit1-0 for AUXFANIN0. All default value of pulse selection registers are 2 pulses of one revolution.

Setting description for “Pulse Selections Bits”:

00: 4 pulses per revolution

01: 1 pulse per revolution
10: 2 pulses per revolution (default)
11: 3 pulses per revolution

8.9.7 Weight Value Control

The NCT6776F / NCT6776D supports weight value control for fan duty output. By register configuration, the results of weight value circuit can be added to the fan duty of SMART FAN™ I or IV and output to the fan. Take CPUFANOUT for example, if SMART FAN™ IV is selected, CPUTIN is the temperature source, and weight value control is enabled, SMART FAN™ IV will calculate the output duty, and weight value circuit will calculate the corresponding weight value based on SYSTIN. As the SYSTIN temperature rises, its corresponding weight value increases. Then, the two values will be summed up and output to CPU fan. In other words, the CPU fan duty is affected not only by the CPUTIN but also the SYSTIN temperature.

Figure 8-16 SYS TEMP and Weight Value Relations shows the relation between the SYSTIN temperature and the weight value. Tolerance setup is offered on each change point to avoid weight value fluctuation resulted from SYSTIN temperature change. The weight value will increase by one weight value step only when the SYSTIN temperature is higher than the point value plus tolerance. Likewise, the weight value decreases by one weight value step only when the SYSTIN temperature is lower than the point value minus tolerance.

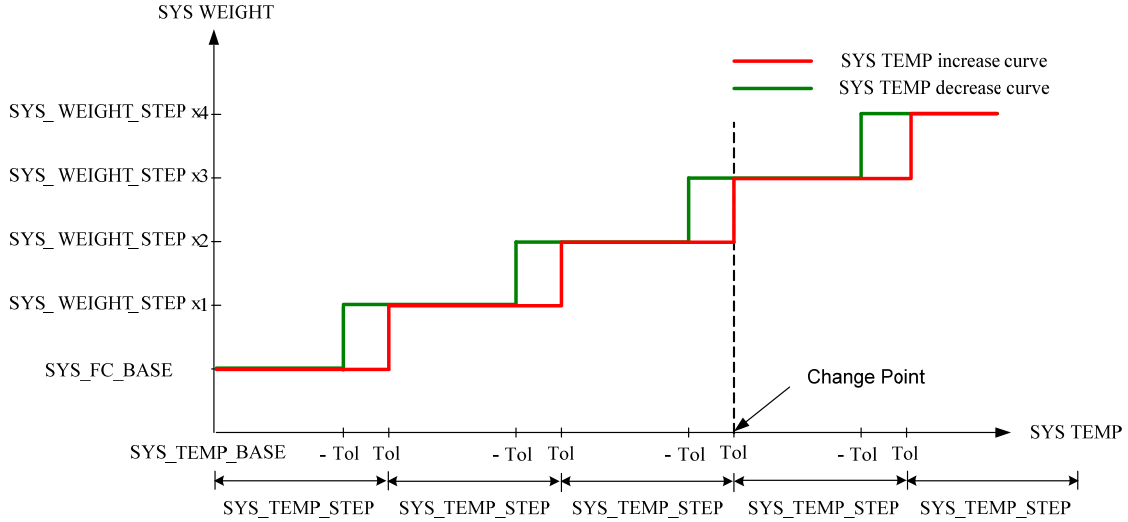


Figure 8-16 SYS TEMP and Weight Value Relations

Table 8-5 Relative Register-at Weight Value Control

DESCRIPTION	TEMP_BASE	FC_ BASE	TEMP_STEP	TEMP_STEP_ TOL	WEIGHT_STEP
SYSFANOUT	Bank 1, Index 3Dh	Bank 1, Index 3Eh	Bank 1, Index 3Ah	Bank 1, Index 3Bh	Bank 1, Index 3Ch
CPUFANOUT	Bank 2, Index 3Dh	Bank 2, Index 3Eh	Bank 2, Index 3Ah	Bank 2, Index 3Bh	Bank 2, Index 3Ch
AUXFANOUT	Bank 3, Index 3Dh	Bank 3, Index 3Eh	Bank 3, Index 3Ah	Bank 3, Index 3Bh	Bank 3, Index 3Ch

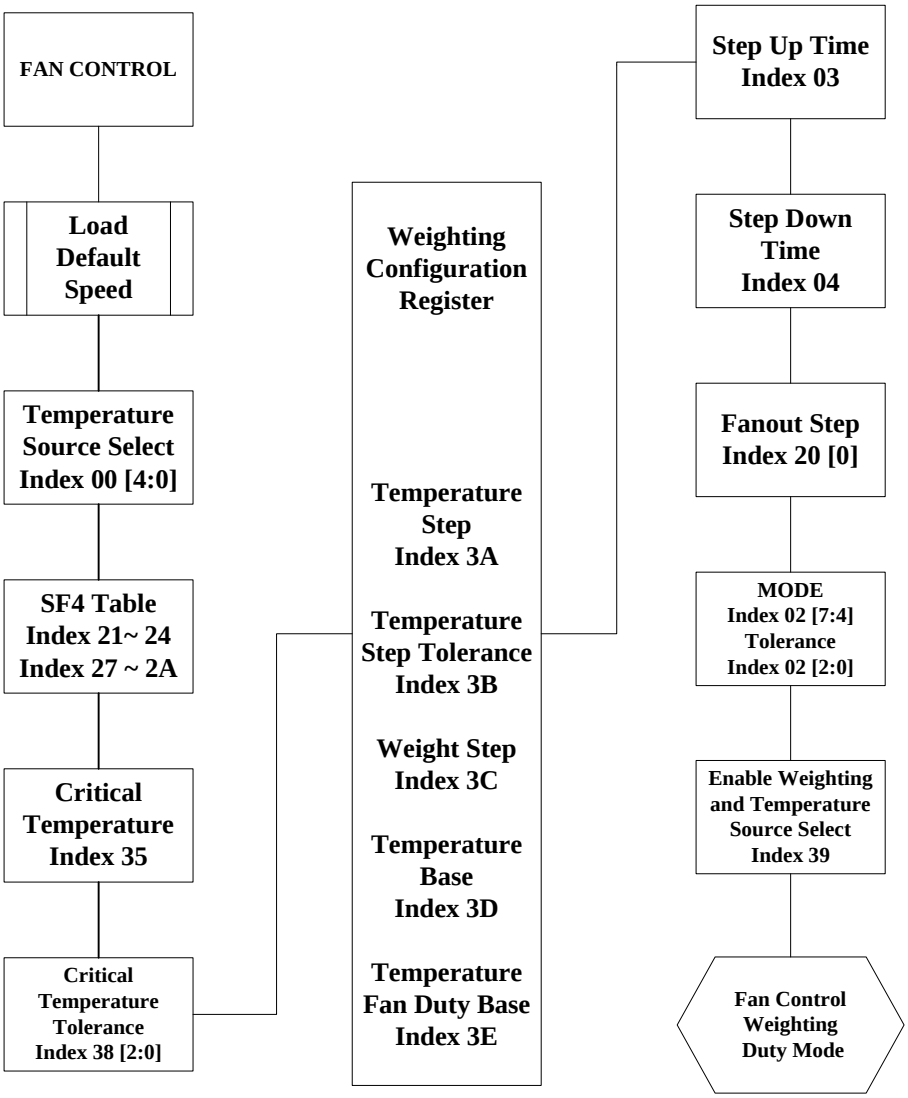


Figure 8-17 Fan Control Weighting Duty Mode Programming Flow

8.10 Alert and Interrupt

NCT6776F / NCT6776D supports 6 Temperature Sensors for interrupt detection depending on selective monitor temperature source.

	SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4	SMIOVT5	SMIOVT6
Temperature source select	Bank6, index21 bit[4:0] default: SYSTIN	Bank6, index22 bit[4:0] default: CPUTIN	Bank6, index23 bit[4:0] default: AUXTIN	Bank6, index24 bit[4:0] default: SYSTIN	Bank6, index25 bit[4:0] default: SYSTIN	Bank6, index26 bit[4:0] default: SYSTIN
Temperature reading (2's complement)	Bank0, index27	Bank1, index50 & index51 bit7	Bank2, index50 & index51 bit7	Bank6, index2B & index2E bit0	Bank6, index2C & index2E bit1	Bank6, index2D & index2E bit2
Temperature High Limit	Bank0, index39	Bank1, index55 & index56 bit7	Bank2, index55 & index56 bit7	Bank6, index72 & index74 bit7	Bank6, index77 & index79 bit7	Bank6, index7C & index7E bit7
Temperature Low Limit	Bank0, index3A	Bank1, index53 & index54 bit7	Bank2, index53 & index54 bit7	Bank6, index73 & index74 bit0	Bank6, index78 & index79 bit0	Bank6, index7D & index7E bit0

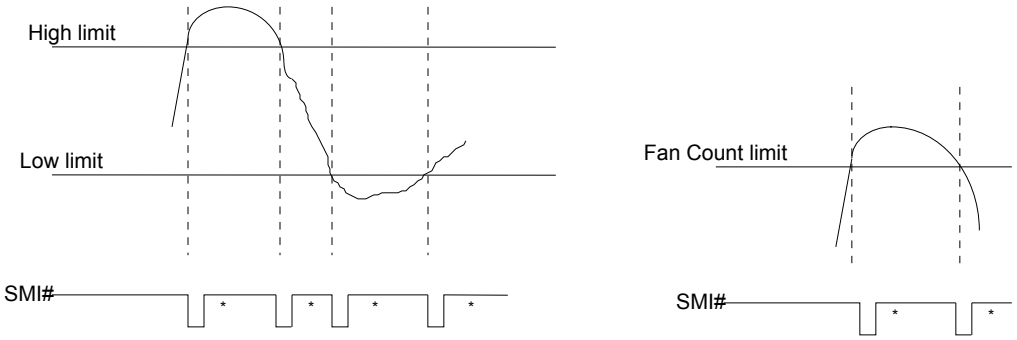
SMIOVT Relative Temperature Registers

8.10.1 SMI# Interrupt Mode

The SMI#/OVT# pin (pin.128) is a multi-function pin. It can be in HM_SMI# mode or in OVT# mode by setting Configuration Register CR24h, bit 2. In HM_SMI# mode, it can monitor voltages, fan counts, or temperatures.

8.10.2 Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage exceeds a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

Figure 8-18 SMI Mode of Voltage and Fan Inputs

8.10.3 Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

8.10.4 Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN, CPUTIN, and AUXTIN. These interrupts are divided into two parts, one for SYSTIN and the other for CPUTIN / AUXTIN.

8.10.4.1. Temperature Sensor 1 SMI# Interrupt (Default: SYSTIN)

The SMI# pin has four interrupt modes with Temperature Sensor 1.

(1) Shut-down Interrupt Mode

This mode is enabled by setting Bank0 Index 40h, bit 4 to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

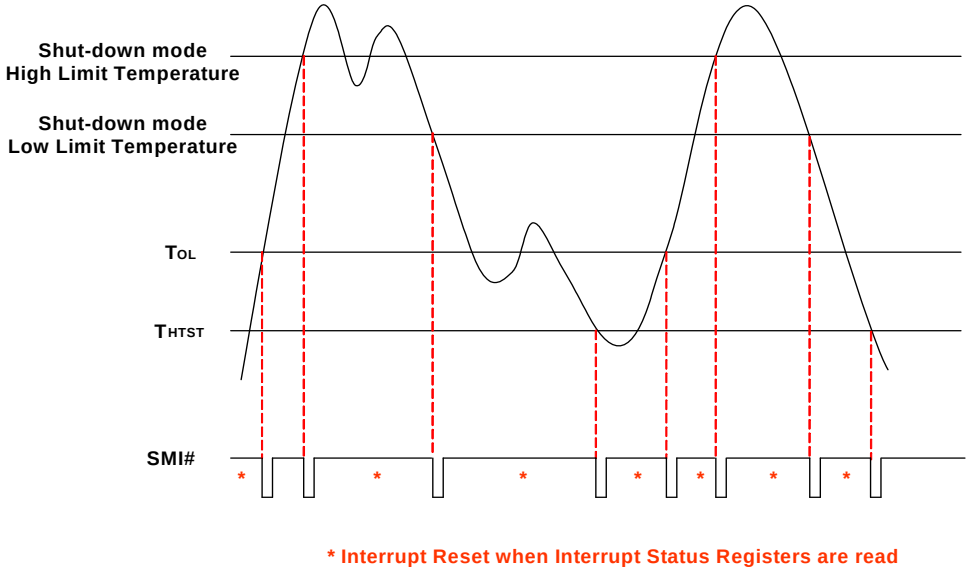
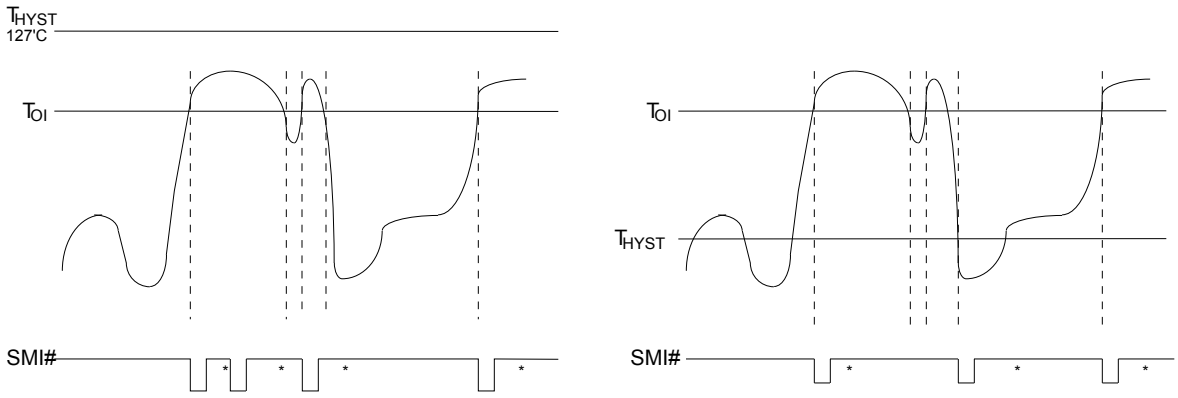


Figure 8-19 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C. This mode is enabled by setting Bank0 Index 40h, bit 4 to 0.

In this mode, the SMI# pin can create an interrupt as long as the current temperature exceeds T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode Two-Times Interrupt Mode

Figure 8-20 SMI Mode of SYSTIN I

(3) Two-Times Interrupt Mode

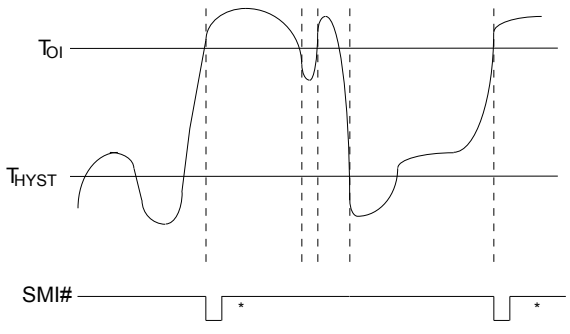
This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to zero. This mode is enabled by setting Bank0 Index 40h, bit 4 to 0.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(4) One-Time Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) lower than T_O and setting Bank0 Index 4Ch, bit 5 to one. This mode is enabled by setting Bank0 Index 40h, bit 4 to 0.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-21 SMI Mode of SYSTIN II

8.10.4.2. SMI# Interrupt of Temperature Sensor 2 (Default: CPUTIN) and Temperature Sensor 3 (Default: AUXTIN) and Temperature Sensor 4 (Default: SYSTIN) and Temperature Sensor 5 (Default: SYSTIN) and Temperature Sensor 6 (Default: SYSTIN).

The SMI# pin has 3 interrupt modes with Temperature Sensor 2~6.

(1) Shut-down Interrupt Mode

This mode is enabled by Bank0 Index 40h, bit5 to one for Temperature Sensor 2; Bank0 Index 40h, bit6 to one for Temperature Sensor 3; Bank6 Index 74h, bit1 to one for Temperature Sensor 4; Bank6 Index 79h, bit1 to one for Temperature Sensor 5 and Bank6 Index 7Eh, bit1 to one for Temperature Sensor 6.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

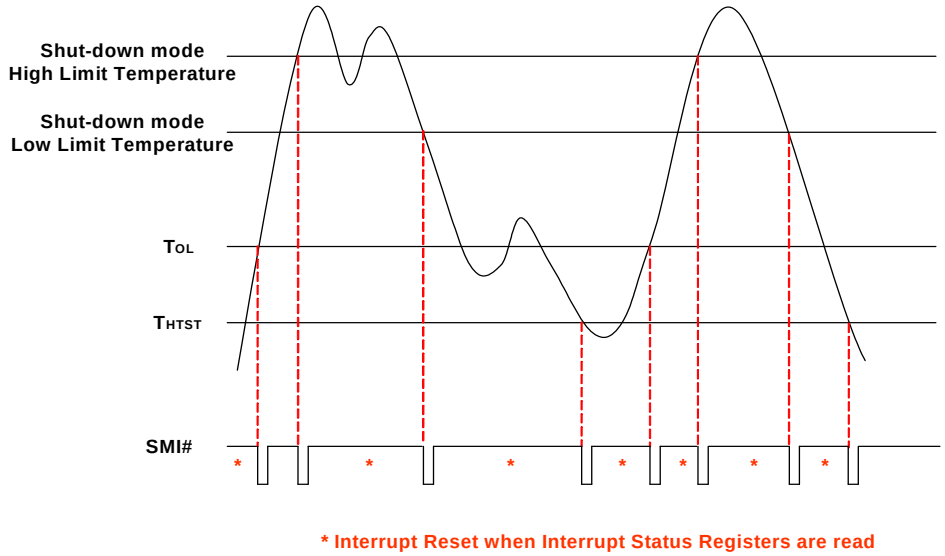


Figure 8-22 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature exceeds T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST}. This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.

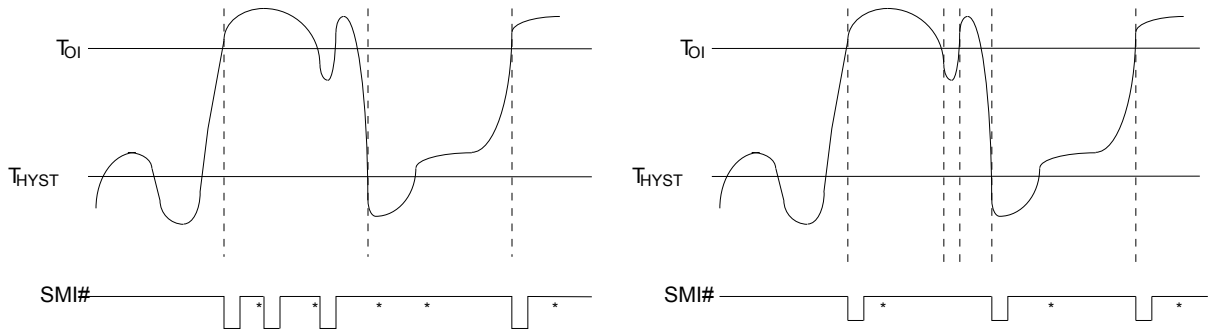


Figure 8-23 SMI Mode of CPUTIN

(3) Two-Times Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

Table 8-6 Relative Register of SMI functions

	SHUTDOWN MODE	COMPARATOR MODE	TWO-TIME INTERRUPT MODE	ONE-TIME INTERRUPT MODE
SMIOVT1	Bank0,Index40_Bit4 (EN_WS=1) Bank0,Index43 _Bit4(TIN=0) Bank0,Index46 _Bit3 (Shut = 0)	Bank0,Index43_Bit4 (TIN=0) Bank0,Index3A (Thyst = 8'h7F)	Bank0,Index43_Bit4 (TIN=0) Bank0,Index4C_Bit5 (EN_T1_One = 0)	Bank0,Index43_ Bit4 Bank0,Index4C_ Bit5
SMIOVT2	Bank0,Index40_Bit5 (EN_WS=1) Bank0,Index43_ Bit5(TIN=0) Bank0,Index46_ Bit 4 (Shut = 0)	Bank0,Index43_Bit5 (TIN=0) Bank0,Index4C_ Bit6 (T2T3_INT=1)	Bank0,Index43_ Bit5(TIN=0) Bank0,Index4C_ Bit6 (T2T3_INT=0)	
SMIOVT3	Bank0,Indx40_Bit6 (EN_WS=1) Bank0,Indx44_ Bit5(TIN=0) Bank0,Index46_ Bit 5 (Shut = 0)	Bank0,Indx44_Bit5 (TIN=0) Bank0,Indx4C_ Bit6 (T2T3_INT=1)	Bank0,Index44_ Bit5(TIN=0) Bank0,Indx4C_ Bit6 (T2T3_INT = 0)	
SMIOVT4	Bank6,Index74_Bit1 (EN_WS=1)	Bank4,Index40_Bit0 (TIN=0) Bank0,Index4C_Bit6	Bank4,Index40_Bit0 (TIN=0) Bank0,Index4C_Bit6	

	Bank4,Indx40_ Bit0(TIN=0) Bank4,Inex40_ Bit 3 (Shut = 0)	(T2T3_INT = 1)	(T2T3_INT = 0)	
SMIOVT5	Bank6,Index79_Bit1 (EN_WS=1) Bank4,Index40_Bit1 (TIN=0) Bank4,Index40_Bit4 (Shut = 0)	Bank4,Index40_Bit1 (TIN=0) Bank0,Index4C_Bit6 (T2T3_INT = 1)	Bank4,Index40_Bit1 (TIN=0) Bank0,Index4C_Bit6 (T2T3_INT = 0)	
SMIOVT6	Bank6,Index7E_Bit1 (EN_WS=1) Bank4,Inex40_Bit2 (TIN=0) Bank4,Index40_Bit5 (Shut = 0)	Bank4,Inex40_Bit2 (TIN=0) Bank0,Index4C_Bit6 (T2T3_INT = 1)	Bank4,Inex40_Bit2 (TIN=0) Bank0,Index4C_Bit6 (T2T3_INT = 0)	

Table 8-7 Relative Register of OVT functions

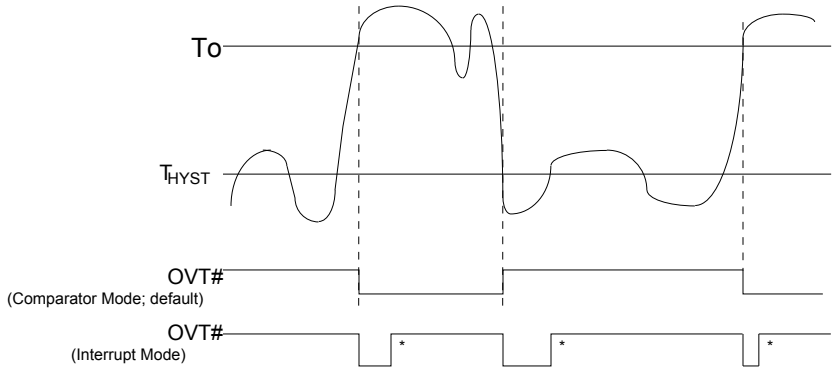
SMIOVT1	SMIOVT2	SMIOVT3
Bank0,Index18_Bit6=0 (Enable OVT output) **Bank0,Index18_Bit4** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank0, Index18_Bit0** **0:** Start to monitor the source of SMIOVT1 temperature. **1:** Stop monitoring the source of SMIOVT1 temperature.	**Bank1, Index52_Bit0** **0:** Start to monitor the source of SMIOVT2 temperature. **1:** Stop monitoring the source of SMIOVT2 temperature. **Bank 0, Inedex4C_Bit 3** **0:** Disable SMIOVT2 temperature sensor over temperature output **1:** Enable SMIOVT2 temperature sensor over temperature output **Bank 1, Index52_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 1, Index52_Bit 3~4** Number of faults to detect before setting OVT# output.	**Bank2, Index52_Bit0** **0:** Start to monitor the source of SMIOVT3 temperature. **1:** Stop monitoring the source of SMIOVT3 temperature. **Bank 0, Inedex4C_Bit 4** **0:** Disable SMIOVT3 temperature sensor over temperature output **1:** Enable SMIOVT3 temperature sensor over temperature output **Bank 2, Index52_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 2, Index52_Bit3~4** Number of faults to detect before setting OVT# output.
SMIOVT4	**SMIOVT5**	**SMIOVT6**

Bank6, Index28_Bit0 **0:** Start to monitor the source of SMIOVT4 temperature. **1:** Stop monitoring the source of SMIOVT4 temperature. **Bank 6, Inedex74_Bit 2** **0:** Disable SMIOVT4 temperature sensor over temperature output **1:** Enable SMIOVT4 temperature sensor over temperature output **Bank 6, Index28_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 6, Index28_Bit3~4** Number of faults to detect before setting OVT# output.	**Bank6, Index29_Bit0** **0:** Start to monitor the source of SMIOVT5 temperature. **1:** Stop monitoring the source of SMIOVT5 temperature. **Bank 6, Inedex79_Bit 2** **0:** Disable SMIOVT5 temperature sensor over temperature output **1:** Enable SMIOVT5 temperature sensor over temperature output **Bank 6, Index29_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 6, Index29_Bit3~4** Number of faults to detect before setting OVT# output.	**Bank6, Index2A_Bit0** **0:** Start to monitor the source of SMIOVT6 temperature. **1:** Stop monitoring the source of SMIOVT6 temperature. **Bank 6, Inedex7E_Bit 2** **0:** Disable SMIOVT6 temperature sensor over temperature output **1:** Enable SMIOVT6 temperature sensor over temperature output **Bank 6, Index2A_Bit 1** **0:** Comparator Mode **1:** Interrupt Mode **Bank 6, Index2A_Bit3~4** Number of faults to detect before setting OVT# output.

8.10.5 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR[24h], bit 2 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and OVT pin could be enabled to OVT output by Bank0 Index 18h, bit 6 for Temperature Sensor 1(default: SYSTIN); Bank1 Index 52h, bit 1 for Temperature Sensor 2(default: CPUTIN); Bank2 Index 52h, bit1 for Temperature Sensor 3(default: AUXTIN); Bank6 Index 28h, bit1 for Temperature Sensor 4(default: SYSTIN); Bank6 Index 29h, bit1 for Temperature Sensor 5(default: SYSTIN)and Bank6 Index 2Ah, bit1 for Temperature Sensor 6(default: SYSTIN).

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.



*Interrupt Reset when Temperature sensor registers are read

Figure 8-24 OVT# Modes of Temperature Inputs

If Bank0 Index 18h, bit 4, is set to zero, the OVT# pin is in comparator mode. In comparator mode, the OVT# pin can create an interrupt once the current temperature exceeds T_O and continues to create interrupts until the

temperature falls below T_{HYST}. The OVT# pin is asserted once the temperature has exceeded T_O and has not yet fallen below T_{HYST}.

If Bank0 Index 18h, bit 4, is set to one, the OVT# pin is in interrupt mode. In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

8.10.6 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case has been opened and possible tampered with. This feature must function even when there is no 3VSB power. Consequently, the power source for the circuit is from either Pin 99 (VBAT) or Pin 85 (3VSB). 3VSB is the default power source. If there is no 3VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, CASEOPEN0# or CASEOPEN1# (pin 100) must be pulled high by an externally pulled-up 2MΩ resistor that is connected to VBAT (pin 99). When the case is opened, CASEOPEN0# or CASEOPEN1# will be switched from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be read at the registers next time when the computer is powered. The CASEOPEN0# status will not be cleared unless CR[46h], bit 7, or CR[E6h] bit 5 at Logical Device A is set to “1” first and then to “0”. The CASEOPEN1# status will not be cleared unless CR[46h], bit 6, or CR[EEh] bit 0 at Logical Device A is set to “1” first and then to “0”.

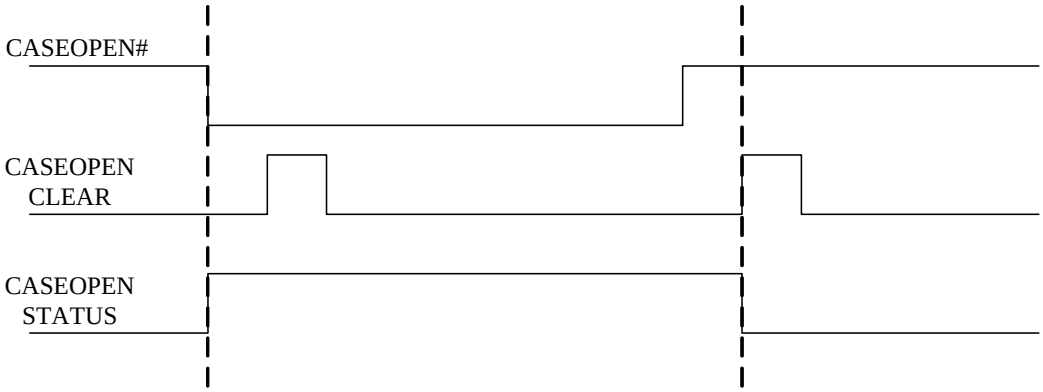


Figure 8-25 Caseopen Mechanism

8.11 Power Measurement

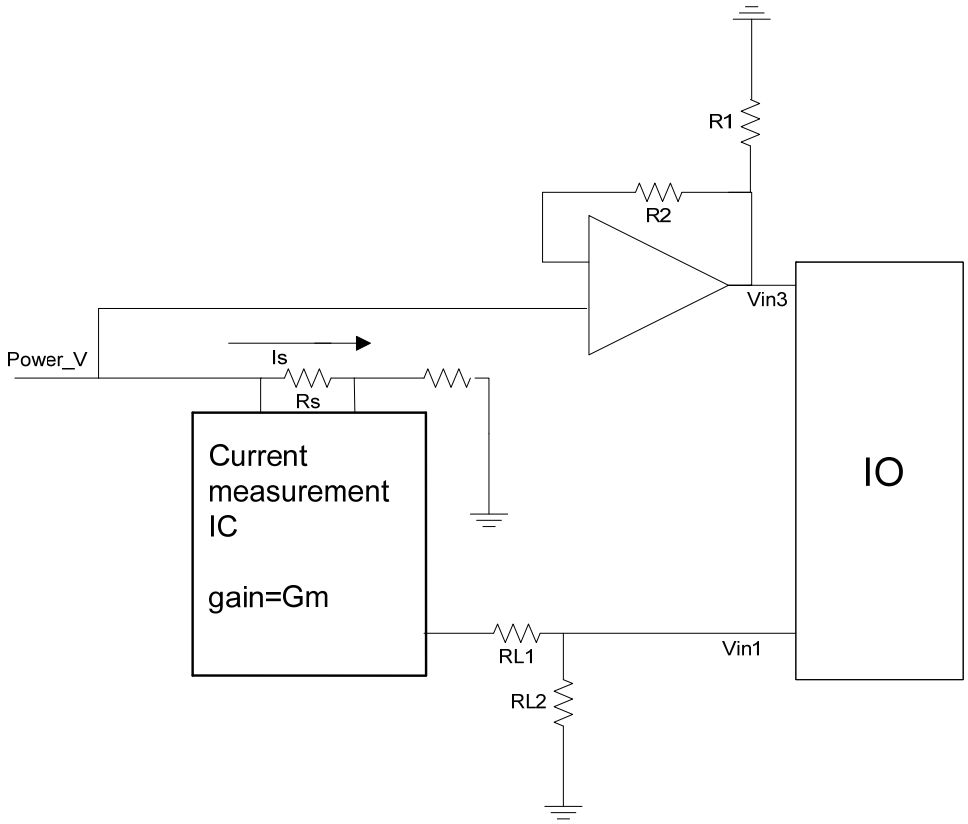


Figure 8-26 Power measurement architecture

This function will detect the voltage from current measurement IC on board and calculate the current and power. Fig 8.26 is the architecture. Vin3 ($Vin3 = Power_V \times \frac{R1}{R1+R2}$) and Vin1 ($Vin1 = Is \times Rs \times Gm \times RL2$) could not over 2.048. We suggest the ratio $\frac{R1}{R1+R2} = \frac{1}{15}$.

	HM Register	Note
Is	Bank4 Index 60h & Index 61h	Calculate by IO
POWER	Bank4 Index 62h & Index 63h	Calculate by IO
VIN	Bank4 Index 64h	Given by user
Rre	Bank4 Index 65h	Given by user Rreg=Rs*RL2*Gm
Reg_Ration_K	Bank4 Index 66h	Given by user Reg_Ration_K = (R1+R2)/(R1)
Power_Volt_En	Bank4 Index 66h	Given by user
POWER_V	Bank4 Index 67h	Calculate by IO or given by user depend on Power_Volt_En
Vin1	Bank0 Index 24h	Measure by IO

9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are "banked" with the bank number located at Bank0, index 04Eh.

9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/Write , Bit 7: Reserved

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED.**
6-0	**READ/WRITE.**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved (Power On default 0)	Address Pointer (Power On default 00h)						
	A6	A5	A4	A3	A2	A1	A0

9.2 Data Port (Port x6h)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

9.3 SYSFANOUT PWM Output Frequency Configuration Register – Index 00h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when SYSFANOUT is progarmmed for PWM output (i.e., Bank0, Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL1. SYSFANOUT PWM Input Clock Source Select.** This bit selects the clock source for PWM output frequency. Refer the Divisor table.
6-0	**PWM_SCALE1. SYSFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	**93.9KHz**	.....		
0000001	2	**46.95KHz**			
0000010	3	**31.3KHz**			
0000011	4	**23.47KHz**			
0000100	5	**18.78KHz**	0001111	16	**5.86KHz**
0000101	6	**15.65KHz**	0011111	32	**2.93KHz**
0000110	7	**13.41KHz**	0111111	64	**1.46KHz**
0000111	8	**11.73KHz**	1111111	128	**734Hz**

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	**1008Hz**	1000	**12**	**84Hz**
0001	2	**504Hz**	1001	**16**	**63Hz**
0010	3	**336Hz**	1010	**32**	**31.5Hz**
0011	4	**252Hz**	1011	**64**	**15.75Hz**
0100	5	**201Hz**	1100	**128**	**7.875Hz**
0101	6	**168Hz**	1101	**256**	**3.94Hz**
0110	7	**144Hz**	1110	**512**	**1.97Hz**
0111	8	**126Hz**	1111	**1024**	**0.98Hz**

9.4 SYSFANOUT Output Value Select Register – Index 01h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	FFh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is approx 2.048V.						Reserved	
This register could be programmed by Bank1, Index 09									

9.5 CPUFANOUT PWM Output Frequency Configuration Register – Index 02h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when CPUFANOUT is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL2. CPUFANOUT PWM Input Clock Source Select.** This bit selects the clock source for the PWM output. Refer the Divisor table.
6-0	**PWM_SCALE2. CPUFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency. If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**

MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	**93.9KHz**	.....		
0000001	2	**46.95KHz**			
0000010	3	**31.3KHz**			
0000011	4	**23.47KHz**			
0000100	5	**18.78KHz**	0001111	16	**5.86KHz**
0000101	6	**15.65KHz**	0011111	32	**2.93KHz**
0000110	7	**13.41KHz**	0111111	64	**1.46KHz**

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000111	8	**11.73KHz**	1111111	128	**734Hz**

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	**1008Hz**	1000	**12**	**84Hz**
0001	2	**504Hz**	1001	**16**	**63Hz**
0010	3	**336Hz**	1010	**32**	**31.5Hz**
0011	4	**252Hz**	1011	**64**	**15.75Hz**
0100	5	**201Hz**	1100	**128**	**7.875Hz**
0101	6	**168Hz**	1101	**256**	**3.94Hz**
0110	7	**144Hz**	1110	**512**	**1.97Hz**
0111	8	**126Hz**	1111	**1024**	**0.98Hz**

9.6 CPUFANOUT Output Value Select Register – Index 03h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	CPUFANOUT PWM Duty. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and creates a duty cycle of 0%.							
This register could be programmed by Bank2, Index 09									

9.7 SYSFANOUT Configuration Register I – Index 04h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED							SYSFANOUT_SEL
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-1	Reserved.
0	**SYSFANOUT Output Mode Selection.** 0: SYSFANOUT pin produces a PWM duty cycle output. 1: SYSFANOUT pin produces DC output. **(Default)**

9.8 Reserved Register – Index 05h ~ 0Fh (Bank 0)

9.9 AUXFANOUT PWM Output Frequency Configuration Register – Index 10h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL3	PWM_SCALE3						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT is programmed for PWM output (i.e. Bank0, Index 12h, bit 0 is 0)

BIT	DESCRIPTION
7	**PWM_CLK_SEL3. AUXFANOUT PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE3. AUXFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	**93.9KHz**	.....		
0000001	2	**46.95KHz**			
0000010	3	**31.3KHz**			
0000011	4	**23.47KHz**			
0000100	5	**18.78KHz**	0001111	16	**5.86KHz**
0000101	6	**15.65KHz**	0011111	32	**2.93KHz**
0000110	7	**13.41KHz**	0111111	64	**1.46KHz**
0000111	8	**11.73KHz**	1111111	128	**734Hz**

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	**1008Hz**	1000	**12**	**84Hz**
0001	2	**504Hz**	1001	**16**	**63Hz**
0010	3	**336Hz**	1010	**32**	**31.5Hz**
0011	4	**252Hz**	1011	**64**	**15.75Hz**
0100	5	**201Hz**	1100	**128**	**7.875Hz**
0101	6	**168Hz**	1101	**256**	**3.94Hz**
0110	7	**144Hz**	1110	**512**	**1.97Hz**
0111	8	**126Hz**	1111	**1024**	**0.98Hz**

9.10 AUXFANOUT Output Value Select Register – Index 11h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value							
DEFAULT	FFh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by Bank3, Index 09									

9.11 Reserved Register – Index 12-17h (Bank 0)

9.12 OVT# Configuration Register – Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	RESERVED	DIS_OVT1	RESERVED	OVT1_Mode	RESERVED			STOP
DEFAULT	0	1	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**DIS_OVT1.** 0: Enable SMIOVT1 OVT# output. (Default) 1: Disable temperature sensor SMIOVT1 over-temperature (OVT#) output.
5	**Reserved.**
4	**OVT1_Mode. SMIOVT1 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
3-1	**Reserved.**
0	**STOP.** **0: Monitor SMIOVT1 temperature source.** **1: Stop monitoring SMIOVT1 temperature source.**

9.13 Reserved Registers – Index 19h ~ 1Fh (Bank 0)

9.14 Value RAM — Index 20h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
20h	CPUVCORE reading
21h	VIN0 reading

ADDRESS A6-A0	DESCRIPTION
22h	AVCC reading
23h	3VCC reading
24h	VIN1 reading
25h	VIN2 reading
26h	VIN3 reading
27h	SMIOVT1 temperature source reading.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN0 High Limit
2Eh	VIN0 Low Limit
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN1 High Limit
34h	VIN1 Low Limit
35h	VIN2 High Limit
36h	VIN2 Low Limit
37h	VIN3 High Limit
38h	VIN3 Low Limit
39h	SMIOVT1 temperature sensor High Limit
3Ah	SMIOVT1 temperature sensor Hysteresis Limit

9.15 Configuration Register – Index 40h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	EN_WS2	EN_WS1	EN_WS	INT_CLEAR	RESERVED	SMI#ENABLE	START
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Initialization.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	**Output type of SMIOVT3:** 1: SMI# output type of SMIOVT Source3 temperature (Default: AUXTIN) is Shut-down Interrupt Mode. 0: Depond on the value of Bank0, Index 4C, bit6.
5	**Output type of SMIOVT2:** 1: SMI# output type of SMIOVT Source2 temperature (Default: CPUTIN) is Shut-down

BIT	DESCRIPTION
	Interrupt Mode. 0: Depond on the value of Bank0, Index 4C, bit6.
4	**Output type of SMIOVT3** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: Depond on the value of Bank0, Index 4C, bit5.
3	**INT_Clear.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	**Reserved.**
1	**SMI# Enable.** A one enables the SMI# Interrupt output. 1: Enable SMI# function (Deafult) 0: Disable SMI# function
0	**Start.** A one enables startup of monitoring operations. A zero puts the part in standby mode. **Note:** Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

9.16 Interrupt Status Register 1 – Index 41h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	SOURCE2 _ SMI	SOURCE1 _ SMI	3VCC	AVCC	VIN0	CPUVCORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN.** A one indicates the fan count limit of CPUFANIN has been exceeded.
6	**SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.
5	**SMIOVT2.** A one indicates the high limit of SMIOVT2 temperature has been exceeded. (CPUTIN is default temperature)
4	**SMIOVT1.** A one indicates the high limit of SMIOVT1 temperature has been exceeded. (SYSTIN is default temperature)
3	**3VCC.** A one indicates the high or low limit of 3VCC has been exceeded.
2	**AVCC (Pin 106).** A one indicates the high or low limit of AVCC has been exceeded.
1	**VIN0.** A one indicates the high or low limit of VIN0 has been exceeded.
0	**CPUVCORE.** A one indicates the high or low limit of CPUVCORE has been exceeded.

9.17 Interrupt Status Register 2 – Index 42h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	Reserved.	CASEOPEN1	SOURCE3 _ SMI	CASEOPEN0	AUXFANIN0	VIN2	VIN3	VIN1
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**CASEOPEN1.** A one indicates the case has been opened.
5	**SMIOVT3.** A one indicates the high limit of SMIOVT3 temperature has been exceeded. (AUXTIN is default temperature)
4	**CASEOPEN0.** A one indicates the case has been opened.
3	**AUXFANIN0.** A one indicates the fan count limit of AUXFANIN0 has been exceeded.
2	**VIN2.** A one indicates the high or low limit of VIN2 has been exceeded.
1	**VIN3.** A one indicates the high or low limit of VIN3 has been exceeded.
0	**VIN1.** A one indicates the high or low limit of VIN1 has been exceeded.

9.18 SMI# Mask Register 1 – Index 43h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	CPUTIN	SYSTIN	3VCC	AVCC	VIN0	CPUVCORE
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**CPUFANIN.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))
6	**SYSFANIN.**	
5	**SMIOVT2.**	
4	**SMIOVT1.**	
3	**3VCC.**	
2	**AVCC (Pin 106).**	
1	**VIN0.**	
0	**CPUVCORE.**	

9.19 SMI# Mask Register 2 – Index 44h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	AUXTIN	CASEOPEN0	AUXFANIN0	VIN3	VIN2	VIN1
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION

BIT	DESCRIPTION	
7	**TAR2.**	A one disables the corresponding interrupt status bit for the interrupt. (See Interrupt Status Register 2 – Index 42h (*Bank 0*))
6	**TAR1.**	
5	**SMIOVT3.**	
4	**CASEOPEN0.**	
3	**AUXFANIN0.**	
2	**VIN3.**	
1	**VIN2.**	
0	**VIN1.**	

9.20 Interrupt Status Register 4 – Index 45h (Bank 0)

Attribute: Read Clear

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VID	VID (Auto Clear)	AUX FANOUT	CPU FANOUT	SYS FANOUT	Shut_ SOURCE3_SMI	Shut_ SOURCE2_SMI	Shut_ SOURCE1_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**VID.** "1" indicates that the VIDI is on the flying.
6	**VID (Auto Clear).** "1" indicates that the VIDI is on the flying.
5	**AUXFANOUT.** "1" indicates that AUXFANOUT works for three minutes at the full fan speed.
4	**CPUFANOUT.** "1" indicates that CPUFANOUT works for three minutes at the full fan speed.
3	**SYSFANOUT.** "1" indicates that SYSFANOUT works for three minutes at the full fan speed.
2	**Shut_SOURCE3_SMI.** "1" indicates the high limit of SMIOVT_SOURCE3 temperature of SMI# Shut-down mode has been exceeded. (AUXTIN is default temperature)
1	**Shut_SOURCE2_SMI.** "1" indicates the high limit of SMIOVT _SOURCE2 temperature of SMI# Shut-down mode has been exceeded. (CPUTIN is default temperature)
0	**Shut_SOURCE1_SMI.** "1" indicates the high limit of SMIOVT _SOURCE1 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)

9.21 SMI# Mask Register 3 – Index 46h (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CASEOPEN CLEAR0	CASEOPEN CLEAR1	Shut_AUX	Shut_CPU	Shut_SYS	AUXFANIN2	AUXFANIN1	CASEOPEN1
DEFAULT	0	0	1	1	1	1	1	0

BIT	DESCRIPTION	
7	**CASEOPEN0 Clear Control.** Writing 1 to this bit will clear CASEOPEN status. This bit will be cleared itself. The function is the same as LDA, CR[E6h], bit 5.	
6	**CASEOPEN1 Clear Control.** Writing 1 to this bit will clear CASEOPEN status. This bit will be cleared itself. The function is the same as LDA, CR[E6h], bit 5**..**	
5	**Shut_SOURCE3_SMI**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 4 – Index 45h (Bank 0)).
4	**Shut_SOURCE2_SMI**	
3	**Shut_SOURCE1_SMI**	
2	**AUXFANIN2**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt.
1	**AUXFANIN1**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt
0	**CASEOPEN1**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt.

9.22 Reserved Register – Index 47h (Bank 0)

9.23 Serial Bus Address Register – Index 48h (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	SERIAL BUS ADDRESS						
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	**Reserved (Read Only).**
6-0	**Serial Bus Address <7:1>**

9.24 Reserved Register – Index 49h ~ 4Bh (Bank 0)

9.25 SMI/OVT Control Register1 – Index 4Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	T2ToT6_INT MODE	EN_T1 _ONE	DIS_ OVT3	DIS_ OVT2	OVTPOL	RESERVED	
DEFAULT	0	0	0	1	1	0	0	0

BIT	DESCRIPTION
7	**Reserved**

BIT	DESCRIPTION
6	**T2ToT6_INTMode.** 1: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Comparator Interrupt mode. 0: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Two-Times Interrupt mode. (Default)
5	**EN_T1_ONE.** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is One-Time Interrupt Mode. 0: SMI# output type is in Two-Times Interrupt Mode. (Default)
4	**DIS_OVT3.** 1: Disable SMIOVT Source3 temperature sensor (Default: AUXTIN) over-temperature (OVT) output. (Default) 0: Enable SMIOVT Source3 temperature OVT output through pin OVT#.
3	**DIS_OVT2.** 1: Disable SMIOVT Source2 temperature sensor (Default: CPUTIN) over-temperature (OVT) output. 0: Enable SMIOVT Source2 temperature OVT output through pin OVT#. (Default)
2	**OVTPOL (Over-temperature polarity).** 1: OVT# is active high. 0: OVT# is active low (Default).
1-0	**Reserved.**

9.26 FAN IN/OUT Control Register – Index 4Dh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	0	0	0	0	0	1	0	1

BIT	DESCRIPTION
7-4	**Reserved.**
3	**FANOPV2. CPUFANIN output value**, only if bit 2 is set to zero. 1: Pin 124 (CPUFANIN) generates a logic-high signal. 0: Pin 124 generates a logic-low signal. (Default)
2	**FANINC2. CPUFANIN Input Control.** 1: Pin 124 (CPUFANIN) acts as a fan tachometer input. (Default) 0: Pin 124 acts as a fan control signal, and the output value is set by bit 3.
1	**FANOPV1. SYSFANIN output value**, only if bit 0 is set to zero. 1: Pin 126 (SYSFANIN) generates a logic-high signal. 0: Pin 126 generates a logic-low signal. (Default)
0	**FANINC1. SYSFANIN Input Control.** 1: Pin 126 (SYSFANIN) acts as a fan tachometer input. (Default) 0: Pin 126 acts as a fan control signal, and the output value is set by bit 1.

9.27 Bank Select Register – Index 4Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	Reserved				BANK SEL2	BANK SEL1	BANK SEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**HBACS. HBACS – High Byte Access.** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.	
6	**Reserved.**	
5	**Reserved.**	
4	**Reserved.**	
3	**Reserved.**	
2	**BANKSEL2.**	Bank Select for Bank0 to Bank7. The Three-bit binary value corresponds to the bank number. For example, "010" selects bank2.
1	**BANKSEL1.**	
0	**BANKSEL0.**	

9.28 Nuvoton Vendor ID Register – Index 4Fh (Bank 0)

Attribute: Read Only
Size: 16 bits

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.29 Reserved Register – Index 50h ~ 57h (Bank 0)

9.30 Chip ID – Index 58h (Bank 0)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Nuvoton Chip ID number. Default C1h.

9.31 Reserved Register – Index 59h ~ 5Ch (Bank 0)

9.32 VBAT Monitor Control Register – Index 5Dh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				DIODES3	DIODES2	DIODES1	EN_VBAT_MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-4	**Reserved**
3	**DIODES 3. Sensor type selection for AUXTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
2	**DIODES 2. Sensor type selection for CPUTIN.** 1: Diode sensor. (default) 0: Thermistor sensor.
1	**DIODES 1. Sensor type selection for SYSTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
0	**EN_VBAT_MNT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor.

9.33 Current Mode Enable Register – Index 5Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				EN_AUXTIN CURRENT MODE	EN_CPUTIN CURRENT MODE	EN_SYSTIN CURRENT MODE	Reserved
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-4	**Reserved.**
3	**Enable AUXTIN Current Mode**. With AUXTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN by Current Mode. 0: Temperature sensing of AUXTIN depends on the setting of Index 5Dh. **(Default)**
2	**Enable CPUTIN Current Mode.** With CPUTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 2 = 1). 1: Temperature sensing of CPUTIN by Current mode. **(Default)** 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh.
1	**Enable SYSTIN Current Mode.** With SYSTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 1 = 1). 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh. **(Default)**
0	**Reserved.**

9.34 Reserved Register – Index 5F (Bank 0)

9.35 PORT 80 DATA INPUT Register – Index 60 (Bank 0)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	P80_IN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PORT 80 DATA INPUT**

9.36 Reserved Register – Index 61F ~ 62F (Bank 0)

9.37 Reserved Register – Index 65 (Bank 0)

9.38 Reserved Register – Index 66 (Bank 0)

9.39 Reserved register – Index 67h ~ 72h (Bank 0)

9.40 MONITOR TEMPERATURE 1 Register (Integer Value)- Index 73h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 1 [8:1]							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 1 [8:1]** SYSFANOUT fan control temperature reading. (Source is selected by Bank1, Index00 bit[4:0])

9.41 MONITOR TEMPERATURE 1 Register (Fractional Value)- Index 74h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 1 [0]**	**Reserved**						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**MONITOR TEMPERATURE 1 [0]** SYSFANOUT fan control temperature reading. (Source is selected by Bank1, Index00 bit[4:0])
6-0	**Reserved**

9.42 MONITOR TEMPERATURE 2 Register (Integer Value)- Index 75h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 2 [8:1]**							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 2 [8:1]** CPUFANOUT fan control temperature reading. (Source is selected by Bank2, Index00 bit[4:0])

9.43 MONITOR TEMPERATURE 2 Register (Fractional Value)- Index 76h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 2 [0]**	**Reserved**						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**MONITOR TEMPERATURE 2 [0]** CPUFANOUT fan control temperature reading. (Source is selected by Bank2, Index00 bit[4:0])
6-0	**Reserved**

9.44 MONITOR TEMPERATURE 3 Register (Integer Value)- Index 77h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 3 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 3 [8:1]** AUXFANOUT fan control temperature reading. (Source is selected by Bank3, Index00 bit[4:0])

9.45 MONITOR TEMPERATURE 3 Register (Fractional Value)- Index 78h (Bank 0)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 3 [0]	Reserved						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 3 [0]** AUXFANOUT fan control temperature reading. (Source is selected by Bank3, Index00 bit[4:0])
6-0	**Reserved.**

9.46 Reserved Register – Index 79h~ADh (Bank 0)

9.47 PECI Temperature Reading Enable for SMIOVT and SMART FAN Control Register – Index AEh (Bank 0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_PECI1	EN_PECI0

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**Reserved.**
1	**Enable PECI Agent1**
0	**Enable PECI Agent0**

9.48 BEEP Control Register 1 – Index B2h (Bank0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En3VSB_BP	EnVIN3_BP	EnVIN2_BP	EnVIN1_BP	En3VCC_BP	EnAVCC_BP	EnVIN0_BP	EnCPUVCORE_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En3VSB_BP** **1 : Enable 3VSB Beep function** **0 : Disable 3VSB Beep fuction**
6	**EnVIN3_BP** **1 : Enable VIN3 Beep function** **0 : Disable VIN3 Beep fuction**
5	**EnVIN2_BP** **1 : Enable VIN2 Beep function** **0 : Disable VIN2 Beep fuction**
4	**EnVIN1_BP** **1 : Enable VIN1 Beep function** **0 : Disable VIN1 Beep fuction**
3	**En3VCC_BP** **1 : Enable 3VCC Beep function** **0 : Disable 3VCC Beep fuction**
2	**EnAVCC_BP** **1 : Enable AVCC Beep function** **0 : Disable AVCC Beep fuction**
1	**EnVIN0_BP** **1 : Enable VIN0 Beep function** **0 : Disable VIN0 Beep fuction**
0	**EnCPUVCORE_BP** **1 : Enable CPUVCORE Beep function** **0 : Disable CPUVCORE Beep fuction**

9.49 BEEP Control Register 2 – Index B3h (Bank0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	User Mode	Reserved						EnVBAT_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**User control for Beep alarm** **1 : Enable** **0 : Disable**
6-1	**Reserved**
0	**EnVBAT_BP** **1 : Enable VBAT Beep function** **0 : Disable VBAT Beep fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.50 BEEP Control Register 3 – Index B4h (Bank0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	RESERVED	EnT6_BP	EnT5_BP	EnT4_BP	EnT3_BP	EnT2_BP	EnT1_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved**
0	**EnT6_BP** **1 : Enable SMIOVT6 Beep function** **0 : Disable SMIOVT6 Beep fuction**
0	**EnT5_BP** **1 : Enable SMIOVT5 Beep function** **0 : Disable SMIOVT5 Beep fuction**
0	**EnT4_BP** **1 : Enable SMIOVT4 Beep function** **0 : Disable SMIOVT4 Beep fuction**
0	**EnT3_BP** **1 : Enable SMIOVT3 Beep function** **0 : Disable SMIOVT3 Beep fuction**
0	**EnT2_BP** **1 : Enable SMIOVT2 Beep function** **0 : Disable SMIOVT2 Beep fuction**
0	**EnT1_BP**

BIT	DESCRIPTION
	1 : Enable SMIOVT1 Beep function **0 : Disable SMIOVT1 Beep fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.51 BEEP Control Register 4 – Index B5h (Bank0)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	En Caseopen1_BP	En Caseopen0_BP	En AUXFANIN2 _BP	En AUXFANIN1 _BP	En AUXFANIN0 _BP	En CPUFANIN _BP	En SYSFANIN _BP	En_Beep
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En Caseopen1_BP** **1 : Enable Caseopen1 Beep function** **0 : Disable Caseopen1 Beep fuction**
6	**En Caseopen0_BP** **1 : Enable Caseopen0_bp Beep function** **0 : Disable Caseopen0_bp Beep fuction**
5	**En AUXFANIN2_BP** **1 : Enable AUXFANIN2 Beep function** **0 : Disable AUXFANIN2 Beep fuction**
4	**En AUXFANIN1_BP** **1 : Enable AUXFANIN1 Beep function** **0 : Disable AUXFANIN1 Beep fuction**
3	**En AUXFANIN0_BP** **1 : Enable AUXFANIN0 Beep function** **0 : Disable AUXFANIN0 Beep fuction**
2	**En CPUFANIN _BP** **1 : Enable CPUFANIN Beep function** **0 : Disable CPUFANIN Beep fuction**
1	**En SYSFANIN _BP** **1 : Enable SYSFANIN Beep function** **0 : Disable SYSFANIN Beep fuction**
0	**Enable Beep Function:** **1 : Enable Beep Function** **0 : Disable Beep Fuction**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.52 SYSFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		SYSFAN SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to SYSFANOUT Stop Value (Bank1, index05h) at most if necessary. (This function is for SMART FAN I and III.)
6-5	**Reserved**
4-0	**SYSFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as SYSFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.53 SYSFAN Target Temperature Register / SYSFANIN Target Speed_L Register – Index 01h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN Target Temperature / SYSFANIN Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	SYSFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.54 SYSFAN MODE Register / SYSFAN TOLERRANCE Register – Index 02h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN MODE				Reserved	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**SYSFANOUT Mode Select.** 0000: SYSFANOUT is in Manual Mode. **(Default)** 0001: SYSFANOUT is in Thermal Cruise Mode. 0010: SYSFANOUT is in Speed Cruise Mode. 0100: SYSFANOUT is in SMART FAN IV Mode.
3	**Reserved**
2-0	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L.

9.55 SYSFANOUT Step Up Time Register – Index 03h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.56 SYSFANOUT Step Down Time Register – Index 04h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Down Time							

DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.57 SYSFANOUT Stop Value Register – Index 05h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.58 SYSFANOUT Start-up Value Register – Index 06h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.59 SYSFANOUT Stop Time Register – Index 07h (Bank 1)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In SMART FAN™ mode, this register determines the amount of time it takes SYSFANOUT value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:
The units are intervals of 0.4 second. The default time is 4 seconds.

9.60 Reserved Register – Index 08h (Bank 1)

9.61 SYSFANOUT Output Value Select Register – Index 09h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is approx 2.048V.							Reserved

9.62 SYSFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	SYSFANIN TOL_H			SYSFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	SYSFANIN Tolerance_H [5:3]
3-0	SYSFANIN Target Speed_H [11:8]

9.63 Reserved Register – Index 0Dh (Bank 1)

9.64 SMART FAN IV SYSFANOUT STEP Register – Index 20h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	Reserved							En_SYSFANOUT_STEP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_SYSFANOUT_STEP** 0: Disable SMART FAN IV has Stepping SYSFANOUT. (default) 1: Enable SMART FAN IV has Stepping SYSFANOUT.

9.65 SYSFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.66 SYSFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.67 SYSFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.68 SYSFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.69 SYSFAN (SMART FAN™ IV) DC/PWM 1 Register – Index 27h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 1 Register.

9.70 SYSFAN (SMART FAN™ IV) DC/PWM 2 Register – Index 28h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 2 Register.

9.71 SYSFAN (SMART FAN™ IV) DC/PWM 3 Register – Index 29h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION

7-0	SYSFAN (SMART FAN™ IV) DC/PWM 3 Register.

9.72 SYSFAN (SMART FAN™ IV) DC/PWM 4 Register – Index 2Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 4 Register.

9.73 Reserved Register – Index 2Bh~30h (Bank 1)

9.74 SYSFAN 3-Wire Enable Register – Index 31h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_SYS_3WFAN
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_SYS_3WFAN (SYSFAN type setting)** 0: 4-wire fan 1: 3-wire fan

9.75 Reserved Register – Index 32h ~ 34h(Bank 1)

9.76 SYSFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Critical Temperature Register.

9.77 Reserved Register – Index 36h ~ 37h (Bank 1)

9.78 SYSFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SYSFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	SYSFANOUT Critical Temperature Tolerance

9.79 Weight value Configuration Register – Index 39h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_SYSFAN_WEIGHT	Reserved		SYS_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_SYSFAN_WEIGHT.** 0: Disable Weight Value Control for SYSFAN. 1: Enable Weight Value Control for SYSFAN.
6-5	**Reserved**
4-0	**SYSFAN Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as SYSFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SYSFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SYSFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SYSFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SYSFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SYSFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source.

BIT	DESCRIPTION
	1 0 0 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SYSFAN monitoring source.

9.80 SYSFANOUT Temperature Step Register – Index 3Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Step (SYS_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Temperature Step**

9.81 SYSFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Step Tolerance (SYS_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Temperature Step Tolerance**

9.82 SYSFANOUT Weight Step Register – Index 3Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Weight Step (SYS_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**SYSFANOUT Weight Step**

9.83 SYSFANOUT Temperature Base Register – Index 3Dh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Base (SYS_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	SYSFANOUT Temperature Base

9.84 SYSFANOUT Temperature Fan Duty Base Register – index 3Eh (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Temperature Base (SYS_FC_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	SYSFANOUT Start point of Fan Duty increasing

9.85 Reserved Register – Index 3Fh (Bank 1)

9.86 Reserved Register – Index 40h (Bank 1)

9.87 Reserved Register – Index 41h (Bank 1)

9.88 Reserved Register – Index 42h ~ 44h (Bank 1)

9.89 Reserved Register – Index 45h (Bank 1)

9.90 Reserved Register – Index 46h (Bank 1)

9.91 Reserved Register – Index 49h ~ 4Fh (Bank1)

9.92 SMIOVT2 Temperature Source (High Byte) Register – Index 50h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION

7-0	**Temperature <8:1> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.93 SMIOVT2 Temperature Source (Low Byte) Register – Index 51h (Bank 1)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	**Temperature <0> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.94 SMIOVT2 Temperature Source Configuration Register – Index 52h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.** This bit should be set to zero.
4-3	**Fault.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**Reserved.** This bit should be set to zero.
1	**OVTMOD. SMIOVT2 Mode Select.** 0 : Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP.** 0: Monitor SMIOVT2 temperature source. 1: Stop monitoring SMIOVT2 temperature source.

9.95 SMIOVT2 Temperature Source Hysteresis (High Byte) Register – Index 53h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and

BIT	DESCRIPTION
	the default is 75°C.

9.96 SMIOVT2 Temperature Source Hysteresis (Low Byte) Register – Index 54h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**THYST<0>. Hysteresis temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.97 SMIOVT2 Temperature Source Over-temperature (High Byte) Register – Index 55h (Bank1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.98 SMIOVT2 Temperature Source Over-temperature (Low Byte) Register – Index 56h (Bank 1)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TOVF<0>. Over-temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.99 Reserved Register – Index 57h ~ 7Fh (Bank 1)

9.100 CPUFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		CPUFAN SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to CPUFANOUT Stop Value (Bank2, index05h) at most if necessary. (This function is for SMART FAN I and III.)
6-5	**Reserved**
4-0	**CPUFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as CPUFAN monitoring source. 0 0 0 1 0: Select **CPUTIN** as CPUFAN monitoring source. (Default) 0 0 0 1 1: Select **AUXTIN** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as CPUFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as CPUFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as CPUFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as CPUFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as CPUFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as CPUFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as CPUFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as CPUFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as CPUFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as CPUFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as CPUFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as CPUFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as CPUFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as CPUFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as CPUFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as CPUFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as CPUFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as CPUFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as CPUFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.101 CPUFAN Target Temperature Register / CPUFANIN Target Speed_L Register – Index 01h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	CPUFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	CPUFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.102 CPUFAN MODE Register / CPUFAN TOLERRANCE Register – Index 02h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN MODE				Reserved	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-4	**CPUFANOUT Mode Select.** 0000: CPUFANOUT is in Manual Mode. (Default) 0001: CPUFANOUT is in Thermal Cruise Mode. 0010: CPUFANOUT is in Speed Cruise Mode. 0100: CPUFANOUT is in SMART FAN IV Mode.
3	**Reserved**
2-0	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L.

9.103 CPUFANOUT Step Up Time Register – Index 03h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.104 CPUFANOUT Step Down Time Register – Index 04h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.105 CPUFANOUT Stop Value Register – Index 05h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the CPUFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.106 CPUFANOUT Start-up Value Register – Index 06h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, CPUFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.107 CPUFANOUT Stop Time Register – Index 07h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In SMART FAN™ mode, this register determines the amount of time it takes CPUFANOUT value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.108 Reserved Register – Index 08h (Bank 2)

9.109 CPUFANOUT Output Value Select Register – Index 09h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	Depends on strapping pin – Pin.34 FAN_SET							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output Only	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.110 CPUFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	CPUFANIN TOL_H			CPUFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	CPUFANIN Tolerance_H [5:3]
3-0	CPUFANIN Target Speed_H [11:8]

9.111 Reserved Register – Index 0Dh (Bank 2)

9.112 SMART FAN IV CPUFANOUT STEP Register – Index 20h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_CPUFANOUT_STEP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

7-1	**Reserved**
0	**En_CPUFANOUT_STEP** 0: Disable SMART FAN IV has Stepping CPUFANOUT. (default) 1: Enable SMART FAN IV has Stepping CPUFANOUT.

9.113 CPUFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.114 CPUFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.115 CPUFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.116 CPUFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	CPUFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	0	1	0	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.117 CPUFAN (SMART FAN™ IV) DC or DUTY_SMF4 PWM1 Register – Index 27h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) DC/ DUTY_SMF4 PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) DC/ DUTY_SMF4 PWM1 Register.

9.118 CPUFAN (SMART FAN™ IV) DC or DUTY_SMF4 PWM2 Register – Index 28h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) DC/DUTY_SMF4 PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) DC/DUTY_SMF4 PWM2 Register.

9.119 CPUFAN (SMART FAN™ IV) DC or DUTY_SMF4 PWM3 Register – Index 29h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) DC/ DUTY_SMF4 PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) DC/DUTY_SMF4 PWM3 Register.

9.120 CPUFAN (SMART FAN™ IV) DC or DUTY_SMF4 PWM4 Register – Index 2Ah (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) DC/ DUTY_SMF4 PWM4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) DC/DUTY_SMF4 PWM4 Register.

9.121 Reserved Register – Index 2Dh~ 30h (Bank 2)

9.122 CPUFAN 3-Wire FAN Enable Register – Index 31h (Bank 2)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_CPU_3WFAN
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_CPU_3WFAN (CPUFAN type setting)** 0: 4-wire fan 1: 3-wire fan

9.123 Reserved Register – Index 32h ~ 34h(Bank 2)

9.124 CPUFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Critical Temperature Register.

9.125 Reserved Register – Index 36h ~ 37h (Bank 2)

9.126 CPUFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					CPUFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**CPUFANOUT Critical Temperature Tolerance**

9.127 Weight value Configuration Register – Index 39h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_CPUFAN_ WEIGHT	Reserved		CPU_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_CPUFAN_WEIGHT.** 0: Disable Weight Value Control for CPUFAN. 1: Enable Weight Value Control for CPUFAN.
6-5	**Reserved**
4-0	**CPUFAN Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as CPUFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as CPUFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER** as CPUFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as CPUFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as CPUFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as CPUFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as CPUFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as CPUFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as CPUFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as CPUFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as CPUFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as CPUFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as CPUFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as CPUFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as CPUFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as CPUFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as CPUFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as CPUFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as CPUFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as CPUFAN monitoring source.

BIT	DESCRIPTION
	1 0 1 0 1: Select **PCH_DIM3_TEMP** as CPUFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as CPUFAN monitoring source.

9.128 CPUFANOUT Temperature Step Register – Index 3Ah (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step (CPU_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step**

9.129 CPUFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step Tolerance**

9.130 CPUFANOUT Weight Step Register – Index 3Ch (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Weight Step (CPU_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Weight Step**

9.131 CPUFANOUT Temperature Base Register – Index 3Dh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_TEMP_BASE)							

DEFAULT	0

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Base**

9.132 CPUFANOUT Temperature Fan Duty Base Register – Index 3Eh (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_FC_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Start point of Fan Duty increasing**

9.133 Reserved Register – Index 3Fh (Bank 2)

9.134 Reserved Register – Index 40h (Bank 2)

9.135 Reserved Register – Index 41h (Bank 2)

9.136 Reserved Register – Index 42h ~ 44h (Bank 2)

9.137 Reserved Register – Index 45h (Bank 2)

9.138 Reserved Register – Index 46h (Bank 2)

9.139 Reserved Register – Index 49h ~ 4Fh (Bank2)

9.140 SMIOVT3 Temperature Source (High Byte) Register – Index 50h (Bank 2)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**TEMP<8:1> (default: AUXTIN temperature source).** The nine-bit value is in units of 0.5°C.

9.141 SMIOVT3 Temperature Source (Low Byte) Register – Index 51h (Bank 2)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	**Temperature <0> (default: AUXTIN temperature source).** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.142 SMIOVT3 Temperature Source Configuration Register – Index 52h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.** This bit should be set to zero.
4-3	**Fault.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**Reserved.** This bit should be set to zero.
1	**OVTMOD. SMIOVT3 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP.** 0: Monitor SMIOVT3 temperature source. 1: Stop monitoring SMIOVT3 temperature source.

9.143 SMIOVT3 Temperature Source Hysteresis (High Byte) Register – Index 53h (Bank 2)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.144 SMIOVT3 Temperature Source Hysteresis (Low Byte) Register – Index 54h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**THYST<0>. Hysteresis temperature, bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.145 SMIOVT3 Temperature Source Over-temperature (High Byte) Register – Index 55h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Over-temperature, bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.146 SMIOVT3 Temperature Source Over-temperature (Low Byte) Register – Index 56h (Bank 2)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TOVF<0>. Over-temperature, bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**Reserved.**

9.147 Reserved Register – Index 57h ~ 7Fh (Bank 2)

9.148 AUXFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT Stop Value (Bank3, index05h) at most if necessary. (This function is for SMART FAN I and III.)
6-5	**Reserved**
4-0	**AUXFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as AUXFAN monitoring source. (Default) 0 0 1 0 0: Select **SMBUSMASTER 0** as AUXFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as AUXFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as AUXFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as AUXFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as AUXFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as AUXFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as AUXFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as AUXFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as AUXFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as AUXFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as AUXFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as AUXFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as AUXFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as AUXFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as AUXFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as AUXFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as AUXFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as AUXFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.149 AUXFAN Target Temperature Register / AUXFANIN Target Speed_L Register – Index 01h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN Target Temperature / AUXFANIN Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.150 AUXFAN MODE Register / AUXFAN TOLERRANCE Register – Index 02h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN MODE				Reseved	Tolerance of AUXFAN Target Temperature or AUXFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT Mode Select.** 0000: AUXFANOUT is in Manual Mode. **(Default)** 0001: AUXFANOUT is in Thermal Cruise Mode. 0010: AUXFANOUT is as Fan Speed Cruise Mode. 0100: AUXFANOUT is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN Target Temperature or AUXFANIN Target Speed_L.

9.151 AUXFANOUT Step Up Time Register – Index 03h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.152 AUXFANOUT Step Down Time Register – Index 04h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value Step Down Time							

DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.153 AUXFANOUT Stop Value Register – Index 05h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.154 AUXFANOUT Start-up Value Register – Index 06h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan.

9.155 AUXFANOUT Stop Time Register – Index 07h (Bank 3)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In SMART FAN™ mode, this register determines the amount of time it takes AUXFANOUT value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.156 Reserved Register – Index 08h (Bank 3)

9.157 AUXFANOUT Output Value Select Register – Index 09h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Value							
DEFAULT	1	1	1	1	1	1	1	1

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.158 AUXFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN TOL_H			AUXFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN Tolerance_H [5:3]
3-0	AUXFANIN Target Speed_H [11:8]

9.159 Reserved Register – Index 0Dh (Bank 3)

9.160 SMART FAN IV AUXFANOUT STEP Register – Index 20h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUXFANOUT_STEP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUXFANOUT_STEP** 0: Disable SMART FAN IV has Stepping AUXFANOUT. (default) 1: Enable SMART FAN IV has Stepping AUXFANOUT.

9.161 AUXFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.162 AUXFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.163 AUXFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.164 AUXFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.165 AUXFAN (SMART FAN™ IV) DC/PWM 1 Register – Index 27h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) DC/PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) DC/PWM 1 Register.

9.166 AUXFAN (SMART FAN™ IV) DC/PWM 2 Register – Index 28h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) DC/PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) DC/PWM 2 Register.

9.167 AUXFAN (SMART FAN™ IV) DC/PWM 3 Register – Index 29h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) DC/PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) DC/PWM 3 Register.

9.168 AUXFAN (SMART FAN™ IV) DC/PWM 4 Register – Index 2Ah (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) DC/PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) DC/PWM 4 Register.

9.169 Reserved Register – Index Index 2Dh~ 30h (Bank 3)

9.170 AUXFAN 3-Wire Enable Register – Index 31h (Bank 3)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX_3WFAN
DEFAULT	0		0					0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX_3WFAN (AUXFAN type setting)** 0: 4-wire fan 1: 3-wire fan

9.171 Reserved Register – Index 32h ~ 34h(Bank 3)

9.172 AUXFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN (SMART FAN™ IV) Critical Temperature Register

9.173 Reserved Register – Index 36h ~ 37h (Bank 3)

9.174 AUXFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT Critical Temperature Tolerance		

DEFAULT	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT Critical Temperature Tolerance**

9.175 Weight value Configuration Register – Index 39h (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	EN_AUXFAN_WEIGHT	Reserved		AUX_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_AUXFAN_WEIGHT.** 0: Disable Weight Value Control for AUXFAN. 1: Enable Weight Value Control for AUXFAN.
6-5	**Reserved**
4-0	**AUXFAN Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as AUXFAN monitoring source. 0 0 0 1 1: Select **AUXTIN** as AUXFAN monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as AUXFAN monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as AUXFAN monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as AUXFAN monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as AUXFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as AUXFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as AUXFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as AUXFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as AUXFAN monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as AUXFAN monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as AUXFAN monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as AUXFAN monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as AUXFAN monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as AUXFAN monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as AUXFAN monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as AUXFAN monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as AUXFAN monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as AUXFAN monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as AUXFAN monitoring source.

9.176 AUXFANOUT Temperature Step Register – Index 3Ah (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Temperature Step (AUX_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT Temperature Step**

9.177 AUXFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Temperature Step Tolerance (AUX_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT Temperature Step Tolerance**

9.178 AUXFANOUT Weight Step Register – Index 3Ch (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Weight Step (AUX_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT Weight Step**

9.179 AUXFANOUT Temperature Base Register – Index 3Dh (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Temperature Base (AUX_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION

7-0	**AUXFANOUT Temperature Base**

9.180 AUXFANOUT Temperature Fan Duty Base Register – Index 3Eh (Bank 3)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT Temperature Base (AUX_FC_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**AUXFANOUT Start point of Fan Duty increasing**

9.181 Reserved Register – Index 3Fh (Bank 3)

9.182 Reserved Register – Index 40h (Bank 3)

9.183 Reserved Register – Index 41h (Bank 3)

9.184 Reserved Register – Index 42h ~ 44h (Bank 3)

9.185 Reserved Register – Index 45h (Bank 3)

9.186 Reserved Register – Index 46h (Bank 3)

9.187 Reserved Register – Index 47h ~ 7Fh (Bank3)

9.188 PCH_CHIP_CPU_MAX_TEMP Register – Index 00h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_CPU_MAX_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_CPU_MAX_TEMP:** The maximum temperature in absolute degree C, of the CPU and MCH.

9.189 PCH_CHIP_TEMP Register – Index 01h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_TEMP** The IBX_CHIP temperature in degree C.

9.190 PCH_CPU_TEMP_H Register – Index 02h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CPU_TEMP_H** The CPU temperature in degree C. (Integer Part)

9.191 PCH_CPU_TEMP_L Register – Index 03h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_L						Reserved	Reading _Flag
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**PCH_CPU_TEMP_L** The CPU temperature in degree C. (Fractional Part)
1	**Reserved**
0	**Reading_Flag:** If there is an error when the IBX read the data from the CPU, then Bit0 is set to '1'.

9.192 PCH_MCH_TEMP Register – Index 04h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_MCH_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**PCH_MCH_TEMP** The MCH temperature in degree C.

9.193 PCH_DIM0_TEMP Register – Index 05h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM0_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM0_TEMP** The DIM0 temperature in degree C.

9.194 PCH_DIM1_TEMP Register – Index 06h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM1_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM1_TEMP** The DIM1 temperature in degree C.

9.195 PCH_DIM2_TEMP Register – Index 07h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM2_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM2_TEMP** The DIM2 temperature in degree C.

9.196 PCH_DIM3_TEMP Register – Index 08h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_DIM3_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_DIM3_TEMP** The DIM3 temperature in degree C.

9.197 PCH_TSI0_TEMP_H Register – Index 09h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI0_TEMP_H** The TSI High-Byte temperature in degree C.

9.198 PCH_TSI0_TEMP_L Register – Index 0Ah (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI0_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.199 PCH_TSI1_TEMP_H Register – Index 0Bh (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI1_TEMP_H** The TSI High-Byte temperature in degree C.

9.200 PCH_TSI1_TEMP_L Register – Index 0Ch (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	PCH_TSI1_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI1_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.201 PCH_TSI2_TEMP_H Register – Index 0Dh (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI2_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI2_TEMP_H** The TSI High-Byte temperature in degree C.

9.202 PCH_TSI2_TEMP_L Register – Index 0Eh (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI2_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI2_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.203 PCH_TSI3_TEMP_H Register – Index 0Fh (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI3_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI3_TEMP_H** The TSI High-Byte temperature in degree C.

9.204 PCH_TSI3_TEMP_L Register – Index 10h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI3_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI3_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.205 PCH_TSI4_TEMP_H Register – Index 11h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI4_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI4_TEMP_H** The TSI High-Byte temperature in degree C.

9.206 PCH_TSI4_TEMP_L Register – Index 12h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI4_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI4_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.207 PCH_TSI5_TEMP_H Register – Index 13h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI5_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**PCH_TSI5_TEMP_H** The TSI High-Byte temperature in degree C.

9.208 PCH_TSI5_TEMP_L Register – Index 14h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI5_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI5_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.209 PCH_TSI6_TEMP_H Register – Index 15h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI6_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI6_TEMP_H** The TSI High-Byte temperature in degree C.

9.210 PCH_TSI6_TEMP_L Register – Index 16h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI6_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI6_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.211 PCH_TSI7_TEMP_H Register – Index 17h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	PCH_TSI7_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI7_TEMP_H** The TSI High-Byte temperature in degree C.

9.212 PCH_TSI7_TEMP_L Register – Index 18h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI7_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI7_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.213 ByteTemp_H Register – Index 19h (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_H** The TSI Byte format High-Byte temperature in degree C.

9.214 ByteTemp_L Register – Index 1Ah (Bank 4)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_L							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp_L** The TSI Byte format Low-Byte temperature in degree C.

9.215 Reserved Register – Index 1Bh ~ 22h (Bank 4)

9.216 VIN0 High Limit Compared Voltage Register – Index 23h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 High Limit Compared Voltage (VIN0_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**VIN0 High Limit Compared Voltage.** Default: 0x96h (1.2V)

9.217 VIN0 Low Limit Compared Voltage Register – Index 24h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 Low Limit Compared Voltage (VIN0_LimtH)							
DEFAULT	0	1	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	**VIN0 Low Limit Compared Voltage.** Default: 0x64h (0.8V)

9.218 VIN1 High Limit Compared Voltage Register – Index 25h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 High Limit Compared Voltage (VIN1_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**VIN1 High Limit Compared Voltage.** Default: 0x96h (1.2V)

9.219 VIN1 Low Limit Compared Voltage Register – Index 26h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 Low Limit Compared Voltage (VIN1_LimtH)							
DEFAULT	0	1	1	0	0	1	0	0

BIT	DESCRIPTION

7-0	**VIN1 Low Limit Compared Voltage.** Default: 0x64h (0.8V)

9.220 AVCC High Limit Compared Voltage Register – Index 27h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AVCC High Limit Compared Voltage (AVCC _LimtH)							
DEFAULT	1	1	1	0	0	0	0	1

BIT	DESCRIPTION
7-0	**AVCC High Limit Compared Voltage.** Default: 0xE1h (1.8V *2)

9.221 AVCC Low Limit Compared Voltage Register – Index 28h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AVCC Low Limit Compared Voltage (AVCC_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**AVCC Low Limit Compared Voltage (AVCC_LimtH).** Default: 0x96h (1.2V *2)

9.222 Reserved Register – Index 29h ~ 3Fh (Bank 4)

9.223 SMI_TEMP4-6 SMI# Mask Register - Index 40h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		SMSK TEMP_T6_Shut	SMSK TEMP_T5_Shut	SMSK TEMP_T4_Shut	SMSK TEMP_T6	SMSK TEMP_T5	SMSK TEMP_T4
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7-6	**Reserved.**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 4 – Index 45h (*Bank 0*))
5	**Shut_SOURCE6_SMI**	
4	**Shut_SOURCE5_SMI**	
3	**Shut_SOURCE4_SMI**	
2	**SMIOVT6**	
1	**SMIOVT5**	
0	**SMIOVT4**	

9.224 SMI_TEMP4-6 Interrupt Status Register - Index 41h (Bank 4)

Attribute: Read Clear
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	STS_TEMP_ Shut_T6	STS_TEMP_ Shut_T5	STS_TEMP_ Shut_T4	Reserved	STS_ TEMP_T6	STS_ TEMP_T5	STS_ TEMP_T4
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**Shut_SOURCE6_SMI** A one indicates the high limit of SMI_SOURCE6 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)
5	**Shut_SOURCE5_SMI** A one indicates the high limit of SMI_SOURCE5 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)
4	**Shut_SOURCE4_SMI** A one indicates the high limit of SMI_SOURCE4 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)
3	**Reserved.**
2	**SMIOVT6** A one indicates the high limit of SMI SOURCE6 temperature has been exceeded. (SYSTIN is default temperature)
1	**SMIOVT5** A one indicates the high limit of SMI SOURCE5 temperature has been exceeded. (SYSTIN is default temperature)
0	**SMIOVT4** A one indicates the high limit of SMI SOURCE4 temperature has been exceeded. (SYSTIN is default temperature)

9.225 Voltage Comparation Interrupt Status Register - Index 42h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					AVCC_Warn	VIN1_Warn	VIN0_Warn
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved.**
2	**AVCC_Warn.** A one indicates the limit of AVCC voltage has been exceeded.
1	**VIN1_Warn.** A one indicates the limit of VIN1 voltage has been exceeded.

BIT	DESCRIPTION
0	**VIN0_Warn** A one indicates the limit of VIN0 voltage has been exceeded.

9.226 Interrupt Status Register 3 – Index 50h (Bank 4)

Attribute: Read Clear
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		AUXFANIN2	AUXFANIN1	RESERVED		VBAT	3VSB
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved.**
5	**AUXFANIN2. A one indicates the fan count limit of AUXFANIN2 has been exceeded.**
4	**AUXFANIN1. A one indicates the fan count limit of AUXFANIN1 has been exceeded.**
2-3	**Reserved.**
1	**VBAT.** A one indicates the high or low limit of VBAT has been exceeded.
0	**3VSB.** A one indicates the high or low limit of 3VSB has been exceeded.

9.227 SMI# Mask Register 4 – Index 51h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			TAR3	RESERVED		SMSKVBAT	SMSKVSB
DEFAULT	0	0	0	1	0	0	1	1

BIT	DESCRIPTION
7-5	**Reserved.**
4	**TAR3.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
3-2	**Reserved.**
1	**SMSKVBAT.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
0	**SMSKVSB.** A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))

9.228 Reserved Register – Index 52h ~ 53h (Bank 4)

9.229 SYSTIN Temperature Sensor Offset Register – Index 54h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.230 CPUTIN Temperature Sensor Offset Register – Index 55h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.231 AUXTIN Temperature Sensor Offset Register – Index 56h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.232 Reserved Register – Index 57h-58h (Bank 4)

9.233 Real Time Hardware Status Register I – Index 59h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN _STS	SYSFANIN _STS	CPUTIN _STS	SYSTIN _STS	3VCC _STS	AVCC _STS	VIN0 _STS	CPUVCORE _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN_STS. CPUFANIN Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	**SYSFANIN_STS. SYSFANIN Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
5	**CPUTIN_STS. CPUTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	**SYSTIN_STS. SYSTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
3	**3VCC_STS. 3VCC Voltage Status.** 1: 3VCC voltage is over or under the allowed range. 0: 3VCC voltage is in the allowed range.
2	**AVCC_STS. AVCC Voltage Status.** 1: AVCC voltage is over or under the allowed range. 0: AVCC voltage is in the allowed range.
1	**VIN0_STS. VIN0 Voltage Status.** 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.
0	**CPUVCORE_STS. CPUVCORE Voltage Status.** 1: CPUVCORE voltage is over or under the allowed range. 0: CPUVCORE voltage is in the allowed range.

9.234 Real Time Hardware Status Register II – Index 5Ah (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TAR2_STS	TAR1_STS	AUXTIN_STS	CASEOPEN0_STS	AUXFANIN0_STS	AUXFANIN1_STS	CASEOPEN1_STS	VIN1_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2_STS. Smart Fan of CPUFANIN Warning Status.** 1: Selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: Selected temperature has not reached the warning range.
6	**TAR1_STS. Smart Fan of SYSFANIN Warning Status.** 1: SYSTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: SYSTIN temperature has not reached the warning range.
5	**AUXTIN_STS. AUXTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.

BIT	DESCRIPTION
4	**CASEOPEN0_STS. CaseOpen Status.** 1: Caseopen is detected and latched. 0: Caseopen is not latched.
3	**AUXFANIN0_STS. AUXFANIN0 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
2	**AUXFANIN1_STS. AUXFANIN1 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
1	**CASEOPEN1_STS. CaseOpen Status.** 1: Caseopen is detected and latched. 0: Caseopen is not latched.
0	**VIN1_STS. VIN1 Voltage Status.** 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.

9.235 Real Time Hardware Status Register III – Index 5Bh (Bank 4)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 _STS	RESERVED	VIN2 _STS	VIN3 _STS	RESERVED	TAR3 _STS	VBAT _STS	VSB _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**AUXFANIN1_STS. AUXFANIN2 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	**Reserved.**
5	**VIN2_STS. VIN2 Voltage Status.** 1: VIN2 Voltage is over or under the allowed range. 0: VIN2 Voltage is in the allowed range.
4	**VIN3_STS. VIN3 Voltage Status.** 1: VIN3 voltage is over or under the allowed range. 0: VIN3 voltage is in the allowed range.
3	**Reserved.**
2	**TAR3_STS. Smart Fan of AUXFANIN Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode. 0: The selected temperature has not reached the warning range.
1	**VBAT_STS. VBAT Voltage Status.** 1: The VBAT voltage is over or under the allowed range. 0: The VBAT voltage is in the allowed range.
0	**VSB_STS. 3VSB Voltage Status.**

BIT	DESCRIPTION
	1: The 3VSB voltage is over or under the allowed range. 0: The 3VSB voltage is in the allowed range.

9.236 Reserved Register – Index 5Ch ~ 5Fh (Bank 4)

9.237 Is<8:1> Current Register – Index 60h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Is<8:1>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Is<8:1>.** Current measure by current measure IC (1LSB=31.25mA)

9.238 Is<0> Current Register – Index 61h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							Is<0>
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**Is<0>.** Current measure by current measure IC (1LSB=31.25mA)

9.239 POWER <9:2> Register – Index 62h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	POWER <9:2>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**POWER <9:2>.** Power calculate by IO (1LSB=0.25W)

9.240 POWER<1:0> Register – Index 63h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						POWER<1:0>	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
1:0	**POWER<1:0>.** Power calculate by IO (1LSB=0.25W)

9.241 VIN Register – Index 64h (Bank 4)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	VIN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VIN.** Power voltage given by customer. (1LSB=128mV)

9.242 Rreg Setting Register – Index 65h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Rreg							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Rreg.** Equivalent electric impedance in order to calculate Is. (1LSB=1m ohm)

9.243 Reg_Ratio_K and POWER_Voltage Enable Register – Index 66h (Bank 4)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reg_Ration_K				Reserved			Power_ Volt_En
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**Reg_Ration_K:** The ration in order to make power voltage input to IO is below 2.048. Reg_Ration_K=(R1+R2)/(R1)
3-1	**Reserved**

BIT	DESCRIPTION
0	**Power_Volt_En** 0:Power voltage is monitored by IO 1:Power voltage is given by customer

9.244 POWER_V Register – Index 67h (Bank 4)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	POWER_V							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**POWER_V:** Power voltage (1LSB=128mV)

9.245 Reserved Register – Index 68h ~ 7Fh (Bank 4)

9.246 Reserved Register – Index 00h ~ 4Fh (Bank 5)

9.247 Value RAM 2 — Index 50h-5Fh (Bank 5)

ADDRESS A6-A0	DESCRIPTION
50h	**3VSB reading**
51h	**VBAT reading.** The reading is meaningless unless EN_VBAT_MN (Bank0 Index 5Dh, bit0) is set.
52-53h	Reserved
54h	**3VSB High Limit**
55h	**3VSB Low Limit**
56h	**VBAT High Limit**
57h	**VBAT Low Limit**
58h – 5Fh	Reserved

9.248 Reserved Register – Index 60h ~ 7Fh (Bank 5)

9.249 Close-Loop Fan Control RPM mode Register – Index 00 (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED							TwoDimension
DEFAULT	0							0

BIT	DESCRIPTION
7-1	RESERVED
0	**Close-Loop Fan Control RPM mode** (This mode is only useful in Smart FAN IV.) 0: Disable (Default) 1: Eanble

9.250 Close-Loop Fan Control RPM Mode Tolerance Register – Index 01 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM.

9.251 SMIOVT1 Temperature Source Select Register – Index 21 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC1				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT1 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT1 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT1 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT1 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT1 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT1 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT1 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT1 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT1 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT1 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT1 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT1 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT1 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT1 monitoring source.

	0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT1 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT1 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT1 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT1 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT1 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT1 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT1 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT1 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT1 monitoring source.

9.252 SMIOVT2 Temperature Source Select Register – Index 22 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC2				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT2 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT2 monitoring source. 0 0 0 1 0: Select **CPUTIN** as SMIOVT2 monitoring source. (Default) 0 0 0 1 1: Select **AUXTIN** as SMIOVT2 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT2 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT2 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT2 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT2 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT2 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT2 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT2 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT2 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT2 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT2 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT2 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT2 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT2 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT2 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT2 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT2 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT2 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT2 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT2 monitoring source.

9.253 SMIOVT3 Temperature Source Select Register – Index 23 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT3 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT3 monitoring source. 0 0 0 1 0: Select **CPUTIN** as SMIOVT3 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT3 monitoring source. (Default) 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT3 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT3 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT3 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT3 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT3 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT3 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT3 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT3 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT3 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT3 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT3 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT3 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT3 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT3 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT3 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT3 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT3 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT3 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT3 monitoring source.

9.254 SMIOVT4 Temperature Source Select Register – Index 24 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC4				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT4 Temperature selection.**

	Bits **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT4 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT4 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT4 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT4 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT4 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT4 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT4 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT4 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT4 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT4 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT4 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT4 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT4 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT4 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT4 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT4 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT4 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT4 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT4 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT4 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT4 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT4 monitoring source.

9.255 SMIOVT5 Temperature Source Select Register – Index 25 (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC5				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT5 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT5 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT5 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT5 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT5 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT5 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT5 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT5 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT5 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT5 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT5 monitoring source.

	0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT5 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT5 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT5 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT5 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT5 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT5 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT5 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT5 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT5 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT5 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT5 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT5 monitoring source.

9.256 SMIOVT6 Temperature Source Select Register – Index 26 (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC6				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT6 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT6 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT6 monitoring source. 0 0 0 1 1: Select **AUXTIN** as SMIOVT6 monitoring source. 0 0 1 0 0: Select **SMBUSMASTER 0** as SMIOVT6 monitoring source. 0 0 1 0 1: Select **SMBUSMASTER 1** as SMIOVT6 monitoring source. 0 0 1 1 0: Select **SMBUSMASTER 2** as SMIOVT6 monitoring source. 0 0 1 1 1: Select **SMBUSMASTER 3** as SMIOVT6 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 4** as SMIOVT6 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 5** as SMIOVT6 monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 6** as SMIOVT6 monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 7** as SMIOVT6 monitoring source. 0 1 1 0 0: Select **PECI Agent 0** as SMIOVT6 monitoring source. 0 1 1 0 1: Select **PECI Agent 1** as SMIOVT6 monitoring source. 0 1 1 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT6 monitoring source. 0 1 1 1 1: Select **PCH_CHIP_TEMP** as SMIOVT6 monitoring source. 1 0 0 0 0: Select **PCH_CPU_TEMP** as SMIOVT6 monitoring source. 1 0 0 0 1: Select **PCH_MCH_TEMP** as SMIOVT6 monitoring source. 1 0 0 1 0: Select **PCH_DIM0_TEMP** as SMIOVT6 monitoring source. 1 0 0 1 1: Select **PCH_DIM1_TEMP** as SMIOVT6 monitoring source. 1 0 1 0 0: Select **PCH_DIM2_TEMP** as SMIOVT6 monitoring source. 1 0 1 0 1: Select **PCH_DIM3_TEMP** as SMIOVT6 monitoring source. 1 0 1 1 0: Select **BYTE_TEMP** as SMIOVT6 monitoring source.

9.257 Reserved Register – Index 27h (Bank 6)

9.258 SMIOVT4 Temperature Source Configuration Register – Index 28h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.** This bit should be set to zero.
4-3	**Fault.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**Reserved.** This bit should be set to zero.
1	**OVTMOD. SMIOVT4 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP.** 0: Monitor SMIOVT4 temperature source. 1: Stop monitoring SMIOVT4 temperature source.

9.259 SMIOVT5 Temperature Source Configuration Register – Index 29h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.** This bit should be set to zero.
4-3	**Fault.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**Reserved.** This bit should be set to zero.
1	**OVTMOD. SMIOVT5 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP.** 0: Monitor SMIOVT5 temperature source. 1: Stop monitoring SMIOVT5 temperature source.

9.260 SMIOVT6 Temperature Source Configuration Register – Index 2Ah (Bank 6)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.** This bit should be set to zero.
4-3	**Fault.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**Reserved.** This bit should be set to zero.
1	**OVTMOD. SMIOVT6 Mode Select.** 0: Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP.** 0: Monitor SMIOVT6 temperature source. 1: Stop monitoring SMIOVT6 temperature source.

9.261 SMIOVT4 Temperature Source (High Byte) Register – Index 2Bh (Bank 6)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**TEMP<8:1> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.

9.262 SMIOVT5 Temperature Source (High Byte) Register – Index 2Ch (Bank 6)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**TEMP<8:1> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.

9.263 SMIOVT6 Temperature Source (High Byte) Register – Index 2Dh (Bank 6)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	TEMP<8:1>

BIT	DESCRIPTION
7-0	**TEMP<8:1> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.

9.264 SMIOVT4/SMIOVT5/SMIOVT6 Temperature Source (Low Byte) Register – Index 2Eh (Bank 6)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					TEMP6<0>	TEMP5<0>	TEMP4<0>

BIT	DESCRIPTION
7-3	**Reserved.**
2	**SMIOVT6 Temperature <0> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.
1	**SMIOVT5 Temperature <0> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.
0	**SMIOVT4 Temperature <0> (default: SYSTIN temperature source).** The nine-bit value is in units of 0.5°C.

9.265 Reserved Register – Index 2Fh (Bank 6)

9.266 (SYSFANIN) FANIN1 COUNT High-byte Register – Index 30h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT1 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT1_H:** 13-bit SYSFANIN Fan Count, High Byte

9.267 (SYSFANIN) FANIN1 COUNT Low-byte Register – Index 31h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT1 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT1_L:** 13-bit SYSFANIN Fan Count, Low Byte

9.268 (CPUFANIN) FANIN2 COUNT High-byte Register – Index 32h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT2 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT2_H:** 13-bit CPUFANIN Fan Count, High Byte

9.269 (CPUFANIN) FANIN2 COUNT Low-byte Register – Index 33h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT2[4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT2_L:** 13-bit CPUFANIN Fan Count, Low Byte

9.270 (AUXFANIN0) FANIN3 COUNT High-byte Register – Index 34h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT3 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT3_H:** 13-bit AUXFANIN Fan Count, High Byte

9.271 (AUXFANIN0) FANIN3 COUNT Low-byte Register – Index 35h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	RESERVED	FANCNT3 [4:0]
DEFAULT	0	1F

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT3_L:** 13-bit AUXFANIN Fan Count, Low Byte

9.272 (AUXFANIN1) FANIN4 COUNT High-byte Register – Index 36h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT4 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT4_H:** 13-bit AUXFANIN0 Fan Count, High Byte

9.273 (AUXFANIN1) FANIN4 COUNT Low-byte Register – Index 37h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT4 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT4_L:** 13-bit AUXFANIN0 Fan Count, Low Byte

9.274 (AUXFANIN2) FANIN5 COUNT High-byte Register – Index 38h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT5 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT5_H:** 13-bit AUXFANIN1 Fan Count, High Byte

9.275 (AUXFANIN2) FANIN5 COUNT Low-byte Register – Index 39h (Bank 6)

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT5 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANCNT5_L:** 13-bit AUXFANIN1 Fan Count, Low Byte

9.276 (SYSFANIN) Fan Count Limit High-byte Register – Index 3Ah (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN1_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, High Byte

9.277 (SYSFANIN) Fan Count Limit Low-byte Register – Index 3Bh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN1_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, Low Byte

9.278 (CPUFANIN) Fan Count Limit High-byte Register – Index 3Ch (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN2_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

7-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, High Byte

9.279 (CPUFANIN) Fan Count Limit Low-byte Register – Index 3Dh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN2_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, Low Byte

9.280 (AUXFANIN0) Fan Count Limit High-byte Register – Index 3Eh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN3_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, High Byte

9.281 (AUXFANIN0) Fan Count Limit Low-byte Register – Index 3Fh (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN3_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, Low Byte

9.282 (AUXFANIN1) Fan Count Limit High-byte Register – Index 40h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN4_HL [12:5]							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, High Byte

9.283 (AUXFANIN1) Fan Count Limit Low-byte Register – Index 41h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN4_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, Low Byte

9.284 (AUXFANIN2) Fan Count Limit High-byte Register – Index 42h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FANIN5_HL [12:5]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FANIN5_HL:** 13-bit AUXFANIN2 Fan Count Limit, High Byte

9.285 (AUXFANIN2) Fan Count Limit Low-byte Register – Index 43h (Bank 6)

Attribute: Read /Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN5_HL [4:0]				
DEFAULT	0			0				

BIT	DESCRIPTION
7-5	**Reserved.**
4-0	**FANIN5_HL:** 13-bit AUXFANIN2 Fan Count Limit, Low Byte

9.286 SYSFANIN Revolution Pulses Selection Register – Index 44h (Bank 6)

Attribute: Read /Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan1_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**SYSFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.287 CPUFANIN Revolution Pulses Selection Register – Index 45h (Bank 6)

Attribute: Read /Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan2_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**CPUFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.288 AUXFANIN Revolution Pulses Selection Register – Index 46h (Bank 6)

Attribute: Read /Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan3_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.289 SMIOVT1 SMI# Shut-down mode High Limit Temperature Register – Index 50h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT1 SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT1 SMI# Shut-down mode High Limit Temperature.**

9.290 SMIOVT1 SMI# Shut-down mode Low Limit Temperature Register – Index 51h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT1 SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT1 SMI# Shut-down mode Low Limit Temperature.**

9.291 SMIOVT2 SMI# Shut-down mode High Limit Temperature Register – Index 52h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT2 SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT2 SMI# Shut-down mode High Limit Temperature.**

9.292 SMIOVT2 SMI# Shut-down mode Low Limit Temperature Register – Index 53h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT2 SMI# Shut-down mode Low Limit Temperature							

DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT2 SMI# Shut-down mode Low Limit Temperature.**

9.293 SMIOVT3 SMI# Shut-down mode High Limit Temperature Register – Index 54h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT3 SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT3 SMI# Shut-down mode High Limit Temperature.**

9.294 SMIOVT3 SMI# Shut-down mode Low Limit Temperature Register – Index 55h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT3 SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT3 SMI# Shut-down mode Low Limit Temperature.**

9.295 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index 56h (Bank 6)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED HIGH-BYTE VALUE.**

9.296 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index 57h (Bank 6)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED LOW-BYTE VALUE							
DEFAULT	1	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	SYSFANIN SPEED LOW-BYTE VALUE.

9.297 CPUFANIN SPEED HIGH-BYTE VALUE (RPM) – Index 58h (Bank 6)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFANIN SPEED HIGH-BYTE VALUE.

9.298 CPUFANIN SPEED LOW-BYTE VALUE (RPM) – Index 59h (Bank 6)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED LOW-BYTE VALUE							
DEFAULT	1	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	CPUFANIN SPEED LOW-BYTE VALUE.

9.299 AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) – Index 5Ah (Bank 6)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIN0 SPEED HIGH-BYTE VALUE.

9.300 AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) – Index 5Bh (Bank 6)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED LOW-BYTE VALUE							
DEFAULT	1	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	AUXFANIN0 SPEED LOW-BYTE VALUE.

9.301 AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) – Index 5Ch (Bank 6)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED HIGH –BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIIN1 SPEED HIGH-BYTE VALUE.

9.302 AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) – Index 5Dh (Bank 6)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED LOW-BYTE VALUE							
DEFAULT	1	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	AUXFANIN1 SPEED LOW-BYTE VALUE.

9.303 AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) – Index 5Eh (Bank 6)

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED HIGH –BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFANIIN2 SPEED HIGH-BYTE VALUE.

9.304 AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) – Index 5Fh (Bank 6)

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED LOW-BYTE VALUE							
DEFAULT	1	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN2 SPEED LOW-BYTE VALUE.**

9.305 SMIOVT4 SMI# Shut-down mode High Limit Temperature Register – Index 70h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT4 SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT4 SMI# Shut-down mode High Limit Temperature.**

9.306 SMIOVT4 SMI# Shut-down mode Low Limit Temperature Register – Index 71h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT4 SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT4 SMI# Shut-down mode Low Limit Temperature.**

9.307 SMIOVT4 Temperature Source Over-temperature (High Byte) Register – Index 72h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.308 SMIOVT4 Temperature Source Hysteresis (High Byte) Register – Index 73h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.309 SMIOVT4 Over-temperature and Hysteresis LSB Temperature and DIS_OVT and EN_WS Register – Index 74h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	Reserved				DIS_OVT_T4	SMIOVT4	THYST<0>
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**TOVF<0>:** Over-temperature bits0.
6-3	**Reserved**
2	**DIS_OVT_T4:** 0: Enable SMIOVT4 OVT Output 1: Disable SMIOVT4 OVT Output
1	**SMIOVT4** 1: SMI# output type of temperature SMIOVT4 temperature is Shut-down Interrupt Mode. 0: Depend on Bank0, Index 4Ch, bit6. (Default)
0	**THYST<0>:** Hysteresis temperature bit0.

9.310 SMIOVT5 SMI# Shut-down mode High Limit Temperature Register – Index 75h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT5 SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT5 SMI# Shut-down mode High Limit Temperature.**

9.311 SMIOVT5 SMI# Shut-down mode Low Limit Temperature Register – Index 76h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT5 SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT5 SMI# Shut-down mode Low Limit Temperature.**

9.312 SMIOVT5 Temperature Source Over-temperature (High Byte) Register – Index 77h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.313 SMIOVT5 Temperature Source Hysteresis (High Byte) Register – Index 78h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.314 SMIOVT5 Over-temperature and Hysteresis LSB Temperature and DIS_OVT and EN_WS Register – Index 79h (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	Reserved				DIS_OVT_T5	SMIOVT5	THYST<0>
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**TOVF<0>:** Over-temperature bits0.
6-3	**Reserved**
2	**DIS_OVT_T5:** 0: Enable SMIOVT5 OVT Output 1: Disable SMIOVT5 OVT Output
1	**SMIOVT5:** 1: SMI# output type of temperature SMIOVT5 temperature is Shut-down Interrupt Mode. 0: Depend on Bank0, Index 4Ch, bit6. (Default)
0	**THYST<0>:** Hysteresis temperature bit0.

9.315 SMIOVT6 SMI# Shut-down mode High Limit Temperature Register – Index 7Ah (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT6 SMI# Shut-down mode High Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT6 SMI# Shut-down mode High Limit Temperature.**

9.316 SMIOVT6 SMI# Shut-down mode Low Limit Temperature Register – Index 7Bh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	SMIOVT6 SMI# Shut-down mode Low Limit Temperature							
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SMIOVT6 SMI# Shut-down mode Low Limit Temperature.**

9.317 SMIOVT6 Temperature Source Over-temperature (High Byte) Register – Index 7Ch (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.318 SMIOVT6 Temperature Source Hysteresis (High Byte) Register – Index 7Dh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.319 SMIOVT6 Over-temperature and Hysteresis LSB Temperature and DIS_OVT and EN_WS Register – Index 7Eh (Bank 6)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	Reserved				DIS_OVT_T6	SMIOVT6	THYST<0>
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**TOVF<0>:** Over-temperature bits0.
6-3	**Reserved**
2	**DIS_OVT_T6:** 0: Enable SMIOVT6 OVT Output 1: Disable SMIOVT6 OVT Output
1	**SMIOVT6:** 1: SMI# output type of temperature SMIOVT6 temperature is Shut-down Interrupt Mode. 0: Depend on Bank0, Index 4C, bit6. (Default)
0	**THYST<0>:** Hysteresis temperature bit0.

9.320 Reserved Register – Index 7Fh (Bank 6)

9.321 PECI Function Control Registers – Index 01 ~ 04h (Bank 7)

9.322 PECI Enable Function Register – Index 01h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI_En	Reserved				Is_PECI30	Manual_En	Routine_En
DEFAULT	0	0	0	1	0	1	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable PECI Function. (**PECI_En**)
6 ~ 3	R / W	Reserved
2	R / W	Enable PECI 3.0 Command function (**Is_PECI30**)
1	R / W	Enable PECI 3.0 Manual Function (**Manual_En**) (**One-shot clear**)
0	R / W	Enable PECI 3.0 Routine Function (**Routine_En**)

9.323 PECI Timing Config Register – Index 02h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		TN_Extend		Adj[2:0]			PECI_DC
DEFAULT	0	0	0	0	0	0	1	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserve
5	R / W	**TN_Extend[1:0]** Adjust Transaction Rate. 00_{BIN} = 1.5 MHz (Default) 01_{BIN} = 750 KHz 10_{BIN} = 375 KHz 11_{BIN} = 187.5 KHz
4	R / W	
3	R / W	**Adj[2:0]** Compensate the effect of rising time on physical bus Default Value = 001
2	R / W	
1	R / W	
0	R / W	Adjust PECI Tbit Duty cycle selection. **(PECI_DC)** 0 = 75% Tbit high duty cycle time. (Default) 1 = 68% Tbit high duty cycle time.

9.324 PECI Agent Config Register – Index 03h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		En_Agt[1:0]		Reserved		Domain1_Agt1	Domain1_Agt0
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserved
5	R / W	**En_Agt[1:0] Enable Agent** 00 = Disable Agent. 01= Enable Agent0. 10 = Reserved. 11 = Enable Agent0 and Agent1.
4	R / W	
3 ~ 2	R / W	Reserved
1	R / W	Enable domain 1 for Agent1 0 = Agent1 without domain1 1 = Agent1 with domain 1
0	R / W	Enable domain 1 for Agent0 0 = Agent0 without domain 1 1 = Agent0 with domain 1

9.325 PECI Temperature Config Register – Index 04h (Bank 7)

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Virtual_En	Reserved		Clamp	Reserved	RtDmn_Agt[1:0]		RtHigher
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Virtual Temp Function Enable.(**Virtual_En)** When enable this function, the temperature raw data can use LPC to write raw data to CR 17_{HEX} ~ CR $1E_{HEX}$
6 ~ 5	R / W	Reserved
4	R / W	When temperature data reading is positive or less than -128, can enable this function to clamp temperature data.(**Clamp**)
3	R / W	Reserved
2	R / W	**RtDmn_Agt[1:0]**

BIT	READ / WRITE	DESCRIPTION
1	R / W	Agent 1 – Agent 0 always return the relative domain Temperature. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
0	R / W	Return High Temperature of doamin0 or domain1.(**RtHigher**) 0 = The temperature of each agent is returned from domain 0 or domain 1, which is controlled by (CR 04_{HEX}) 1 = Return the highest temperature in domain 0 and domain 1 of individual Agent.

9.326 PECI Command Write Date Registers – Index 05 ~ 1Eh (Bank 7)

9.327 PECI Command Address Register – Index 05h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Address							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.328 PECI Command Write Length Register – Index 06h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Write Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.329 PECI Command Read Length Register – Index 07h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Read Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.330 PECI Command Code Register – Index 08h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Code							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.331 PECI Command Tbase0 Register – Index 09h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 0						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.332 PECI Command Tbase1 Register – Index 0Ah (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 1						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.333 PECI Command Write Data 1 Register – Index 0Bh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.334 PECI Command Write Data 2 Register – Index 0Ch (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.335 PECI Command Write Data 3 Register – Index 0Dh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.336 PECI Command Write Data 4 Register – Index 0Eh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.337 PECI Command Write Data 5 Register – Index 0Fh (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.338 PECI Command Write Data 6 Register – Index 10h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.339 PECI Command Write Data 7 Register – Index 11h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.340 PECI Command Write Data 8 Register – Index 12h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.341 PECI Command Write Data 9 Register – Index 13h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.342 PECI Command Write Data 10 Register – Index 14h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 10							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.343 PECI Command Write Data 11 Register – Index 15h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 11							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.344 PECI Command Write Data 12 Register – Index 16h (Bank 7)

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 12							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.345 PECI Agent Relative Temperature Register (ARTR) – Index 17h-1Eh (Bank 7)

These registers return the **"raw data"** retrieved from PECI GetTemp() command. These data could be the error codes (range: 8000H~81FFH) or relative temperatures to process the defined Tbase. The error code will only be update in **ARTR**; while "Temperature Reading Register", Bank7 Index 20h and 21h, will not be updated when the error code is received. If the **RtHigher** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is $8001_{HEX,}$ in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Attribute: Read / Write(When Virtual_En enable)

ADDRESS 17-1E	DESCRIPTION
17h[15:8],18h[7:0]	Domain0 Relative Temperature Agent0 [15:0]
19h[15:8],1Ah[7:0]	Domain1 Relative Temperature Agent0 [15:0]
1Bh[15:8],1Ch[7:0]	Domain0 Relative Temperature Agent1 [15:0]
1Dh[15:8],1Eh[7:0]	Domain1 Relative Temperature Agent1 [15:0]

GetTemp() PECI Temperature format:

BIT	DESCRIPTION
15	Sign Bit. **(Sign)** In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	The integer part of the relative temperature. (**Temperature[8:0]**)
5	**TEMP_2**. 0.5℃ unit.
4	**TEMP_4**. 0.25℃ unit.
3	**TEMP_8**. 0.125℃ unit.
2	**TEMP_16**. 0.0625℃ unit.
1	**TEMP_32**. 0.03125℃ unit.
0	**TEMP_64**. 0.015625℃ unit.

GetTemp() Response Definition:

RESPONSE	MEANING
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.
0x0000	Processor is running at its maximum temperature or is currently being reset.

All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature. The valide temperature reading is referred to GetTemp() PECI Temperature format

Error Code	Description	Host operation
8000_{HEX}	General Sensor Error	No further processing.
8001_{HEX}	Sensing Device Missing	
8002_{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0℃ back to the temperature readouts.
8003_{HEX}	Operational, but the temperature is higher than the sensor operation range.	Compulsorily write 127℃ back to the temperature readouts.
8004_{HEX} ~ $81FF_{HEX}$	Reserved.	No further operation.

9.346 PECI Command Read Date Registers – Index 1F ~ 32h (Bank 7)

9.347 PECI Alive Agent Register – Index 1Fh (Bank 7)

Attribute: Read only
Size: 8 bits
Record which agentis able to respond to Ping().**Default value is 00_{HEX}.**
1: agent is able to respond to Ping() command. Agent alive
0: agent isn't able to respond to Ping() command. Agent is not alive

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Alive Agent	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~2	Reserve
1	1: agent1 is able to respond to Ping() command. Agent alive 0: agent1 isn't able to respond to Ping() command. Agent is not alive
0	1: agent0 is able to respond to Ping() command. Agent alive 0: agent0 isn't able to respond to Ping() command. Agent is not alive

9.348 PECI Temperature Reading Register (Integer) – Index 20h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Temperature Reading---Integer [9:2]							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7~0	**Temperature value [9] (Sign bit)** **Temperature value [8:2] (Integer bits)** Temperature value [1:0] (Fraction bits)

Note. Temperature reading register is count from raw data and Tbase, for example:

Raw data	+	*Tbase*	=	*Temp Reading*
Bank7, Index [17][18]	+	Bank7, Index [09]	=	Bank7, Index [20][21]

9.349 PECI Temperature Reading Register (Fraction) – Index 21h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Temperature Vaule[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Temperature value [9] (Sign bit) Temperature value [8:2] (Integer bits) **Temperature value [1:0] (Fraction bits)**

9.350 PECI Command TN Count Value Register – Index 22h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Timing Negotiation count Value[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.351 PECI Command TN Count Value Register – Index 23h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				PECI Timing Negotiation count Value[11:8]			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.352 PECI Command Warning Flag Register – Index 24h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						Alert Value[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
1~0	**Agent Alert Bit** (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions. **Default value is 00_{HEX}.**

9.353 PECI Command FCS Data Register – Index 25h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserve		Wraning	CC_Fail	ZeroWFCS	AbortWFCS	BadRFCS	BadWFCS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
5~0	Retrieve PECI related data from client and host. **Default value is 00_{HEX}.**

9.354 PECI Command WFCS Data Register – Index 26h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	PECI WFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI WFCS related data from client. **Default value is 00_{HEX}.**

9.355 PECI RFCS Data Register – Index 27h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI RFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI related data from client. **Default value is 00_{HEX}.**

9.356 PECI AWFCS Data Register – Index 28h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI AWFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PCI related data from client. **Default value is 00_{HEX}.**

9.357 PECI CRC OUT WFCS Data Register – Index 29h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI CRC OUT WFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI related data from client. **Default value is 00_{HEX}.**

9.358 PECI Command Read Data 1 Register – Index 2Ah (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.359 PECI Command Read Data 2 Register – Index 2Bh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.360 PECI Command Read Data 3 Register – Index 2Ch (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.361 PECI Command Read Data 4 Register – Index 2Dh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.362 PECI Command Read Data 5 Register – Index 2Eh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.363 PECI Command Read Data 6 Register – Index 2Fh (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.364 PECI Command Read Data 7 Register – Index 30h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 7							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.365 PECI Command Read Data 8 Register – Index 31h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.366 PECI Command Read Data 9 Register – Index 32h (Bank 7)

Attribute: Read only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

PECI Manual Command Address Table

Command Bank 7	Address CR 05_{HEX}	WriteLength CR 06_{HEX}	Read Length CR 07_{HEX}	Command Code CR 08_{HEX}
Ping	Addr	00	00	
GetDIB		01	08	F7
GetTemp		01	02	01
PCIRd30		06	02 / 03 / 05	61
PCIWr30		08 / 09 / 0B	01	65
PCIRdLocal30		05	02 / 03 / 05	E1
PCIWrLocal30		07 / 08 / 0A	01	E5
PKGRd30		05	02 / 03 / 05	A1

PKGWr30		07 / 08 / 0A	01	A5
IAMSRRd30		05	02 / 03 / 05 / 09	B1
IAMSRWr30		07 / 08 / 0A / 0E	01	B5

PECI Manual Command Read Data Table

Command	PCI Rd30	PCI Wr30	PCIRd Local30	PCIWr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30	GetDIB	GetTemp
Command Code	61	65	E1	E5	A1	A5	B1	B5	F7	01
RdData 1 CR $2A_{HEX}$	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	X	X
RdData 2 CR $2B_{HEX}$	X	X	X	X	X	X	Data LSB_1	X	Device Info	X
RdData 3 CR $2C_{HEX}$	X	X	X	X	X	X	Data LSB_2	X	Revision Number	X
RdData 4 CR $2D_{HEX}$	X	X	X	X	X	X	Data LSB_3	X	Reserved 1	X
RdData 5 CR $2E_{HEX}$	X	X	x	X	X	X	Data LSB_4	X	Reserved 2	X
RdData 6 CR $2F_{HEX}$	Data LSB_1	X	Data LSB_1	X	Data LSB_1	X	Data LSB_5	X	Reserved 3	X
RdData 7 CR 30_{HEX}	Data LSB_2	X	Data LSB_2	X	Data LSB_2	X	Data LSB_6	X	Reserved 4	X
RdData 8 CR 31_{HEX}	Data LSB_3	X	Data LSB_3	X	Data LSB_3	X	Data LSB_7	X	Reserved 5	Temp_LB
RdData 9 CR 32_{HEX}	Data MSB	x	Data MSB	X	Data MSB	X	Data MSB	X	Reserved 6	Temp_HB

PECI Manual Command Write Data Table

Command	PCI Rd30	PCI Wr30	PCIRd Local30	PCIWr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30
Command Code	**61**	**65**	**E1**	**E5**	**A1**	**A5**	**B1**	**B5**
WrData 1 CR 0B$_{HEX}$	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID
WrData 2 CR 0C$_{HEX}$	Addr LSB_1	Addr LSB_1	Addr LSB_1	Addr LSB_1	Index	Index	Processor ID	Processor ID
WrData 3 CR 0D$_{HEX}$	Addr LSB_2	Addr LSB_2	Addr LSB_2	Addr LSB_2	Param LSB	Param LSB	Addr LSB	Addr LSB
WrData 4 CR 0E$_{HEX}$	Addr LSB_3	Addr LSB_3	Addr MSB	Addr MSB	Param MSB	Param MSB	Addr MSB	Addr MSB
WrData 5 CR 0F$_{HEX}$	Addr MSB	Addr MSB	X	Data LSB_1	X	Data LSB_1	X	Data LSB_1
WrData 6 CR 10$_{HEX}$	X	Data LSB_1	X	Data LSB_2	X	Data LSB_2	X	Data LSB_2
WrData 7 CR 11$_{HEX}$	X	Data LSB_2	X	Data LSB_3	X	Data LSB_3	X	Data LSB_3
WrData 8 CR 12$_{HEX}$	X	Data LSB_3	X	Data MSB	X	Data MSB	X	Data LSB_4
WrData 9 CR 13$_{HEX}$	X	Data MSB	X	X	X	X	X	Data LSB_5
WrData10 CR 14$_{HEX}$	X	X	X	X	X	X	X	Data LSB_6
WrData11 CR 15$_{HEX}$	X	X	X	X	X	X	X	Data LSB_7
WrData12 CR 16$_{HEX}$	X	X	X	X	X	X	X	Data MSB

10. FLOPPY DISK CONTROLLER

10.1 FDC Functional Description

The floppy disk controller (FDC) of the NCT6776F / NCT6776D integrates all of the logic required for floppy disk control. The FDC implements a FIFO which provides better system performance in multi-master systems, and the digital data separator supports data rates up to 2 M bits/sec.

The FDC includes the following blocks: Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core. The rest of this section discusses these blocks through the following topics: FIFO, Data Separator, Write Precompensation, Perpendicular Recording mode, FDC core, FDC commands, and FDC registers.

10.1.1 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM (Request fro Master) and DIO (Data Input / Output) bits in the Main Status Register.

The FIFO is defaulted to disabled mode after any form of reset, which maintains PC/AT hardware compatibility. The default values can be changed through the configure command. The advantage of the FIFO is that it lets the system have a larger DMA latency without causing disk errors. The following tables give several examples of the delays with the FIFO. The data are based upon the following formula:

DELAY = THRESHOLD # x (1 / DATA RATE) * 8 – 1.5 μs

Table 10-1 The Delays of the FIFO

FIFO THRESHOLD	MAXIMUM DELAY UNTIL SERVICING AT 500K BPS
	Data Rate
1 Byte	1 x 16 μs – 1.5 μs = 14.5 μs
2 Byte	2 x 16 μs – 1.5 μs = 30.5 μs
8 Byte	8 x 16 μs – 1.5 μs = 6.5 μs
15 Byte	15 x 16 μs – 1.5 μs = 238.5 μs
FIFO THRESHOLD	**MAXIMUM DELAY UNTIL SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 x 8 μs – 1.5 μs = 6.5 μs
2 Byte	2 x 8 μs – 1.5 μs = 14.5 μs
8 Byte	8 x 8 μs – 1.5 μs = 62.5 μs
15 Byte	15 x 8 μs – 1.5 μs = 118.5 μs

At the start of a command, the FIFO is always disabled, and command parameters must be sent based upon the RQM and DIO bit settings in the Main Status Register. When the FDC enters the command execution phase, it clears the FIFO off any data to ensure that invalid data are not transferred.

An overrun or underrun terminates the current command and data transfer. Disk writes complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled by the specify command and are initiated by the FDC when the LDRQ pin is activated during a data transfer command.

10.1.2 Data Separator

The function of the data separator is to lock onto incoming serial read data. When a lock is achieved, the serial front-end logic in the chip is provided with a clock that is synchronized with the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial-to-parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The control logic generates RDD and RWD for every pulse input, and any data pulse input is synchronized and then adjusted immediately by error adjustment. A digital integrator keeps track of the speed changes in the input data stream.

10.1.3 Write Precompensation

The write precompensation logic minimizes bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and depends on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known, so, depending on the pattern, the bit is shifted either early or late, relative to the surrounding bits.

10.1.4 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5” floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. Perpendicular mode requires a 1 Mbps data rate for the FDC, and, at this data rate, the FIFO manages the host interface bottleneck due to the high speed of data transfer to and from the disk.

10.1.5 FDC Core

The NCT6776F / NCT6776D FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor, and the result may be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information are provided to the microprocessor.

The next section introduces each of the commands.

10.1.6 FDC Commands

Command Symbol Descriptions:

C: Cylinder Number 0 – 256

D: Data Pattern
DIR: Step Direction
DIR = 0: step out
DIR = 1: step in
DS0: Disk Drive Select 0
DS1: Disk Drive Select 1
DTL: Data Length
EC: Enable Count
EFIFO: Enable FIFO
EIS: Enable Implied Seek
EOT: End of Track
FIFOTHR: FIFO Threshold
GAP: Gap Length Selection
GPL: Gap Length
H: Head Number
HDS: Head Number Select
HLT: Head Load Time
HUT: Head Unload Time
LOCK: Lock EFIFO, FIFOTHR, and PTRTRK bits to prevent being affected by software reset
MFM: MFM or FM Mode
MT: Multitrack
N: The number of data bytes written in a sector
NCN: New Cylinder Number
ND: Non-DMA Mode
OW: Overwritten
PCN: Present Cylinder Number
POLL: Polling Disable
PRETRK: Precompensation Start Track Number
R: Record
RCN: Relative Cylinder Number
R/W: Read/Write
SC: Sectors per Cylinder
SK: Skip deleted data address mark
SRT: Step Rate Time
ST0: Status Register 0
ST1: Status Register 1
ST2: Status Register 2
ST3: Status Register 3
WG: Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
	W	---------- R ----------	
	W	---------- N ----------	
	W	---------- EOT ----------	
	W	---------- GPL ----------	
	W	---------- DTL ----------	
Execution			Data transfer between the FDD and system
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- C ----------	Sector ID information after command execution
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in the Data Register
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Disk status after the command has been completed
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
		---------- DTL/SC ----------								
Execution										No data transfer takes place
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to Command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and the system
Result	R	---------- ST0 ----------								Status information after Command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								

	R	---------- C ----------	Sector ID information after Command execution
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and the system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes per Sector
	W	---------- SC ----------								Sectors per Cylinder
	W	---------- GPL ----------								Gap 3
	W	---------- D ----------								Filler Byte
Execution for Each Sector: (Repeat)	W	---------- C ----------								Input Sector Parameters
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								

	R	---------- Undefined ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								Status information at the end of each seek operation
	R	---------- PCN ----------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ---------- | --------- HUT ---------- |								
	W	|---------- HLT ----------| ND								

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution	R									Head positioned over proper cylinder on the diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL | ------ FIFOTHR ----|					
	W	| ----------PRETRK ---------- |								
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	| ---------- RCN ---------- |								

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------								
	R	---------- PCN-Drive 1 ----------								
	R	---------- PCN-Drive 2----------								
	R	---------- PCN-Drive 3 ----------								
	R	--------SRT ---------- | --------- HUT --------								
	R	---------- HLT ----------| ND								
	R	---------- SC/EOT ----------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WG	
	R	0	EIS	EFIFO	POLL | ------ FIFOTHR --------					
	R	----------PRETRK ----------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information about the disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	---------- Invalid Codes ----------								Invalid codes (no operation-FDC goes to standby state)
Result	R	---------- ST0 ----------								ST0 = 80h

10.2 Register Descriptions

There are several status, data, and control registers in the NCT6776F / NCT6776D. These registers are defined below, and the rest of this section provides more details about each one of them.

Table 10-2 FDC Registers

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

10.2.1 Status Register A (SA Register) (Read base address + 0)

Along with the SB register, the SA register is used to monitor several disk-interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRV 2#	STEP	TRAK0#	HEAD	INDEX#	WP#	DIR
DEFAULT	0	0	NA	1	NA	1	1	NA

BIT	DESCRIPTION
7	**INIT PENDING**. Indicates the value of the floppy disk interrupt output.
6	**DRV2#.** 0: A second drive has been installed. 1: A second drive has not been installed.
5	**STEP.** Indicates the complement of the STEP# output.
4	**TRAK0#.** Indicates the value of the TRAK# input.
3	**HEAD.** Indicates the complement of the HEAD# output. 0: Side 0. 1: Side 1.
2	**INDEX#.** Indicates the value of the INDEX# output.
1	**WP#.** 0: The disk is write-protected. 1: The disk is not write-protected.
0	**DIR.** Indicates the direction of head movement. 0: Outward direction. 1: Inward direction.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	INIT PENDING	DRQ	STEP F/F	TRAK0	HEAD#	INDEX	WP	DIR#
DEFAULT	0	0	NA	0	NA	0	0	NA

BIT	DESCRIPTION
7	**INIT PENDING.** Indicates the value of the floppy disk interrupt output.
6	**DRQ.** Indicates the value of the DRQ output pin.
5	**SETP F/F.** indicates the complement of latched STEP# output.
4	**TRAK0.** Indicates the complement of the TRAK0# input.
3	**HEAD#.** Indicates the value of the HEAD# output. 0: Side 1. 1: Side 0.
2	**INDEX.** Indicates the complement of the INDEX# output.
1	**WP.** 0: The disk is not write-protected. 1: The disk is write-protected.
0	**DIR#.** Indicates the direction of the head movement. 0: Inward direction. 1: Outward direction.

10.2.2 Status Register B (SB Register) (Read base address + 1)

Along with the SA register, the SB register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Drive SEL0	WDTA Toggle	RDTA Toggle	WE	Reserved	MOT EN A
DEFAULT	1	1	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved.**
5	**Drive SEL0.** Indicates the status of the DO Register, bit 0 (drive-select bit 0).
4	**WDATA Toggle.** Changes state on every rising edge of the WD# output pin.
3	**RDATA Toggle.** Changes state on every rising edge of the RDATA# output pin.
2	**WE.** Indicates the complement of the WE# output pin.
1	**Reserved.**
0	**MOT EN A.** Indicates the complement of the MOA# output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DSA#	WD F/F	RDATA F/F	WE F/F	DSD#	DSC#

DEFAULT	0	1	1	0	0	0	1	1

BIT	DESCRIPTION
7-6	**Reserved.**
5	**DSA#.** This bit indicates the status of the DSA# output pin.
4	**WD F/F.** Indicates the complement of the WD# output pin, which is latched on every rising edge of the WD# output pin.
3	**RDATA F/F.** Indicates the complement of the latched RDATA# output pin.
2	**WE F/F.** Indicates the complement of the latched WE# output pin.
1	**DSD#.** 0: Drive D has been selected. 1: Drive D has not been selected.
0	**Reserved.**

10.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register that controls drive motors, drive selection, DRQ/IRQ enable, and FDC reset. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			MOTOR ENABLE A	DMA&INT ENABLE	FDC RESET	DRIVE SELECT	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**MOTOR ENABLE A.** A logical 1 enables Motor A.
3	**DMA & INT ENABLE.** A logical 1 enables DRQ/IRQ.
2	**FDC RESET.** Floppy Disk Controller Reset. A logical 0 resets the FDC.
1-0	**DRIVE SELECT.** **Bits** **1 0** 0 0: Select Drive A. 0 1: Select Drive B. 1 0: Select Drive C. 1 1: Select Drive D.

10.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information for the floppy disk drive.

In normal floppy mode, this register only has bits 0 and 1, and the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						Tape sel 1	Tape sel 0

DEFAULT	NA	NA	NA	NA	NA	NA	0	0

BIT	DESCRIPTION
7-2	**RESERVED.**
1	**Tape sel 1.**
0	**Tape sel 0.**

If the three-mode FDD function is enabled (EN3MODE = 1 in LD0 CRF0, Bit 0), the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Media ID1	Media ID0	Drive Type ID1	Drive Type ID0	Floppy Boot Drive 1	Floppy Boot Drive 0	Tape Sel 1	Tape Sel 0
DEFAULT	0	0	1	1	0	0	0	0

BIT	DESCRIPTION	
7	**Media ID1.** Read only. Reflects the value of LD0, CRF1, bit 5.	
6	**Media ID0.** Read only. Reflects the value of LD0, CRF1, bit 4.	
5	**Drive Type ID1.**	Reflect the bit in LD0, CR[F2h]. Which bit is reflected depends on the last drive selected in the PO register.
4	**Drive Type ID0.**	
3	**Floppy Boot Drive 1.** Reflects the value of LD0, CRF1, bit 7.	
2	**Floppy Boot Drive 0.** Reflects the value of LD0, CRF1, bit 6.	
1	**Tape Sel 1.**	Assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved for the floppy disk boot drive.
0	**Tape Sel 0.**	

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

10.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RQM	DIO	Non-DMA mode	FDC Busy	RESRVED			FDD 0 Busy
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**Request for Master (RQM).** A high on this bit indicates Data Register is ready to send or receive data to or from the processor.
6	**DATA INPUT/OUTPUT (DIO).** If DIO = HIGH, then the transfer is from Data Register to the processor. If DIO = LOW, the transfer is from processor to Data Register.
5	**Non-DMA mode.** The FDC is in the non-DMA mode, this bit is set only during the execution phase in non-DMA mode.
4	**FDC Busy** (CB). A read or write command is in the process when CB = HIGH.
3-1	**Reserved.**
0	**FDD 0 Busy.** (D0B = 1) FDD number 0 is in the SEEK mode.

10.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. However, in PC-AT and PS/2 Model 30 and PS/2 modes, the data rate is controlled by the CC register, not by the DR register. As a result, the real data rate is determined by the most recent write to either the DR or CC register. The bit definitions for this register are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	S/W RESET	POWER DOWN	RESERVED	PRECOMP2	PRECOMP1	PRECOMP0	DRATE1	DRATE0
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION	
7	**S/W RESET.** The software reset bit.	
6	**POWER DOWN.** 0: FDC in normal mode. 1: FDC in power-down mode.	
5	**RESERVED.**	
4	**PRECOMP 2.**	Selects the value of write precompensation. The following tables show the precompensation values for every combination of these bits. Please see the tables below.
3	**PRECOMP 1.**	
2	**PRECOMP 0.**	
1	**DRATE 1.**	Select the data rate of the FDC and reduced write-current control. **Bits** **1 0** 0 0: 500 KB/S (MFM), 250 KB/S (FM), RWC# = 1 0 1: 300 KB/S (MFM), 150 KB/S (FM), RWC# = 0 1 0: 250 KB/S (MFM), 125 KB/S (FM), RWC# = 0 1 1: 1 MB/S (MFM), Illegal (FM), RWC# = 1
0	**DRATE 0.**	

The 2 MB/S data rate for the tape drive is only supported by setting DRATE1 and DRATE0 to 01, as well as setting DRT1 and DRT0 (CRF4 and CRF5 for logical device 0) to 10. Please see the functional description of CRF4 or CRF5 and the data rate table for individual data-rate settings.

PRECOMP	PRECOMPENSATION DELAY	
2 1 0	250K – 1 Mbps	2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 ns	20.8 ns
0 1 0	83.34 ns	41.17 ns
0 1 1	125.00 ns	62.5ns
1 0 0	166.67 ns	83.3 ns
1 0 1	208.33 ns	104.2 ns
1 1 0	250.00 ns	125.00 ns
1 1 1	0.00 ns (disabled)	0.00 ns (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 ns
300 KB/S	125 ns
500 KB/S	125 ns
1 MB/S	41.67ns
2 MB/S	20.8 ns

10.2.7 FIFO Register (R/W base address + 5)

The FIFO register consists of four status registers in a stack, and only one register is presented to the data bus at a time. The FIFO register stores data, commands, and parameters, and it provides disk-drive status information. In addition, data bytes pass through the data register to program or obtain results after a command. In the NCT6776F / NCT6776D, this register is disabled after reset. The FIFO can enable it and change its values through the CONFIGURE command.

BIT	7	6	5	4	3	2	1	0
NAME	IC		SE	EC	NR	HD	US1, US0 Drive Select	

Status Register 0 (ST0)

BIT	DESCRIPTION
7-6	**IC (Interrupt Code).** **Bits** **7 6** 0 0: Normal termination of the command. 0 1: Abnormal termination of the command. 1 0: Invalid command issue. 1 1: Abnormal termination because the ready signal from FDD changed state during command execution.
5	**SE (Seek End).** 1: Seek end. 0: Seek error.
4	**EC (Equipment Check).** 1: When a fault signal is received from the FDD or the track. Signal fails to occur after 77 step pulses. 0: No error.

BIT	DESCRIPTION
3	**NR (Not Ready).** 1: Drive is not ready. 0: Drive is ready.
2	**HD Head Address. (The current head address)** 1: Head selected. 0: Head selected.
1-0	**US 1, US0 Drive Select.** **Bits** **1 0** 0 0: Drive A selected. 0 1: Drive B selected. 1 0: Drive C selected. 1 1: Drive D selected.

Status Register 1 (ST1)

BIT	7	6	5	4	3	2	1	0
NAME	EN	Reserved	OE	OR	Reserved	ND	NW	MAM

BIT	DESCRIPTION
7	**EN (End of Track).** 1 will be written to this bit if the FDC tries to access a sector beyond the final sector or a cylinder.
6	Reserved. This bit is always 0.
5	**DE (Data Error).** 1 will be written to this bit if the FDC detects a CRC error in either the ID field or the data field.
4	**OR (Over Run).** 1 will be written to this bit if the FDC is not served by the host system within a certain time interval during data transfer.
3	Reserved. This bit is always 0.
2	**ND (No Data).** 1 will be written to this bit if the specified sector cannot be found during execution of a read, write or verity data.
1	**NW (Not Writable).** 1 will be written to this bit if a write protect signal is detected from the diskette drive during execution of write data.
0	**MAM (Missing Address Mark).** 1 will be written to this bit if the FDC cannot detect the data address mark or the data address mark has been deleted.

Status Register 2 (ST2)

BIT	7	6	5	4	3	2	1	0
NAME	NOT USED	CM	DD	WC	SH	SN	BC	MD

BIT	DESCRIPTION
7	Not used. This bit is always 0.
6	**CM (Control Mark).** 1: During execution of the read data or scan command. 0: No error.

BIT	DESCRIPTION
5	**DD (Data error in the Data field).** 1: If the FDC detects a CRC error in the data field. 0: No error.
4	**WC (Wrong Cylinder).** 1: Indicates wrong cylinder.
3	**SH (Scan Equal Hit).** 1: During execution of the Scan command, if the equal condition is satisfied. 0: No error.
2	**SN (Scan Not Satisfied).** 1: During execution of the Scan command. 0: No error.
1	**BC (Bad Cylinder).** 1: Bad Cylinder. 0: No error.
0	**MD (Missing Address Mark in Data Field).** 1: If FDC cannot find a data address mark (or the address mark has been deleted) when reading data from the media. 0: No error.

Status Register 3 (ST3)

BIT	7	6	5	4	3	2	1	0
NAME	FT	WP	RY	T0	TS	HD	US1	US0

BIT	DESCRIPTION
7	**FT.** Fault.
6	**WP.** Write protected.
5	**RY.** Ready.
4	**T0.** Track 0.
3	**TS.** Two-side.
2	**HD.** Head Address.
1	**US1.** Unit Select 1.
0	**US0.** Unit Select 0.

10.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit, read-only register used for diagnostic purposes. In PC/XT or PC/AT mode, only bit 7 is checked by the BIOS. When the register is read, bit 7 shows the complement of DSKCHG#, while the other bits remain in tri-state. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG	RESERVED						
DEFAULT	0	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DSKCHG.**
6-0	**RESERVED.** Reserved for the hard disk controller. During a read of this register, these bits are in tri-state.

In PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG	RESERVED				DRATE1	DRATE0	HIGH DENS#
DEFAULT	0	1	1	1	1	1	0	1

BIT	DESCRIPTION	
7	**DSKCHG.** Indicates the complement of the DSKCHG# input.	
6-3	**RESERVED.** Always 1 during a read.	
2	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
1	**DRATE 0.**	
0	**HIGHDENS#.** 0: 500 KB/S or 1 MB/S data rate (high-density FDD). 1: 250 KB/S or 300 KB/S data rate.	

In PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	DSKCHG#	RESERVED			DMAEN	NOPREC	DRATE1	DRATE0
DEFAULT	1	0	0	0	0	0	1	0

BIT	DESCRIPTION	
7	**DSKCHG.** Indicates the status of the DSKCHG# input.	
6-4	**RESERVED.** Always 0 during a read.	
3	**DMAEN.** Indicates the value of DO register, bit 3.	
2	**NOPREC.** Indicates the value of the NOPREC bit in the CC REGISTER.	
1	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address +4)) for how the settings correspond to individual data rates.
0	**DRATE 0.**	

10.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In PC/AT and PS/2 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						DRATE1	DRATE0

DEFAULT	NA	NA	NA	NAN	NA	NA	1	0

BIT	DESCRIPTION	
7-2	**RESERVED.** Should be set to 0.	
1	**DRATE 1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address +4)) for how the settings correspond to individual data rates.
0	**DRATE 0.**	

In the PS/2 Model 30 mode, the bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					NOPREC	DRATE1	DRATE0
DEFAULT	NA	NA	NA	NA	NA	0	1	0

BIT	DESCRIPTION	
7-3	**RESERVED.** Should be set to 0.	
2	**NOPREC.** Disables the precompensation function. This bit can be set by the software.	
1	**DRATE1.**	Select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.
0	**DRATE0.**	

11. UART PORT

11.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 11-1 Register Summary for UART

Bit Number										
Register Address Base			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

11.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. in 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

11.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved.**
4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

11.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

11.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	**RESERVED.**	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

11.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.
5-4	**RESERVED.**
3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table

	below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT 0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

11.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	En_address_byte	RX_ctrl	RESERVED		EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5-4	**RESERVED.**
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.

BIT	DESCRIPTION
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

11.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
50	400	650	2304	**
75	600	975	1536	**
110	880	1430	1047	0.18%
134.5	1076	1478.5	857	0.099%
150	1200	1950	768	**
300	2400	3900	384	**
600	4800	7800	192	**
1200	9600	15600	96	**
1800	14400	23400	64	**
2000	16000	26000	58	0.53%
2400	19200	31200	48	**
3600	28800	46800	32	**
4800	38400	62400	24	**
7200	57600	93600	16	**
9600	76800	124800	12	**
19200	153600	249600	6	**
38400	307200	499200	3	**
57600	460800	748800	2	**
115200	921600	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

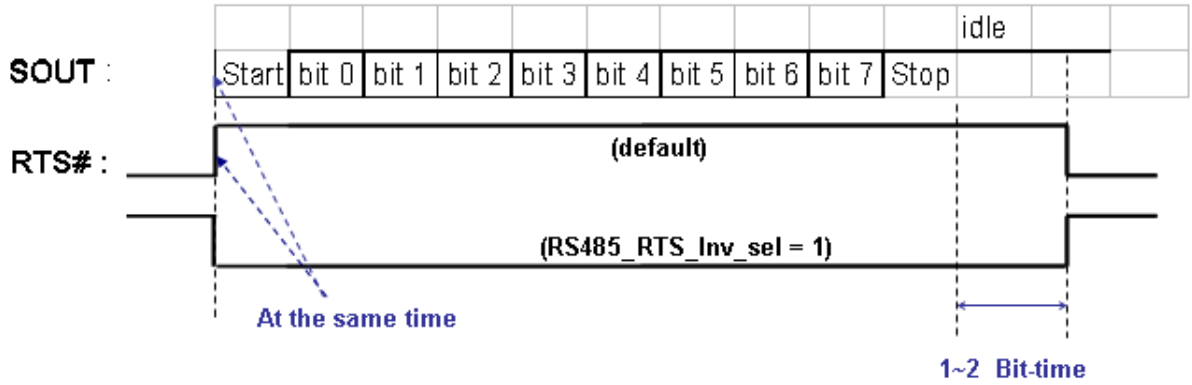
11.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

11.10 UART RS485 Auto Flow Control

NCT6776F / NCT6776D supports RS485 auto flow control function for UARTA and UARTB. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for UARTA and UARTB when UART TX block transmits the data.

The diagram shown below illustrates the RS485 auto flow control function for UARTA adn UARTB.



The default behavior of RTS# pin will drive logic high the time edge between **Start bit** and **bit0** when the UART TX Block start to transmits the data on SOUT pin. Then the RTS# pin will drive logic low later than **Stop bit** about 1~2 x Bit-time when UART TX Block completes the data transmission. The driving behavior of RTS# will be inverted when we set RS485_RTS_inv_sel bit = 1'b1. (Bit-time: Depends on the baud rate of transmission)

The bellowing control register table relates to the RS485 auto flow control function for UARTA and UARTB.

	UARTA	**UARTB**
RTS485_enable	Logic Device 2, CRF2_Bit7	Logic Device 3, CRF2_Bit7
RTS485_inv_sel	Logic Device 2, CRF2_Bit6	Logic Device 3, CRF2_Bit6

12. PARALLEL PORT

12.1 Printer Interface Logic

The NCT6776F / NCT6776D parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The NCT6776F / NCT6776D supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP).

The following tables show the pin definitions for different modes of the parallel port.

Table 12-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN NUMBER OF NCT6776F / NCT6776D	PIN ATTRIBUTE	SPP	EPP	ECP
1	55	O	Nstb	nWrite	nSTB, HostClk[2]
2-9	421-45, 47-50	I/O	PD<7:0>	PD<7:0>	PD<7:0>
10	41	I	nACK	Intr	nACK, PeriphClk[2]
11	40	I	BUSY	nWait	BUSY, PeriphAck[2]
12	39	I	PE	PE	Peerror, nAckReverse[2]
13	38	I	SLCT	Select	SLCT, Xflag[2]
14	54	O	Nafd	nDStrb	nAFD, HostAck[2]
15	53	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	52	O	Ninit	nInit	nINIT[1], nReverseRqst[2]
17	51	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN NUMBER OF NCT6776F / NCT6776D	PIN ATTRIBUTE	SPP
1	55	O	nSTB
2	50	I/O	PD0
3	49	I/O	PD1
4	48	I/O	PD2
5	47	I/O	PD3
6	45	I/O	PD4
7	44	I/O	PD5
8	43	I/O	PD6
9	42	I/O	PD7
10	41	I	nACK
11	40	I	BUSY
12	39	I	PE
13	38	I	SLCT
14	54	O	nAFD

HOST CONNECTOR	PIN NUMBER OF NCT6776F / NCT6776D	PIN ATTRIBUTE	SPP
15	53	I	nERR
16	52	O	nINIT
17	51	O	nSLIN

12.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

Table 12-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data pot (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 12-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

12.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

12.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	BUSY#	ACK#	PE	SLCT	ERROR#	RESERVED		TMOUT
DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	**BUSY#.** This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
6	**ACK#.** This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 μs before BUSY# stops.
5	**PE.** A logical 1 means the printer has detected the end of paper.
4	**SLCT.** A logical 1 means the printer is selected.
3	**ERROR#.** A logical 0 means the printer has encountered an error condition.
2-1	**RESERVED.**
0	**TMOUT.** This bit is only valid in EPP mode. A logical 1 indicates that a 10-μs time-out has occurred on the EPP bus; a logical 0 means hat no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

12.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**RESERVED.** These two bits are always read as logical 1 and can be written.
5	**DIR (Direction Control Bit).** When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
4	**IRQ ENABLE.** A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	**SLCT IN.** a logical 1 selects the printer.
2	**INIT#.** A logical 0 starts the printer (50 microsecond pulse, minimum).
1	**AUTO FD.** A logical 1 causes the printer to line-feed after a line is printed.
0	**STROBE.** A logical 1 generates an active-high pulse for a minimum of 0.5 μs to clock data into the printer. Valid data must be presented for a minimum of 0.5 μs before and after the strobe pulse.

12.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

12.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

12.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
Nwrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
Nwait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

12.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

12.2.8 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

12.2.9 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it does not finish until nWait changes from active low to inactive high.

12.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the NCT6776F / NCT6776D parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The NCT6776F / NCT6776D ECP supports the following modes.

Table 12-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)

MODE	DESCRIPTION
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

12.3.1 ECP Register and Bit Map

The next two tables list the registers used in ECP mode and provide a bit map of the parallel port and ECP registers.

Table 12-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

Table 12-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	Perror	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

12.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Address/RLE	Address or RLE						

12.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBusy	nAck	Perror	Select	nFault	1	1	1

BIT	DESCRIPTION
7	**nBusy.** This bit reflects the complement of the Busy input.
6	**nAck.** This bit reflects the nAck input.
5	**Perror.** This bit reflects the Perror input.
4	**Select.** This bit reflects the Select input.
3	**nFault.** This bit reflects the nFault input.
2-0	These three bits are not implemented and are always logical 1 during a read.

12.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Director	ackInEn	SelectIn	nInit	Autofd	Strobe
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**Reserved.** These two bits are always read as logical 1 and cannot be written.
5	**Director.** If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes, 0: The parallel port is in the output mode. 1: The parallel port is in the input mode.

BIT	DESCRIPTION
4	**ackInEn** (Interrupt Request Enable). When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	**SelectIn.** This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.
2	**nInit.** This bit is output to the INIT# output.
1	**Autofd.** This bit is inverted and output to the AFD# output.
0	**Strobe.** This bit is inverted and output to the STB# output.

12.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

12.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

12.3.7 TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

12.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates that this is an 8-bit implementation.

12.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	intrVALUE	IRQx2	IRQx1	IRQx0	RESERVED		
DEFAULT	0	0	0	0	0	1	1	1

BIT	DESCRIPTION
7	**Compress.** This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.
6	**intrValue.** Returns the value on the ISA IRQ line to determine possible conflicts.

BIT	DESCRIPTION
5	**IRQx2.** Reflects the IRQ resource assigned for ECP port.
4	**IRQx1.**
3	**IRQx0.**

cnfgB[5:3]	IRQ resource
000	Reflects other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

2-0	**Reserved.** These three bits are logical 1 during a read and can be written.

12.3.10ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE			nErrIntrEn	dmaEn	ServiceIntr	Full	Empty
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-5	**Mode.** Read/Write. These bits select the mode.

000	Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.
001	PS/2 Parallel Port mode. This is the same as SPP mode except that direction may be used to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.
010	Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
100	EPP Mode. EPP mode is activated if the EPP mode is selected.
101	Reserved.
110	Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port.
111	Configuration Mode. The confgA and confgB registers are accessible at

BIT	DESCRIPTION
	0x400 and 0x401 in this mode.
4	**nErrIntrEn.** Read/Write (Valid only in ECP Mode) 0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR. 1: Disables the interrupt generated on the asserting edge of nFault.
3	**dmaEn.** Read/Write. 0: Disable DMA unconditionally. 1: Enable DMA.
2	**serviceIntr.** Read/Write. 0: Enable one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be rest to logical 0 to re-enable the interrupts. (a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached. (b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO. (c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO. 1: Disable DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt.
1	**Full.** Read Only. 0: The FIFO has at least one free byte. 1: The FIFO is completely full; it cannot accept another byte.
0	**Empty.** Read Only. 0: The FIFO contains at least one byte of data. 1: The FIFO is completely empty.

12.3.11ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
Nstrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
Perror (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.

NAME	TYPE	DESCRIPTION
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

12.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

I Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

12.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

12.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

12.3.12.3. Data Compression

The NCT6776F / NCT6776D hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

12.3.13FIFO Operation

The FIFO threshold is set in CR5. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

12.3.14DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or Cfifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

12.3.15Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400H and ecpAFifo at 000H
2. From the ecpDFifo located at 400H
3. To / from the tFifo at 400H.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

13. KEYBOARD CONTROLLER

The NCT6776F / NCT6776D KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

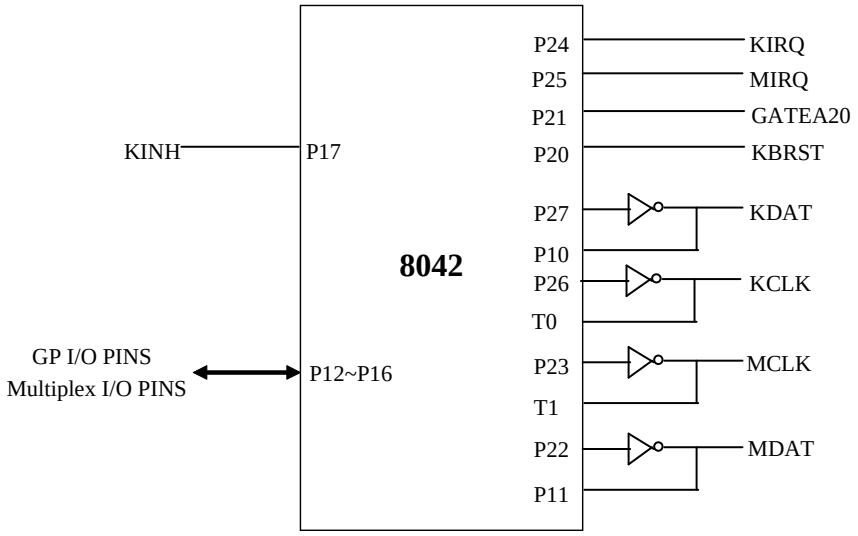


Figure 13-1 Keyboard and Mouse Interface

13.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

13.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

13.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 13-1 Bit Map of Status Register

BIT	BUT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

13.4 Commands

Table 13-2 KBC Command Sets

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>Aah</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>Abh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
<tr><td>Adh</td><td>Disable Keyboard Interface</td></tr>
</table>

COMMAND	FUNCTION
Aeh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into the STATUS register
C2h	Continuously puts the upper four bits of Port1 into the STATUS register
D0h	Send Port 2 value to the system
D1h	Only set / reset GateA20 line based on system data bit 1
D2h	Send data back to the system as if it came from the Keyboard
D3h	Send data back to the system as if it came from Auxiliary Device
D4h	Output next received byte of data from system to Auxiliary Device
E0h	Reports the status of the test inputs
FXh	Pulse only RC (the reset line) low for 6μs if the Command byte is even

13.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

13.5.1 KB Control Register (Logic Device 5, CR-F0)

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1.**	Select the KBC clock rate. **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: KBC clock input is 12 MHz. 1 1: Reserved
6	**KCLKS0.**	
5-3	**RESERVED.**	
2	**P92EN (Port 92 Enable).** 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	**HGA20 (Hardware GATEA 20).** 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	**HKBRST# (Hardware Keyboard Reset).** 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a “D1” command, the hardware control logic sets or clears GATE A20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an “FE” command, the KBRESET is pulse low for 6 μs (Min.) with a 14 μs (Min.) delay.

GATE A20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATE A20 and KBRESET are merged with Port92 when the P92EN bit is set.

13.5.2 Port 92 Control Register (Default Value = 0x24)

BIT	7	6	5	4	3	2	1	0
NAME	RES. (0)		RES. (1)	RES. (0)		RES. (1)	SGA20	PLKBRST#
DEFAULT	0	0	1	0	0	1	0	0

BIT	DESCRIPTION
7-6	**RES. (0)**
5	**RES. (1)**
4-3	**RES. (0)**
2	**RES. (1)**
1	**SGA20 (Special GATE A20 Control)** 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST# (Pulled-low KBRESET).** A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

14. CONSUMER INFRARED REMOTE (CIR)

Regarding the receiving of IR Block, the hardware uses the sampling rates of 1us, 25us, 50us and 100us to calculate the widths of H Level and L Level. The results are saved/stored in 32*8 RX FIFO. The max widths of H Level and L Level will be determined by Sample Limit Count Register. During the receiving, the hardware will reflect the FIFO status in RX FIFO Status Register. In addition, the hardware also generates status, such as Data Ready, Trigger Level Reach, FIFO Overrun and FIFO underrun, in RC Status Register.

As for the transmission, the user has to set up the Carrier frequency and the transmission mode first and then writes the widths of H Level and L Level via TX FIFO. The hardware will add Carrier to H Level according to the transmission mode.

14.1 CIR Register Table

Table 14-1 CIR Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	R	WIREN	TXEN	RXEN	WRXINV	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
base+2	IREN	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
base+3	RXFCONT	RXFIFO Count							
base+4	CP	MODE	Reserved						Carrier Prescalar
base+5	CC	Carrier Period							
base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	TXFIFOCLR	R	Tx Trigger Level		RXFIFOCLR	R	Rx Trigger Level	
base+9	IRFIFOSTS	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	TX_FTA	TX_Empty	TX_Full
base+A	SRXFIFO	Sample RX FIFO							
base+B	TXFCONT	TX FIFO Count							
base+C	STXFIFO	Sample TX FIFO							
base+D	FCCH	Frame Carrier Count High Byte							
base+E	FCCL	Frame Carrier Count Low Byte							
base+F	IRFSM	R	Decoder FSM			R	Encoder FSM		

14.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**Received**	**WIREN**	**TXEN**	**RXEN**	**WRXINV**	**RXINV**	**Sample Period Select**	
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**Received**.
6	**Wide-band IR Enable**

5	**TX Enable** 1: Transmission Enable. After confirming that FIFO is not empty, the transmission starts (the hardware will wait until TX FIFO data are written). If TX Enable is set to 0 during the transmission, the transmission stops when the transmission of FIFO data is completed. 0: Transmission Disable.
4	**RX Enable**
3	**Wide-band IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1~0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

14.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
Name	**RDR**	**RTR**	**PE**	**RFO**	**TE**	**TTR**	**TFU**	**GH**
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**TX FIFO Empty** (Writing 1 will clear the bit).
2	**TX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
1	**TX FIFO Underrun** (Writing 1 will clear the bit).
0	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.

14.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0

NAME	RDR	RTR	PE	RFO	TE	TTR	TFU	GH
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**TX FIFO Empty**
2	**TX FIFO Trigger Level Reach**
1	**TX FIFO Underrun**
0	**Min Length Detected**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

14.1.4 RX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	**RX FIFO Count**

14.1.5 IR TX Carrier Prescalar Configuration Register (CP) – Base Address + 4

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Mode	Reserved						CP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Mode** 0 : DC Mode 1 : Pulse Mode
6~1	**Reserved**.
0	**Carrier Prescalar** (CP). This bit is set for the Prescalar value of the IR TX carrier

	frequency.

14.1.6 IR TX Carrier Period Configuration Register (CC) – Base Address + 5

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Period (CC)							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is set for IR TX carrier period. The actual carrier period will be: Period = 2 * (2 ^ (CP*2)) * (CC+1) / (System Clock), where the frequency = 1 / period, and System Clock = 24MHz. Setting CP and CC to 0 will cause stop the device to from use using anyno carrier at all (that is, no light modulation, just constant on and off periods). The period count value CC can be any number from 0 to 255.

14.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the high byte of the limited count in the IR RX mode.

14.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

14.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TXFIFOCLR	Reserved	TX Trigger Level		RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TX FIFO Cleared**.
6	**Reserved**.
5~4	**TX Trigger Level** **Bits** **5 4** 0 0: 31 0 1: 24 1 0: 16 1 1: 8
3	**RX FIFO Cleared**.
2	**Reserved**.
1~0	**RX Trigger Level** **Bits** **1 0** 0 0: 1 0 1: 8 1 0: 16 1 1: 24

14.1.10IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	TX_FTA	TX_Empty	TX_Full
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**IR Pending** 1: No Interrupt 0: Interrupt issue
6	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
5	**RX FIFO Trigger Level Active**.
4	**RX FIFO Empty Flag**.
3	**RX FIFO Full Flag**.
2	**TX FIFO Trigger Level Active**.

BIT	DESCRIPTION
1	**TX FIFO Empty Flag**.
0	**TX FIFO Full Flag**.

14.1.11IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6~0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

14.1.12TX FIFO Count– Base Address + 5

Attribute: Read

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	TX FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	**TX FIFO Count**

14.1.13IR Sample TX FIFO Register – Base Address + C

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample TX FIFO						

BIT	DESCRIPTION

7	**Voltage Level** 0: Low, 1: High
6~0	**TX data length** (Unit : Sample Period)

14.1.14IR Carrier Count High Byte Register – Base Address + D

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Count High Byte							

BIT	DESCRIPTION
7~0	**Carrier Count High Byte**. This byte records the total amount of the total rising edges until time-out event appears.

14.1.15IR Carrier Count Low Byte Register – Base Address + E

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Carrier Count Low Byte							

BIT	DESCRIPTION
7~0	**Carrier Count Low Byte**. This byte records the total amount of the the rising edges until time-out event appears.

After a time-out of reception on the learning receiver, this response is sent to tell the host the carrier frequency of the previous sample. The Carrier Count High Byte (ch) and Carrier Count Low Byte (cl) specify the cycle counts of cycles of the carrier. Carrier counts can also be thought ofregarded as the number of leading edges in the previous sample.

This is used toe calculation of the calculate carrier frequency is as followsfollowed:

$lastCarrierCount_{(decimal)}$ = ch*256+cl;

Thus,

Carrier frequency = (lastCarrierCount) / (irPacketOnDuration);

The **irPacketOnDuration** value is the total amount of time that the envelope of the signal was is high. The IR receiver should keep track of the time that of the high envelope is high and return it using this response.

This response is unsolicited. It is returned by the receiver when IR arrives but is never explicitly requested.

14.1.16IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved	Encoder FSM		

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved.**
6	**Decoder over status**
5	**Decoder continuing status**
4	**Decoder wait H status** 1: idle, 0: RX busy
3	**Reserved**.
2	**Encoder Idle Status**. 1: idle, 0: TX busy
1	**Encoder Read Status**
0	**Encoder Level Output Status**

14.1.17IR Minimum Length Register – Base Address + F

Attribute: Write Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	**Min Length Register**. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

15. CONSUMER INFRARED REMOTE (CIR) WAKE-UP

One of the features of the NCT6776F / NCT6776D is system boot-up by a remote controller. The hardware will store a specifically appointed key command from the IR remote controller in the FIFO of 67Byte.

The same key is required to re-boot the system after the computer shut-down. Such way can be applied to any remote controllers. Learning is necessary only at the first time.

15.1 CIR WAKE-UP Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	DEC_RST	Mode[1]	Mode[0]	RXEN	IgnoreEN	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	GH	R	R	IR Pending
base+2	IREN	RDR	RTR	PE	RFO	GH	R		
Base+3		FIFO_COMPARE_DEEP							
base+4		FIFO_COMPARE_TOLERANCE							
base+5		FIFO_Count							
Base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	R				RXFIFOCLR	R	Rx Trigger Level	
base+9	SRXFSTS	GS	FTA	Empty	Full	R			
base+A		Sample RX FIFO							
base+B		WR_FIFO_DATA							
Base+C		Read FIFO Only							
Base+D		Read FIFO Only Index							
Base+E		FIFO_Ignore							
Base+F	IRFSM	R	Decoder FSM			R			Wakeup Event

15.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	**DEC_RST**	**Mode[1]**	**Mode[0]**	**RXEN**	**Received**	**RXINV**	**Sample Period Select**	
DEFAULT	0	0	1	0	0	1	1	0

BIT	DESCRIPTION
7	**Reset CIR DECODER** (Write 1 to clear)
6	**Mode[1]** : 0: FIFO can't be written 1: FIFO can be written
5	**Mode[0]** 0: Learning Mode

BIT	DESCRIPTION
	1: Wake up Mode (Before enter in Power S3 state, this bit should be set) This bit reset by VCC.
4	**RX Enable**
3	**Ignore Bit Enable**
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1~0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

15.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Received		IR_Pending
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.
2~1	**Reserved**.
0	**IR Pending** 1: No Interrupt 0: Interrupt issue

15.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**Min Length Detected**
2~0	**Reserved**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

15.1.4 IR TX Configuration Register – Base Address + 3

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Deep							
DEFAULT	0	1	0	0	0	0	1	1

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	When in S3 state, how many bytes need to compare. Default is 67 bytes.

15.1.5 IR FIFO Compare Tolerance Configuration Register – Base Address + 4

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Tolerance							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	**FIFO Data Tolerance between Learning mode and Wakeup mode**. (Every byte) FIFO Date Tolerance = (Learning mode data) – (Wakeup mode data)

15.1.6 RX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7~0	RX FIFO Count

15.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the high byte of the limited count in the IR RX mode.

15.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

15.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~4	**Reserved**
3	**RX FIFO Cleared.**
2	**Reserved.**
1~0	**RX Trigger Level** **Bits** **1 0** 0 0: 67

	0 1: 66 1 0: 65 1 1: 64

15.1.10IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	GS	FTA	Empty	Full	Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
6	**RX FIFO Trigger Level Active.**
5	**RX FIFO Empty Flag**.
4	**RX FIFO Full Flag**.
3~0	**Reserved**

15.1.11IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

15.1.12Write FIFO – Base Address + B

Attribute: Write Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Write Sample RX FIFO						

BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	**RX data length** (Unit : Sample Period)

Note. Before writing FIFO Data, mode[1] register should be set.

15.1.13Read FIFO Only – Base Address + C

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7~6	**Voltage Level** 0: Low, 1: High
0	RX data length (Unit : Sample Period)

Note. Only Read FIFO Data.

15.1.14Read FIFO Index – Base Address + D

Attribute: Read Only

Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Index							

BIT	DESCRIPTION
7~0	Indicate that FIFO Index when only read FIFO data(Base Address + C)

Note. Only Read FIFO Data.

15.1.15Reserved – Base Address + E

15.1.16 IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved			Wake up event
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6~4	CIR State Machine
3~1	Reserved
0	**Wake up event:** 0: CIR wake up event has not been triggered. 1: CIR wake up event has been triggered. (Wake up event clear: Write 11b to “Logic Decice A, CRE8h, bit7~6” then 00b.)

15.1.17IR Minimum Length Register – Base Address + F

Attribute: Write Only
Size: 8 bits

BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Min Length Register. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

16. POWER MANAGEMENT EVENT

The PME# (pin 65) signal is connected to the South Bridge and is used to wake up the system from S1 sleeping states.

One control bit and four registers in the NCT6776F / NCT6776D are associated with the PME function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME function. If this bit is set to "0", the NCT6776F / NCT6776D won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events Note.1.

1) The PME status registers of wake-up event:
   - At Logical Device A, CR[F3h] and CR[F4h]
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
2) The PME interrupt registers of wake-up event:
   - At Logical Device A, CR[F6h] and CR[F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the NCT6776F / NCT6776D supports include:

- Mouse event*
- Keyboard event*
- GP41, GP46, GP92, GP93 events
- CIR*
- Printer IRQ event
- Floppy IRQ event
- UART A IRQ event
- IR IRQ event
- Hardware Monitor IRQ event
- WDT1 event
- RIB (UARTB Ring Indicator) event

Note.2 All the above support both S0 and S1 states. Events with the "*" mark can use PSOUT# to wake up the system from S3 ~ S5 states.

16.1 Power Control Logic

This chapter describes how the NCT6776F / NCT6776D implements its ACPI function via these power control pins: PSIN# (Pin 61), PSOUT# (Pin 60), SLP_S3# (Pin 64) and PSON# (Pin 63). The following figure illustrates the relationships.

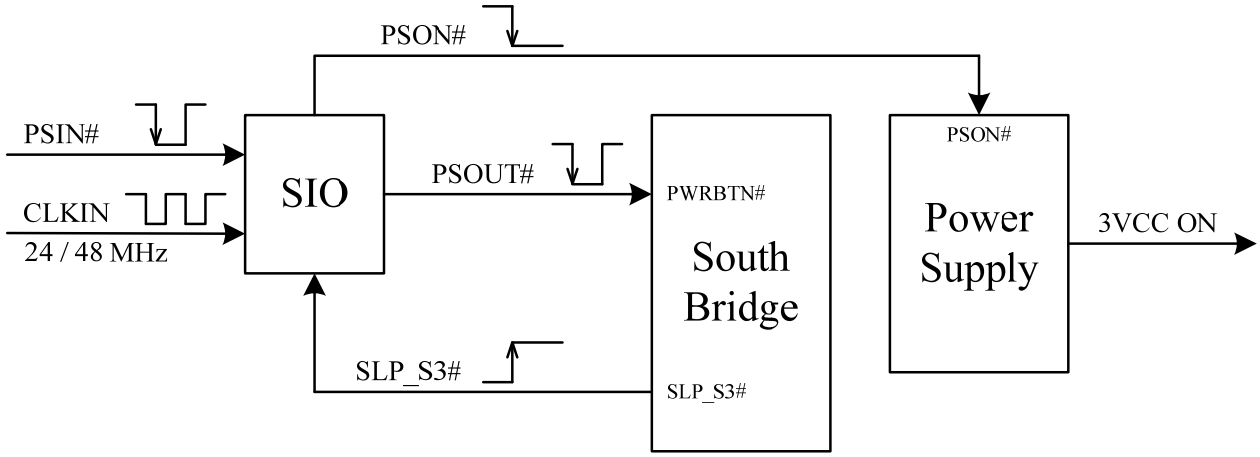


Figure 16-1 Power Control Mechanism

16.1.1 PSON# Logic

16.1.1.1. Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SLP_S3# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 16-2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

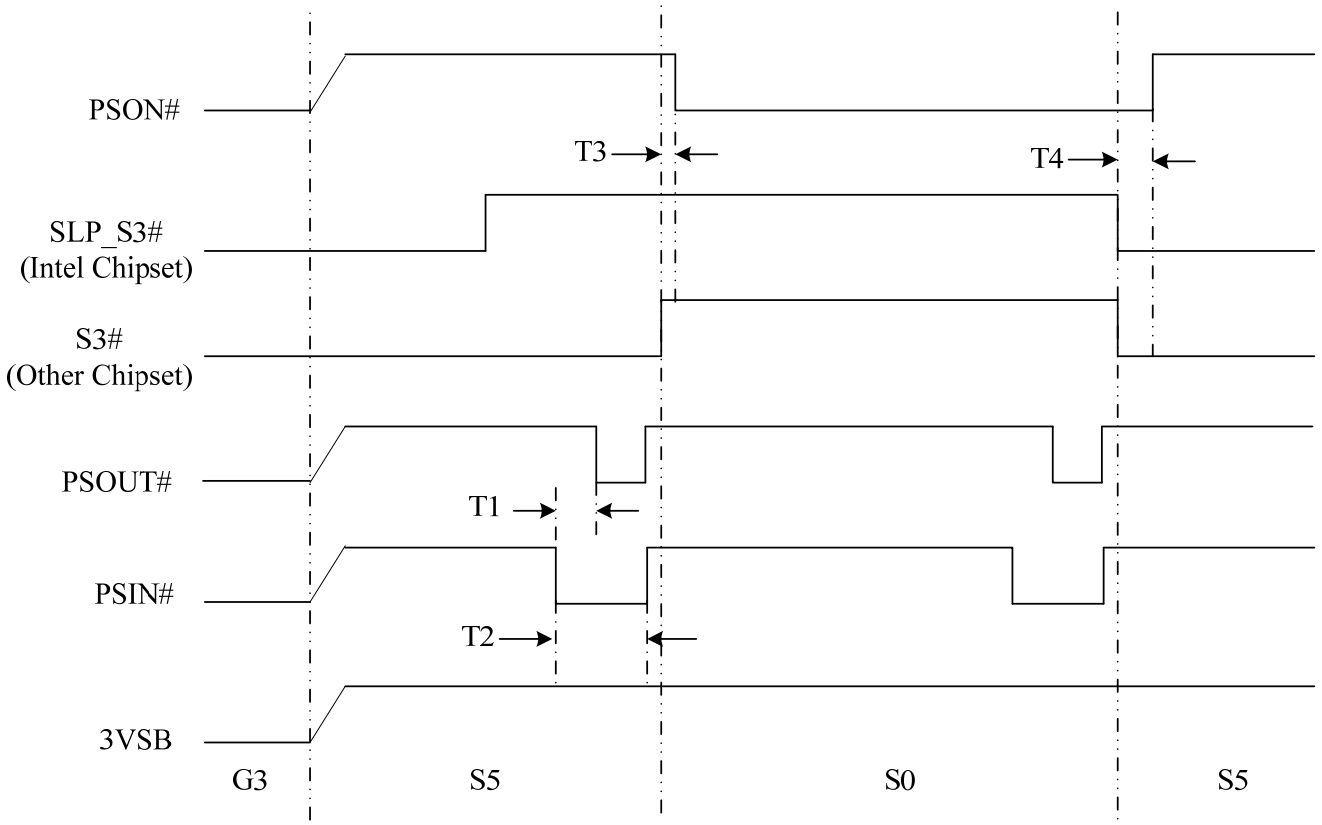


Figure 16-2 Power Sequence from S5 to S0, then Back to S5

16.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the NCT6776F / NCT6776D is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

Table 16-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
11	User defines the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

Note1. The NCT6776F / NCT6776D detects the state before power failure (on or off) through the SLP_S3# signal and the 3VCC power. The relation is illustrated in the following two figures.

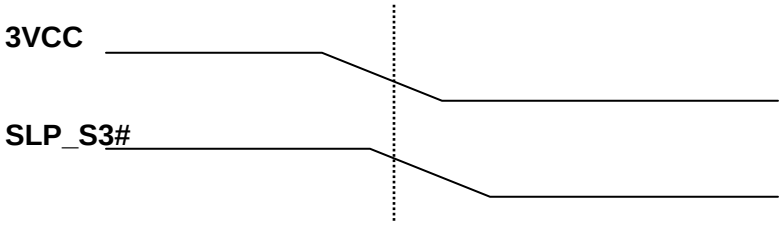


Figure 16-3 The previous state is “on”

3VCC falls to 2.6V and SLP_S3# keeps at 2.0V.

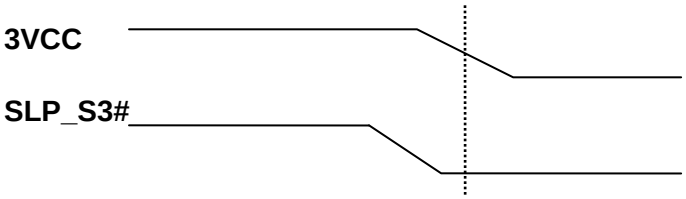


Figure 16-4 The previous state is “off”.

3VCC falls to 2.6V and SLP_S3# keeps at 0.8V.

Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6776F / NCT6776D adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system is returned to the pre-defined state after the AC power recovery.

16.2 Wake Up the System by Keyboard and Mouse

The NCT6776F / NCT6776D generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the NCT6776F / NCT6776D works.

16.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to “1”.

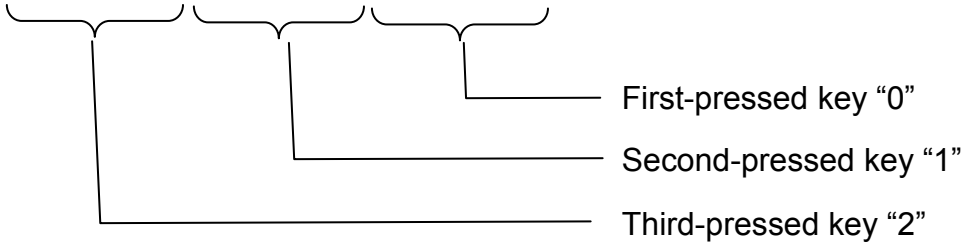
There are two keyboard events can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR[E0h] to “1” (Default).
2) Specific keys (Password) – Set bit 0 at Logical Device A, CR[E0h] to “0”.

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make code and a 2-byte break code. For example, the make code of “0” is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set “012” as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.

Index(CRE1)→	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data(CRE2)→	1E	F0	1E	16	F0	16	45	F0	45	00	00	00	00	00	00



16.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to “1”.

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 16-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

16.3 Resume Reset Logic

The RSMRST# (Pin 101) signal is a reset output and is used as the VSB power on reset signal for the South Bridge.

When the NCT6776F / NCT6776D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 16-5 and Table 16-3.

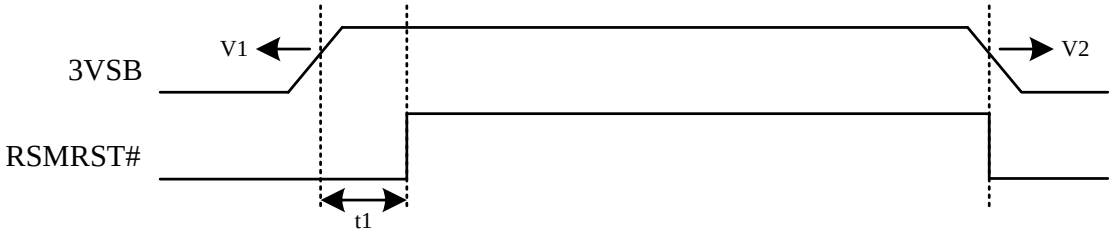


Figure 16-5 Mechanism of Resume Reset Logic

Table 16-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	-	3.033	V
V2	3VSB Ineffective Voltage	2.882	-	V
t1	Valid 3VSB to RSMRST# inactive	100	200	mS

17. SERIALIZED IRQ

The NCT6776F / NCT6776D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

17.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT6776F / NCT6776D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT6776F / NCT6776D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

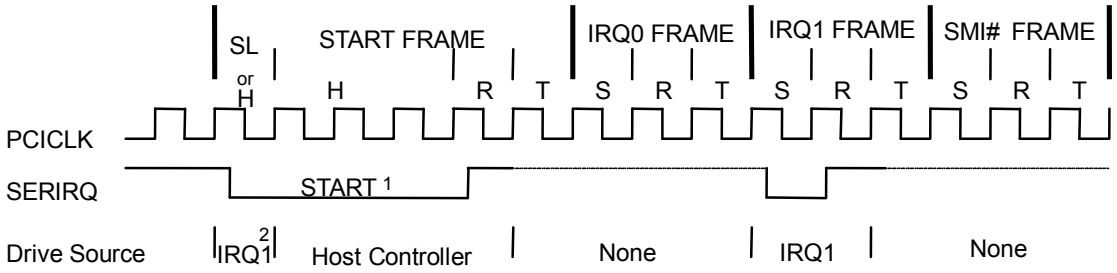


Figure 17-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT6776F / NCT6776D because IRQ1 of the NCT6776F / NCT6776D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

17.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT6776F / NCT6776D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT6776F / NCT6776D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT6776F / NCT6776D device drives the SERIRQ high. During the Turn-around phase, the NCT6776F / NCT6776D device leaves the SERIRQ tri-stated. The NCT6776F / NCT6776D starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 17-1.

Table 17-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	IR
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	FDC
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

17.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

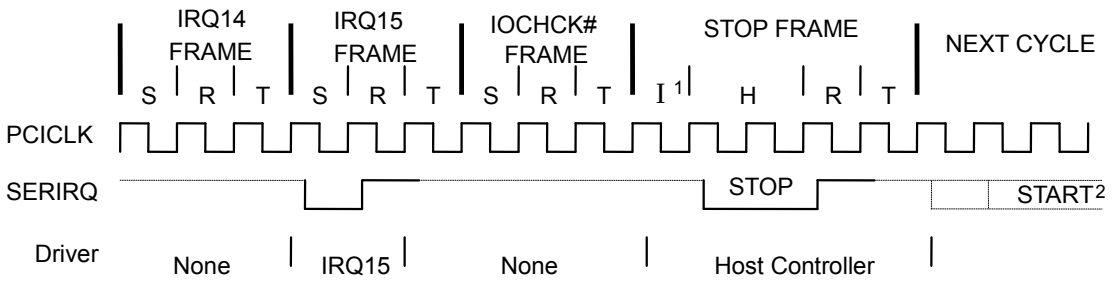


Figure 17-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

18. WATCHDOG TIMER

The Watchdog Timer of the NCT6776F / NCT6776D consists of an 8-bit programmable time-out counter and a control and status register. GPIO0, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO8, GPIO9, GPIOA provides an alternative WDT1 function. This function can be configured by the relative GPIO control register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 1 time-out event is occurring, GPIO0, bit[0],[3],[4],[7], GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO8, bit[0],[4], and GPIO9, GPIOA, bit[0] will trigger a low pluse apporx 100mS. In other words, when the value is counted down to zero, the timer stops, and the NCT6776F / NCT6776D sets the WDT1 status bit in Logical Device 8, CR[F7h], bit[4]. Writing a zero will clear the status bit. it. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

19. GENERAL PURPOSE I/O

19.1 GPIO ARCHITECTURE

The NCT6776F / NCT6776D provides 76 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non–inverse, 1 = inver-se). Port value is read/write through data register.

In addition, only **GP41, GP46, GP92 and GP93** are designed to be able to assert **PSOUT# or PME#** signal to wake up the system if any of them has any transitions. There are about 16ms debounced circuit inside these 4 GPIOs and it can be disabled by programming respective bit (LD9, CR[Feh] bit 4~7). Users can set what kind of event type, level or edge, and polarity, rising or falling, to perform the wake-up function. The following table gives more detailed register map on GP41, GP46, GP92 and GP93.

Table 19-1 Relative Control Registers of **GPIO 41, 46, 92 and 93** that Support Wake-Up Function

	EVENTROUTE I (PSOUT#) **0: DISABLE** **1: ENABLE**	**EVENTROUTE II (PME#)** **0: DISABLE** **1: ENABLE**	**EVENT DEBOUNCED** **0 : ENABLE** **1 : DISABLE**	**EVENT TYPE** **0 : EDGE** **1: LEVEL**	**EVENT POLARITY** **0 : RISING** **1 : FALLING**	**EVENT STATUS**
GPIO41 (PIN52)	LDA, CR[FEh] bit7	LDA, CR[FEh] bit3	LD9, CR[FEh] bit4	LD9, CR[FEh] bit0	LD9, CR[F2h] bit1	LD9, CR[E8h] bit1
GPIO46 (PIN38)	LDA, CR[FEh] bit6	LDA, CR[FEh] bit2	LD9, CR[FEh] bit5	LD9, CR[FEh] bit1	LD9, CR[F2h] bit6	LD9, CR[E8h] bit6
GPIO92 (PIN76)	LDA, CR[FEh] bit5	LDA, CR[FEh] bit1	LD9, CR[FEh] bit6	LD9, CR[FEh] bit2	LD7, CR[EAh] bit2	LD9, CR[EBh] bit2
GPIO93 (PIN75)	LDA, CR[FEh] bit4	LDA, CR[FEh] bit0	LD9, CR[FEh] bit7	LD9, CR[FEh] bit3	LD7, CR[EAh] bit3	LD9, CR[EBh] bit3

Table 19-2 GPIO Group Programming Table

Equips maximum 76-pin GPIOs.

GPIO0 Group

Enable: Logic Device 8, CR30[1]
Data: Logic Device 8, E0~E3
Multi-function: WDTO, SMI, BEEP, WDTO, WDTO, SMI, BEEP, WDTO (Logic Device 8, CRE4[0~7])
Reset: Logic Device A, CRE9[0]
OD/PP: Logic Device F, CRE9

Name	**Pin**	**Default function**	**Default type**	**GPIO power plane**	**Switch default function to GPIO**
GP00	2	DEVDEN0	output (OD)	3VCC	CR24[6] =1

GP01	4	MOA#	output (OD)	3VCC	
GP02	5	DSA#	output (OD)	3VCC	
GP03	8	WD#	output (OD)	3VCC	
GP04	9	WE#	output (OD)	3VCC	
GP05	11	WP#	input	3VCC	
GP06	12	RDATA#	input	3VCC	
GP07	13	HEAD#	output (OD)	3VCC	

GPIO1 Group

Enable: Logic Device 9, CR30[1]
Data: Logic Device 8, F0~F3
Multi-function: GRN, YLW, GRN, YLW, GRN, YLW, GRN, YLW (Logic Device 8, CRF4[0~7])
Reset: Logic Device A, CRE9[1]
OD/PP: Logic Device F, CRE0

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP10	123	VIDI0	input	3VSB	CR2A[5]=1
GP11	122	VIDI1	input	3VSB	
GP12	121	VIDI2	input	3VSB	
GP13	120	VIDI3	input	3VSB	
GP14	119	VIDI4	input	3VSB	
GP15	118	VIDI5	input	3VSB	
GP16	117	VIDI6	input	3VSB	
GP17	116	VIDI7	input	3VSB	

GPIO2 Group

Enable: Logic Device 9, CR30[2]
Data: Logic Device 9, E0~E3
Multi-function: WDTO, SMI, BEEP, GRN, WDTO, SMI, BEEP, GRN (Logic Device 9, CRE9[0~7])
Reset: Logic Device A, CRE9[2]
OD/PP: Logic Device F, CRE1

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP20	59	KDAT	bi-direction	3VSB	CR2A[0]=1
GP21	58	KCLK	bi-direction	3VSB	
GP22	57	MDAT	bi-direction	3VSB	CR2A[1]=1
GP23	56	MCLK	bi-direction	3VSB	
GP24	95	CIRRX	input	3VSB	CR27[3]=0, CR1B[4]=0
GP25	96	GP25	output	3VSB	
GP27	98	AUXFANOUT	output	3VSB	CR2C[7]=0

GPIO3 Group

Enable: Logic Device 9, CR30[3]
Data: Logic Device 9, E4~E7
Multi-function: WDTO, SMI, BEEP, GRN, WDTO, SMI, BEEP, GRN (Logic Device 9, CREA[0~7])
Reset: Logic Device A, CRE9[3]
OD/PP: Logic Device F, CRE2

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP30	84	SLP_S5#		input		3VSB	CR2B[0]=1
GP31	83	RESETCON#		input		3VSB	CR2B[1]=1
GP32	82	PWROK		output (OD)		3VSB	CR2B[2]=1
GP33	81	CPUPWRGD		output (OD)		3VSB	CR2B[3]=1
GP34	80	ATXPGD		input		3VSB	CR2B[4]=1
GP35	79	RSTOUT0#		output (OD)		3VSB	CR2B[5]=1
GP36	78	RSTOUT1#		output (OD)		3VSB	CR2B[6]=1
GP37	77	{ DSW_EN }		{ DSW_EN }		3VSB	CR2B[7]=1, DSW_EN = 0
		0	RSTOUT2#	0	output		
		1	SLP_SUS_FET	1	output (OD)		

GPIO4 Group

Enable: Logic Device 9, CR30[4]
Data: Logic Device 9, F0~F2, E8
Multi-function: WDTO, SMI, BEEP, YLW, WDTO, SMI, BEEP, YLW (Logic Device 9, CREE[0~7])
Reset: Logic Device A, CRE9[4]
OD/PP: Logic Device F, CRE3

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP40	62	SLP_S5#_LATCH		output		3VSB	CR1B[3]=0
GP41	52	{ LPT_EN }		{ LPT_EN }		3VSB	CR1A[3:2]=10, LPT_EN=0
		0	MSCL	0	input		
		1	INIT#	1	otput		
GP42	51	{ LPT_EN }		{ LPT_EN }		3VSB	CR1B[2:1]=11, LPT_EN=0
		0	MSDA	0	input		
		1	SLIN#	1	output		
GP43	41	{ LPT_EN }		{ LPT_EN }		3VSB	CR27[4]=1, LPT_EN=0
		0	DGL#	0	output		
		1	ACK#	1	input		
GP44	40	{ LPT_EN }		{ LPT_EN }		3VSB	CR1B[6]=0, LPT_EN=0
		0	GRN_LED	0	output		
		1	BUSY	1	input		
GP45	39	{ LPT_EN }		{ LPT_EN }		3VSB	
		0	YLW_LED	0	output		
		1	PE	1	input		
GP46	38	{ LPT_EN }		{ LPT_EN }		3VSB	
		0	GP46	0	input		
		1	SLCT	1	input		
GP47	37	RESETCONO#		output(OD)		3VSB	CR1B[7]=1

GPIO5 Group
Enable: Logic Device 9, CR30[5]
Data: Logic Device 9, F4~F7
Multi-function: WDTO, SMI, BEEP, GRN, WDTO, SMI, BEEP, GRN (Logic Device 8, CREB[0~7])
Reset: Logic Device A, CRE9[5]
OD/PP: Logic Device F, CRE4

Name	Pin	Default function		Default type		GPIO power plane	Switch default function to GPIO
GP50	71	3VSBSW#		output		3VSB	CR2C[6:5]=01
GP51	64	SLP_S3#		input		3VSB	CR2D[1]=1
GP52	63	{ AMDPWR_EN }		{ AMDPWR_EN }		3VSB	CR2D[2]=1
		0	PSON#	0	output		
		1	AMD_PSON#	1	output		
GP53	61	PSIN#		Input		3VSB	CR2D[3]=1
GP54	60	PSOUT#		output		3VSB	CR2D[4]=1
GP55	55	{ DSW_EN, AMDPWR_EN, LPT_EN }		{ DSW_EN, AMDPWR_EN, LPT_EN }		3VSB	CR27[0]=0
		1XX	GP55	1XX	input		
		00X	ALERTO#	00x	output		
		011	STB#	011	output		
GP56	54	{ DSW_EN, AMDPWR_EN, LPT_EN }		{ DSW_EN, AMDPWR_EN, LPT_EN }		3VSB	
		1XX	SLP_SUS#	1XX	input		
		00X	ALERTI#	00X	input		
		011	AFD#	010	output		
		010	GP56	011	input		
GP57	53	{ LPT_EN }		{ LPT_EN }		3VSB	CR1B[5]=0, LPT_EN=0
		0	VID_RST#	0	input		
		1	ERR#	1	input		

GPIO6 Group
Enable: Logic Device 9, CR30[6]
Data: Logic Device 7, F4~F7
Multi-function: WDTO, SMI, BEEP, GRN, WDTO, SMI, BEEP, GRN (Logic Device 8, CRF8[0~7])
Reset: Logic Device A, CRE5[3]
OD/PP: Logic Device F, CRE5

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP60	50	LPT_EN = 0	LPT_EN = 0	3VSB	CR27[4]=1, LPT_EN=0
GP61	49	LED_A~LED_G, DGH#	output	3VSB	
GP62	48			3VSB	
GP63	47	LPT_EN = 1	LPT_EN = 1	3VSB	
GP64	45	PD0 ~ PD7	bi-direction	3VSB	
GP65	44			3VSB	
GP66	43			3VSB	

GP67	42			3VSB	

GPIO7 Group
Enable: Logic Device 9, CR30[7]
Data: Logic Device 7, E0~E3
Multi-function: GRN, YLW, GRN, YLW, GRN, YLW, GRN, YLW (Logic Device 8, CREC[0~7])
Reset: Logic Device A, CRE5[4]
OD/PP: Logic Device F, CRE7

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP70	93	DSW_EN | AMDPWR_EN = 1 VIDO0~VIDO5 DSW_EN | AMDPWR_EN = 0 DSW function	DSW_EN | AMDPWR_EN = 1 output	3VSB	CR27[7]=1
GP71	92			3VSB	
GP72	91			3VSB	
GP73	90			3VSB	
GP74	89			3VSB	
GP75	88			3VSB	
GP76	87	{ AMDPWR_EN } 0 VIDO6 1 VCORE_EN	{ AMDPWR_EN } 0 output 1 output	3VSB	CR27[6]=1
GP77	86	{ AMDPWR_EN } 0 VIDO7 1 VLDT_EN	{ AMDPWR_EN } 0 VIDO7 1 VLDT_EN	3VSB	

GPIO8 Group
Enable: Logic Device 7, CR30[0]
Data: Logic Device 7, E4~E7
Multi-function: WDTO, SMI, BEEP, YLW, WDTO, SMI, BEEP, YLW (Logic Device 7, CRED[0~7])
Reset: Logic Device A, CRE5[5]
OD/PP: Logic Device F, CRE7

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP80	29	GP80	input	3VSB	
GP81	30	GP81	input	3VSB	
GP82	31	GP82	output	3VSB	
GP83	32	GP83	output	3VSB	
GP84	33	GP84	input	3VSB	
GP85	34	GP85	output	3VSB	
GP86	35	GP86	input	3VSB	
GP87	36	GP87	input	3VSB	

GPIO9 Group
Enable: Logic Device 7, CR30[1]
Data: Logic Device 7, E8~EB
Multi-function: WDTO, SMI, BEEP, GRN (Logic Device 7, CREE[0~3])
Reset: Logic Device A, CRE5[6]
OD/PP: Logic Device F, CRE8

Name	Pin	Default function	Default type	GPIO power plane	Switch default function to GPIO
GP90	102	SKTOCC#	input	3VSB	CR2D[7]=1

GP91	101	RSMRST#	output	3VSB	CR2D[6]=1
GP92	76	GP92	input	3VSB	
GP93	75	GP93	input	3VSB	
GPIOA Group Enable: Logic Device 8, CR30[2] Data: Logic Device 17, E0~E3 Multi-function: WDTO (Logic Device 17, CRE5[0]) Reset: Logic Device A, CRE5[7] OD/PP: Logic Device 17, CRE4					
Name	**Pin**	**Default function**	**Default type**	**GPIO power plane**	**Switch default function to GPIO**
GPA0	113	TSIC	output	3VCC	CR2C[0]=0

19.2 ACCESS CHANNELS

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS trapping). The registers can be read / written only when the respective logical device ID and port number are selected.

The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 7 registers are defined in table 19-2. Base address plus 0 to 4 are GPIO registers, base address plus 5 and 6 are watchdog registers.Since the base address is set, the GPIO number can be selected by writing the group number to GSR [INDEX] (GPIO Select Register, #0~#A for GPIO0 ~ GPIOA respectively). Then the I/O register, the Data register and the Inversion register are mapped to addresses Base+0, Base+1 and Base+2 respectively. Only one GPIO can be accessed at one time.

Table 19-3 GPIO Register Addresses

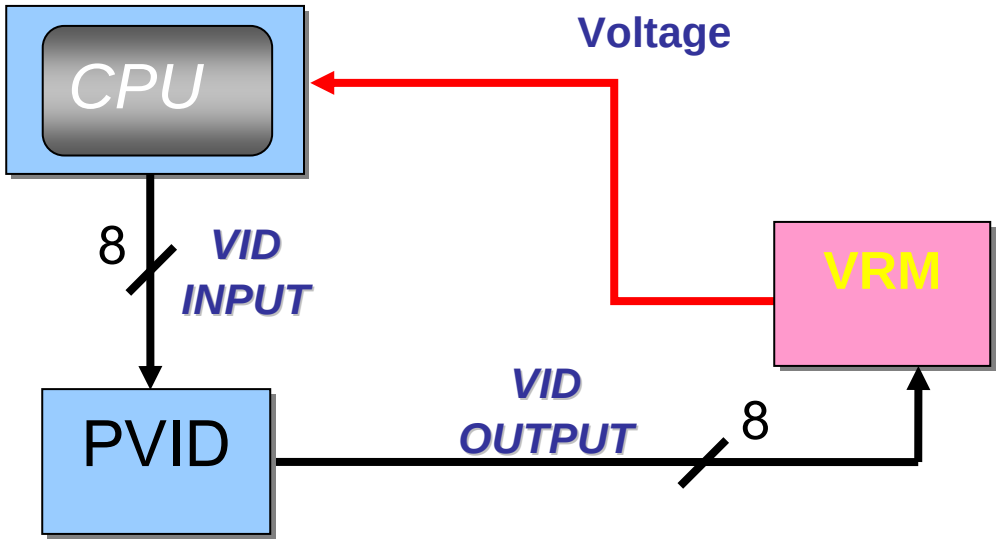
ADDRESS	ABBR	BIT NUMBER							
		7	6	5	4	3	2	1	0
Base + 0	GSR	Reserved				INDEX			
Base + 1	IOR	GPIO I/O Register							
Base + 2	DAT	GPIO Data Register							
Base + 3	INV	GPIO Inversion Register							
Base + 4	DST	GPIO Status Register							
Base + 5	Wdtmod	Watchdog Timer I (WDT1) and KBC P20 Control Mode Register							
Base + 6	Wdttim	Watchdog Timer I (WDT1) Control Register							

20. PARALLEL VID (PVID)

The NCT6776F / NCT6776D provides individual eight pins for VID input and output function. These pins can be configured by setting Logical Device D, CR [E0h] to CR [E4h]. The configuration is applied to four modes, By-pass mode, Manual mode, Offset mode, and Maximum mode. More details can refer to Logical Device D, CR [E0h] to CR [E4h].

Logic Device D, CRE4 bit [7:6]	VID Mode Selection
00	Bypass mode (default)
01	Offset makeup mode
10	Manual mode
11	Max mode (manual, VID_IN)

Logic Device D, CRE4 bit[2:0]	Tables	Voltage/step
000	AMD 5-bit	25mV
010	AMD 6-bit	25mV
100	VRM 10.1 (6-bit)	12.5 mV
101	VRM 10.2 (7-bit)	6.25 mV
11x	VRM 11.1 (8-bit) (default)	6.25 mV



VID input is decoded by SIO according VID table to VID output，and fed to VRM。

We support 2 table (amd6bit and vrm11) and 4 mode (bypass，offset，manual，compare) to decode different VID output。

To decide VID function，user should make sure CR2A[6:5] are 2'b10，if not， pin116~123 and pin 86~93 will be other function。

20.1 VID Input Detection

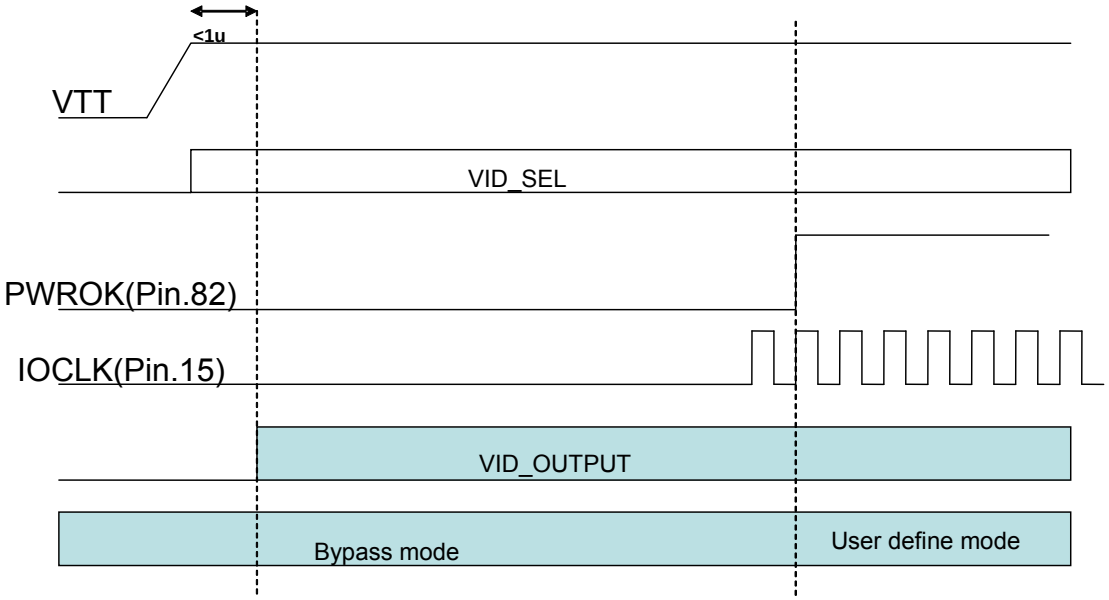
The NCT6776F / NCT6776D supports Intel VRM 9/10/11 and AMD 5/6-bit VID detections. VID input level is design for GTL. The transition point is at 0.7V ~ 0.8V.

20.2 VID Output Control

The output type of the eight VID pins is open-drain stage. The output data can be read in the data register (Logical Device D, CR[E2h], bit 7 ~ 0).

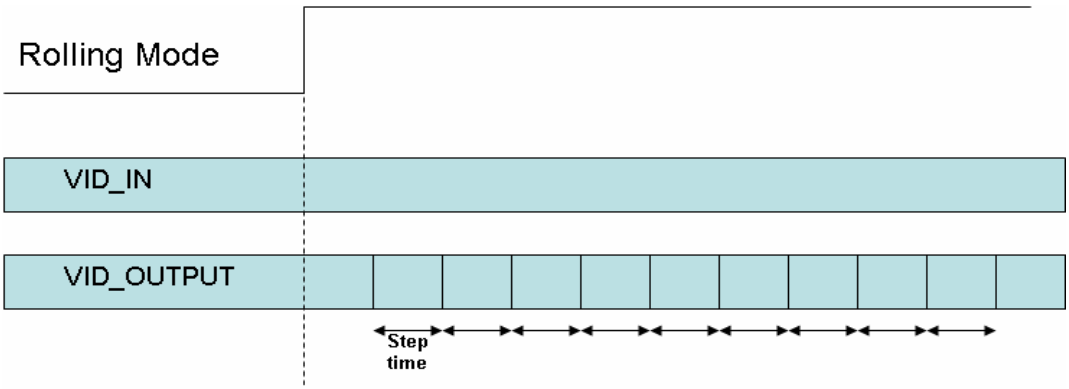
20.3 VID Reset Source

The reset source is illustrated below. SKTOCC# and RSMRST# are always effective. WDT1, POWEROK and LRESET# are optional and can be enable/disable by the respective mask registers.



User define mode includes: By-pass, Offset, Manual, MAX, and Rolling mode.
It will translate into user define mode after PWROK rising edge.

Mode configuration registers are reset by RSMRST



Rolling Mode :

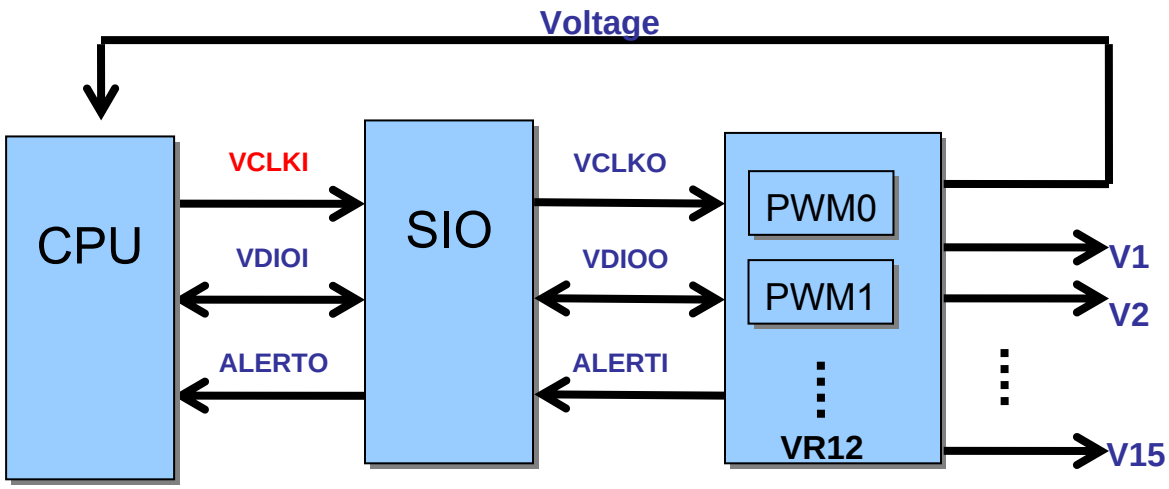
Disable : VID_OUT will reflect the VID_IN

Enable : VID_OUT will increase/decrease one step every step time when PWROK assert.

step time can set by register.

21. INTEL SERIAL VID (SVID)

Block Diagram



Intel Serial VID use *pmbus* to transmit serial data SVC and SVD, thus its max speed can up to 33MHz.We support 4 mode (Bypass; offset; manual; compare) liked as Parallel VID.

There are two strapping control to decide AMD SVID. One is DSW_EN, if it is “1”, then pin 69~66 will be DSW function, otherwise they are SVID function. Two is GP25 (CR2F[5]) , if it is “0”, then pin 69~66 will be Intel_SVID function, otherwise they are AMD_SVID function.

DSW_EN(Pin69)	GP25 (CR2F[5])	Pin69~66 Function
1	-	DSW function
0	1	AMD SVID
0	0	Intel SVID

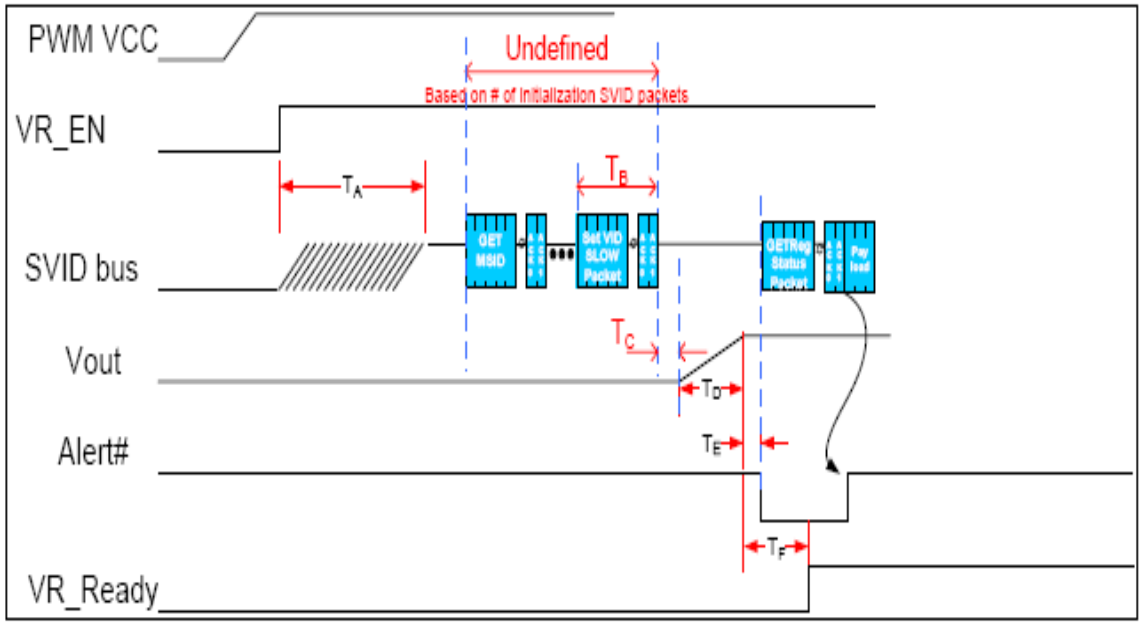


Fig. VRM Start Up Timing

As the Figure above showing，after VRM_EN active，SVID bus can transmit serial code by CPU to VRM。SVID will have multiple data packets to initialize the VRM and the process。Example of this are setting Vout_Max register，reading Icc_Max register etc, followed by SetVID_Slow to the initial voltage to start voltage ramp。

Description		Min	Typ	Max	Note
T_A	VR_EN until VR Controller is ready accept SVID command			**1 ms**	PWM IC must complete all internal analog and digital configuration and reset protocols during T_A.
T_B	Duration of SVID data packets and SetVID CMD @25 MHz typical.	**SVID protocol dependent**			Any number of packets may occur before 1 SetVID_Slow command
T_C	Acknowledge of SetVID_x CMD to start of voltage ramp, SVID protocol parameter	**0**		**600 ns**	Validate using reference change (600ns is IMVP spec today)
T_D	Voltage ramp time, (SetVID_slow ramp, target voltage dependent)		**440 us**	**2 ms**	Typ represents 1.1V @ SetVID slow 2.5 mV/us. Maximum represents maximum time with optional soft start programmed.
T_E	Completion of SetVID ramp to assertion of ALERT# signal			**1 us**	
T_F	Completion of SetVID ramp to assertion of associated VR_READY	**T_E actual**		**5 ms**	

Table. VR Start Up Timing

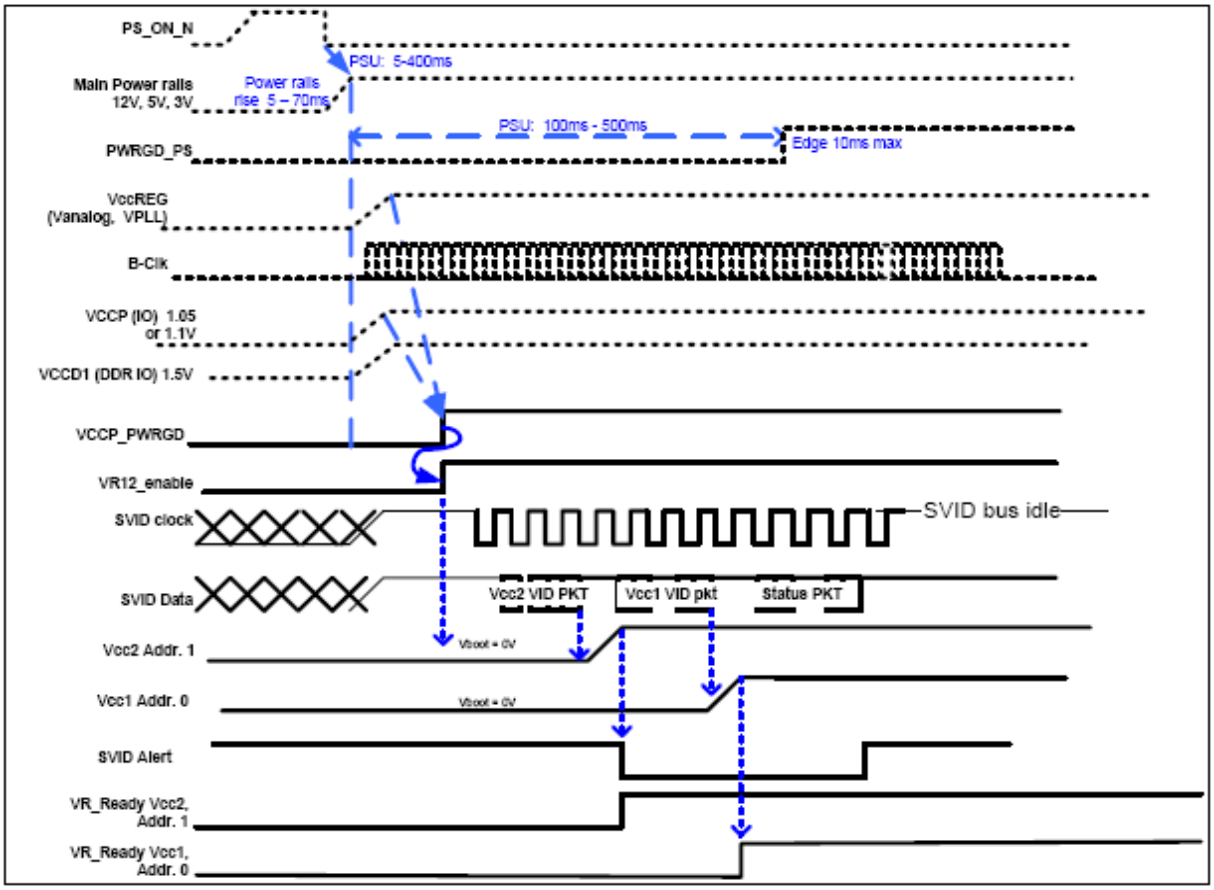


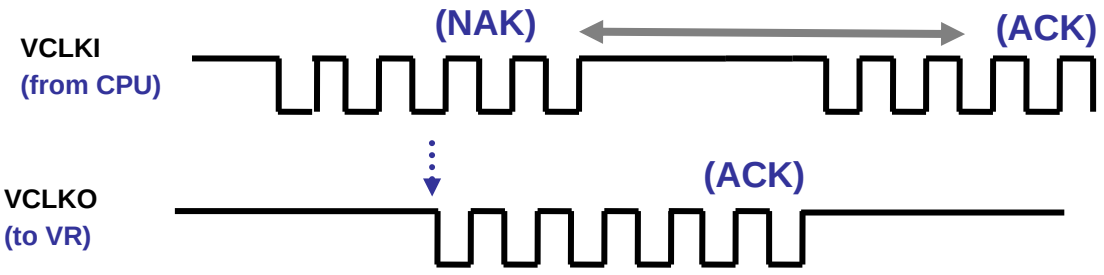
Fig. Typical Start Up Sequence On Each Rail

Intel define 16 individual address to multi_rail and 32 command to write or read from VR，but it reserve 8bit command to extend in the future。CPU can control the slew rate when set VID target by SetVID_fast or SetVID_slow or SetVID_Decay，and it can also Set specified register liked as SetRegADR and SetRegDAT。

	Command	Master Payload	Slave Payload
00h	Extended	Extended Command index	
01h	SetVID-fast(10mv/us)	VID code	N/A
02h	SetVID-slow(2.5mv/us)	VID code	N/A
03h	SetVID-Decay	VID code	N/A
04h	SetPS	Information to VR	N/A
05h	SetRegADR	Address pointer	N/A
06h	SetRegDAT	Data content	N/A
07h	GetReg	Address of Register	Specified register content
08h	Test Mode		N/A
…	Reserved		N/A
1Fh	Reserved		N/A

Table. Command Set (max:32)

If a VRM does not respond with acknowledge，the master detect the open drain 11b called NAK as reject。In order to intercept CPU Serial Code and transmit to VRM synchronously，we send *NAK* to CPU first when we receive a command frame and send the copy of Serial code to VRM。Because CPU can resend serial code，in the next transmission，we will send back CPU the real *ACK and data* from VRM。

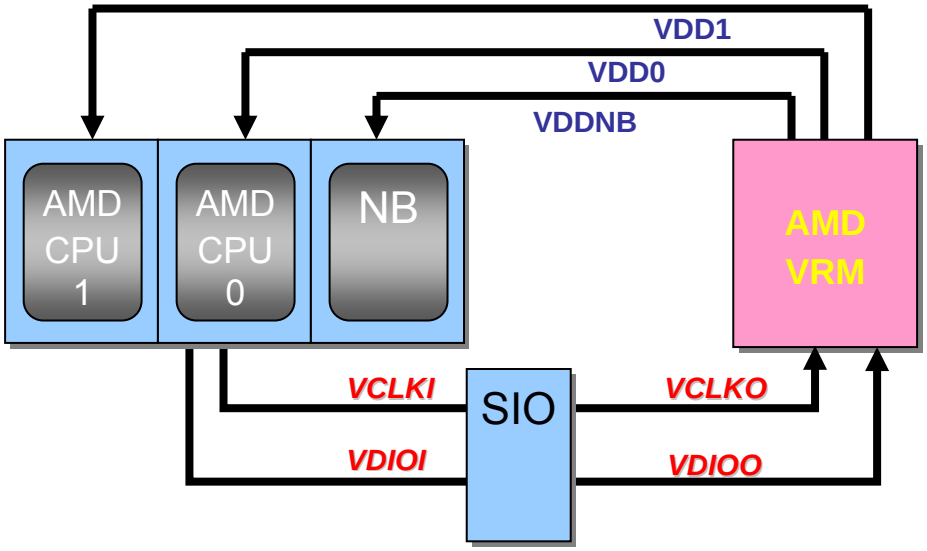


Pin out

PIN	SYMBOL	I/O	POWER WELL	Description
74 69 68 54	VRM_EN VDIOI VCLKI ALERTI	I	VSB	VR Enable VID input VID input ALERT input
67 66 55	VDIOO VCLKO ALERTO	O	VSB	VID output VID output ALERT output

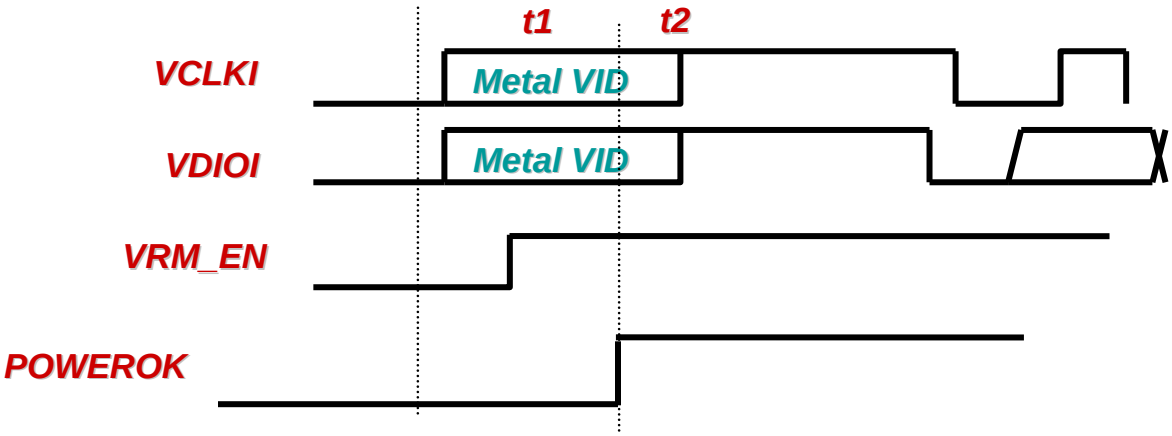
22. AMD SERIAL VID (SVID)

Block Diagram



AMD SVID use *smbus* to transmit serial data VCLK and VDIO, thus its max speed can up to 400KHz. We support 4 mode (Bypass; offset; manual; compare) liked as PVID, and we can control output frequency according *Factor_L* and *Factor_M* register.

There are two strapping control to decide AMD SVID. One is DSW_EN，if it is “1”. then pin 69~66 will be DSW function, otherwise they are SVID function. Two is GP25 (CR2F[5]), if it is “0”, then pin 69~66 will be Intel_SVID function, otherwise they are AMD_SVID function.

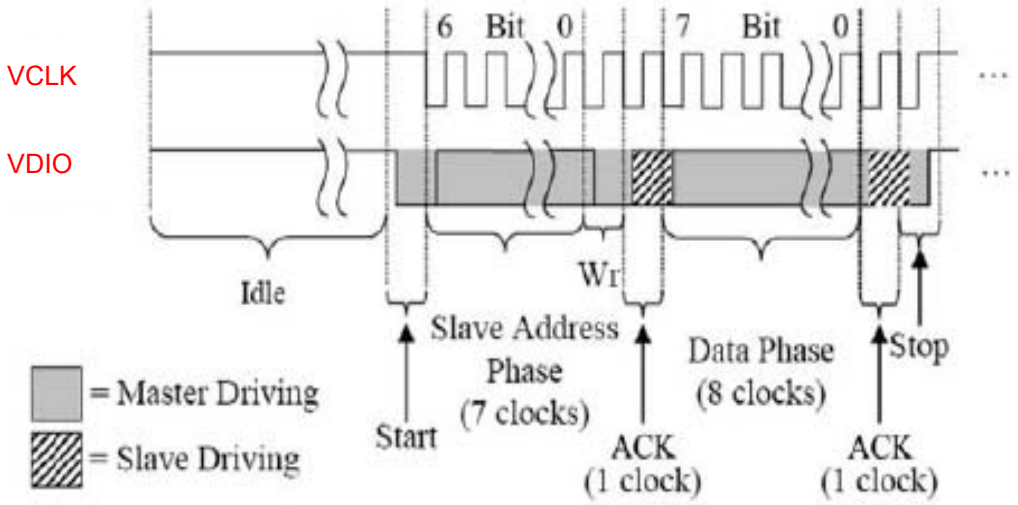


AMD SVID has two table, one is metal VID table and another is Serial table. When VRM_EN = 1 (t1), VRM should look up metal VID table to decode。After a while (t2), as CPU send Serial Code，VRM should look up serial table.

VCLK	VDIO	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Pre-PWROK 2-Bit Metal VID Codes

After system POWEROK signal detect，AMD processor will transmit serial VID code to VRM, and it is byte mode. It define three address (VDD0; VDD1; VDDNB) and six-bits table, thus we support three offsets and three manual data to control each VID code. Maybe process want to change VDD0 and VDD1 at the same time and it send ADD 0x66, but user could set different offset，thus, SIO will send two frame of serial VID protocol to VRM separately.



Bits	Description
6:4	Always 110b
3	Reserved for future use
2	VDD1, if set then the following data byte contains the VID for VDD1
1	VDD0, if set then the following data byte contains the VID for VDD0
0	VDDNB, if set then the following data byte contains the VID for VDDNB

Table: Serial VID Address table

SVID[6:0]	Voltage (V)	SVID[6:0]	Voltage (V)	SVID[6:0]	Voltage (V)		SVID[6:0]	Voltage (V)	
000_0000b	1.5500	010_0000b	1.1500	100_0000b	0.7500		110_0000b	0.3500	*
000_0001b	1.5375	010_0001b	1.1375	100_0001b	0.7375		110_0001b	0.3375	*
000_0010b	1.5250	010_0010b	1.1250	100_0010b	0.7250		110_0010b	0.3250	*
000_0011b	1.5125	010_0011b	1.1125	100_0011b	0.7125		110_0011b	0.3125	*
000_0100b	1.5000	010_0100b	1.1000	100_0100b	0.7000		110_0100b	0.3000	*
000_0101b	1.4875	010_0101b	1.0875	100_0101b	0.6875		110_0101b	0.2875	*
000_0110b	1.4750	010_0110b	1.0750	100_0110b	0.6750		110_0110b	0.2750	*
000_0111b	1.4625	010_0111b	1.0625	100_0111b	0.6625		110_0111b	0.2625	*
000_1000b	1.4500	010_1000b	1.0500	100_1000b	0.6500		110_1000b	0.2500	*
000_1001b	1.4375	010_1001b	1.0375	100_1001b	0.6375		110_1001b	0.2375	*
000_1010b	1.4250	010_1010b	1.0250	100_1010b	0.6250		110_1010b	0.2250	*
000_1011b	1.4125	010_1011b	1.0125	100_1011b	0.6125		110_1011b	0.2125	*
000_1100b	1.4000	010_1100b	1.0000	100_1100b	0.6000		110_1100b	0.2000	*
000_1101b	1.3875	010_1101b	0.9875	100_1101b	0.5875		110_1101b	0.1875	*
000_1110b	1.3750	010_1110b	0.9750	100_1110b	0.5750		110_1110b	0.1750	*
000_1111b	1.3625	010_1111b	0.9625	100_1111b	0.5625		110_1111b	0.1625	*
001_0000b	1.3500	011_0000b	0.9500	101_0000b	0.5500		111_0000b	0.1500	*
001_0001b	1.3375	011_0001b	0.9375	101_0001b	0.5375		111_0001b	0.1375	*
001_0010b	1.3250	011_0010b	0.9250	101_0010b	0.5250		111_0010b	0.1250	*
001_0011b	1.3125	011_0011b	0.9125	101_0011b	0.5125		111_0011b	0.1125	*
001_0100b	1.3000	011_0100b	0.9000	101_0100b	0.5000		111_0100b	0.1000	*
001_0101b	1.2875	011_0101b	0.8875	101_0101b	0.4875	*	111_0101b	0.0875	*
001_0110b	1.2750	011_0110b	0.8750	101_0110b	0.4750	*	111_0110b	0.0750	*
001_0111b	1.2625	011_0111b	0.8625	101_0111b	0.4625	*	111_0111b	0.0675	*
001_1000b	1.2500	011_1000b	0.8500	101_1000b	0.4500	*	111_1000b	0.0500	*
001_1001b	1.2375	011_1001b	0.8375	101_1001b	0.4375	*	111_1001b	0.0375	*
001_1010b	1.2250	011_1010b	0.8250	101_1010b	0.4250	*	111_1010b	0.0250	*
001_1011b	1.2125	011_1011b	0.8125	101_1011b	0.4125	*	111_1011b	0.0125	*
001_1100b	1.2000	011_1100b	0.8000	101_1100b	0.4000	*	111_1100b	OFF	
001_1101b	1.1875	011_1101b	0.7875	101_1101b	0.3875	*	111_1101b	OFF	
001_1110b	1.1750	011_1110b	0.7750	101_1110b	0.3750	*	111_1110b	OFF	
001_1111b	1.1625	011_1111b	0.7625	101_1111b	0.3625	*	111_1111b	OFF	

*Note: *Indicates a VID not required for AMD Family 10h processors. The vendor may either choose to support the indicated voltage at very low load (<1A) or supply the lowest supported non-zero voltage.*

Table: Serial VID 7 bits codes

Pin out

PIN	SYMBLE	I/O	POWER WELL	Description
74 69 68	VRM_EN VDIOI VCLKI	I	VSB	VRM Enable SVID input SVID input
67 66	VDIOO VCLKO	O	VSB	SVID output SVID output

23. SMBUS MASTER INTERFACE

23.1 General Description

The SMBus interface module is two wire serial interface compatible to the SMBus physical layer. It is also compatible with Intel's SMBus and Philips' I^2C bus.

The rest of this section introduces the various features of the SMBus master capability. These features are divided into the following sections:

- SMBus and I^2C compliant
- AMD-TSI
- PCH
- SMBus master

23.2 Introduction to the SMBus Master

23.2.1 Data Transfer Format

Every byte transferred on the bus consists of 8 bits. After the start condition, the master places the 7-bit address to the slave device it wants to address on the bus. The address followed an eight bit indicating the direction of the data transfer (R/W#); a zero indicates a transmission for data while a one indicates a request for data. Each byte is transferred with the most significant bit first, and after each byte, an acknowledge signal must follow. A data transfer is always terminated by stop condition generated by master.

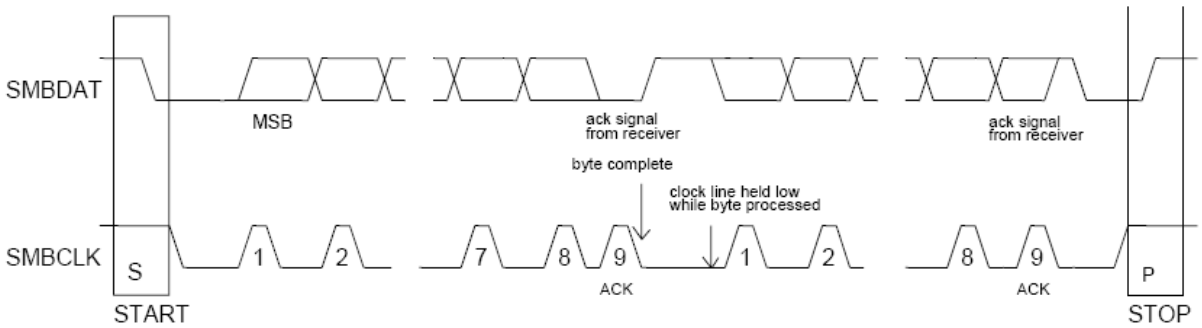


Figure 23-1 Data Transfer Format

23.2.2 Arbitration

Arbitration takes place on the SMBDAT data line while the SMBCLK line is high. Two devices may generate a start condition at the same time and enter the arbitration procedure. Arbitration continues until one master generates a HIGH level on the SMBDAT line while another competing master generates a LOW level on the SMBDAT line while SMBCLK is high. The master device which generated the HIGH level on SMBDAT loses arbitration. If a device loses arbitration during the first byte following a start condition i.e. while transmitting a slave address it becomes a slave receiver and monitors the address for a potential match. Arbitration may also be lost in the master receive mode during the acknowledge cycle.

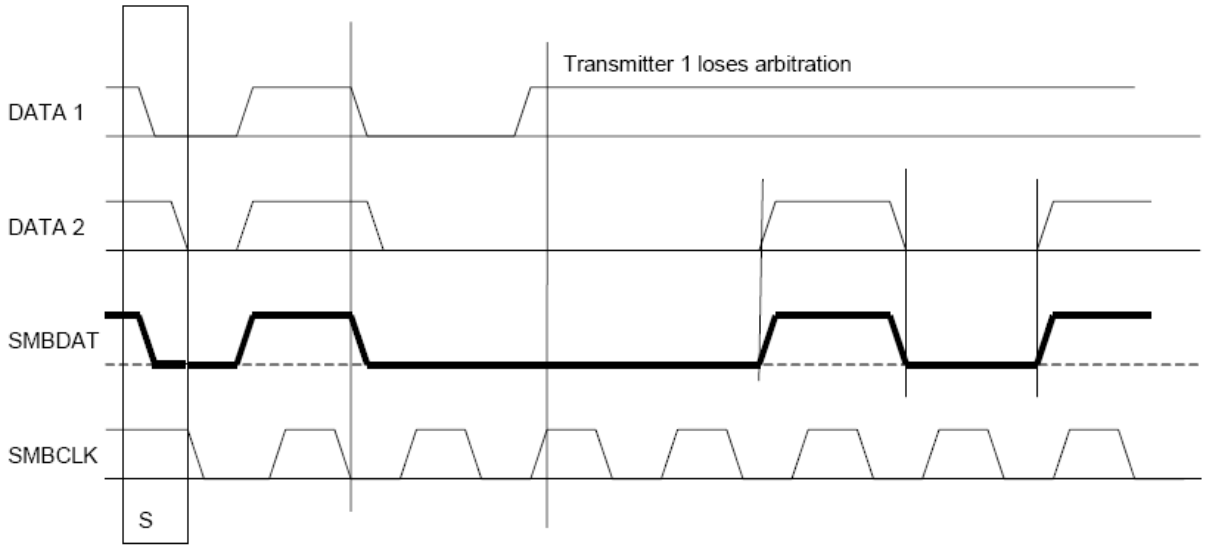


Figure 23-2 SMBus Arbitration

23.2.3 Clock Synchronization

Clock synchronization is performed while the arbitration procedure described above is in effect. Clock Synchronization takes place between two competing devices by utilizing the wired-AND nature of the SMBCLK line. The SMBCLK line will go low as soon as the master with the shortest high time pulls SMBCLK low. SMBCLK will remain low until the device with the longest SMBCLK low time relinquishes the SMBCLK line. Therefore the SMBCLK high time is determined by device with the shortest high time while the SMBCLK low time is determined by the device with the longest low time.

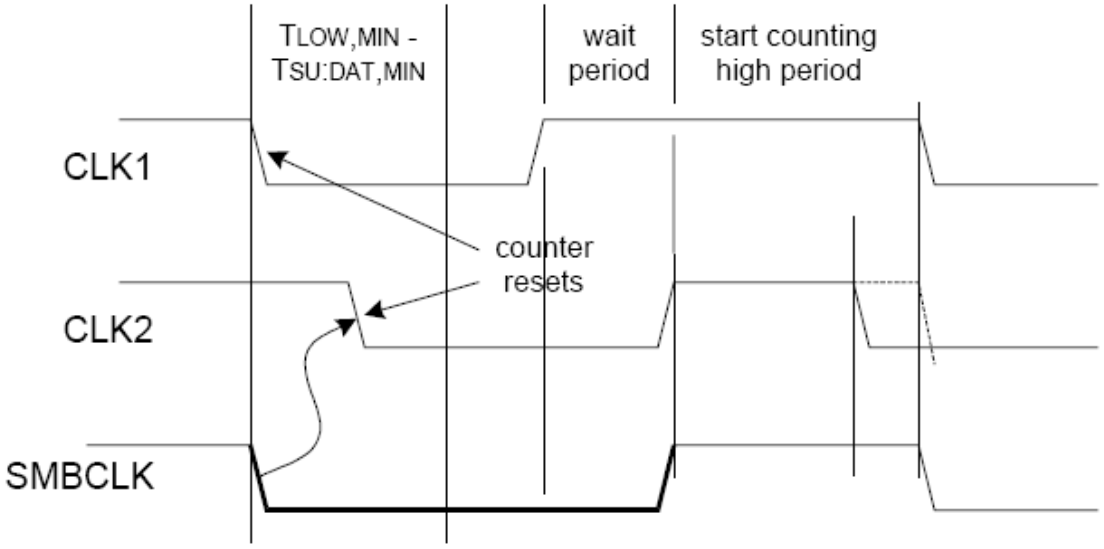


Figure 23-3 Clock synchronization

23.3 SB-TSI

The combined-format repeated start sequence is not supported in standard-mode and fast-mode.

- Only 7-bit SMBus addresses are supported.
- SB-TSI implements the Send/Receive Byte and Read/Write Byte protocols.
- SB-TSI registers can only by written using a write byte command.
- Address Resolution Protocol (ARP) is not implemented.
- Packet Error Checking (PEC) is not supported.

23.3.1 SB-TSI Address

The SMBus address is really 7 bits. The SB-TSI address is normally 98h or 4Ch. The address could vary with address select bits.

Table 23-1 SB-TSI Address Encoding

Address Select Bits	SB-TSI Address
000b	98h
001b	9Ah
010b	9Ch
011b	9Eh
100b	90h
101b	92h
110b	94h
111b	96h

23.4 PCH

The PCH provide system thermal data to EC. The EC can manage the fans and other cooling elements based on this data. A subset of the thermal collection is that the PCH and be programmed to alert the EC when a device has gone outside of its temperature limits.

23.4.1 Command Summary

Table 23-2 PCH Command Summary

Trans-action	Slave Addr.	Data Byte 0 =Command	Data Byte 1 =Byte Count	Data Byte 2	Data Byte 3	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7
Write STS Preferences	I2C	0x41	0x6	STS [47:40]	STS [39:32]	STS [31:24]	STS [23:16]	STS [15:8]	STS [7:0]
Write CPU Temp Limits	I2C	0x42	0x6	Lower Limit [15:8]	Lower Limit [7:0]	Upper Limit [15:8]	Upper Limit [15:8]		
Write MCH	I2C	0x43	0x2	Lower	Upper	na	na		

Temp Limits				Limit [7:0]	Limit [7:0]				
Write IBX Temp Limits	I2C	0x44	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write DIMM Temp Limits	I2C	0x45	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write MPC CPU Power Clamp	I2C	0x50	0x2	Lower Limit [7:0]	Power Clamp [7:0]				
Block Read	Block Read Address	0x40	Block Read Address	Byte Count	Data 0	Data N	PEC (optional)		

23.5 SMBus Master

23.5.1 Block Diagram

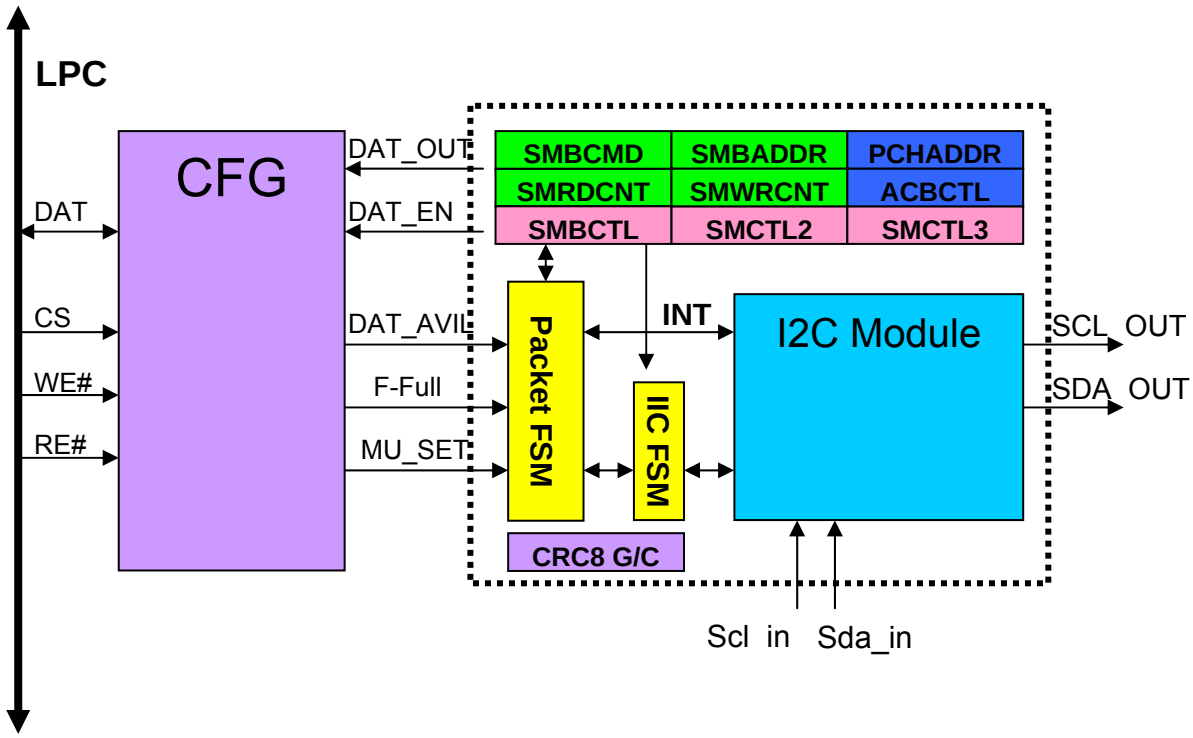


Figure 23-4 SMBus Master Block Diagram

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23.5.2 Programming Flow

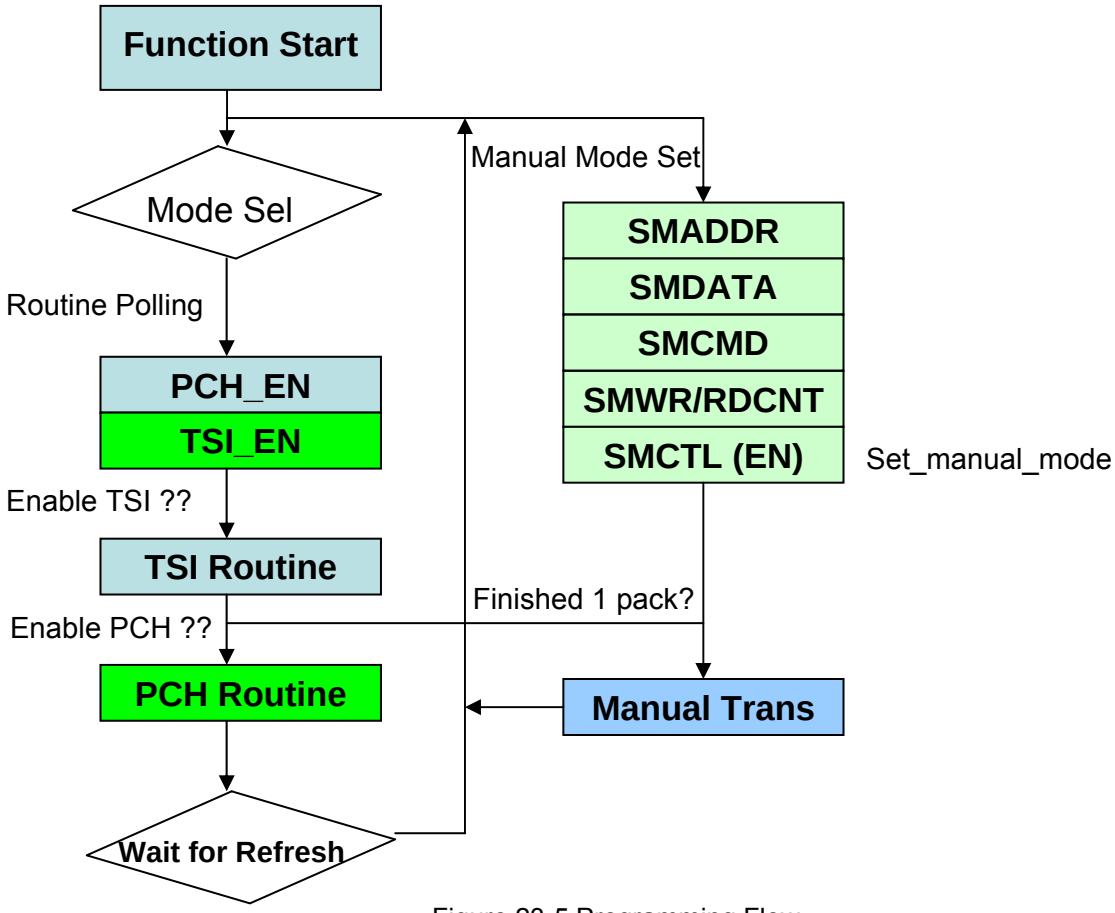

Figure 23-5 Programming Flow

23.5.3 TSI Routine

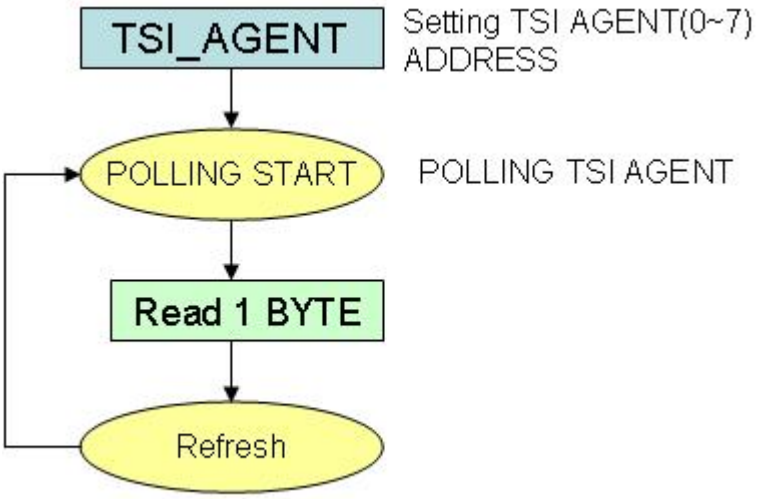

Figure 23-6 TSI Routine

23.5.4 PCH Routine

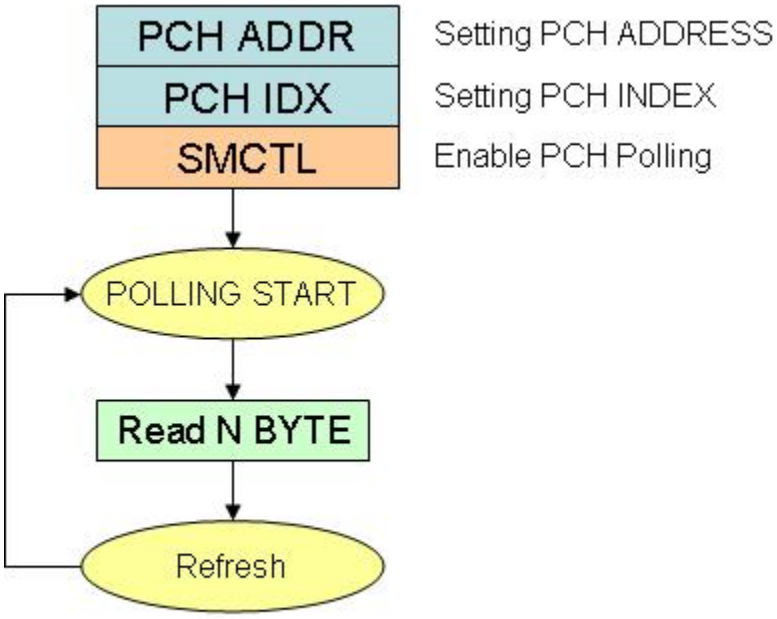

Figure 23-7 PCH Routine

23.5.5 BYTE Ruttine

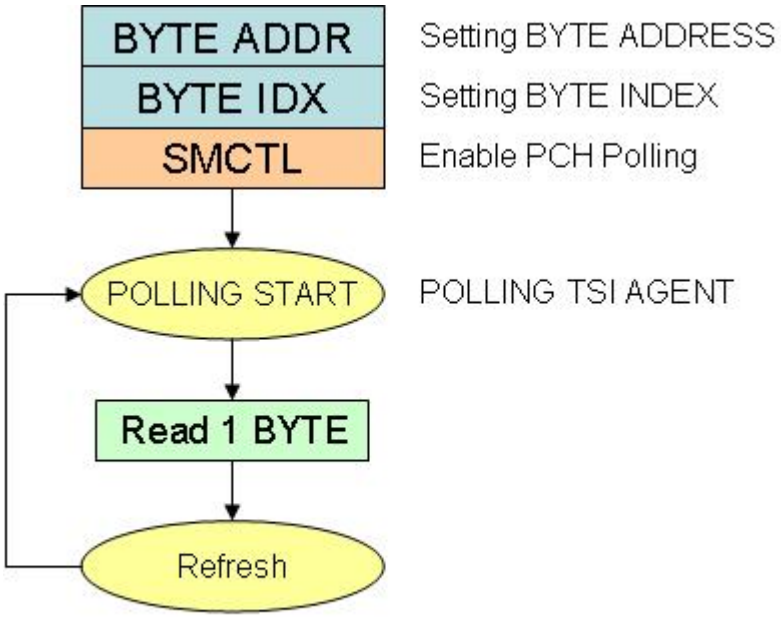

Figure 23-8 PCH Routine

23.5.6 Manual Mode interface

The SMBus host supports Block/Word/Byte Write and Block/Word/Byte read with PEC. The SMBus host can use the interface to access the smbus slave. The timing diagrams below illustrate how to use the smbus interface to write the data or read the data to the smbus slave.

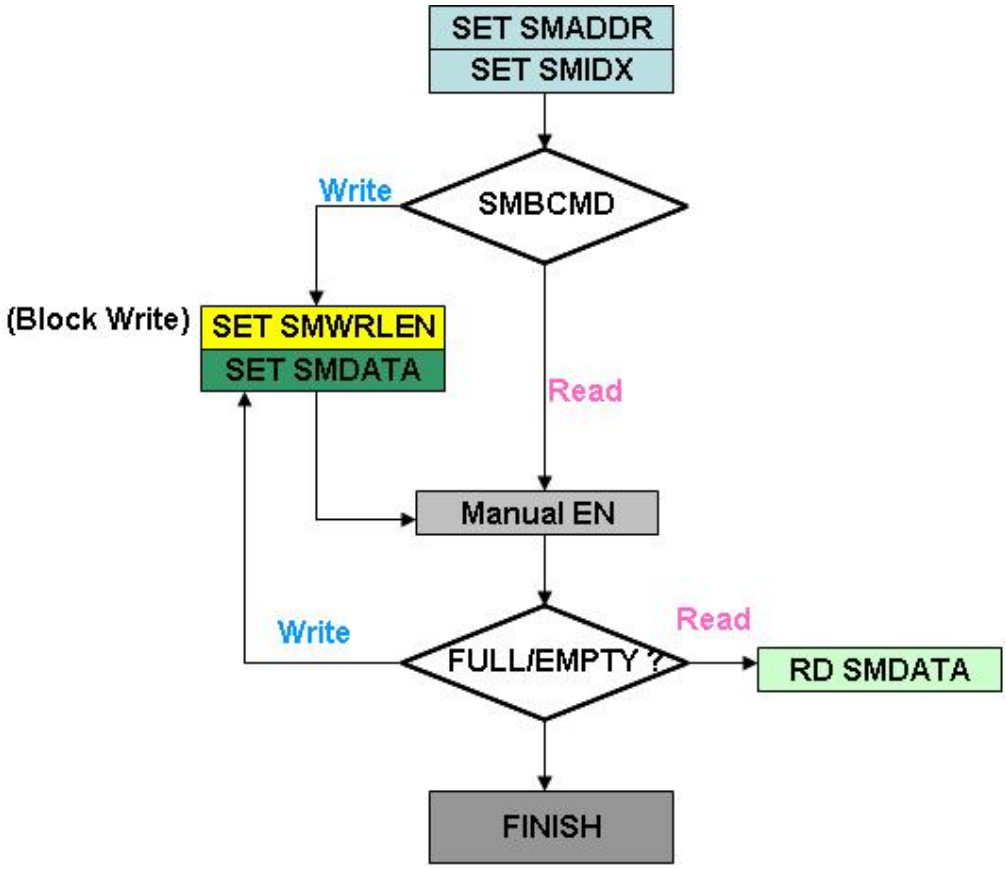

Figure 23-9 Manual Mode Programming Flow

23.6 Register Type Abbreviations

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register.
- W = Write.
- RO = Read-only.

To program the SMBus master configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

23.6.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x26 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

23.6.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

23.7 SMBus Master Register Set

23.7.1 SMBus Register Map

SMBus Master base address in register Logic Device B CR62h(MSB), CR63h(LSB).

Table 23-3 SMBus Master Bank 0 Registers

Offset	Type	Name	Section
0	R/W	**SMBus Data**	23.7.2
1	R/W	**SMBus Write Data Size**	23.7.3
2	R/W	**SMBus Command**	23.7.4
3	R/W	**SMBus Index**	23.7.5
4	R/W	**SMBus Control**	23.7.6
5	R/W	**SMBus Address**	23.7.7
6	R/W	**SMBCLK Frequency**	23.7.8
7	RO	**Reserved**	--
8	R/W	**PCH Address**	23.7.9
9	R/W	**Error status**	23.7.10
A	R/W	**Reserved**	--
B	R/W	**PCH Command**	23.7.11
D	R/W	**TSI Agent Enable**	23.7.12
E	R/W	**SMBus Control 3 Register**	23.7.13
F	R/W	**SMBus Control 3 Register**	23.7.14
10	R/W	**BYTE_ADDR**	23.7.15
11	R/W	**BYTE Index High Byte**	23.7.16
12	R/W	**BYTE Index Low Byte**	23.7.17
13	R/W	**Reserved**	
14	R/W	**Reserved**	

23.7.2 SMBus Data (SMDATA) – Bank 0

This 32 bits register is the data in and out register of SMBus data register. Before writing to SMDATA register, this register contains the input data, after writing to SMDATA register, this register contains the output data.

Offset: 0h

Type: R/W

Byte	3	2	1	0
Name	**SMFIFO3**	**SMFIFO2**	**SMFIFO1**	**SMFIFO0**
Default	00h	00h	00h	00h

Byte	Description
3	**SMFIFO3 (SMBus FIFO 3).** This byte represents the high byte of the 32 bits SMBus data.
2	**SMFIFO2 (SMBus FIFO 2).** This byte represents the second byte of the 32 bits SMBus data.
1	**SMFIFO1 (SMBus FIFO 1).** This byte represents the first byte of the 32 bits SMBus data.
0	**SMFIFO0 (SMBus FIFO 0).** This byte represents the low byte of the 32 bits SMBus data.

23.7.3 SMBus Write Data Size (SMWRSIZE) – Bank 0

Offset: 1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**SMWRSIZE**				
Default	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4-0	**SMWRSIZE (SMBus Write Byte Counter).** This field sets the write byte counter, the max counter size is 32 bytes, and the minimal size is 1 bytes.

23.7.4 SMBus Command (SMCMD) – Bank 0

Offset: 2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
NAME	REV				SMBus CMD			
Default	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**

3-0	**SMBCMD (SMBus Command).** This field sets SMBus Command: 0000 : Read Byte (Default) 0001 : Read Word 0010 : Read Block 0011 : Block Write and Read Process Call 0100 : Process Call 1000 : Write Byte 1001 : Write Word 1010 : Write Block

23.7.5 SMBus INDEX (SMIDX) – Bank 0

Offset: 3h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SMCMD**							
Default	0	0	0	0	0	0	0	0

Bit	Description
7-0	**SMIDX (SMBus INDEX).** This field represents the index data of the SMBus.

23.7.6 SMBus Control (SMCTL) – Bank 0

Offset: 4h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**MMODE_S**	**S_RST**	**CRC8_EN**	**REFLASH_CLK**			**BYTE_EN**	**PCH_EN**
Default	0	0	0	0	0	0	0	0

Bit	Description
7	**MMODE_S (Manual Mode Set).** 0 : Disable. 1 : Enable.
6	**S_RST (Soft Reset SMBus).** 0 : Disable. 1 : Enable.
5	**CRC8_EN (CRC8 Enable).** 0 : CRC8 function is disable. 1 : CRC8 function is enable.

4-2	**REFRASH_CLK (Refrash Clock Select).** 000, 100 – 128ms 001, 101 – 256ms 010, 110 – 512ms 011, 111 – 64ms (1KHz)
1	**BYTE_EN (BYTE Enable).** 0 : BYTE function is disable. 1 : BYTE function is enable.
0	**PCH_EN (PCH Enable).** 0 : PCH function is disable. 1 : PCH function is enable.

23.7.7 SMBus Address (SMADDR) – Bank 0

Offset: 5h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SMADDR**							**REV**
Default	0	0	0	0	0	0	0	0

Bit	Description
7-1	**SMADDR (SMBus Address).** AMD-TSI only supports 7-bit SMBus address.
0	**Reserved:** 0 : Write. If the protocol is write, the WR_SIZE can't be zero. (Default)

23.7.8 SCL FREQ (SCLFREQ) – Bank 0

Offset: 6h

Type: R/W

Bit	7	6	5	4	3	2	1	0
	Reserved:				**SCLFREQ**			
Default	0	0	0	0	0	1	1	1

Bit	Description
7-4	Reserved

3-0	**SCLFQ (SMBCLK Frequency).** This field defines the SMBCLK period (low time and high time). The clock low time and high time ate defined as follows: 0000 : 365KHz 0001 : 261KHz 0010 : 200KHz 0011 : 162KHz 0100 : 136KHz 0101 : 117KHz 0110 : 103KHz 0111 : 92KHz (Default) 1000 : 83KHz 1001 : 76KHz 1010 : 71KHz 1011 : 65KHz 1100 : 61KHz 1101 : 57KHz 1110 : 53KHz 1111 : 47KHz

23.7.9 PCH Address (PCHADDR) – Bank 0

Offset: 8h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PCHADDR**							**REV**
Default	1	0	0	1	0	1	0	0

Bit	Description
7-1	**PCHADDR (PCH Address).** PCH supports 8-bit SMBus address. The default address is 94h. The last bit is read or write bit. It needs to set to “0”.

23.7.10 SMBus Error Status (Error_status) – Bank 0

Offset: 9h

Type: RO/W1C

Bit	7	6	5	4	3	2	1	0
Name	**REV**		**ADNACK**	**Timeout**	**Reserved**	**BER**	**NACK**	**Reserved**
Default	1	0	0	1	0	1	0	0

Bit	Description
7-6	**Reserved.**
5	**ADDR Non ACK.** This bit reflects SMBus occurred ADDRESS NON ACK in Manual mode..
4	**Timeout.** This bit reflects when SMBus occurs timeout.

3	**Reserved.**
2	**BER (Bus Error).** This bit reflects when a start or stop condition is detected during data transfer, or when an arbitration problem is detected.
1	**NACK (Negative acknowledge).** This bit is set by hardware when a transmission is not acknowledged on the ninth clock. While NACK is set SCL will be drive low and subsequent bus transactions are stalled until NACK is cleared.
0	**Reserved.**

23.7.11PCH Command (PCHCMD) – Bank 0

Offset: Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PCHCMD**							
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**PCHCMD (PCH Command).** This field represents the command data of the PCH. The default command is block read (40h).

23.7.12TSI Agent Enable Register (TSI_AGENT) – Bank

Offset: Dh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	AG7	AG6	AG5	AG4	AG3	AG2	AG1	AG0
Default	0	0	0	0	0	0	0	0

Bit	Description
7	**TSI AGENT7 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
6	**TSI AGENT6 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
5	**TSI AGENT5 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
4	**TSI AGENT4 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable

3	**TSI AGENT3 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
2	**TSI AGENT2 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
1	**TSI AGENT1 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable
0	**TSI AGENT0 Enable. :** This bit reflects AMD-TSI Agent enbale. 0: Diable 1: Enable

23.7.13SMBus Control 3 Register (SMCTL3) – Bank 0

Offset: Eh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**CRC_CHK**	**M_MODE**	**F_FULL**	**F_EMPT**
Default	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3	**CRC_CHK (CRC Check).** 0 : incorrect 1 : correct
2	**M_MODE (Manual Mode).** 0 : Non-active 1 : Active
1	**F_FULL (fifo_full). :** This bit reflects SMBus data fifo is full. 0 : Non-full 1 : Full
0	**F_EMPT (fifo empty). :** This bit reflects the SMBus data fifo is empty. 0 : Non-empty 1 : Empty

23.7.14SMBus Control 2 Register (SMCTL2) – Bank 0

Offset: Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**INT_LCH_E**	**Reserved**		**BYTE_SEL**	**BANKSEL**	
Default	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**INT_LCH_E (Interrupt Latch Enable). :** This bit will latch the I2CSTA register. 0 : Disable. 1 : Enable.
2	**BYTE_SEL :**This field represents byte polling 8-bit/16bit select bits. 0: BYTE_TEMP is 16 bit data 1: BYTE_TEMP is 8 bit data
1-0	**BANKSEL (Bank Select).** 00 – Bank 0. 01 – Bank 1. 10 – Bank 2.

23.7.15BYTE ADDRESS (BYTE ADDR) – Bank 0

Offset: 10h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_ADDRESS**							
Default	0	1	0	0	0	0	0	0

Bit	Description
7-0	**BYTE ADDRESS (BYTE ADDR).** This field represents the address data of the BYTE.

23.7.16BYTE INDEX_H (BYTE_IDX_H) – Bank 0

Offset: 11h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_H**							
Default	0	0	0	0	0	0	0	1

Bit	Description
7-0	**BYTE_IDX_H (High BYTE INDEX).** This field represents the high byte index of the Byte polling. The default command is byte read (01h).

23.7.17BYTE INDEX_L (BYTE_IDX_L) – Bank 0

Offset: 12h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_L**							
Default	0	0	0	1	0	0	0	0

Bit	Description
7-0	**BYTE_IDX_L (LOW BYTE INDEX).** This field represents the low byte index of the Byte polling. The default command is byte read (10h).

The EC may read thermal information from IBX using the SMBus block read command. The IBX doesn't support byte-read or word-read SMBus commands. The read use a different address that the writes. The address must be different so that the IBX knows which target Is intended, either the I2C target or the block read buffer.

The IBX and EC are set up by BIOS with the length of the read that is supported by the platform. The EC must always do reads of the lengths set up by BIOS. There is no way to change the length of the read after BIOS has set things up.

An EC that only wants the single highest temperature among MCH, and CPU could read one byte. A 2 byte read would provide both IBX and CPU/MCH package temperature. An EC that wanted each components temperature would do a 4 byte read. An EC that also wanted DIMM information would read 9 bytes. If an EC wanted to read the HOST STS status, it must read 19 bytes. An EC can also read the energy data provided by the CPU by reading 12 bytes.

24. CONFIGURATION REGISTER

24.1 Chip (Global) Control Register

Default Value of Global Control Register:

Register	Default	Register	Default	Register	Default
CR 10h	FFh	CR 21h	3Xh (ID_L)	CR 2Bh	00h
CR 11h	FFh	CR 22h	FFh	CR 2Ch	81h
CR 13h	00h	CR 24h	64h	CR 2Dh	00h
CR 14h	00h	CR 25h	00h	CR 2Fh	00ssssssb
CR 1Ah	F0h	CR 26h	0s000000b		
CR 1Bh	78h	CR 27h	00h		
CR 1Ch	00h	CR 28h	00h		
CR 20h	C3h (ID_H)	CR 2Ah	C0h		

Note. The value of “s” means hardware strapping result: strapping high will report 1; strapping low will report 0.
In addition, BIOS can write the value of strapping result after hardware strapping.

Note. The CR21h is low-byte of the Chip-ID; the “X” means IC version. EX. 31=A version, 32=B version, 33=C version.

Reserved Registers of Global Control Register:

Register	Default	Register	Default
CR 02h	00h	CR 1Dh	00h
CR 16h	FFh	CR 1Eh	FFh
CR 17h	FFh	CR 1Fh	FFh
CR 18h	FFh	CR 23h	00h
CR 19h	FFh	CR 2Eh	00h

Note. All reserved registers must keep default value.

Note. Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 02h. Reserved.Software Reset Register

Attribute: Write Only
Power Well: VCC
Reset by: LRESET#
Default : 00h

CR 07h. Logical Device Selection

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	FDC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	PRT IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTB IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3	R / W	KBC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	MOUSE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1	R / W	CIR IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	R / W	CIRWAKUP IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	HM IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

BIT	READ / WRITE	DESCRIPTION
6	R / W	WDTO IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	Reserved.	
4	Reserved.	
3	Reserved.	
2	Reserved.	
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	Reserved.	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 1Ah. Multi Function Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : F0h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>Reserved.</td><td></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin83 function selection
<table>
<tr><th>CR2B [Bit1]</th><th>CR1A [Bit6]</th><th>CR24 [Bit2]</th><th>Pin83</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>GP31</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>OVT#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>SMI#</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESETCONI#</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin76 function selection
<table>
<tr><th>CR1B [Bit0]</th><th>CR1A [Bit5]</th><th>Pin76</th></tr>
<tr><td>1</td><td>x</td><td>MSDA</td></tr>
<tr><td>0</td><td>0</td><td>SDA</td></tr>
<tr><td>0</td><td>1</td><td>GP92 (Default)</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin75 function selection
<table>
<tr><th>CR1B [Bit0]</th><th>CR1A [Bit4]</th><th>Pin75</th></tr>
<tr><td>1</td><td>x</td><td>MSCL</td></tr>
<tr><td>0</td><td>0</td><td>SCL</td></tr>
<tr><td>0</td><td>1</td><td>GP93 (Default)</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin52 function selection
<table>
<tr><th>LPT_EN
(Strapping pin34)</th><th>CR1A [Bit3-2]</th><th>Pin52</th></tr>
<tr><td>1</td><td>xx</td><td>INIT#</td></tr>
<tr><td>0</td><td>00</td><td>MSCL</td></tr>
<tr><td>0</td><td>01</td><td>SCL</td></tr>
<tr><td>0</td><td>10</td><td>GP41</td></tr>
<tr><td>0</td><td>11</td><td>MSCL</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>Reserved.</td><td></td></tr>
</table>

CR 1Bh. Multi Function Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 78h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin37 function selection
<table>
<tr><th>CR1B [Bit7]</th><th>Pin37</th></tr>
<tr><td>0</td><td>RESETCONO#
(Default)</td></tr>
<tr><td>1</td><td>GP47</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>Pin39 function selection
<table>
<tr><th>LPT_EN
(Strapping pin34)</th><th>CR1B [Bit6]</th><th>Pin39</th></tr>
<tr><td>1</td><td>x</td><td>PE</td></tr>
<tr><td>0</td><td>0</td><td>GP45</td></tr>
<tr><td>0</td><td>1</td><td>YLW_LED</td></tr>
</table>
Pin40 function selection
<table>
<tr><th>LPT_EN
(Strapping pin34)</th><th>CR1B [Bit6]</th><th>Pin40</th></tr>
<tr><td>1</td><td>x</td><td>BUSY</td></tr>
<tr><td>0</td><td>0</td><td>GP44</td></tr>
<tr><td>0</td><td>1</td><td>GRN_LED</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin53 function selection
<table>
<tr><th>LPT_EN
(Strapping pin34)</th><th>CR1B [Bit5]</th><th>Pin53</th></tr>
<tr><td>1</td><td>x</td><td>ERR#</td></tr>
<tr><td>0</td><td>0</td><td>GP57</td></tr>
<tr><td>0</td><td>1</td><td>VID_RST#</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin95 function selection
<table>
<tr><th>CR1B [Bit4]</th><th>CR27 [Bit3]</th><th>Pin95</th></tr>
<tr><td>1</td><td>x</td><td>CIRRX (Default)</td></tr>
<tr><td>0</td><td>0</td><td>GP24</td></tr>
<tr><td>0</td><td>1</td><td>IRRX1</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin62 function selection
<table>
<tr><th>CR1B [Bit3]</th><th>Pin62</th></tr>
<tr><td>0</td><td>GP40</td></tr>
<tr><td>1</td><td>SLP_S5#_LATCH
(Default)</td></tr>
</table></td></tr>
<tr><td>2-1</td><td>R / W</td><td>Pin51 function selection
<table>
<tr><th>LPT_EN
(Strapping pin34)</th><th>CR1B [Bit2-1]</th><th>Pin51</th></tr>
<tr><td>1</td><td>x</td><td>SLIN#</td></tr>
<tr><td>0</td><td>00</td><td>MSDA</td></tr>
<tr><td>0</td><td>01</td><td>SDA</td></tr>
<tr><td>0</td><td>10</td><td>BEEP</td></tr>
<tr><td>0</td><td>11</td><td>GP42</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>R / W</td><td>
Pin76 function selection
<table>
<tr><td>CR1B [Bit0]</td><td>CR1A [Bit5]</td><td>Pin76</td></tr>
<tr><td>1</td><td>x</td><td>MSDA</td></tr>
<tr><td>0</td><td>0</td><td>SDA</td></tr>
<tr><td>0</td><td>1</td><td>GP92 (Default)</td></tr>
</table>
Pin75 function selection
<table>
<tr><td>CR1B [Bit0]</td><td>CR1A [Bit4]</td><td>Pin75</td></tr>
<tr><td>1</td><td>x</td><td>MSCL</td></tr>
<tr><td>0</td><td>0</td><td>SCL</td></tr>
<tr><td>0</td><td>1</td><td>GP93 (Default)</td></tr>
</table>
</td></tr>
</table>

CR 1Ch. Multi Function Selection

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>
Pin54 function selection
<table>
<tr><td>CR1C [Bit7]</td><td>DSW_EN (Strapping pin69)</td><td>AMDPWR_EN (Strapping pin96)</td><td>LPT_EN (Strapping pin34)</td><td>Pin54</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>SLP_SUS#</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>ALERTI#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>AFD#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>GP56</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>AFD#</td></tr>
</table>
Pin55 function selection
<table>
<tr><td>CR1C [Bit7]</td><td>DSW_EN (Strapping pin69)</td><td>AMDPWR_EN (Strapping pin96)</td><td>LPT_EN (Strapping pin34)</td><td>CR27 [Bit0]</td><td>Pin55</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>1</td><td>CIRTX3</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>x</td><td>ALERTO#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>x</td><td>STB#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>CIRTX3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>GP55</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>STB#</td></tr>
</table>
</td></tr>
<tr><td>6-2</td><td colspan="2">Reserved.</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>R / W</td><td>Pin5 function selection
<table>
<tr><th>CR1C [Bit1]</th><th>CR24 [Bit6]</th><th>Pin5</th></tr>
<tr><td>1</td><td>x</td><td>AUXFANIN2</td></tr>
<tr><td>0</td><td>0</td><td>GP02</td></tr>
<tr><td>0</td><td>1</td><td>DSA# (Default)</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin4 function selection
<table>
<tr><th>CR1C [Bit0]</th><th>CR24 [Bit6]</th><th>Pin4</th></tr>
<tr><td>1</td><td>x</td><td>AUXFANIN1</td></tr>
<tr><td>0</td><td>0</td><td>GP01</td></tr>
<tr><td>0</td><td>1</td><td>MOA# (Default)</td></tr>
</table></td></tr>
</table>

CR 20h. Chip ID (High Byte)

Attribute: Read Only
Power Well: VCC
Reset by: None
Default : C3h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = C3h (high byte).

CR 21h. Chip ID (Low Byte)

Attribute: Read Only
Power Well: VCC
Reset by: None
Default : 33h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 33h (low byte)

CR 22h. Device Power Down

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	UARTB Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3	R / W	PRT Power Down. 0: Powered down. 1: Not powered down.
2	Reserved.	

BIT	READ / WRITE	DESCRIPTION
1	R / W	IPD (Immediate Power Down). When set to 0, the whole chip is put into power-down mode immediately.
0	R / W	FDC Power Down. 0: Powered down. 1: Not powered down.

CR 24h. Global Option

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET#

Default : 64h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>
Pin2 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin2</td></tr>
<tr><td>0</td><td>GP00</td></tr>
<tr><td>1</td><td>DRVDEN0 (Default)</td></tr>
</table>
Pin3 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin3</td></tr>
<tr><td>0</td><td>AUXFANIN0</td></tr>
<tr><td>1</td><td>INDEX# (Default)</td></tr>
</table>
Pin4 function selection
<table>
<tr><td>CR1C [Bit0]</td><td>CR24 [Bit6]</td><td>Pin4</td></tr>
<tr><td>1</td><td>x</td><td>AUXFANIN1</td></tr>
<tr><td>0</td><td>0</td><td>GP01</td></tr>
<tr><td>0</td><td>1</td><td>MOA# (default)</td></tr>
</table>
Pin5 function selection
<table>
<tr><td>CR1C [Bit1]</td><td>CR24 [Bit6]</td><td>Pin5</td></tr>
<tr><td>1</td><td>x</td><td>AUXFANIN2</td></tr>
<tr><td>0</td><td>0</td><td>GP02</td></tr>
<tr><td>0</td><td>1</td><td>DSA# (Default)</td></tr>
</table>
Pin6 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin6</td></tr>
<tr><td>0</td><td>CIRTX2</td></tr>
<tr><td>1</td><td>DIR# (Default)</td></tr>
</table>
Pin7 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin7</td></tr>
<tr><td>0</td><td>HD_LED#</td></tr>
<tr><td>1</td><td>STEP# (Default)</td></tr>
</table>
Pin8 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin8</td></tr>
<tr><td>0</td><td>GP03</td></tr>
<tr><td>1</td><td>WD# (Default)</td></tr>
</table>
Pin9 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin9</td></tr>
<tr><td>0</td><td>GP04</td></tr>
<tr><td>1</td><td>WE# (Default)</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>
Pin10 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin10</td></tr>
<tr><td>0</td><td>PRIMARY_HD#</td></tr>
<tr><td>1</td><td>TRAK0# (Default)</td></tr>
</table>
Pin11 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin11</td></tr>
<tr><td>0</td><td>GP05 (CIR_SENSE1)</td></tr>
<tr><td>1</td><td>WP# (Default)</td></tr>
</table>
Pin12 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin12</td></tr>
<tr><td>0</td><td>GP06 (CIR_SENSE2)</td></tr>
<tr><td>1</td><td>RDATA# (Default)</td></tr>
</table>
Pin13 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin13</td></tr>
<tr><td>0</td><td>GP07 (CIRLED)</td></tr>
<tr><td>1</td><td>HEAD# (Default)</td></tr>
</table>
Pin14 function selection
<table>
<tr><td>CR24 [Bit6]</td><td>Pin14</td></tr>
<tr><td>0</td><td>SECONDARY_HD#</td></tr>
<tr><td>1</td><td>DSKCHG# (Default)</td></tr>
</table>
</td></tr>
<tr><td>5</td><td>R / W</td><td>Select output type of AUXFANOUT
=0 AUXFANOUT is Push-pull.
=1 AUXFANOUT is Open-drain. (Default)</td></tr>
<tr><td>4</td><td>R / W</td><td>Select output type of SYSFANOUT
=0 SYSFANOUT is Open-drain. (Default)
=1 SYSFANOUT is Push-pull.</td></tr>
<tr><td>3</td><td>R / W</td><td>Select output type of CPUFANOUT
=0 CPUFANOUT is Open-drain. (Default)
=1 CPUFANOUT is Push-pull.</td></tr>
<tr><td>2</td><td>R / W</td><td>
Pin128 function selection
<table>
<tr><td>CR24 [Bit2]</td><td>Pin128</td></tr>
<tr><td>0</td><td>OVT#</td></tr>
<tr><td>1</td><td>SMI# (Default)</td></tr>
</table>
</td></tr>
<tr><td>1</td><td colspan="2">Reserved.</td></tr>
<tr><td>0</td><td>R / W</td><td>PNPCVS =>
= 0 The compatible PNP address-select registers have default values.
= 1 The compatible PNP address-select registers have no default values.</td></tr>
</table>

CR 25h. Interface Tri-state Enable

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W	UARTBTRI
2	R / W	UARTATRI
1	R / W	PRTTRI
0	R / W	FDCTRI.

CR 26h. Global Option s: value by strapping

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 0s000000b

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (Pin 31).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4	Reserved.	
3	R / W	DSFDLGRQ => = 0 Enable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is effective when selecting IRQ. = 1 Disable FDC legacy mode for IRQ and DRQ selection. Then DO register (base address + 2) bit 3 is not effective when selecting IRQ.
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

BIT	READ / WRITE	DESCRIPTION
0	R / W	DSUBLGRQ => = 0 (base address + 4) Enable IR legacy mode for IRQ selection. Then HCR register bit 3 is effective when selecting IRQ. = 1 Disable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h. Global Option

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**Pin88** function selection

CR27 [Bit7]	AMDPWR_EN (Strapping pin96)	DSW_EN (Strapping pin69)	Pin88
1	x	x	GP75
0	1	x	VIDO5
0	x	1	VIDO5
0	0	0	SLP_SUS_FET

Pin89 function selection

CR27 [Bit7]	AMDPWR_EN (Strapping pin96)	DSW_EN (Strapping pin69)	Pin89
1	x	x	GP74
0	1	x	VIDO4
0	x	1	VIDO4
0	0	0	SLP_SUS#

Pin90 function selection

CR27 [Bit7]	AMDPWR_EN (Strapping pin96)	DSW_EN (Strapping pin69)	Pin90
1	x	x	GP73
0	1	x	VIDO3
0	x	1	VIDO3
0	0	0	SUS_WARN_5V DUAL

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>
Pin91 function selection
<table>
<tr><th>CR27 [Bit7]</th><th>AMDPWR_EN (Strapping pin96)</th><th>DSW_EN (Strapping pin69)</th><th>Pin91</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>GP72</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>VIDO2</td></tr>
<tr><td>0</td><td>x</td><td>1</td><td>VIDO2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SUSACK#</td></tr>
</table>
Pin92 function selection
<table>
<tr><th>CR27 [Bit7]</th><th>AMDPWR_EN (Strapping pin96)</th><th>DSW_EN (Strapping pin69)</th><th>Pin92</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>GP71</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>VIDO1</td></tr>
<tr><td>0</td><td>x</td><td>1</td><td>VIDO1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>5VDUAL</td></tr>
</table>
Pin93 function selection
<table>
<tr><th>CR27 [Bit7]</th><th>AMDPWR_EN (Strapping pin96)</th><th>DSW_EN (Strapping pin69)</th><th>Pin93</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>GP70</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>VIDO0</td></tr>
<tr><td>0</td><td>x</td><td>1</td><td>VIDO0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SUSWARN#</td></tr>
</table>
</td></tr>
<tr><td>6</td><td>R / W</td><td>
Pin86 function selection
<table>
<tr><th>CR27 [Bit6]</th><th>AMDPWR_EN (Strapping pin96)</th><th>Pin86</th></tr>
<tr><td>1</td><td>x</td><td>GP77</td></tr>
<tr><td>0</td><td>0</td><td>VIDO7</td></tr>
<tr><td>0</td><td>1</td><td>VLDT_EN</td></tr>
</table>
Pin87 function selection
<table>
<tr><th>CR27 [Bit6]</th><th>AMDPWR_EN (Strapping pin96)</th><th>Pin87</th></tr>
<tr><td>1</td><td>x</td><td>GP76</td></tr>
<tr><td>0</td><td>0</td><td>VIDO6</td></tr>
<tr><td>0</td><td>1</td><td>VCORE_EN</td></tr>
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</td></tr>
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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5</td><td>R / W</td><td>Pin38 function selection
<table>
<tr><th>LPT_EN
(Strapping pin34)</th><th>CR27 [Bit5]</th><th>Pin38</th></tr>
<tr><td>1</td><td>x</td><td>SLCT</td></tr>
<tr><td>0</td><td>0</td><td>GP46</td></tr>
<tr><td>0</td><td>1</td><td>CIRRXWB</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>
Pin41 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin41</td></tr>
<tr><td>1</td><td>x</td><td>ACK#</td></tr>
<tr><td>0</td><td>0</td><td>DGL#</td></tr>
<tr><td>0</td><td>1</td><td>GP43</td></tr>
</table>
Pin42 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin42</td></tr>
<tr><td>1</td><td>x</td><td>PD7</td></tr>
<tr><td>0</td><td>0</td><td>DGH#</td></tr>
<tr><td>0</td><td>1</td><td>GP67</td></tr>
</table>
Pin43 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin43</td></tr>
<tr><td>1</td><td>x</td><td>PD6</td></tr>
<tr><td>0</td><td>0</td><td>LED_G</td></tr>
<tr><td>0</td><td>1</td><td>GP66</td></tr>
</table>
Pin44 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin44</td></tr>
<tr><td>1</td><td>x</td><td>PD5</td></tr>
<tr><td>0</td><td>0</td><td>LED_F</td></tr>
<tr><td>0</td><td>1</td><td>GP65</td></tr>
</table>
Pin45 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin45</td></tr>
<tr><td>1</td><td>x</td><td>PD4</td></tr>
<tr><td>0</td><td>0</td><td>LED_E</td></tr>
<tr><td>0</td><td>1</td><td>GP64</td></tr>
</table>
Pin47 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin47</td></tr>
<tr><td>1</td><td>x</td><td>PD3</td></tr>
<tr><td>0</td><td>0</td><td>LED_D</td></tr>
<tr><td>0</td><td>1</td><td>GP63</td></tr>
</table>
Pin48 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin48</td></tr>
<tr><td>1</td><td>x</td><td>PD2</td></tr>
<tr><td>0</td><td>0</td><td>LED_C</td></tr>
<tr><td>0</td><td>1</td><td>GP62</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>
Pin49 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin49</td></tr>
<tr><td>1</td><td>x</td><td>PD1</td></tr>
<tr><td>0</td><td>0</td><td>LED_B</td></tr>
<tr><td>0</td><td>1</td><td>GP61</td></tr>
</table>
Pin50 function selection
<table>
<tr><td>LPT_EN</td><td>CR27 [Bit4]</td><td>Pin50</td></tr>
<tr><td>1</td><td>x</td><td>PD0</td></tr>
<tr><td>0</td><td>0</td><td>LED_A</td></tr>
<tr><td>0</td><td>1</td><td>GP60</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>R / W</td><td>
Pin95 function selection
<table>
<tr><td>CR1B [Bit4]</td><td>CR27 [Bit3]</td><td>Pin95</td></tr>
<tr><td>1</td><td>x</td><td>CIRRX (Default)</td></tr>
<tr><td>0</td><td>0</td><td>GP24</td></tr>
<tr><td>0</td><td>1</td><td>IRRX1</td></tr>
</table>
Pin96 function selection
<table>
<tr><td>CR2A [Bit3]</td><td>CR27 [Bit3]</td><td>Pin96</td></tr>
<tr><td>1</td><td>x</td><td>CIRTX1</td></tr>
<tr><td>0</td><td>0</td><td>GP25 (Default)</td></tr>
<tr><td>0</td><td>1</td><td>IRTX1</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>R / W</td><td>
Pin120 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin120</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>IRRX2</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP13</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>VIDI3 (Default)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SINB</td></tr>
</table>
Pin121 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin121</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>IRTX2</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP12</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>VIDI2 (Deafult)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SOUTB</td></tr>
</table>
</td></tr>
<tr><td>1</td><td>R / W</td><td>LV_DETECT_L
0: AMD power sequence detect level and time delay
1: AMD power sequence non detect level but time delay</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>R / W</td><td>Pin55 function selection
<table>
<tr><th>CR1C [Bit7]</th><th>DSW_EN (Strapping pin69)</th><th>AMDPWR_EN (Strapping pin96)</th><th>LPT_EN (Strapping pin34)</th><th>CR27 [Bit0]</th><th>Pin55</th></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>1</td><td>CIRTX3</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>x</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>x</td><td>ALERTO#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>x</td><td>STB#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>CIRTX3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>GP55</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>STB#</td></tr>
</table></td></tr>
</table>

CR 28h. Global Option

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2-0	R / W	PRTMODS2 ~ 0 => **Bits** **2 1 0** = 0 x x Parallel Port Mode. = 1 x x Reserved.

CR 2Ah. Multi Function Selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#, GP2X_MRST(Bit0)
Default : C0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**Pin29 ~ Pin36** function selection 0: COM A function. 1: GPIO8 function. (Default) (Pin29, Pin30, Pin31, Pin32, Pin33, Pin34, Pin35, Pin36)

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>
Pin116 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin116</td></tr>
<tr><td>1</td><td>x</td><td>GP17</td></tr>
<tr><td>0</td><td>0</td><td>CTSB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI7</td></tr>
</table>
Pin117 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin117</td></tr>
<tr><td>1</td><td>x</td><td>GP16</td></tr>
<tr><td>0</td><td>0</td><td>DSRB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI6</td></tr>
</table>
Pin118 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin118</td></tr>
<tr><td>1</td><td>x</td><td>GP15</td></tr>
<tr><td>0</td><td>0</td><td>RTSB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI5</td></tr>
</table>
Pin119 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin119</td></tr>
<tr><td>1</td><td>x</td><td>GP14</td></tr>
<tr><td>0</td><td>0</td><td>DTRB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI4</td></tr>
</table>
Pin120 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin120</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>IRRX2</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP13</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>VIDI3</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SINB</td></tr>
</table>
Pin121 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin121</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>IRTX2</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP12</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>VIDI2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SOUTB</td></tr>
</table>
Pin122 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin122</td></tr>
<tr><td>1</td><td>x</td><td>GP11</td></tr>
<tr><td>0</td><td>0</td><td>DCDB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI1</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R/W</td><td>Pin123 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin123</td></tr>
<tr><td>1</td><td>x</td><td>GP10</td></tr>
<tr><td>0</td><td>0</td><td>RIB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI0</td></tr>
</table></td></tr>
<tr><td>5</td><td>R/W</td><td>Pin116 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin116</td></tr>
<tr><td>1</td><td>x</td><td>GP17</td></tr>
<tr><td>0</td><td>0</td><td>CTSB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI7</td></tr>
</table>
Pin117 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin117</td></tr>
<tr><td>1</td><td>x</td><td>GP16</td></tr>
<tr><td>0</td><td>0</td><td>DSRB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI6</td></tr>
</table>
Pin118 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin118</td></tr>
<tr><td>1</td><td>x</td><td>GP15</td></tr>
<tr><td>0</td><td>0</td><td>RTSB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI5</td></tr>
</table>
Pin119 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin119</td></tr>
<tr><td>1</td><td>x</td><td>GP14</td></tr>
<tr><td>0</td><td>0</td><td>DTRB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI4</td></tr>
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Pin120 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin120</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>IRRX2</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP13</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>VIDI3</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SINB</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>5</td><td>R/W</td><td>Pin121 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin121</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>IRTX2</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP12</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>VIDI2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SOUTB</td></tr>
</table>
Pin122 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin122</td></tr>
<tr><td>1</td><td>x</td><td>GP11</td></tr>
<tr><td>0</td><td>0</td><td>DCDB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI1</td></tr>
</table>
Pin123 function selection
<table>
<tr><td>CR2A [Bit5]</td><td>CR2A [Bit6]</td><td>Pin123</td></tr>
<tr><td>1</td><td>x</td><td>GP10</td></tr>
<tr><td>0</td><td>0</td><td>RIB#</td></tr>
<tr><td>0</td><td>1</td><td>VIDI0</td></tr>
</table></td></tr>
<tr><td>4</td><td colspan="2">Reserved.</td></tr>
<tr><td>3</td><td>R/W</td><td>Pin96 function selection
<table>
<tr><td>CR2A [Bit3]</td><td>CR27 [Bit3]</td><td>Pin96</td></tr>
<tr><td>1</td><td>x</td><td>CIRTX1</td></tr>
<tr><td>0</td><td>0</td><td>GP25</td></tr>
<tr><td>0</td><td>1</td><td>IRTX1</td></tr>
</table></td></tr>
<tr><td>2</td><td>R/W</td><td>Enable Over Temperature shutdown Protection (OVT#)
= 0 The thermal shutdown function is disabled. (Default)
= 1 Enable thermal shutdown function.
(If set this bit to 1, the relative registers of OVT# event are:
Bank0, CR18 ,Bit6 → SMIOVT1 OVT# (Default SYSTIN)
Bank0, CR4C ,Bit4 → SMIOVT3 OVT# (Default AUXTIN)
Bank0, CR4C ,Bit3 → SMIOVT2 OVT# (Default CPUTIN)
If current temperature exceeds high-limit setting, OVT# event will be triggered and PSON# will inactive immediately.)</td></tr>
<tr><td>1</td><td>R / W</td><td>Pin56 function selection
<table>
<tr><td>CR2A [Bit1]</td><td>Pin56</td></tr>
<tr><td>0</td><td>MCLK</td></tr>
<tr><td>1</td><td>GP23</td></tr>
</table>
Pin57 function selection
<table>
<tr><td>CR2A [Bit1]</td><td>Pin57</td></tr>
<tr><td>0</td><td>MDAT</td></tr>
<tr><td>1</td><td>GP22</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>R / W</td><td>Pin58 function selection
<table>
<tr><td>CR2A [Bit0]</td><td>Pin58</td></tr>
<tr><td>0</td><td>KCLK</td></tr>
<tr><td>1</td><td>GP21</td></tr>
</table>
Pin59 function selection
<table>
<tr><td>CR2A [Bit0]</td><td>Pin59</td></tr>
<tr><td>0</td><td>KDAT</td></tr>
<tr><td>1</td><td>GP20</td></tr>
</table></td></tr>
</table>

CR 2Bh. Multi Function Selection

Location: Address 2Bh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin77 function selection
<table>
<tr><td>DSW_EN</td><td>CR2B [Bit7]</td><td>Pin77</td></tr>
<tr><td>1</td><td>x</td><td>SLP_SUS_FET</td></tr>
<tr><td>0</td><td>0</td><td>RSTOUT2#</td></tr>
<tr><td>0</td><td>1</td><td>GP37</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin78 function selection
<table>
<tr><td>CR2B [Bit6]</td><td>Pin78</td></tr>
<tr><td>0</td><td>RSTOUT1#</td></tr>
<tr><td>1</td><td>GP36</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin79 function selection
<table>
<tr><td>CR2B [Bit5]</td><td>Pin79</td></tr>
<tr><td>0</td><td>RSTOUT0#</td></tr>
<tr><td>1</td><td>GP35</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin80 function selection
<table>
<tr><td>CR2B [Bit4]</td><td>Pin80</td></tr>
<tr><td>0</td><td>ATXPGD</td></tr>
<tr><td>1</td><td>GP34</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3</td><td>R / W</td><td>Pin81 function selection
<table>
<tr><td>CR2B [Bit3]</td><td>Pin81</td></tr>
<tr><td>0</td><td>CPUPWRGD</td></tr>
<tr><td>1</td><td>GP33</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin82 function selection
<table>
<tr><td>CR2B [Bit2]</td><td>Pin82</td></tr>
<tr><td>0</td><td>PWROK</td></tr>
<tr><td>1</td><td>GP32</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin83 function selection
<table>
<tr><td>CR2B [Bit1]</td><td>CR1A [Bit6]</td><td>Pin83</td></tr>
<tr><td>1</td><td>x</td><td>GP31</td></tr>
<tr><td>0</td><td>0</td><td>OVT#</td></tr>
<tr><td>0</td><td>1</td><td>RESETCONI#</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin84 function selection
<table>
<tr><td>CR2B [Bit0]</td><td>Pin84</td></tr>
<tr><td>0</td><td>SLP_S5#</td></tr>
<tr><td>1</td><td>GP30</td></tr>
</table></td></tr>
</table>

CR 2Ch. Multi Function Selection

Location: Address 2Ch
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 81h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin 98 function selection
<table>
<tr><td>CR2C [Bit7]</td><td>Pin98</td></tr>
<tr><td>0</td><td>GP27</td></tr>
<tr><td>1</td><td>AUXFANOUT</td></tr>
</table></td></tr>
<tr><td>6-5</td><td>R / W</td><td>Pin 71 function selection
<table>
<tr><td>CR2C [Bit6-5]</td><td>Pin71</td></tr>
<tr><td>00</td><td>3VSBSW#</td></tr>
<tr><td>01</td><td>GP50</td></tr>
<tr><td>10</td><td>LATCH_BKFD_CUT#</td></tr>
<tr><td>11</td><td>3VSBSW#</td></tr>
</table></td></tr>
<tr><td>4-1</td><td colspan="2">Reserved.</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>R / W</td><td>Pin 113 function selection
<table>
<tr><td>CR2C [Bit0]</td><td>Pin113</td></tr>
<tr><td>0</td><td>GPA0</td></tr>
<tr><td>1</td><td>TSIC</td></tr>
</table>
Pin 115 function selection
<table>
<tr><td>CR2C [Bit0]</td><td>Pin115</td></tr>
<tr><td>0</td><td>PECI</td></tr>
<tr><td>1</td><td>TSID</td></tr>
</table></td></tr>
</table>

CR 2Dh. Multi Function Selection

Location: Address 2Dh
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#, GP5X_MRST(Bit4-1)
Default : 00h
Size: 8 bits

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin102 function Selection
<table>
<tr><td>CR2D [Bit7]</td><td>Pin102</td></tr>
<tr><td>0</td><td>SKTOCC#</td></tr>
<tr><td>1</td><td>GP90</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin101 function Selection
<table>
<tr><td>CR2D [Bit6]</td><td>Pin101</td></tr>
<tr><td>0</td><td>RSMRST#</td></tr>
<tr><td>1</td><td>GP91</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Reserved.</td></tr>
<tr><td>4</td><td>R / W</td><td>Pin60 function Selection
<table>
<tr><td>CR2D [Bit4]</td><td>Pin60</td></tr>
<tr><td>0</td><td>PSOUT#</td></tr>
<tr><td>1</td><td>GP54</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin61 function Selection
<table>
<tr><td>CR2D [Bit3]</td><td>Pin61</td></tr>
<tr><td>0</td><td>PSIN#</td></tr>
<tr><td>1</td><td>GP53</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>2</td><td>R / W</td><td>Pin63 function Selection
<table>
<tr><th>CR2D [Bit2]</th><th>AMDPWR_EN</th><th>Pin63</th></tr>
<tr><td>1</td><td>x</td><td>GP52</td></tr>
<tr><td>0</td><td>0</td><td>PSON#</td></tr>
<tr><td>0</td><td>1</td><td>AMD_PSON#</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin64 function Selection
<table>
<tr><th>CR2D [Bit1]</th><th>Pin64</th></tr>
<tr><td>0</td><td>SLP_S3#</td></tr>
<tr><td>1</td><td>GP51</td></tr>
</table></td></tr>
<tr><td>0</td><td colspan="2">Reserved.</td></tr>
</table>

CR 2Fh. Strapping Function Result

Location: Address 2Fh

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#(Bit5-2), PWROK(Bit1-0)

Default : by 00ss_ssss

Size: 8 bits

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R/W	AMDPWR_EN Strapping result reading
4	R / W	TEST_MODE2 Strapping result reading
3	R / W	DSW_EN Strapping result reading
2	R / W	TEST_MODE1 Strapping result reading
1	R / W	LPT_EN Strapping result reading
0	R / W	24M_48M_SEL Strapping result reading

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

4) VSB Strapping result can be programming by LPC, and reset by RSMRST#
5) VCC Strapping result can be programming by LPC, and reset by PWROK
6) LRESET Strapping (2E_4E_SEL) : No change

24.2 Logical Device 0 (FDC)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The FDC device is inactive. 1: The FDC device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, F0h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select FDC I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 06h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for FDC.

CR 74h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2-0	R / W	These bits select DRQ resource for FDC. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 0Eh

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	This bit determines the polarity of all FDD interface signals. 0: FDD interface signals are active low. 1: FDD interface signals are active high.
5	R / W	When this bit is logic 0, indicates a second drive is installed and is reflected in status register A. (PS2 mode only)
4	R / W	Swap Drive 0, 1 Mode => 0: No Swap. 1: Drive and Motor select 0 and 1 are swapped.
3-2	R / W	Interface Mode. 00: Model 30. 01: PS/2. 10: Reserved. 11: AT Mode
1	R / W	FDC DMA Mode. 0 : Burst Mode is enabled 1 : Non-Burst Mode.
0	R / W	Floppy Mode. 0 : Normal Floppy Mode. 1: Enhanced 3-mode FDD.

CR F1h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Boot Floppy. 00: FDD A. 01: Reserved. 10: Reserved. 11: Reserved.
5-4	R / W	Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.
3-2	R / W	Density Select. 00: Normal. 01 Normal. 10: 1 (Forced to logic 1). 11: 0 (Forced to logic 0).
1	R / W	DISFDDWR => 0: Enable FDD write. 1: Disable FDD write (forces pins WE, WD to stay high).
0	R / W	SWWP => 0: Normal, use WP to determine whether the FDD is write protected or not. 1: FDD is always write-protected.

CR F2h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1-0	R / W	FDD A Drive Type.

CR F4h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable FDC Pre-compensation. 1: Disable FDC Pre-compensation.
5	Reserved.	
4-3	R / W	Data Rate Table selection (Refer to TABLE A). 00: Select regular drives and 2.88 format. 01: 3-mode drive. 10: 2 Meg Tape. 11: Reserved.
2	Reserved.	
1-0	R / W	Drive Type selection (Refer to TABLE B).

CR F5h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Same as FDD0 of CR F5h.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0

0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0 (pin 2)	DRIVE TYPE
0	0	SELDEN	4/2/1 MB 3.5"“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	
1	0	$\overline{\text{SELDEN}}$	
1	1	DRATE0	

24.3 Logical Device 1 (Parallel Port)

CR 30h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, 78h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select PRT I/O base address. <100h: FFCh> on 4 bytes boundary (EPP not supported) or <100h: FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR 70h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 07h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for PRT.

CR 74h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
2-0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 3Fh

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6-3	R / W	ECP FIFO Threshold.
2-0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). **Bits** **2 1 0** 0 0 0: Standard and Bi-direction (SPP) mode. 0 0 1: EPP – 1.9 and SPP mode. 0 1 0: ECP mode. 0 1 1: ECP and EPP – 1.9 mode. 1 0 0: Printer Mode. 1 0 1: EPP – 1.7 and SPP mode. 1 1 0: Reserved. 1 1 1: ECP and EPP – 1.7 mode.

24.4 Logical Device 2 (UART A)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.

BIT	READ / WRITE	DESCRIPTION
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 0 0: IR clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**UARTA_RS485_enable** 0: Disable RS485 auto flow control function for UARTA 1: Enable RS485 auto flow control function for UARTA
6	R / W	**UARTA_RS485_inv_sel** (Available only when CRF2_Bit7=1) 0: Do not invert the behavior of RTSA# pin for RS485 auto flow control. 1: Invert the behavior of RTSA# pin for RS485 auto flow control.
5-0	Reserved.	

24.5 Logical Device 3 (UART B, IR)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 03h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for IR.

CR F0h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Delay RXCLK for 5 ns for LG issue. 1: No delay of 5 ns for RXCLK.
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5	R / W	0: Using the original RX FIFO Error Indication signal (USR bit 7). 1: Using new RX FIFO Error Indication signal to solve some issues.

BIT	READ / WRITE	DESCRIPTION
4-2	Reserved.	
1-0	R / W	**Bits** **1 0** 0 0: IR clock source is 1.8462 MHz (24 MHz / 13). 0 1: IR clock source is 2 MHz (24 MHz / 12). 0 0: IR clock source is 24 MHz (24 MHz / 1). 0 0: IR clock source is 14.769 MHz (24 MHz / 1.625).

CR F1h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: reserved. 1: Through IRRX / IRTX.
5-3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: IRTX pin of IR function in normal condition. 1: Inverse IRTX pin of IR function.
0	R / W	0: IRRX pin of IR function in normal condition. 1: Inverse IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

CR F2h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**UARTB_RS485_enable** 0: Disable RS485 auto flow control function for UARTB 1: Enable RS485 auto flow control function for UARTB
6	R / W	**UARTB_RS485_inv_sel** (Available only when CRF2_Bit7=1) 0: Do not invert the behavior of RTSB# pin for RS485 auto flow control. 1: Invert the behavior of RTSB# pin for RS485 auto flow control.
5-0	Reserved.	

24.6 Logical Device 5 (Keyboard Controller)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: The logical device is inactive. 1: The logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 83h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	KBC clock rate selection **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: 12MHz 1 1: Reserved
5-3	Reserved.	
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

24.7 Logical Device 6 (CIR)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: CIR Interface is inactive. 1: CIR Interface is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for CIR.

CR F0h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 08h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R/W	CIR wide band filter select 0: Low-pass filter 1: Band-pass filter

BIT	READ / WRITE	DESCRIPTION
2-1	R/W	Timeout margin selection of CIR wide band band-pass filter 00: 200% recording carrier period 01: 100% recording carrier period 10: 50% recording carrier period 11: 25% recording carrier period
0	R/W	Carrier recording mode CIR wide band band-pass filter 0: Second carrier 1: Every carrier

CR F1h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 09h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Highest input period of CIR wide band band-pass filter (unit : us)

CR F2h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 32h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Lowest input period of CIR wide band band-pass filter (unit : us)

CR F3h.
Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	Reserved.
5-0	R / W	Recording carrier period of CIR wide band band-pass filter (unit : us)

24.8 Logical Device 7 (GPIO6, GPIO7, GPIO8, GPIO9)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 03h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	0: GPIO9 is inactive. 1: GPIO9 is active. (Default)
0	R / W	0: GPIO8 is inactive. 1: GPIO8 is active. (Default)

Note. The active and inactive register for GPIO6 and GPIO7 are located in logic device 9, CR30, bit 7~6.

CR E0h. GPIO7 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 I/O register 0: The respective GPIO7 PIN is programmed as an output port 1: The respective GPIO7 PIN is programmed as an input port.

CR E1h. GPIO7 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO7 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO7 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO7 Event Status Bit 7-0 corresponds to GP77-GP70, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO8 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : Efh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 I/O register 0: The respective GPIO8 PIN is programmed as an output port 1: The respective GPIO8 PIN is programmed as an input port.

CR E5h. GPIO8 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. GPIO8 Inversion Registe

Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. GPIO8 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO8 Event Status Bit 7-0 corresponds to GP87-GP80, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E8h. GPIO9 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO9 I/O register 0: The respective GPIO9 PIN is programmed as an output port 1: The respective GPIO9 PIN is programmed as an input port.

CR E9h. GPIO9 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO9 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR EAh. GPIO9 Inversion Register

Attribute: Read/Write
Power Well: VSB

Reset by: GP9X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO9 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR EBh. GPIO9 Status Register
Attribute: Read Only
Power Well: VSB
Reset by: GP9X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO9 Event Status Bit 7-0 corresponds to GP97-GP90, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR ECh. GPIO7 Multi-function Select Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO77 1: GPIO77 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO76 1: GPIO76 → GRN (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO75 1: GPIO75 → YLW (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO74 1: GPIO74 → GRN (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO73 1: GPIO73 → YLW (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO72 1: GPIO72 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO71 1: GPIO71 → YLW (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO70 1: GPIO70 → GRN (Please also set this GPIO to “output” type.)

CR EDh. GPIO8 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO87 1: GPIO87 → YLW (Please also set this GPIO to "output" type.)
6	R / W	0: GPIO86 1: GPIO86 → BEEP (Please also set this GPIO to "output" type.)
5	R / W	0: GPIO85 1: GPIO85 → SMI (Please also set this GPIO to "output" type.)
4	R / W	0: GPIO84 1: GPIO84 → WDTO (Please also set this GPIO to "output" type.)
3	R / W	0: GPIO83 1: GPIO83 → YLW (Please also set this GPIO to "output" type.)
2	R / W	0: GPIO82 1: GPIO82 → BEEP (Please also set this GPIO to "output" type.)
1	R / W	0: GPIO81 1: GPIO81 → SMI (Please also set this GPIO to "output" type.)
0	R / W	0: GPIO80 1: GPIO80 → WDTO (Please also set this GPIO to "output" type.)

CR EEh. GPIO9 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reversed	
3	R / W	0: GPIO93 1: GPIO93 → GRN (Please also set this GPIO to "output" type.)
2	R / W	0: GPIO92 1: GPIO92 → BEEP (Please also set this GPIO to "output" type.)
1	R / W	0: GPIO91 1: GPIO91 → SMI (Please also set this GPIO to "output" type.)
0	R / W	0: GPIO90 1: GPIO90 → WDTO (Please also set this GPIO to "output" type.)

CR F4h. (GPIO6 I/O Register; Default FFh)

Attribute: Read/Write
Power Well: VCC

Reset by: GP6X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an output port 1: The respective GPIO6 PIN is programmed as an input port.

CR F5h. GPIO6 Data Register
Attribute: Read/Write
Power Well: VCC
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. GPIO6 Inversion Register
Attribute: Read/Write
Power Well: VCC
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. GPIO6 Status Register
Attribute: Read Only
Power Well: VCC
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO6 Event Status Bit 7-0 corresponds to GP67-GP60, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F8h. GPIO6 Multi-function Select Register

Attribute: Read/Write

Power Well: VCC

Reset by: GP6X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO67 1: GPIO67 → GRN (Please also set this GPIO to "output" type.)
6	R / W	0: GPIO66 1: GPIO66 → BEEP (Please also set this GPIO to "output" type.)
5	R / W	0: GPIO65 1: GPIO65 → SMI (Please also set this GPIO to "output" type.)
4	R / W	0: GPIO64 1: GPIO64 → WDTO (Please also set this GPIO to "output" type.)
3	R / W	0: GPIO63 1: GPIO63 → GRN (Please also set this GPIO to "output" type.)
2	R / W	0: GPIO62 1: GPIO62 → BEEP (Please also set this GPIO to "output" type.)
1	R / W	0: GPIO61 1: GPIO61 → SMI (Please also set this GPIO to "output" type.)
0	R / W	0: GPIO60 1: GPIO60 → WDTO (Please also set this GPIO to "output" type.)

24.9 Logical Device 8 (WDT1, GPIO0, GPIO1, GPIOA)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved.	
3	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
2	R / W	0: GPIOA is inactive. 1: GPIOA is active.
1	R / W	0: GPIO0 is inactive. 1: GPIO0 is active.
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

Note. The active and inactive register for GPIO1 is located in logic device 9, CR30, bit1.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select GPIO Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR E0h. GPIO0 I/O Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-0	R / W	GPIO0 I/O register 0: The respective GPIO0 PIN is programmed as an output port 1: The respective GPIO0 PIN is programmed as an input port.

CR E1h. GPIO0 Data Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO0 Inversion Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO0 Status Register

Attribute: Read Only
Power Well: VCC
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO0 Event Status Bit 7-0 corresponds to GP05-GP00, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO0 Multi-function Select Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO07 1: GPIO07 → WDTO (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO06 1: GPIO06 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO05 1: GPIO05 → SMI (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
4	R / W	0: GPIO04 1: GPIO04 → WDTO (Please also set this GPIO to "output" type.)
3	R / W	0: GPIO03 1: GPIO03 → WDTO (Please also set this GPIO to "output" type.)
2	R / W	0: GPIO02 1: GPIO02 → BEEP (Please also set this GPIO to "output" type.)
1	R / W	0: GPIO01 1: GPIO01 → SMI (Please also set this GPIO to "output" type.)
0	R / W	0: GPIO00 1: GPIO00 → WDTO (Please also set this GPIO to "output" type.)

CR F0h. GPIO1 I/O Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP0X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an output port 1: The respective GPIO1 PIN is programmed as an input port.

CR F1h. GPIO1 Data Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. GPIO1 Inversion Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. GPIO1 Status Register

Attribute: Read Only
Power Well: VCC
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO1 Event Status Bit 7-0 corresponds to GP17-GP10, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR F4h. GPIO1 Multi-function Select Register

Attribute: Read/Write
Power Well: VCC
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO16 1: GPIO16 → GRN (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO15 1: GPIO15 → YLW (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO14 1: GPIO14 → GRN (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO13 1: GPIO13 → YLW (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO12 1: GPIO12 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO11 1: GPIO11 → YLW (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO10 1: GPIO10 → GRN (Please also set this GPIO to “output” type.)

CR F5h. Watchdog Timer I(WDT1) and KBC P20 Control Mode Register

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK(see LDA E7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	Watchdog Timer I count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer I count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of a KBC reset (P20) to issue a time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the Watchdog Timer I output low pulse to the KBRST# pin (PIN28) 0: Disable. 1: Enable.
0	Reversed	

CR F6h. Watchdog Timer I(WDT1) Counter Register

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK(see LDA E7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. If CR F7h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after 5.03×10^7 CLKIN cycle time, by analogy. (5.03×10^7 x (1/48MHz) = 1.046s)

CR F7h. Watchdog Timer I(WDT1) Control & Status Register

Attribute: Read/Write

Power Well: VCC

Reset by: LRESET# or PWROK(see LDA E7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by mouse interrupt. 1: Watchdog Timer I is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog Timer I is not affected by keyboard interrupt. 1: Watchdog Timer I is reset by keyboard interrupt.
5	Write “1” Only	Trigger Watchdog Timer I event. This bit is self-clearing.
4	R / W Write “0” Clear	Watchdog Timer I status bit 0: Watchdog Timer I is running. 1: Watchdog Timer I issues time-out event.
3-0	R / W	These bits select the IRQ resource for the Watchdog Timer I

24.10 Logical Device 9 (GPIO2, GPIO3, GPIO4, GPIO5)

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 04h

BIT	READ / WRITE	DESCRIPTION	
7	R / W	0: GPIO7 is inactive.	1: GPIO7 is active
6	R / W	0: GPIO6 is inactive.	1: GPIO6 is active
5	R / W	0: GPIO5 is inactive.	1: GPIO5 is active.
4	R / W	0: GPIO4 is inactive.	1: GPIO4 is active.
3	R / W	0: GPIO3 is inactive.	1: GPIO3 is active
2	R / W	0: GPIO2 is inactive.	1: GPIO2 is active.
1	R / W	0: GPIO1 is inactive.	1: GPIO1 is active.
0	Reserved.		

CR E0h. GPIO2 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : DFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an output port 1: The respective GPIO2 PIN is programmed as an input port.

CR E1h. GPIO2 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E2h. GPIO2 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E3h. GPIO2 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO2 Event Status Bit 7-0 corresponds to GP27-GP20, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIO3 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an output port 1: The respective GPIO3 PIN is programmed as an input port.

CR E5h. GPIO3 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E6h. GPIO3 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E7h. GPIO3 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO3 Event Status Bit 7-0 corresponds to GP37-GP30, respectively. 0 : No active edge(rising/falling) has been detected 1 : An active edge(rising/falling) has been detected Read the status bit clears it to 0.

CR E9h. GPIO2 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO27 1: GPIO27 → GRN (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO26 1: GPIO26 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO25 1: GPIO25 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO24 1: GPIO24 → WDTO (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO23 1: GPIO23 → GRN (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO22 1: GPIO22 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO21 1: GPIO21 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO20 1: GPIO20 → WDTO (Please also set this GPIO to “output” type.)

CR EAh. GPIO3 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO37 1: GPIO37 → GRN (Please also set this GPIO to "output" type.)
6	R / W	0: GPIO36 1: GPIO36 → BEEP (Please also set this GPIO to "output" type.)
5	R / W	0: GPIO35 1: GPIO35 → SMI (Please also set this GPIO to "output" type.)
4	R / W	0: GPIO34 1: GPIO34 → WDTO (Please also set this GPIO to "output" type.)
3	R / W	0: GPIO33 1: GPIO33 → GRN (Please also set this GPIO to "output" type.)
2	R / W	0: GPIO32 1: GPIO32 → BEEP (Please also set this GPIO to "output" type.)
1	R / W	0: GPIO31 1: GPIO31 → SMI (Please also set this GPIO to "output" type.)
0	R / W	0: GPIO30 1: GPIO30 → WDTO (Please also set this GPIO to "output" type.)

CR EBh. GPIO5 Multi-function Select Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → GRN (Please also set this GPIO to "output" type.)
6	R / W	0: GPIO56 1: GPIO56 → BEEP (Please also set this GPIO to "output" type.)
5	R / W	0: GPIO55 1: GPIO55 → SMI (Please also set this GPIO to "output" type.)
4	R / W	0: GPIO54 1: GPIO54 → WDTO (Please also set this GPIO to "output" type.)
3	R / W	0: GPIO53 1: GPIO53 → GRN (Please also set this GPIO to "output" type.)
2	R / W	0: GPIO52 1: GPIO52 → BEEP (Please also set this GPIO to "output" type.)
1	R / W	0: GPIO51 1: GPIO51 → SMI (Please also set this GPIO to "output" type.)
0	R / W	0: GPIO50 1: GPIO50 → WDTO (Please also set this GPIO to "output" type.)

CR F0h. GPIO4 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an output port 1: The respective GPIO4 PIN is programmed as an input port.

CR F1h. GPIO4 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F2h. GPIO4 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E8h. GPIO4 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO4 Event Status Bit 7-0 corresponds to GP47-GP40, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR EEh. GPIO4 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO46 1: GPIO46 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO45 1: GPIO45 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO44 1: GPIO44 → WDTO (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO43 1: GPIO43 → YLW (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO42 1: GPIO42 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO41 1: GPIO41 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO40 1: GPIO40 → WDTO (Please also set this GPIO to “output” type.)

CR F4h. GPIO5 I/O Register

Attribute: Read/Write

Power Well: VSB
Reset by: GP5X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4-0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an output port 1: The respective GPIO5 PIN is programmed as an input port.

CR F5h. GPIO5 Data Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4-0	R / W	GPIO5 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F6h. GPIO5 Inversion Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4-0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR F7h. GPIO5 Status Register
Attribute: Read Only
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	

BIT	READ / WRITE	DESCRIPTION
4-0	Read Only Read-Clear	GPIO5 Event Status Bit 7-0 corresponds to GP57-GP50, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR FEh. Input Detected Type Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP9X_MRST(Bit7-6, Bit3-2), GP4X_MRST(Bit5-4, Bit1-0)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Enable GP93 input de-bouncer 1: Disable GP93 input de-bouncer
6	R / W	0: Enable GP92 input de-bouncer 1: Disable GP92 input de-bouncer
5	R / W	0: Enable GP46 input de-bouncer 1: Disable GP46 input de-bouncer
4	R / W	0: Enable GP41 input de-bouncer 1: Disable GP41 input de-bouncer
3	R / W	0: GP93 trigger type: edge 1: GP93 trigger type: level
2	R / W	0: GP92 trigger type: edge 1: GP92 trigger type: level
1	R / W	0: GP46 trigger type: edge 1: GP46 trigger type: level
0	R / W	0: GP41 trigger type: edge 1: GP41 trigger type: level

24.11 Logical Device A (ACPI)

CR E0h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 01h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN is wire-AND and connected to PSOUT#.
1: PSIN is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Enable CIR wake-up
0: Disable CIR wake-up function via PSOUT#.
1: Enable CIR wake-up function via PSOUT#.</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
<tr><td>1</td><td>R / W</td><td>MSXKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.</td></tr>
<tr><td>0</td><td>R / W</td><td>KBXKEY =>
0: Only the pre-determined key combination in sequence can wake up the system.
1: Any character received from the keyboard can wake up the system.</td></tr>
</table>

CR E1h. KBC Wake-Up Index Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. KBC Wake-Up Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. Event Status Register

Attribute: Read Only
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	Read Only Read-Clear	This status flag indicates VSB power off/on.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset, PWROK(Bit4), LRESET#(Bit3-2)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-5	R / W	Power-loss control [Note] (These two bits will determine the system turn on or off after AC resume, from G3 to S5 state.) **Bits** **6 5** 0 0: Always turn off. 0 1: Always turn on. (PSON# will active when S3# is high.) 1 0: Pre-state. (System turns On or Off which depends on the state before the power loss. Pease check the definition of the pre-state is "ON" or "OFF" in chapter 26.2.) 1 1: User defined mode for power loss last-state. (The last-state flag is located on "CRE6h, bit4.")
4	R / W	3VSBSW# enable bit 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for wake-up events set in CRE0. This bit is cleared when any wake-up event is captured. (Note. This bit is use for KB and MS to generate PSOUT# while VCC valid, for example, wake-up from S1 to S0 via PSOUT#.) 0: Disable.(Default) 1: Enable.
1-0	Reserved.	

Note. Whether "Always turn on", "Pre-state" or "User defined mode", the PSON#'s active condition for system to turn-on is S3# goes high. For south-bridge which S3# default is low while AC resume, please refer "CRE7h, bit4" to achieve the power-loss control application.

CR E5h. GPIOs Reset Source Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 02h

BIT	READ / WRITE	DESCRIPTION
7	R / W	GPAX_MRST 0: GPAX reset by LRESET#. (Default) 1: GPAX reset by PWROK.
6	R / W	GP9X_MRST 0: GP9X reset by RSMRST#. (Default) 1: GP9X reset by SLPS5.

BIT	READ / WRITE	DESCRIPTION
5	R / W	GP8X_MRST 0: GP8X reset by RSMRST#. (Default) 1: GP8X reset by SLPS5.
4	R / W	GP7X_MRST 0: GP7X reset by RSMRST#. (Default) 1: GP7X reset by SLPS5.
3	R / W	GP6X_MRST 0: GP6X reset by RSMRST#. (Default) 1: GP6X reset by SLPS5.
2	R / W	RESETCONO# signal to control PWROK 0: Disable (Default) 1: Enable
1	R / W	PWROK source selection. 0: PSON#. 1: SLP_S3#. (Default)
0	R / W	ATXPGD signal to control PWROK 0: Enable. (Default) 1: Disable.

CR E6h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7, Bit5, Bit3-1), Battery reset(Bit6, Bit4), PWROK(Bit0)

Default : 1Ch

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Read Only	SKTOCC Status. This bit is '1' when pin 102 SKTOCC# = 1.
5	R / W	CASEOPEN0 Clear Control. Write 1 to this bit to clear CASEOPEN0 status. This bit will clear the status itself.
4	R / W	Power-loss Last State Flag. 0: ON 1: OFF. (Default)

BIT	READ / WRITE	DESCRIPTION
3-1	R / W	PWROK_DEL Set the delay time when rising from 3VCC to PWROK **Bits** **3 2 1** 0 0 0: 300 ~ 600mS 0 0 1: 330 ~ 670mS 0 1 0: 390 ~ 730mS 0 1 1: 520 ~ 860mS 1 0 0: 200 ~ 300mS 1 0 1: 230 ~ 370mS 1 1 0: 290 ~ 430mS (Default) 1 1 1: 420 ~ 560mS
0	R / W	PWROK_TRIG => 0: PWROK work normally. (Default) 1: Write 1 will let PWROK keep low or from high to low immediately.

CR E7h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7-5, Bit3-2), Battery reset(Bit4, Bit1-0)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (For southbridge which S3# default is low when AC resume, like VIA, AMD…etc.) 0: Disable. (Default) 1: Enable.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Select WDT1 reset source 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK.
2	Reserved.	
1	R / W	SKTOCC Clear Control. Write 1 to this bit to clear SKTOCC status. This bit will clear the status itself.
0	R / W	Hardware Monitor RESET source select 0: PWROK. (Default) 1: LRESET#.

CR E9h. GPIOs Reset Source Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	GP5X_MRST 0: GP5X reset by RSMRST#. 1: GP5X reset by SLPS5.
4	R / W	GP4X_MRST 0: GP4X reset by RSMRST#. 1: GP4X reset by SLPS5.
3	R / W	GP3X_MRST 0: GP3X reset by RSMRST#. 1: GP3X reset by SLPS5.
2	R / W	GP2X_MRST 0: GP2X reset by RSMRST#. 1: GP2X reset by SLPS5.
1	R / W	GP1X_MRST 0: GP1X reset by RSMRST#. 1: GP1X reset by SLPS5.
0	R / W	GP0X_MRST 0: GP0X reset by LRESET#. 1: GP0X reset by PWROK.

CR EEh.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	CASEOPEN1 Clear Control. Write 1 to this bit to clear CASEOPEN1 status. This bit will clear the status itself.

CR F0h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	Pin70 function selection LDA CRF0 [Bit7-5] / Pin70 000 / DEEP_S5 001 / 3VSBSW 010 / LATCH_BKFD_CUT 011 / ATXPGDO 1xx / PWROK
4-0	Reserved.	

CR F2h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 5Ch

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved.	
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#. (Default)
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#. (Default)
2	R / W	Enable RSTOUT0# function. 0: Disable RSTOUT0#. 1: Enable RSTOUT0#. (Default)
1	Reserved.	
0	R / W	EN_PME 0 : Disable PME. (Default) 1 : Enable PME.

CR F3h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W-Clear	PME status of the Mouse event. Write 1 to clear this status.
4	R / W-Clear	PME status of the KBC event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the FDC IRQ event. Write 1 to clear this status.
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	Reserved.	

CR F4h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDT1 event. Write 1 to clear this status.
1	Reserved.	
0	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.

CR F6h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#(Bit7), RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS interrupt of the KBC password event. 1: Enable KB, MS interrupt of the KBC password event.

BIT	READ / WRITE	DESCRIPTION
6	Reserved.	
5	R / W	0: Disable PME interrupt of the Mouse event. 1: Enable PME interrupt of the Mouse event.
4	R / W	0: Disable PME interrupt of the KBC event. 1: Enable PME interrupt of the KBC event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.
2	R / W	0: Disable PME interrupt of the FDC IRQ event. 1: Enable PME interrupt of the FDC IRQ event.
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	Reserved.	

CR F7h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : C0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	RSTOUT2# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
6	R / W	RSTOUT1# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
5	Reserved	
4	R / W	0: Disable PME interrupt of the CIRWAKEUP IRQ event. 1: Enable PME interrupt of the CIRWAKEUP IRQ event.
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.
2	R / W	0: Disable PME interrupt of the WDT1 event. 1: Enable PME interrupt of the WDT1 event.
1	Reserved.	
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

CR FEh. GPIO41, GPIO46, GPIO92 and GPIO93 Event Route Selection Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable GP41 event route to PSOUT#. 1: Enable GP41 event route to PSOUT#.
6	R / W	0: Disable GP46 event route to PSOUT#. 1: Enable GP46 event route to PSOUT#.
5	R / W	0: Disable GP92 event route to PSOUT#. 1: Enable GP92 event route to PSOUT#.
4	R / W	0: Disable GP93 event route to PSOUT#. 1: Enable GP93 event route to PSOUT#.
3	R / W	0: Disable GP41 event route to PME#. 1: Enable GP41 event route to PME#.
2	R / W	0: Disable GP46 event route to PME#. 1: Enable GP46 event route to PME#.
1	R / W	0: Disable GP92 event route to PME#. 1: Enable GP92 event route to PME#.
0	R / W	0: Disable GP93 event route to PME#. 1: Enable GP93 event route to PME#.

24.12 Logical Device B (Hardware Monitor, Front Panel LED)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	AUXFANIN0 Source Select 0: AUXFANIN0 (pin3) 1: GP70 (pin93)
6	R / W	AUXFANIN1 Source Select 0: AUXFANIN1 (pin4) 1: GP72 (pin91)
5	R / W	AUXFANIN2 Source Select 0: AUXFANIN2 (pin5) 1: GP73 (pin90)
4-1	Reserved.	
0	R / W	0: Hardware Monitor & SB-TSI device is inactive. 1: Hardware Monitor & SB-TSI device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

CR 62h, 63h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the SB-TSI base address <100h : FFEh> along a two-byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select the IRQ resource for HM.

CR E0h. SYSFAN Duty Cycle Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SYSFAN Duty Cycle Register

CR E1h. CPUFAN Duty Cycle Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	CPUFAN Duty Cycle Register

CR E2h. AUXFAN Duty Cycle Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN Duty Cycle Register

CR F0h. FANIN De-bouncer Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5	R / W	1: Enable AUXFANIN2 input de-bouncer. 0: Disable AUXFANIN2 input de-bouncer.
4	R / W	1: Enable AUXFANIN1 input de-bouncer. 0: Disable AUXFANIN1 input de-bouncer.
3	R / W	1: Enable AUXFANIN0 input de-bouncer. 0: Disable AUXFANIN0 input de-bouncer.

BIT	READ / WRITE	DESCRIPTION
2	R / W	1: Enable CPUFANIN input de-bouncer. 0: Disable CPUFANIN input de-bouncer.
1	R / W	1: Enable SYSFANIN input de-bouncer. 0: Disable SYSFANIN input de-bouncer.
0	Reserved.	

CR F1h. SMI IRQ Register

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	SMI IRQ Enable
6-0	Reserved.	

CR F2h. Deep S3 Sleeping State Front panel Green & Yellow LED control register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	**Deep S3**_YLW_BLK_FREQ bits (This function affects by LDB CRF9 Bit 7) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. 1XXX: Fading LED.
3-0	R / W	**Deep S3**_GRN_BLK_FREQ bits (This function affects by LDB CRF9 Bit 6) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. 1XXX: Fading LED.

CR F5h. SMBus de-bouncer Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	1: Enable SCL input de-bouncer 160ns. 0: Disable SCL input de-bouncer.
0	R / W	1: Enable SDA input de-bouncer 160ns. 0: Disable SDA input de-bouncer.

CR F6h. Deep S5 Front Panel Green & Yellow LED control register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	**Deep S5**_YLW_BLK_FREQ bits (This function affects by LDB CRF9 Bit 5) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. 1XXX: Fading LED.
3-0	R / W	**Deep S5**_GRN_BLK_FREQ bits (This function affects by LDB CRF9 Bit 4) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. 1XXX: Fading LED.

CR F7h. Front Panel Green LED (GRN_LED) control register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 87h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	**AUTO_EN** (Powered by VSB, RSMRST# reset , default = 1) 0: GRN_LED and YLW_LED are controlled by GRN_ LED_ RST, GRN_BLK_FREQ and YLW_LED_RST, YLW_BLK_FREQ bits. 1: GRN_LED and YLW_LED are controlled by "SLP_S5#" and "SLP_S3#".
6	R / W	**GRN_LED_RST#** (Default= 0) 0: GRN_BLK_FREQ will be set to "0000" (High-Z) when into S3~S5 state. 1: GRN_BLK_FREQ will be kept when into S3~S5 state.
5	R / W	GRN_LED_POL 0: GRN_LED output is active low. (Default) 1: GRN_LED output is active high.
4	Reserved.	
3-0	R / W	**GRN_BLK_FREQ** bits (The reset depends on bit6, GRN_LED_RST#) 0000: High-Z. (The output type of YLW_LED is open-drain.) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. (Default) 1XXX: Fading LED.

CR F8h. Front Panel Yellow LED (YLW_LED) control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 47h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	**YLW_LED_RST#** (Default =1) 0: YLW_BLK_FREQ will be set to "0000" (High-Z) when into S3~S5 state. 1: YLW_BLK_FREQ will be kept when into S3~S5 state.
5	R / W	YLW_LED_POL 0: YLW_LED output is active low. (Default) 1: YLW_LED output is active high.
4	Reserved.	

BIT	READ / WRITE	DESCRIPTION
3-0	R / W	**YLW_BLK_FREQ** bits (The reset depends on bit6,YLW_LED_RST#) 0000: High-Z. (The output type of YLW_LED is open-drain.) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. (Default) 1XXX: Fading LED.

CR F9h. Deep Sleep LED Eanble register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Deep S3_YLW_BLK_FREQ : 0: Depend on setting of CRF2h, bit7~4. 1: Always output high.
6	R / W	Deep S3_GRN_BLK_FREQ : 0: Depend on setting of CRF2h, bit3~0. 1: Always output high.
5	R / W	Deep S5_YLW_BLK_FREQ : 0: Depend on setting of CRF6h, bit7~4. 1: Always output high.
4	R / W	Deep S5_GRN_BLK_FREQ : 0: Depend on setting of CRF2h, bit3~0. 1: Always output high.
3-0	Reserved.	

CR FAh.RESETCONO# and PWROK active Pulse width selection

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-2	R / W	RESETCONO# and PWROK active Pulse width selection 00:54.68ms ~ 58.59ms 01:109.37ms ~ 117.18ms 10:218.75ms ~ 234.37ms 11:218.75ms ~ 234.37ms
1-0	Reserved.	

24.13 Logical Device D (VID)

CR E0h. VID Manual Mode Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	Read/Write	Description
7~0	R/W	VID Manual Mode Control Values.

CR E1h. VID offset Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
6	R/W	VID offset Register

Vrm11	bit7	0: Increase voltage 1: Decrease voltage
	bit6~0	Every step is 6.25mv
amd6bit	bit5	0: Increase voltage 1: Decrease voltage
	bit4~0	Every step is 25mv

CR E2h. VID Output Register

Attribute: Read Only
Power Well: VSB
Reset by: PWROK
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	RO	VID Output Values: This register reflects the behavior on VID output pins.

CR E3h. VID Input Register

Attribute: Read Only
Power Well: VSB
Reset by: PWROK
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	RO	VID Input Values: This register reflects the behavior on VID input pins.

CR E4h. PVID Configuration Register

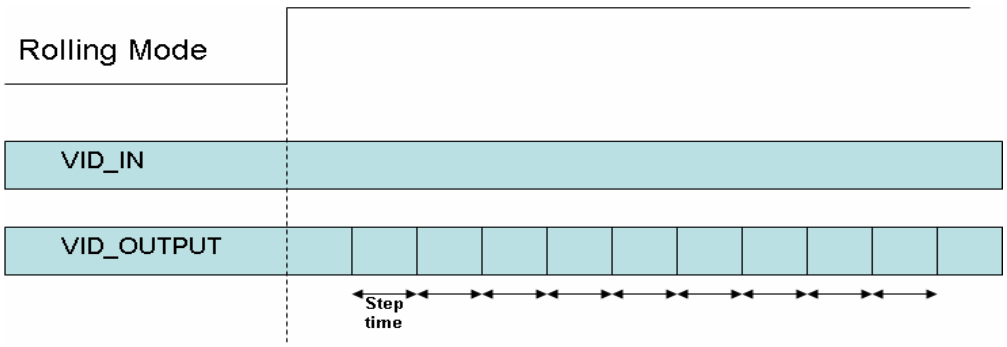
Attribute: Read/Write

Power Well: VSB

Reset by: VID reset(Bit7-6, 2-1), RSMRST#(Bit5-3)

Default : 00h

BIT	Read/Write	Description
7~6	R/W	PVID Mode Select 00: Bypass mode. (VID output = VID input) 01: Offset mode. (VID output = VID input ± Offset) 10: Manual mode. (VID output = VID Manual data) 11: Compare mode. (VID output = Bigger one) (VID input v.s.VID Manual data)
5	R/W	Reserved
4	R/W	Rolling mode 0: Disable Rolling mode. (Default) 1: Enable Rolling mode.
3	R/W	Reserved
2~1	R/W	PVID table selection 10 AMD 6-Bit 01 VRM 11 (8-Bit) **Default: 00 (Bypass mode)**
0	Reserved	



Rolling Mode :

Disable : VID_OUT will reflect the VID_IN

Enable : VID_OUT will increase/decrease one step every step time when PWROK assert.

step time can set by register.

CR E5h. SVID Manual Mode Register

Attribute: Read/Write

Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SVID Manual Mode Control Values.

CR E6h. AMD SVID0 offset Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R/W	1: Increase SVID code 0: Decrease SVID code
5-0	R/W	Every step is 12.5mv

Note: VID code step ↑, CPUVCORE voltage ↑

CR E6h. Intel SVID offset Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R/W	1: Increase SVID code 0: Decrease SVID code
6-0	R/W	Every step is 35mv

Note: VID code step ↑, CPUVCORE voltage ↑

CR E9h. SVID Configure Register
Attribute: Read/Write
Power Well: VSB
Reset by: SVID Reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	SVID Mode Select 00: Bypass mode. (VID output = VID input) 01: Offset mode. (VID output = VID input ± Offset) 10: Manual mode. (VID output = VID Manual data) 11: Compare mode. (VID output = Bigger one) (VID input v.s.VID Manual data)
5-0	**Reserved.**	

CR EEh. Reset Source Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 88h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable Watchdog Timer I as the SVID reset source. 0: Disable 1: Enable (Default)
6	R / W	Enable PWROK as the SVID reset source. 0: Disable 1: Enable
5	R / W	Enable LRESET as the SVID reset source. 0: Disable 1: Enable
4	R / W	Enable pin53 (VID_RST#) as the SVID reset source. 0: Disable 1: Enable
3	R / W	Enable Watchdog Timer I (WDT1) as the PVID reset source. 0: Disable 1: Enable (Default)
2	R / W	Enable PWROK as the PVID reset source. 0: Disable 1: Enable
1	R / W	Enable LRESET as the PVID reset source. 0: Disable 1: Enable
0	R / W	Enable pin53 (VID_RST#) as the PVID reset source. 0: Disable 1: Enable

CR EFh. Rolling rate Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Rolling rate value (Can't input FFh to this register.) Rolling rate = 330ns* (Rolling rate value+1).

CR F4h. SVID Output Register

Attribute: Read Only
Power Well: VSB
Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	RO	SVID Output Values: This register reflects the behavior on SVID output pins.

CR F5h. SVID Input Register

Attribute: Read Only
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	RO	SVID Input Values: This register reflects the behavior on SVID input pins.

CR F0h. Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	RO	Mask WDT1 to affect PWROK 0: Mask disable. (WDT1 default affect PWROK) 1: Mask enable. (WDT1 not affect PWROK)
6-0	Reserved.	

24.14 Logical Device E (CIR WAKE-UP)

CR 30h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	0: CIR Wake-up is inactive. 1: CIR Wake-up Interface is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Wake-up Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VCC
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	These bits select IRQ resource for CIR Wake-up.

24.15 Logical Device F (GPIO Push-pull or Open-drain selection)

CR E0h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP1 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E1h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : DFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP2 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E2h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP3 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E3h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FEh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP4 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E4h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : F6h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP5 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E5h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP6 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E6h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP7 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E7h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : D3h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP8 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E8h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP9X_MRST

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP9 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E9h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 9Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP0 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR F0h. I2C Control & Address Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable I2C_Slave
6-0	R / W	I2C Address

CR F1h. I2C to 80PORT Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1	R / W	80PORT Display 0: Enable 1: Disable
0	R / W	LPC or I2C to 80PORT switch

CR F2h. I2C to 80PORT Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	I2C to 80PORT Data

24.16 Logical Device 14 (SVID)

CR E0h. AMD SVID Factor_L Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Factor_L

CR E1h. AMD SVID Factor_M Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Factor_M

FACTOR_M[7:6] = 10	**SVID_Freq = 1* SCL_IN_Freq (default)**
FACTOR_M[7:6] = 01	SVID_Freq = 2* SCL_IN_Freq
FACTOR_M[7:6] = 11	SVID_Freq = 4* SCL_IN_Freq
FACTOR_M[7:6] = 00	SVID_Freq = $\frac{SYS_CLK}{4*(1+FACTOR_L)*2^{FACTOR_M[1:0]+1}}$

CR E3h. AMD SVID1 offset Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R/W	1: Increase VID code 0: Decrease VID code
5-0	R/W	Every step is 12.5mv

Note: VID code step ↑, CPUVCORE voltage ↓

CR E4h. AMD SVIDNB offset Register

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R/W	1: Increase VID code 0: Decrease VID code
5-0	R/W	Every step is 12.5mv

Note: VID code step ↑, CPUVCORE voltage ↓

Note: We support three offset to conform AMD Serial VID SPEC，but in application，maybe we only use one offset。

24.17 Logical Device 16 (Deep Sleep)

CR 30h. Deep Sleep configuration register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 20h

BIT	READ / WRITE	DESCRIPTION
7	R / W	DIS_SLPSUS_PULLUP (test mode) 0: Enable pin 89 (SLP_SUS#) internal pull-ups when DSW function routes to PVID pins. 1: Disable pin 89 (SLP_SUS#) internal pull-up.
6	R / W	RSMRST# Detect Source Select for Deep Sleep Mode. 0: RSMRST# detected source from PSOUT# voltage (Pin60). 1: RSMRST# detected source from PCHVSB voltage (Pin97). **Note**. Set to 0, if Deep S5 is enabled. Set to 1, if DSW is enabled.
5	R / W	Deep_s3_opt 0: When enter Deep S3 state, the SUS_WARN_5VDUAL will keep low. 1: When enter Deep S3 state, the SUS_WARN_5VDUAL will follow DSW sequence.
4	R / W	dsw_wake_opt (test mode) 0: The PSOUT# will assert until SLPS3# high when deep s5 wakeup event happened. 1: The PSOUT# will assert until RSMRST_L high and SLP_SUS_L high when deep s5 wakeup event happened. **PS. This bit only active when PCH_DSW_EN & (Deep S5 Enable | Deep S3 Enable)**
3	R / W	PCH DSW Enable 0: If PCH disable DSW function. 1: if PCH enable DSW function. (SLP_SUS# affects RSMRST#)
2	R / W	Reserved.
1	R / W	Deep S3 Enable 0: If SLP_S3# state will not enter Deep S3 state. 1: If SLP_S3# state will enter Deep S3 state.
0	R / W	Deep S5 Enable 0: Disable Deep S5 function when into S5 state (SLP_S5#). 1: Enable Deep S5 function when into S5 state (SLP_S5#).

CR E0h. Deep Sleep wake up PSOUT# delay time

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : **20h** (Default: 512ms)

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved.	
5-0	R / W	Deep Sleep wake up PSOUT# delay time. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT# after SYS_3VSB and wait a delay time. DELAY TIME = (Setting Value) * 16ms Example : maximum delay time = $(3F)_{hex}$ * 16ms = 1008ms

CR E1h. Deep Sleep wake up PSOUT# pulse width

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : **04h** (Default: 128 ms)

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved.	
3-0	R / W	Deep Sleep wake up PSOUT# pulse width. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT#.. Pulse Width = (Setting Value) * **32ms** Example : maximum pulse width = $(F)_{hex}$ * **32ms** = 480ms

CR E2h. Reserved

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 05h

24.18 Logical Device 17 (GPIOA)

CR E0h. GPIOA I/O Register

Attribute: Read/Write
Power Well: VCC
Reset by: GPAX_MRST
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reversed	
0	R / W	GPIOA I/O register 0: The respective GPIOA PIN is programmed as an output port 1: The respective GPIOA PIN is programmed as an input port.

CR E1h. GPIOA Data Register

Attribute: Read/Write
Power Well: VCC
Reset by: GPAX_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reversed	
0	R / W	GPIOA Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E2h. GPIOA Inversion Register

Attribute: Read/Write
Power Well: VCC
Reset by: GPAX_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reversed	
0	R / W	GPIOA Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E3h. GPIOA Status Register

Attribute: Read Only
Power Well: VCC
Reset by: GPAX_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reversed	
0	Read Only Read-Clear	GPIOA Event Status Bit 7-0 corresponds to GPA7-GPA0, respectively. 0 : No active edge (rising/falling) has been detected 1 : An active edge (rising/falling) has been detected Read the status bit clears it to 0.

CR E4h. GPIOA PUSH-PULL/OD Register

Attribute: Read/Write
Power Well: VCC
Reset by: GPAX_MRST
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reversed	
0	R / W	GPA Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E5h. GPIOA Multi-function Select Register

Attribute: Read/Write
Power Well: VCC
Reset by: GPAX_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reversed	
0	R / W	0:GPIOA0 1:GPIOA0 → WDTO

25. SPECIFICATIONS

25.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

25.2 DC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

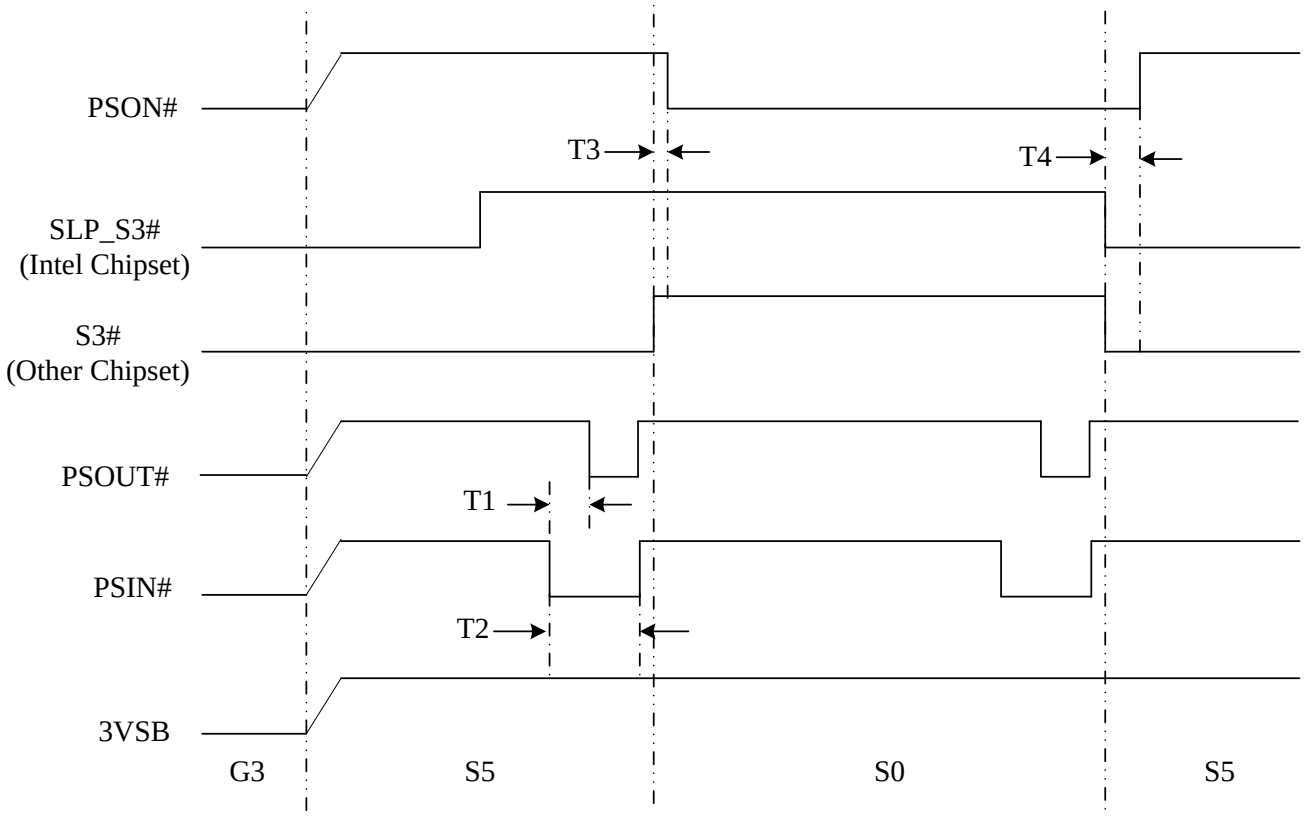
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	IBAT			2.4	μA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IVSB			8.0	mA	VSB = 3.3 V, All ACPI pins are not connected.
VCC Quiescent Current	IVCC			25	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
Vtt Quiescent Current	IVTT			1	mA	VSB = 3.3 V VCC (AVCC)= 3.3 V VTT = 1.2V LRESET = High IOCLK = 48MHz CASEOPEN Pull-Up to VBAT
AIN – Analog input						
AOUT – Analog output						
IN_{tp3} – 3.3V TTL-level input pin						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp3} – 3.3V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{gp5} – 5V GTL-level input pin						
Input Low Voltage	V_{IL}		0.72		V	
Input High Voltage	V_{IH}		0.72		V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tp5} – 5V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tscup5} – 5V TTL-level, Schmitt-trigger input buffer with controllable pull-up						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{CC} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{CC} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{CC} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
O_8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
OD_8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
O_{12} – Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_{12} – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{24} – Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD_{24} – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
O_{48} – Output pin with 48mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -48 mA
OD_{48} – Open-drain output pin with 48mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	0.275*V_{tt}		0.5*V_{tt}	V	
Input High Voltage	V_{IH}	0.55*V_{tt}		0.725*V_{tt}	V	
Output Low Voltage	V_{OL}			0.25*V_{tt}	V	
Output High Voltage	V_{OH}	0.75*V_{tt}			V	
Hysterisis	V_{Hys}	0.1*V_{tt}			V	
O_{12cu} – Output pin 12mA source-sink capability with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_{12cu} – Open-drain 12mA sink capability output pin with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA

26. AC CHARACTERISTICS

26.1 Power On / Off Timing

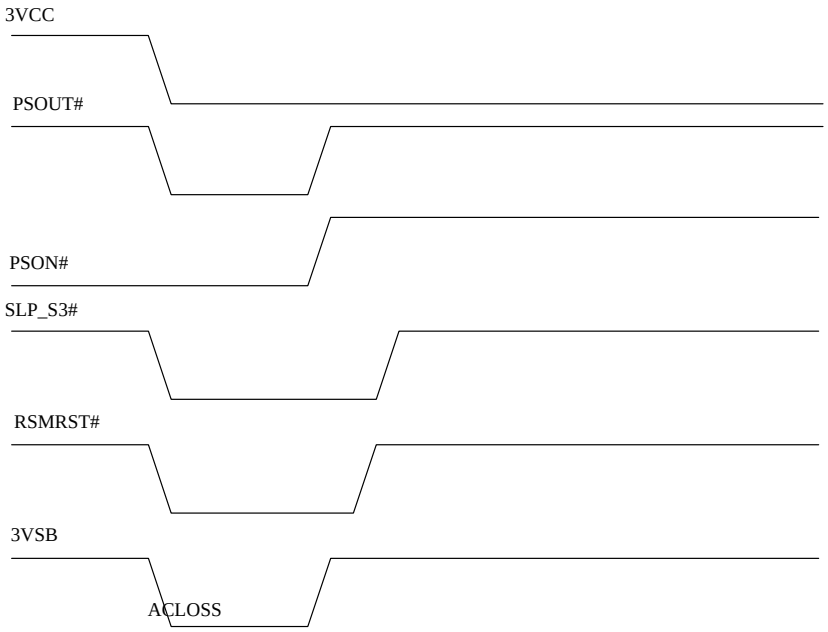


	T1	T2	T3	T4
IDEAL TIMING	64ms	Over 64ms at least	< 10ns	32ms

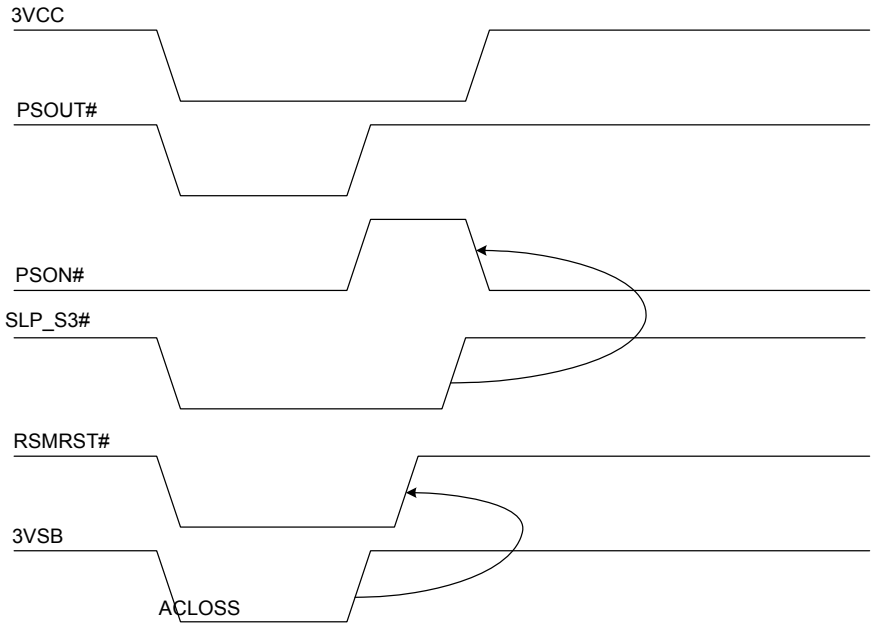
26.2 AC Power Failure Resume Timing

(1) Logical Device A, CR [E4h] bits [6:5] =00 means “OFF” state

(“OFF” means the system is always turned off after the AC power loss recovered.)



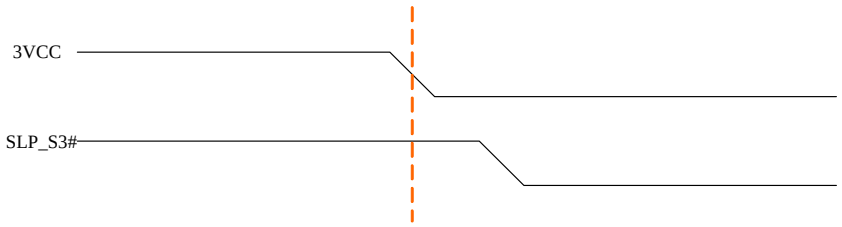
(2) Logical Device A, CR [E4h] bits [6:5]=01 means “ON” state.
(“ON” means the system is always turned on after AC power loss recovered.)



**** What's the definition of former state at AC power failure?**

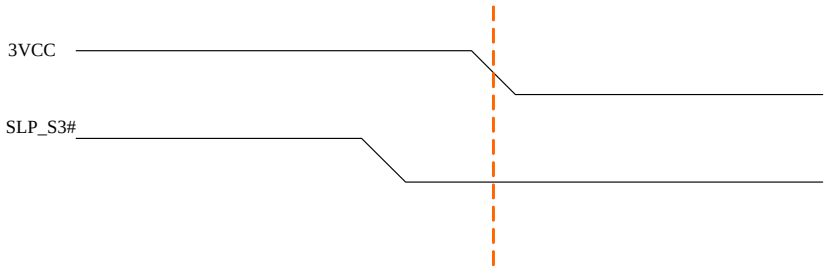
1) The previous state is "ON"

VCC falls to 2.6V and SLP_S3# keeps at VIH 2.0V



2) The previous state is "OFF"

VCC fall to 2.6V and SLP_S3# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6776F / NCT6776D adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6~5 of CR E4h and bit 4 of CR E6h in Logical Device A.

CR E4h

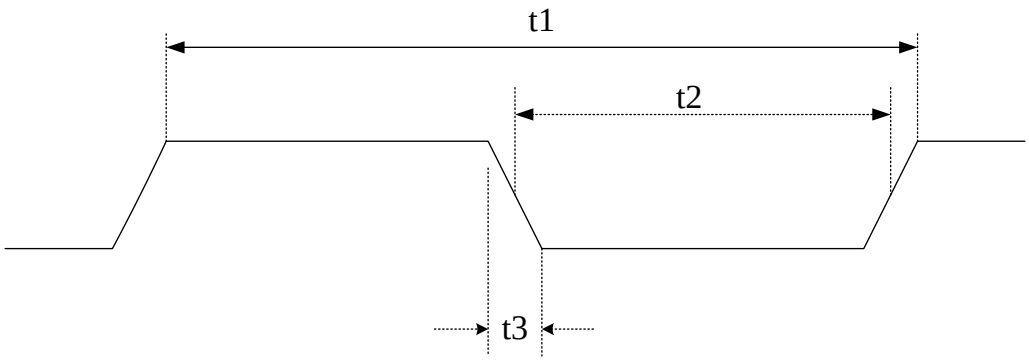
BIT	READ/WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (VBAT) 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logic Device A, CRE6[4])

CR E6h

BIT	READ/WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

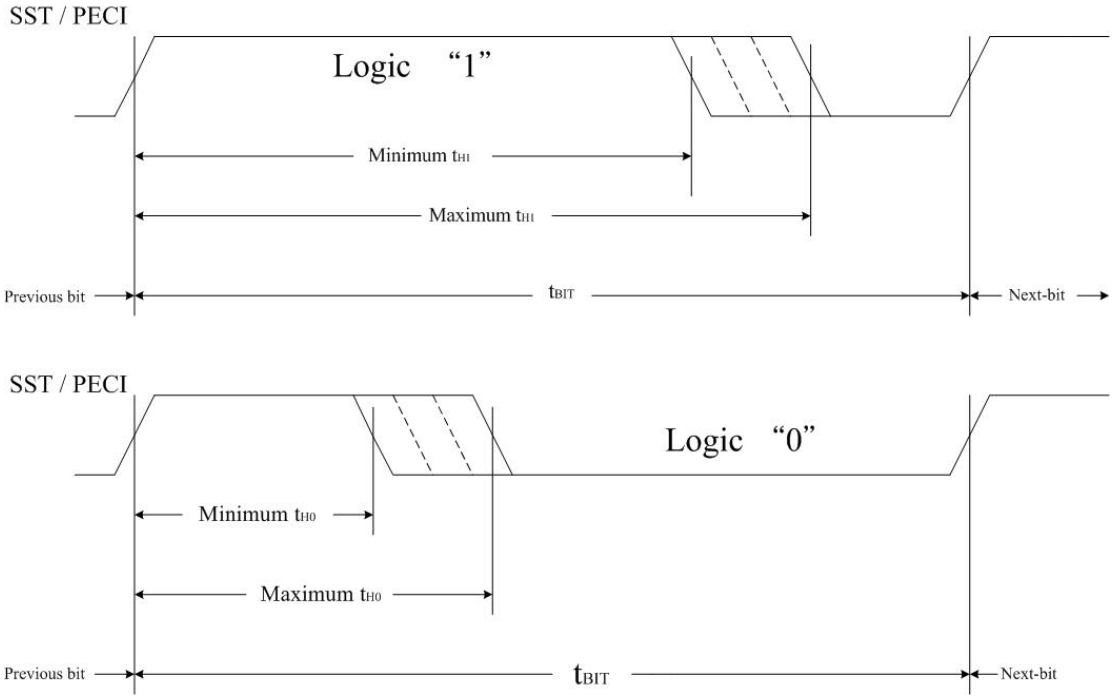
26.3 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



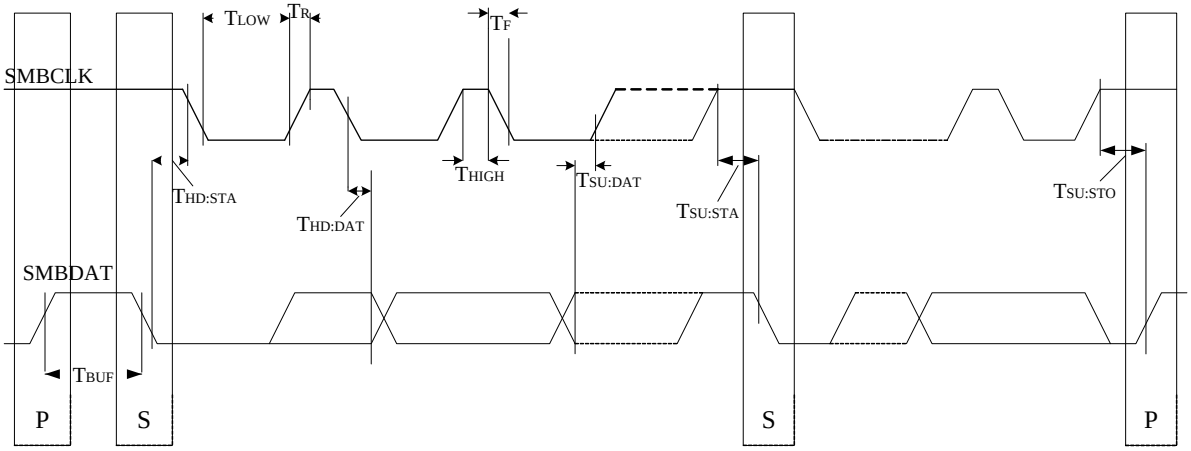
PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

26.4 PECI Timing



SYMBOL		MIN	TYP	MAX	UNITS
t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

26.5 SMBus Timing



26.6 Floppy Disk Drive Timing

FDC: Data rate = 1MB, 500KB, 300KB, 250KB/sec.

PARAMETER	SYM.	MIN.	TYP. (NOTE 1)	MAX.	UNIT
DIR# setup time to STEP#	TDST	1.0/1.6 /2.0/4.0			µS
DIR# hold time from STEP#	TSTD	24/40 /48/96			µS
STEP# pulse width	TSTP	6.8/11.5 /13.8/27. 8	7/11.7 /14/28	7.2/11.9 /14.2/28. 2	µS
STEP# cycle width	TSC	NOTE 2	NOTE 2	NOTE 2	mS
INDEX# pulse width	TIDX	125/250 /417/500			nS
RDATA# pulse width	TRD	40			nS
WD# pulse width	TWD	100/185 /225/475	125/210 /250/500	150/235 /275/525	nS

Notes:

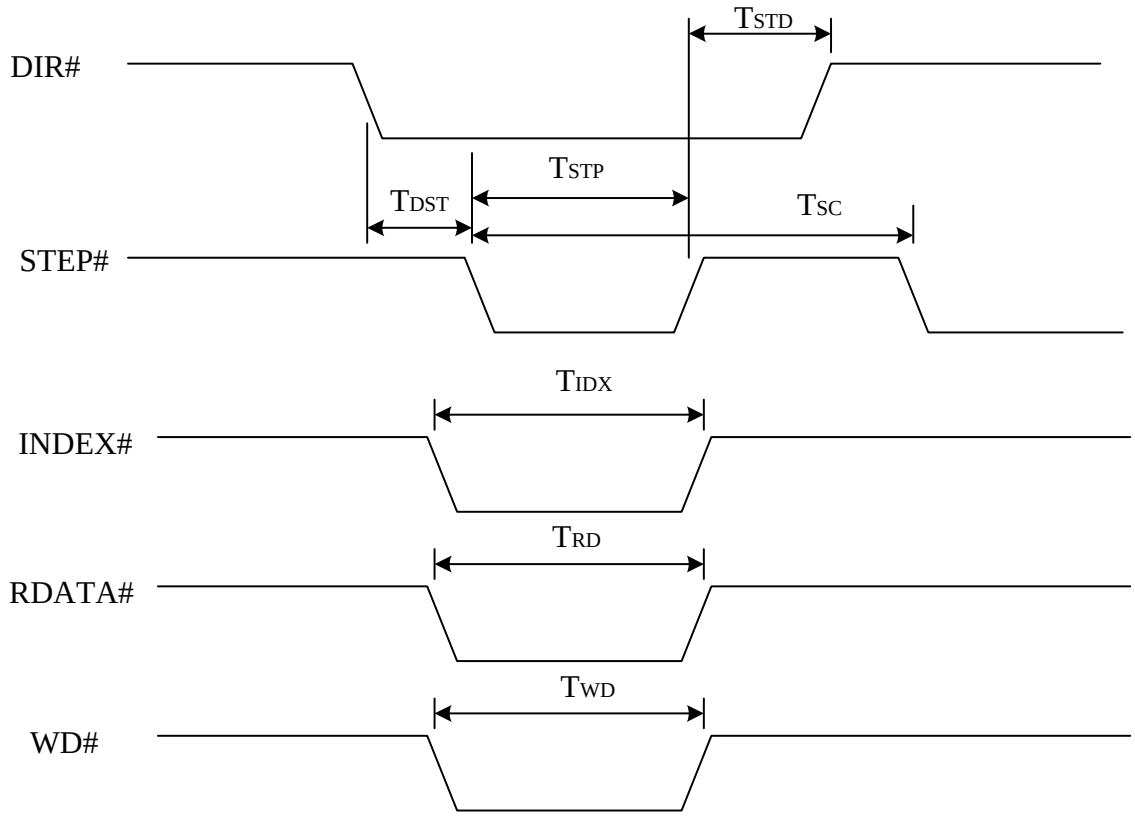
1. Typical values for T = 25°C and normal supply voltage.
2. Programmable from 0.5 mS through 32 mS as described in step rate table. (Please refer to the description of the SPECIFY command set.)

Step Rate Table

DATA RATE / SRT	1MB/S	500KB/S	300KB/S	250KB/S

0	8	16	26.7	32
1	7.5	15	25	30
…	…	…	…	…
E	1.0	2	3.33	4
F	0.5	1	1.67	2

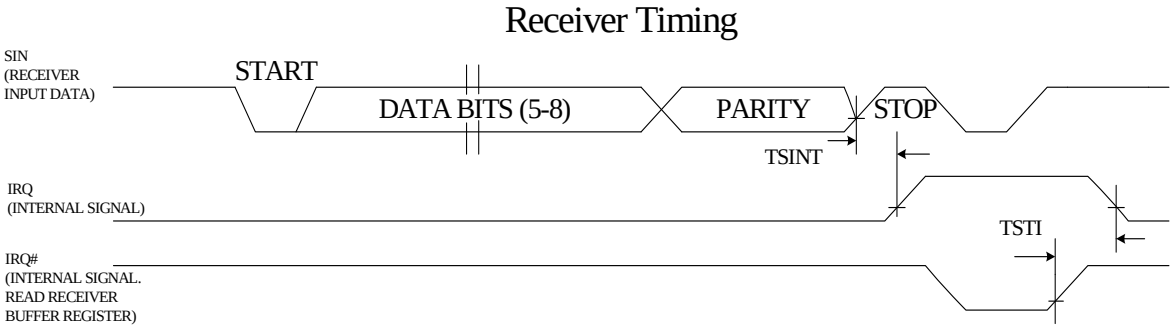
Floppy Disk Driving Timing



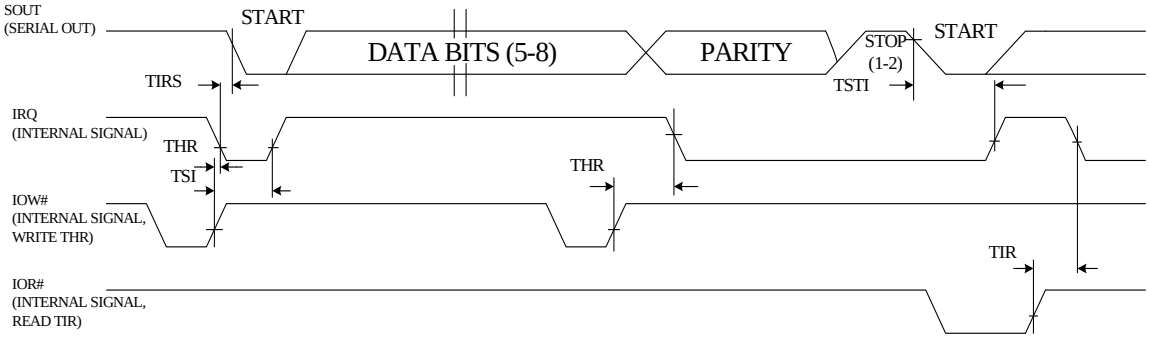
26.7 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

UART Receiver Timing

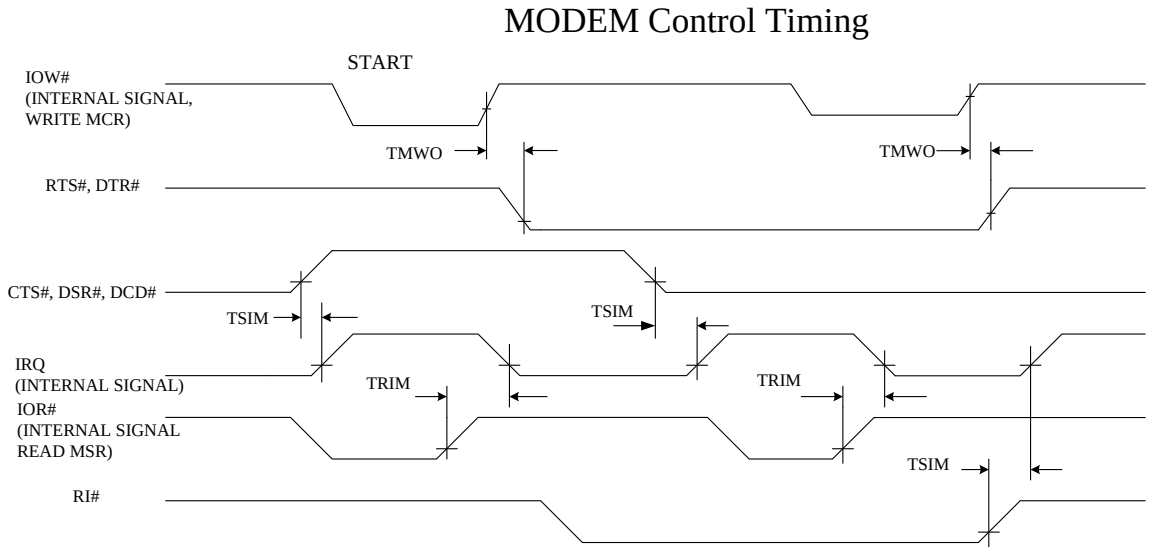


UART Transmitter Timing



26.8 Modem Control Timing

Modem Control Timing



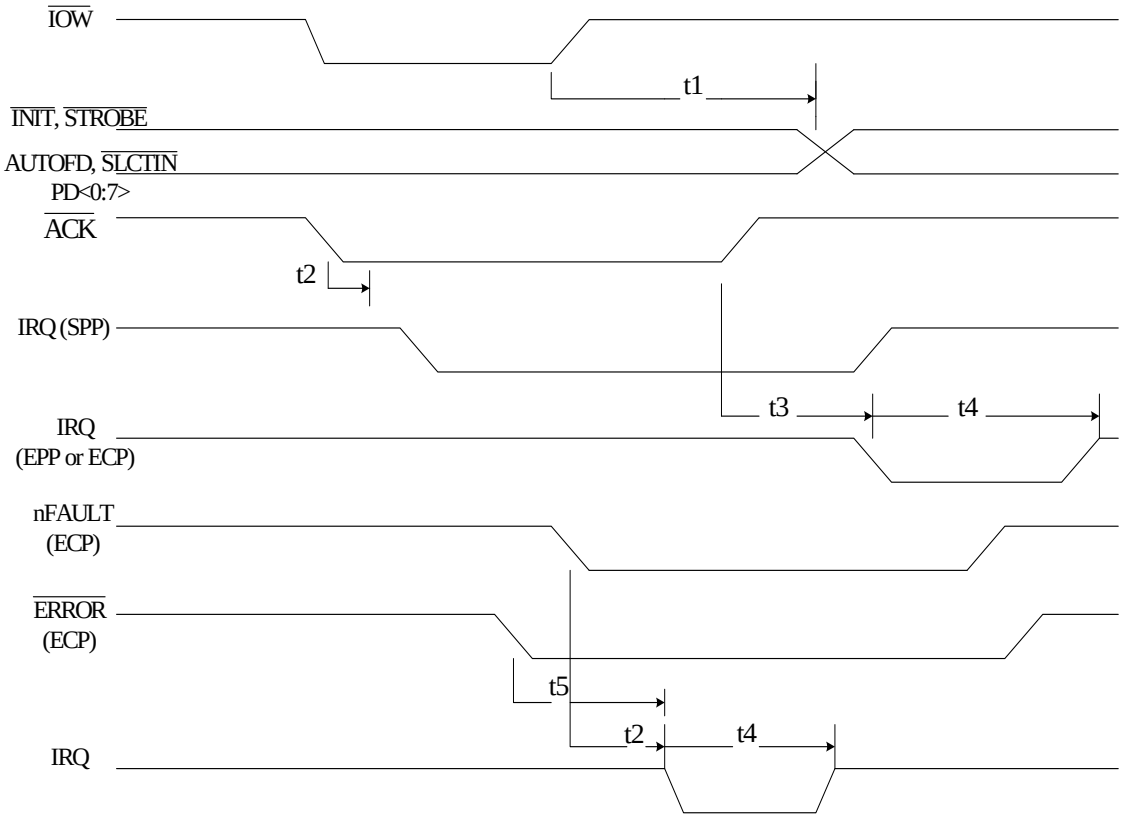
26.9 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS

$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

26.9.1 Parallel Port Timing

Parallel Port Timing



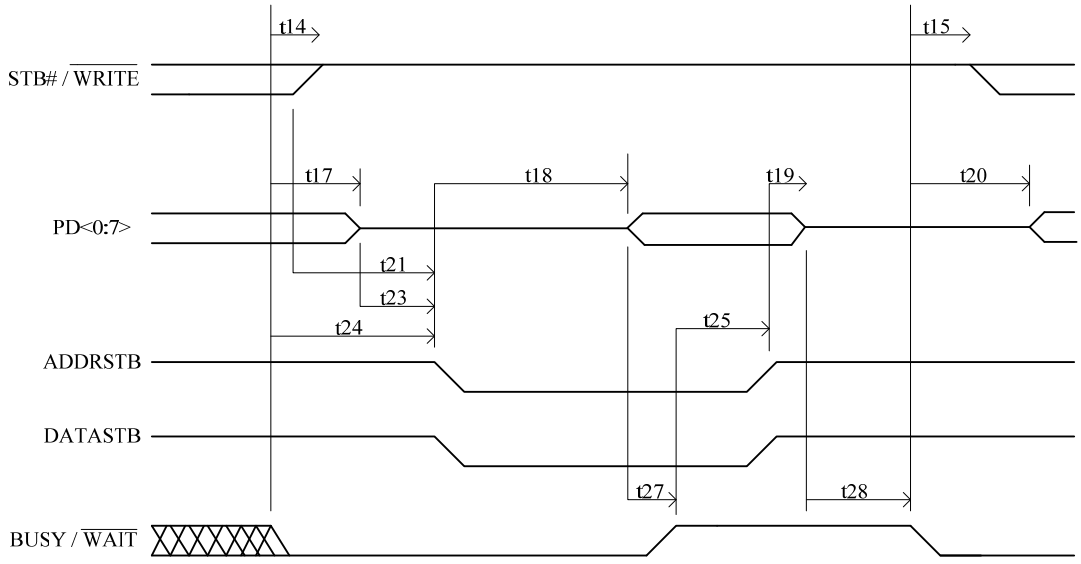
26.9.2 EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		μS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	μS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

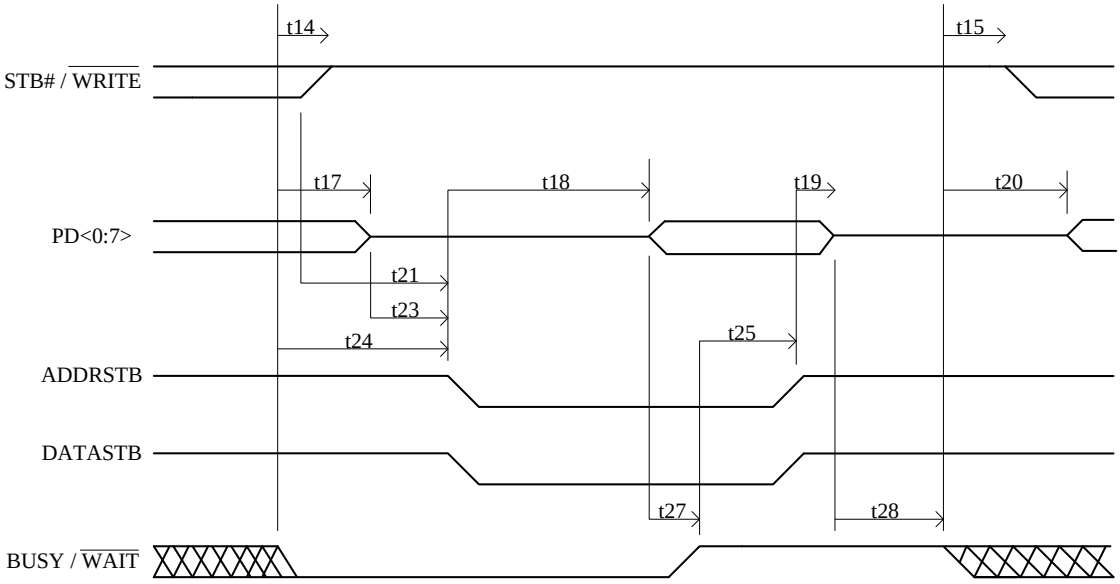
26.9.3 EPP Data or Address Read Cycle (EPP Version 1.9)

EPP Data or Address Read Cycle (EPP Version 1.9)



26.9.4 EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)



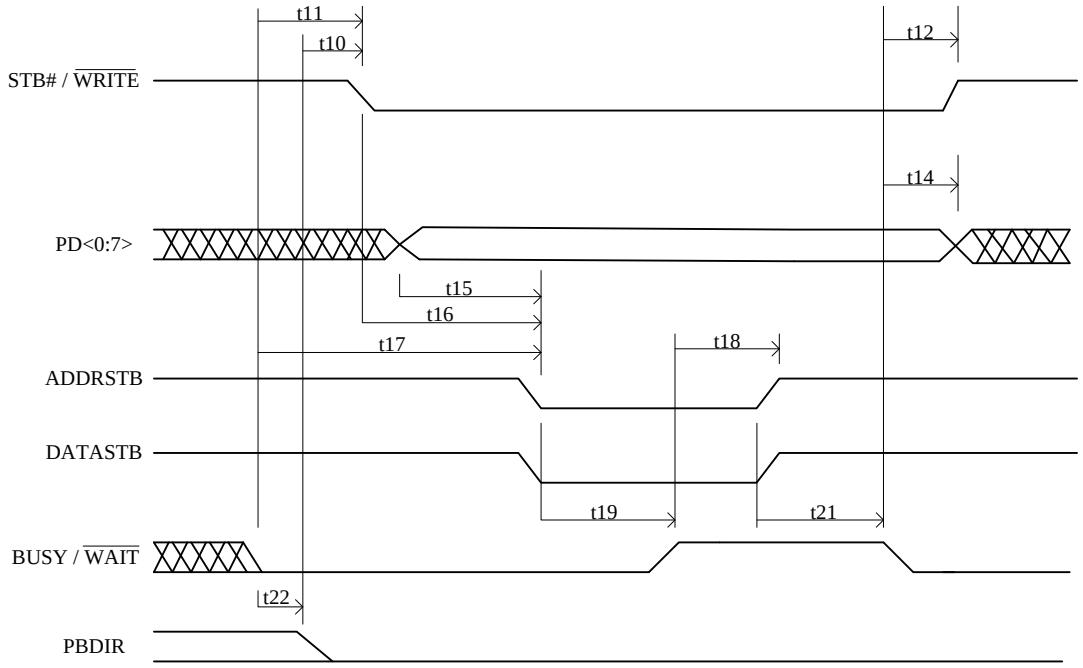
26.9.5 EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid	t22	0		nS
$\overline{\text{WRITE}}$ to Command Asserted	t16	5	35	nS

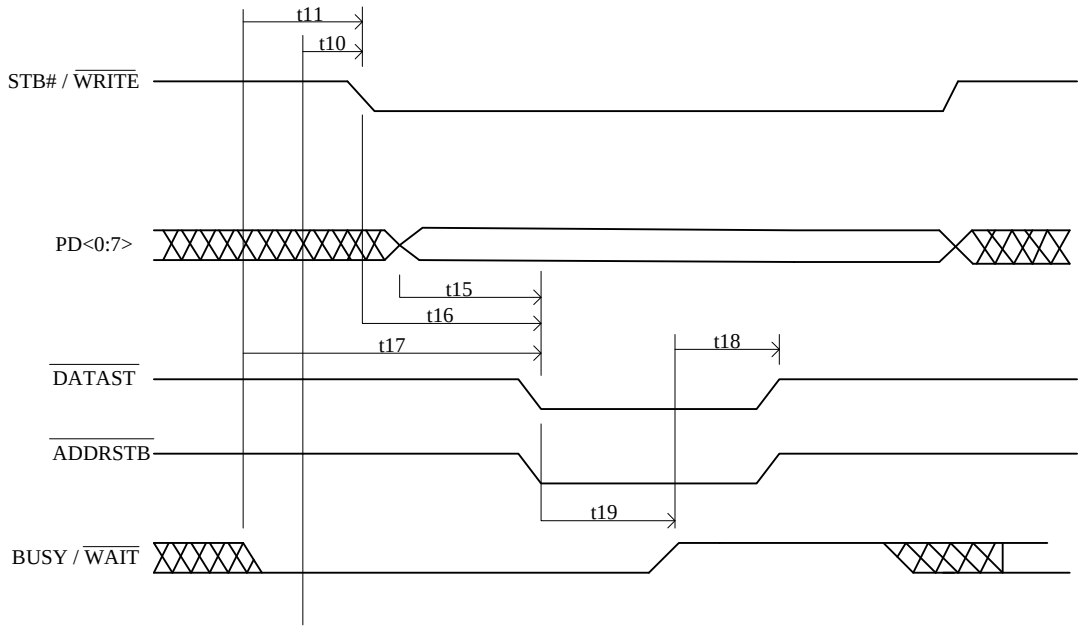
26.9.6 EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)



26.9.7 EPP Data or Address Write Cycle (EPP Version 1.7)

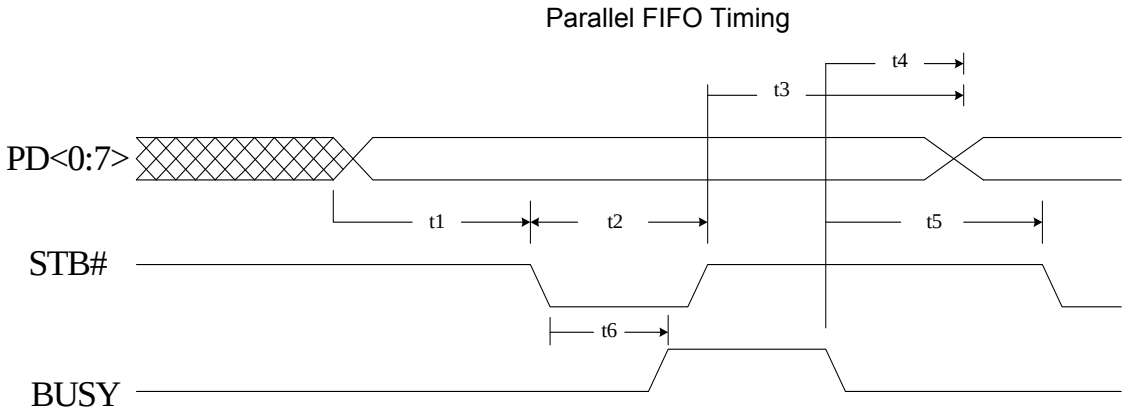
EPP Data or Address Write Cycle (EPP Version 1.7)



26.9.8 Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

26.9.9 Parallel FIFO Timing

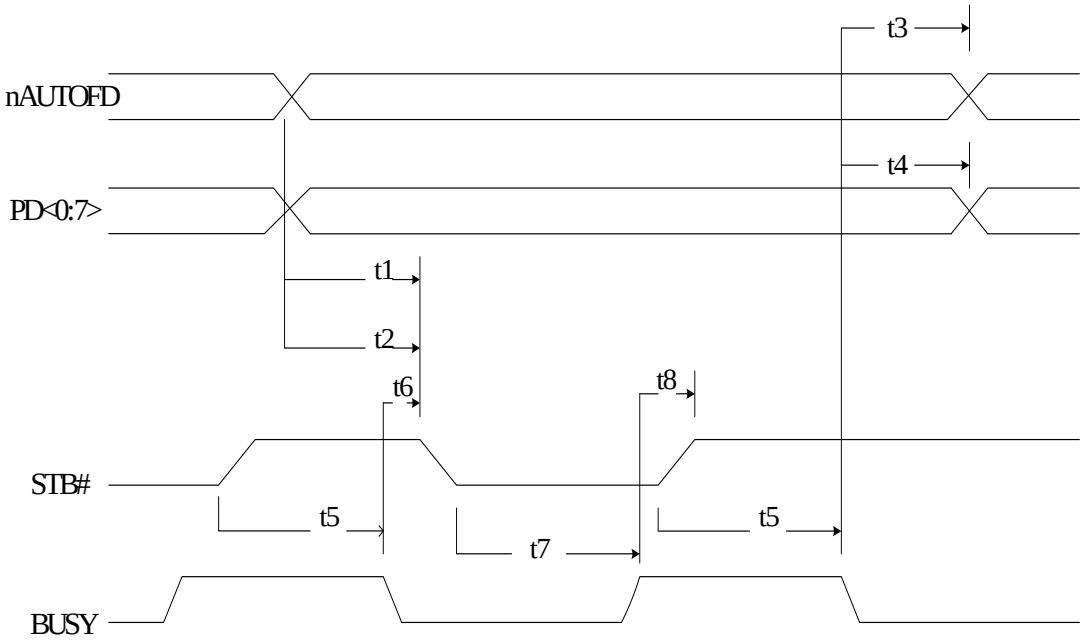


26.9.10ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

26.9.11ECP Parallel Port Forward Timing

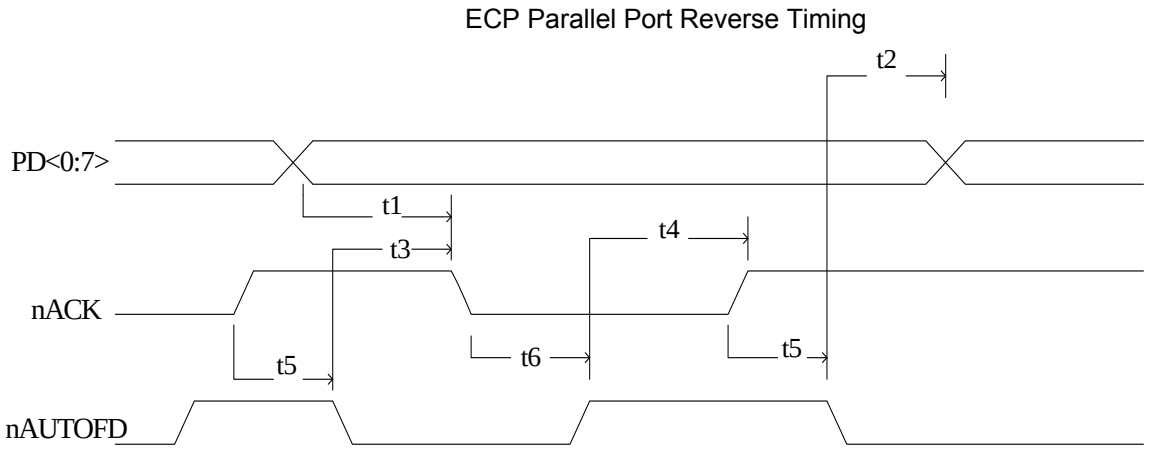
ECP Parallel Port Forward Timing



26.9.12ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

26.9.13ECP Parallel Port Reverse Timing

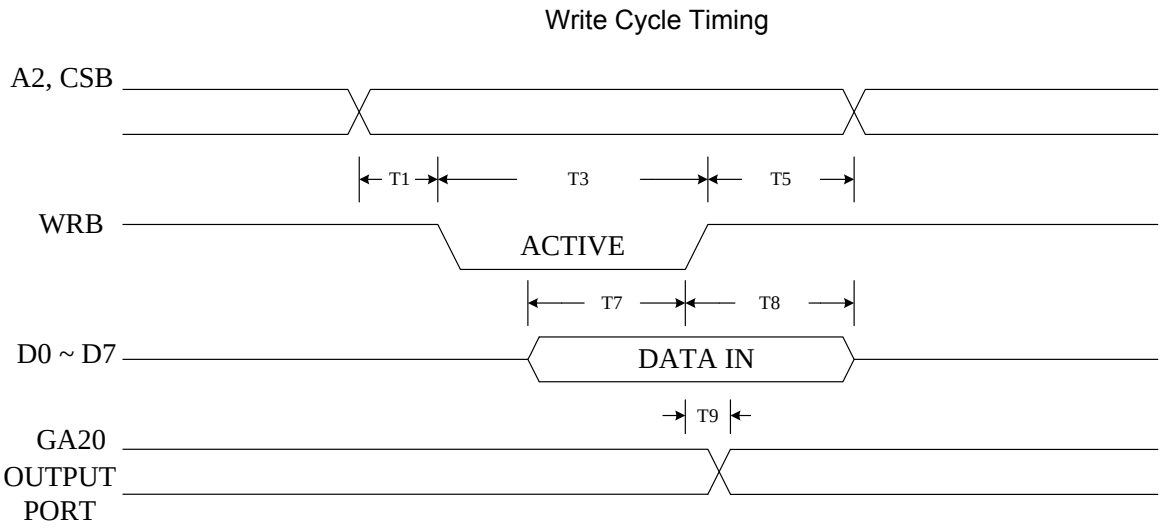


26.9.14KBC Timing Parameters

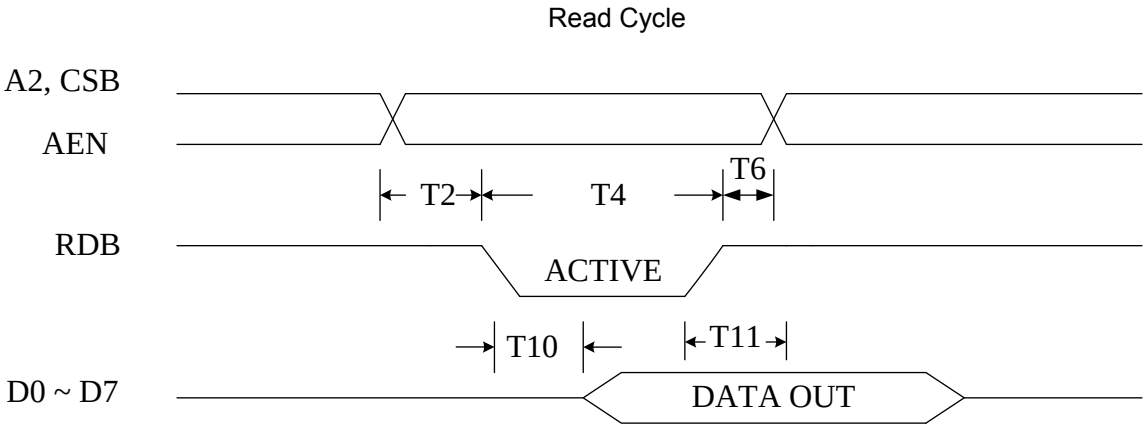
NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–16 Mhz)	63	167	nS

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

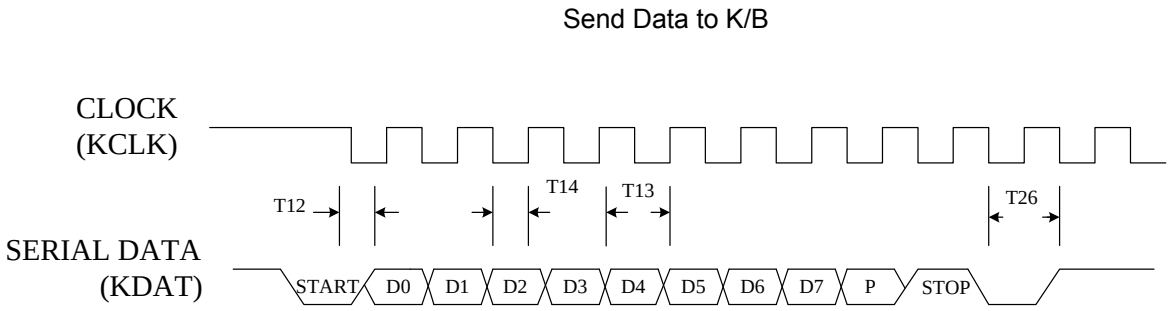
26.9.15Writing Cycle Timing



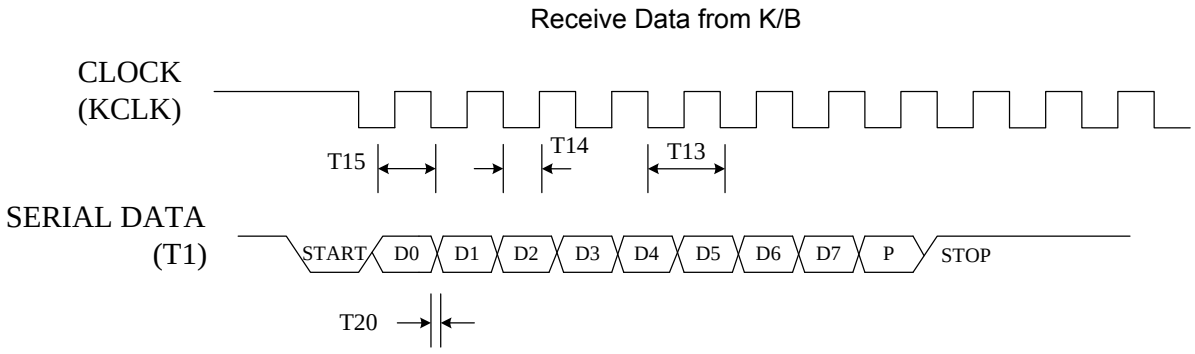
26.9.16Read Cycle Timing



26.9.17Send Data to K/B

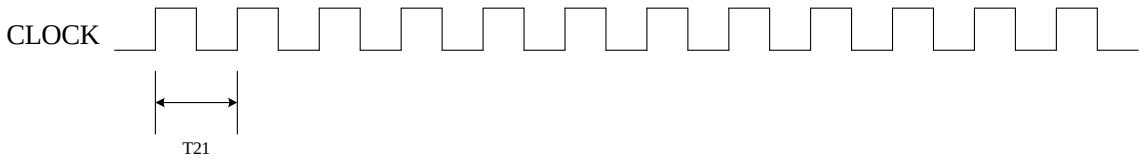


26.9.18Receive Data from K/B



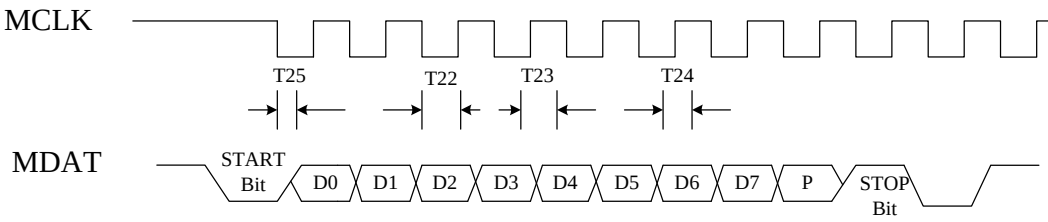
26.9.19 Input Clock

Input Clock



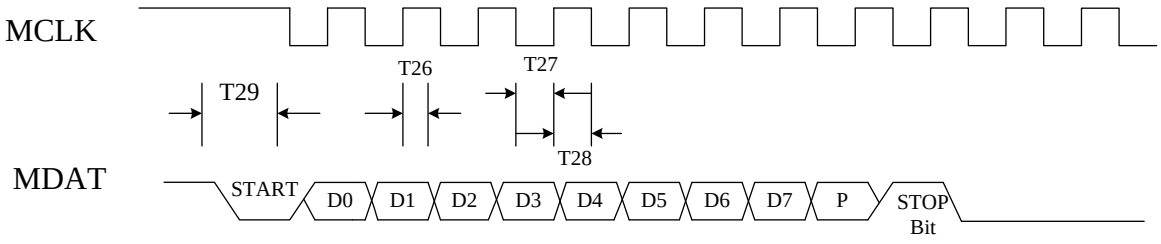
26.9.20 Send Data to Mouse

Send Data to Mouse



26.9.21 Receive Data from Mouse

Receive Data from Mouse



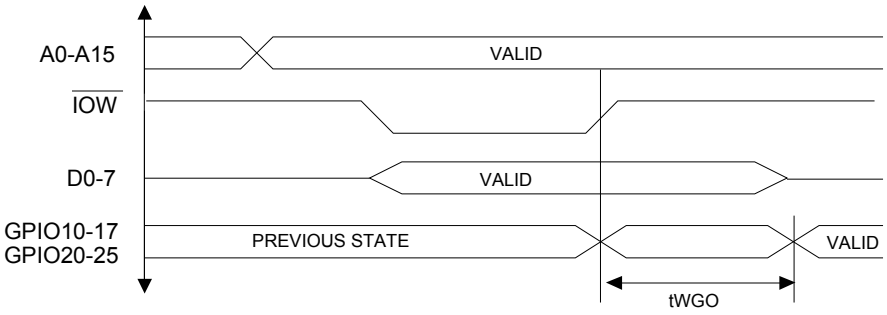
26.10 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns
t_{SWP}	SWITCH pulse width	16		msec

Note: Refer to Microprocessor Interface Timing for Read Timing.

26.10.1 GPIO Write Timing

GPIO Write Timing diagram



27. TOP MARKING SPECIFICATIONS

1st line: Nuvoton logo
2nd line: part number NCT6776F
3rd line: tracking code 123G9A2111B123FA
123: packages made in '2011, week 23
G: assembly house ID; G means GR, A means ASE, etc
9: code version; 9 means code 009
A: IC revision; A means version A; B means version B, and C means version C
2111B123: wafer production series lot number
FA: Nuvoton internal use

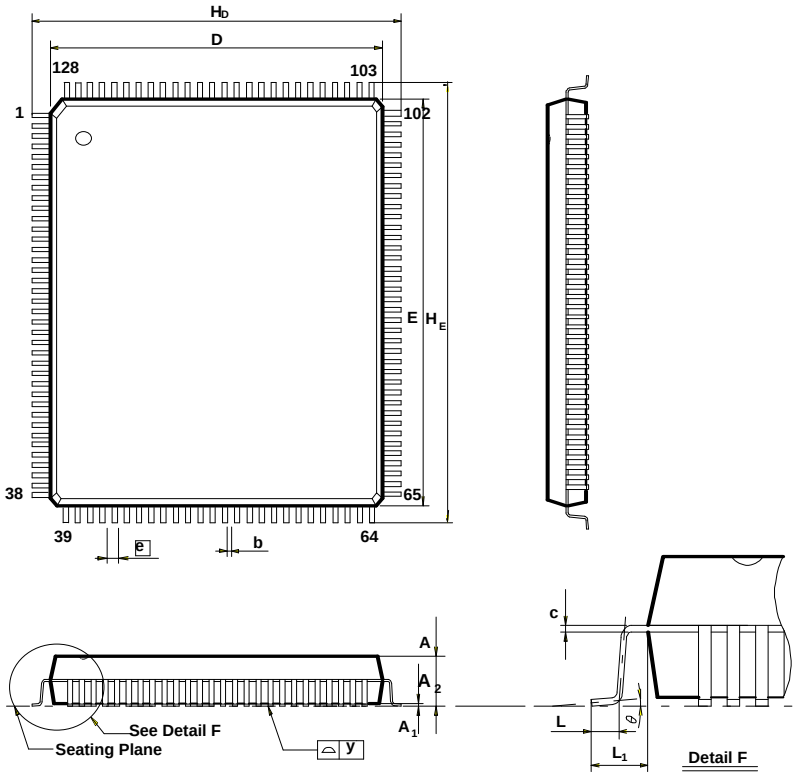
1st line: Nuvoton logo
2nd line: part number NCT6776D
3rd line: wafer production series lot number 2111B123
4th line: tracking code 123G9AFA
123: packages made in 2011, week 23
G: assembly house ID; G means GR, A means ASE, etc.
9: code version; 9 means code 009
A: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use

28. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT6776F	128Pin QFP (Green package)	Commercial, 0°C to +70°C
NCT6776D	128Pin LQFP (Green package)	Commercial, 0°C to +70°C

29. PACKAGE SPECIFICATION

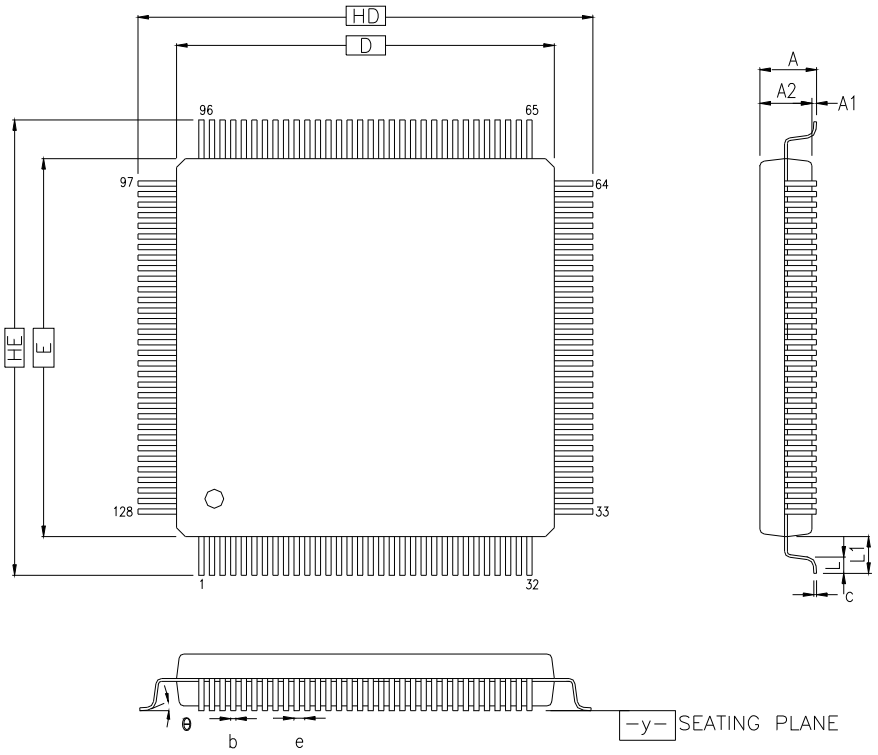
NCT6776F



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.134	—	—	3.40
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e		0.020			0.50	
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.023	0.031	0.039	0.60	0.80	1.00
L_1	0.055	0.063	0.071	1.40	1.60	1.80
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

NCT6776F, 128-pin QFP (14x20x2.75mm foot print 3.2mm)

NCT6776D



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

NCT6776D, 128-pin LQFP (14mm x 14mm x 1.4mm)

30. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	03/16/2010	N.A.	Draft datasheet to define features and pin configuration
0.6	05/26/2010	N.A.	Preliminary datasheet
0.7	07/23/2010	P.305, P.265, P.388, P.264, P.271, P.382, P.33, P.34, P.364, P.39, P.41, P.94, P.92, P.96, P.179, P.180, P.180	1. Update Chip ID at global control register CR 21h. from 31h to 32h 2. Add GPIO group programming table 3. Modify Logical Device F, CRE0~CRE9 default value 4. Modify watchdog1 & watchdog2 description 5. Add watchdog access channel description 6. Modify of SVID0 offset register bit description 7. Modify BKFD_CUT and LATCH_BKFD_CUT waveform 8. Add 3VSBSW# waveform 9. Modify Logical Device A, CRE4 bit6:5 description 10. Modify S0-S5 LED Blink Block Diagram 11. Modify Deeper Sleeping state detection Block Diagram 12. Modify Hardware Monitor, Bank0 Index46h bit1 description 13. Modify Hardware Monitor, Bank0 Index42h description 14. Modify Hardware Monitor, Bank0 Index4Eh description 15. Modify Logical Device B, Bank7 Index01h description 16. Modify Logical Device B, Bank7 Index03h description 17. Modify Logical Device B, Bank7 Index04h description
0.8	09/23/2010	N.A.	Update the contents

1.0	03/01/2011	1. P7 2. P36 3. P82 4. P92 5. P94 6. P100 7. P102 8. P103~105 9. P108 10. P115 11. P120 12. P127 13. P132 14. P139 15. P180 16. P188 17. P222 18. P257 19. P266 20. P301~385 21. P304 22. P320 23. P332 24. P365 25. P367 26. P369 27. P373~376 28. P381 29. P389 30. P392	1. Pin103 rename to VIN2. Pin73 rename to BKFD_CUT 2. Update PWROK block diagram. 3. Update Table 8-8 OVT# function. 4. Update Bank0, Index40h, bit4~6. 5. Update Bank0, Index43h and 44h. 6. Reserved Bank0, Index 65h and 66h, 7. Add Bank0, Index AEh, PECI temperature reading enable register. 8. Add Beep control registers (Bank0, Index B2h~B5h). 9. Rename Bank1, Index 07h register. 10. Reserved Bank1, Index 3Fh, 41h, 45h and 46h. 11. Rename Bank2, Index 07h register. 12. Reserved Bank2, Index 3Fh, 41h, 45h and 46h. 13. Rename Bank3, Index 07h register. 14. Reserved Bank2, Index 3Fh, 41h, 45h and 46h. 15. Add Bank7, Index 01~04h default value table. 16. Rename Bank7, Index 20h and 21h register. 17. Update baud rate table 18. Update PME# support item description. 19. Update GPIO wake-up table 20. Update Global registers' reset source 21. Revise Global register CR1Ah,bit6 22. Revise Global register CR2Ah,bit2 23. Revise Logic Device 2, CRF0h,bit1~0 24. Revise Logic Device A, CRE6h,bit0 25. Reserve Logic Device A, CRF2h,bit5 26. Reserve Logic Device A, CRF6h,bit0 27. Update Front Panel LED blinking frequency 28. Revise Logic Device D, CRF0h 29. Reserve Logic Device 16, CR30h,bit2 30. Revise Logic Device 17, CRE5h
1.1	03/24/2011	257	1. Update PME# support item description.
1.2	07/12/2011	N.A.	Add part number NCT6776D

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