



MIC861

Teeny™ Ultra Low Power Op Amp

General Description

The MIC861 is a rail-to-rail output, input common-mode to ground, operational amplifier in *Teeny™* SC70 packaging. The MIC861 provides 400kHz gain-bandwidth product while consuming an incredibly low 4.6μA supply current.

The SC70 packaging achieves significant board space savings over devices packaged in SOT-23 or MSOP-8 packaging. The SC70 occupies approximately half the board area of a SOT-23 package.

Features

- *Teeny™* SC70 packaging
- 400kHz gain-bandwidth product
- 650kHz, –3dB bandwidth
- 4.6μA supply current
- Rail-to-Rail output
- Ground sensing at input (common mode to GND)
- Drives large capacitive loads (1000pF)
- Unity gain stable

Applications

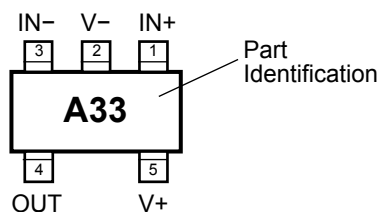
- Portable equipment
- PDAs
- Pagers
- Cordless Phones
- Consumer Electronics

Ordering Information

Part Number				Ambient Temp. Range	Package
Standard	Marking	Pb-Free	Marking*		
MIC861BC5	A33	MIC861YC5	<u>A</u> 33	–40°C to +85°C	SC-70-5

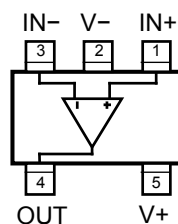
* Underbar marking may not be to scale.

Pin Configuration



SC-70

Functional Pinout



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Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{V+} - V_{-}$).....	+6.0V
Differential Input Voltage ($ V_{IN+} - V_{IN-} $), Note 4	+6.0V
Input Voltage ($V_{IN+} - V_{IN-}$)	$V_{+} + 0.3V$, $V_{-} - 0.3V$
Lead Temperature (soldering, 5 sec.).....	260°C
Output Short Circuit Current Duration	Indefinite
Storage Temperature (T_S)	150°C
ESD Rating, Note 3	

Operating Ratings (Note 2)

Supply Voltage ($V_{+} - V_{-}$)	+2.43V to +5.25V
Ambient Temperature Range.....	-40°C to +85°C
Package Thermal Resistance.....	450°C/W

Electrical Characteristics

$V_{+} = +2.7V$, $V_{-} = 0V$, $V_{CM} = V_{+}/2$; $R_L = 500k\Omega$ to $V_{+}/2$; $T_A = 25^{\circ}C$, unless otherwise noted. **Bold** values indicate $-40^{\circ}C \leq T_A \leq +85^{\circ}C$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	Note 5	-10	2	10	mV
	Input Offset Voltage Temp Coefficient			15		$\mu V/^{\circ}C$
I_B	Input Bias Current			20		pA
I_{OS}	Input Offset Current			10		pA
V_{CM}	Input Voltage Range	CMRR > 60dB		1.8		V
CMRR	Common-Mode Rejection Ratio	$0 < V_{CM} < 1.35V$	45	77		dB
PSRR	Power Supply Rejection Ratio	Supply voltage change of 3V	50	83		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 100k$, V_{OUT} 2V peak to peak	60	74		dB
		$R_L = 500k$, V_{OUT} 2V peak to peak	73	83		dB
V_{OUT}	Maximum Output Voltage Swing	$R_L = 500k$	V+2mV	$V_{+}-0.7mV$		V
V_{OUT}	Minimum Output Voltage Swing	$R_L = 500k$		$V_{-}+0.2mV$	V-2mV	V
GBW	Gain-Bandwidth Product	$R_L = 200k\Omega$, $C_L = 2pF$, $V_{OUT} = 0$		350		kHz
BW	-3dB Bandwidth	$A_V = 1$, $C_L = 2pF$, $R_L = 1M\Omega$		500		kHz
SR	Slew Rate	$A_V = 1$, $C_L = 2pF$, $R_L = 1M\Omega$		0.12		V/ μs
I_{SC}	Short-Circuit Output Current	Source		6		mA
		Sink		5		mA
I_S	Supply Current	No Load		4.2	9	μA

$V_{+} = +5V$, $V_{-} = 0V$, $V_{CM} = V_{+}/2$; $R_L = 500k\Omega$ to $V_{+}/2$; $T_A = 25^{\circ}C$, unless otherwise noted. **Bold** values indicate $-40^{\circ}C \leq T_A \leq +85^{\circ}C$.

V_{OS}	Input Offset Voltage	Note 5	-10	2	10	mV
	Input Offset Voltage Temp Coefficient			15		$\mu V/^{\circ}C$
I_B	Input Bias Current			20		pA
I_{OS}	Input Offset Current			10		pA
V_{CM}	Input Voltage Range	CMRR > 60dB		4.2		V
CMRR	Common-Mode Rejection Ratio	$0 < V_{CM} < 3.5V$	60	80		dB
PSRR	Power Supply Rejection Ratio	Supply voltage change of 1V	45	85		dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 100k$, V_{OUT} 4.0V peak to peak	60	76		dB
		$R_L = 500k$, V_{OUT} 4.0V peak to peak	68	83		dB
V_{OUT}	Maximum Output Voltage Swing	$R_L = 500k$	V+2mV	$V_{+}-0.7mV$		V
V_{OUT}	Minimum Output Voltage Swing	$R_L = 500k$		$V_{-}+0.7mV$	V-2mV	V
GBW	Gain-Bandwidth Product	$R_L = 200k\Omega$, $C_L = 2pF$, $V_{OUT} = 0$		400		kHz
BW	-3dB Bandwidth	$A_V = 1$, $C_L = 2pF$, $R_L = 1M\Omega$		650		kHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
SR	Slew Rate	$A_V = 1$, $C_L = 2\text{pF}$, $R_L = 1\text{M}\Omega$		0.12		V/ μs
I_{SC}	Short-Circuit Output Current	Source	10	24		mA
		Sink	10	24		mA
I_S	Supply Current	No Load		4.6	9	μA

Note 1. Exceeding the absolute maximum rating may damage the device.

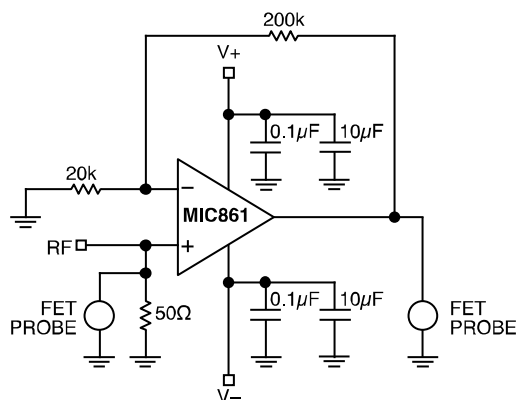
Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF. Pin 4 is ESD sensitive

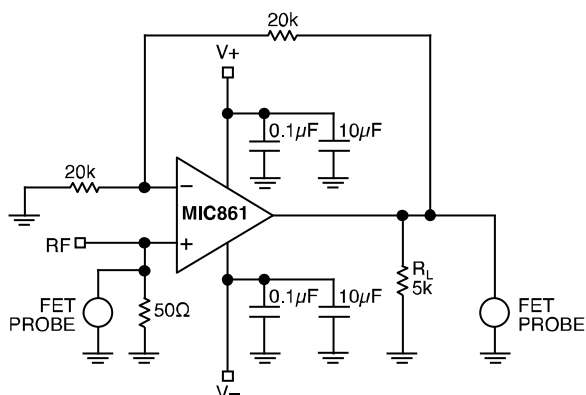
Note 4. Exceeding the maximum differential input voltage will damage the input stage and degrade performance (in particular, input bias current is likely to increase).

Note 5. The offset voltage distribution is centered around 0V. The typical offset number shown, is equal to the standard deviation of the voltage offset distribution.

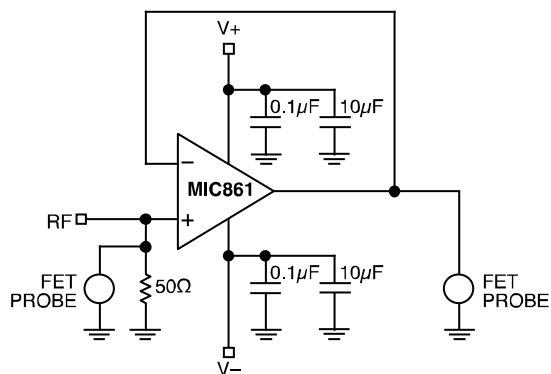
Test Circuits



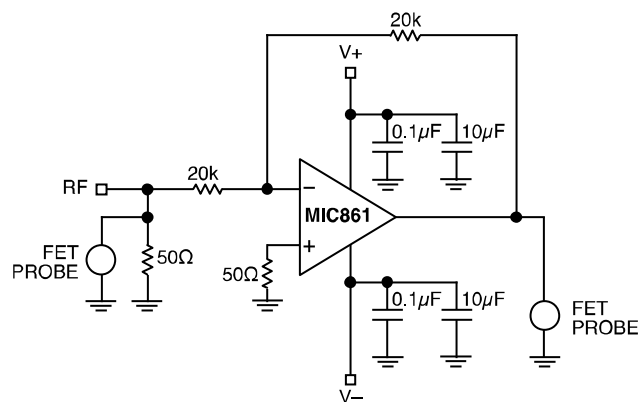
Test Circuit 1. $A_V = 11$



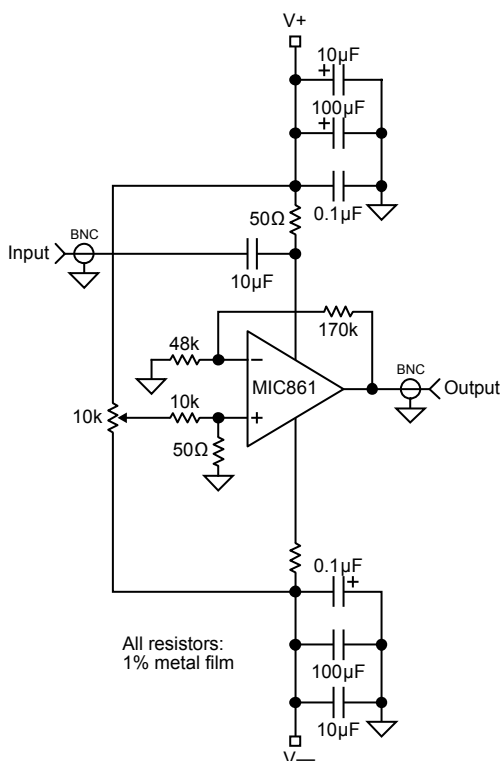
Test Circuit 2: $A_V = 2$



Test Circuit 3. $A_V = 1$

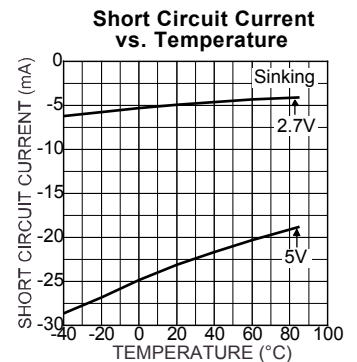
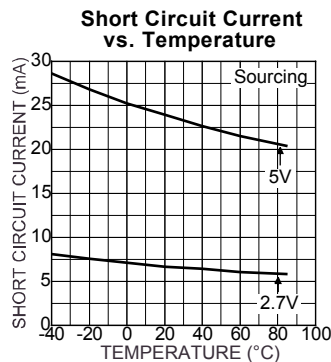
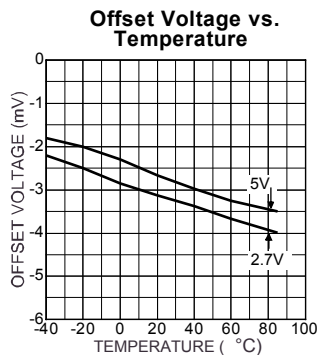
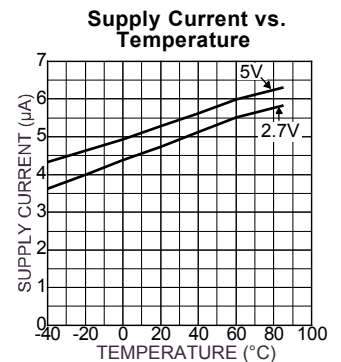
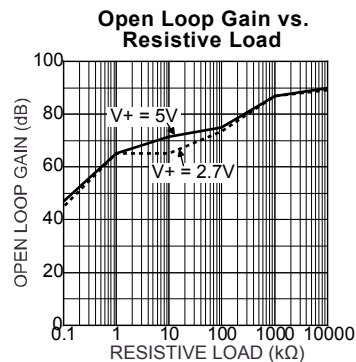
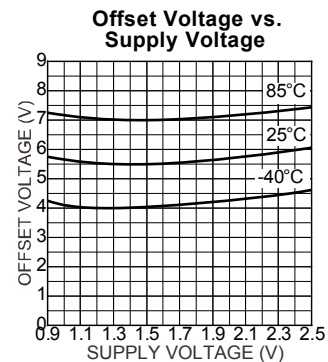
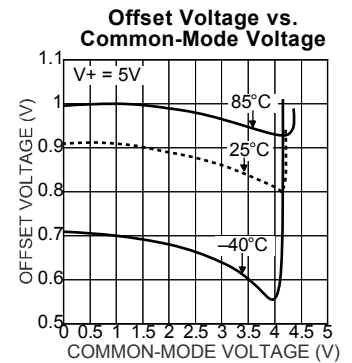
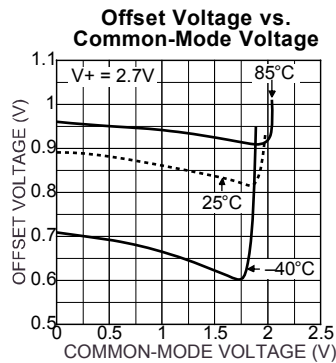
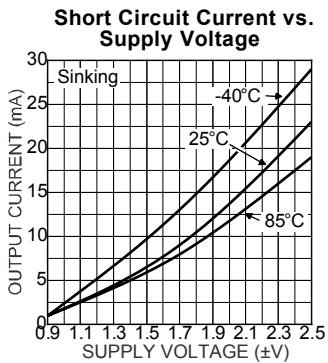
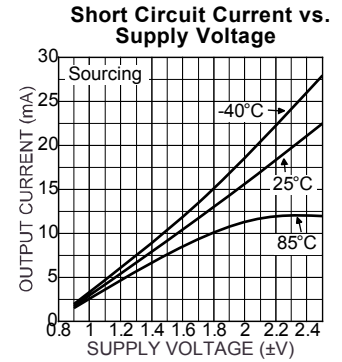
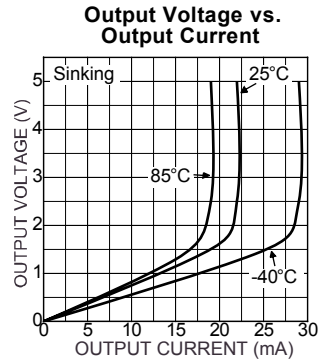
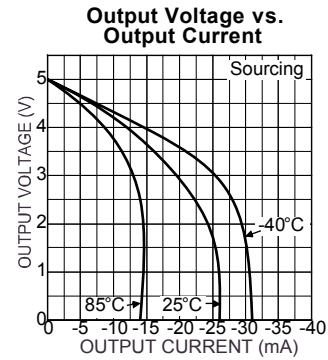


Test Circuit 4. $A_V = -1$

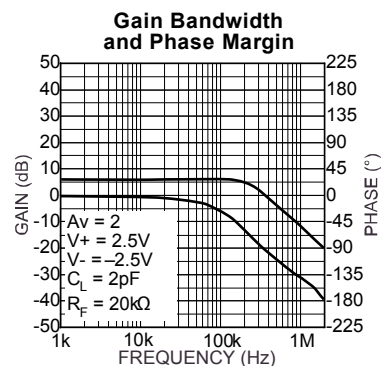
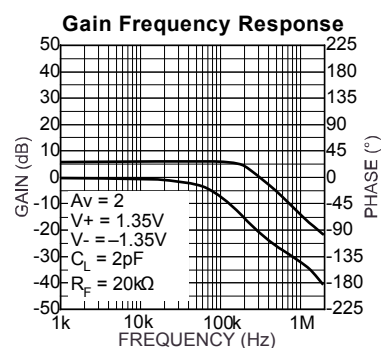
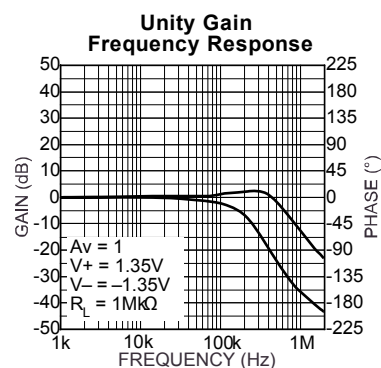
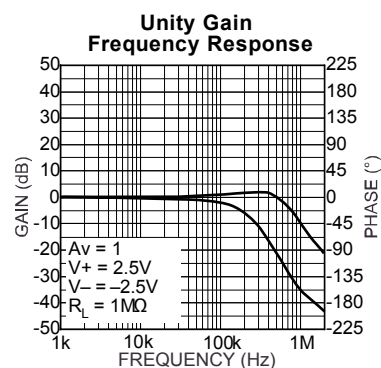
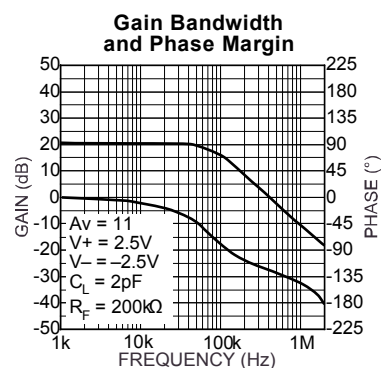
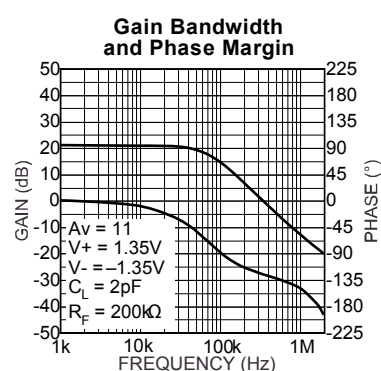
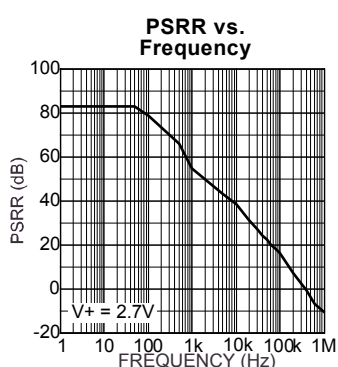
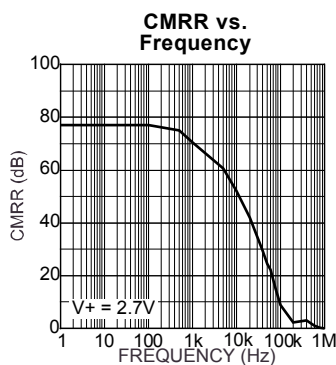
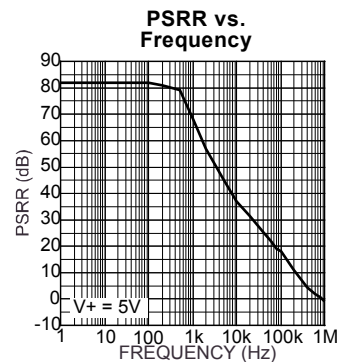
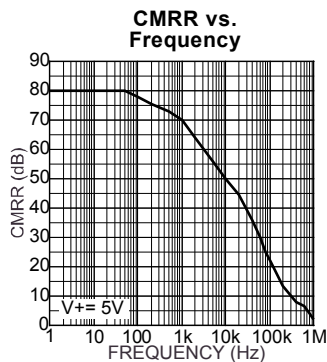
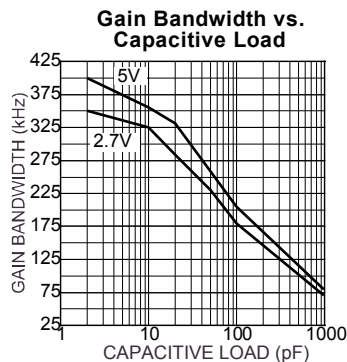


Test Circuit 5. Positive Power Supply Rejection Ratio Measurement

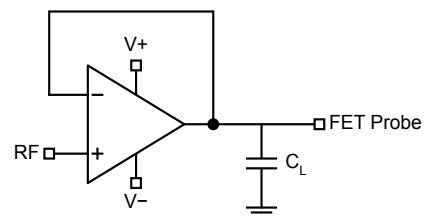
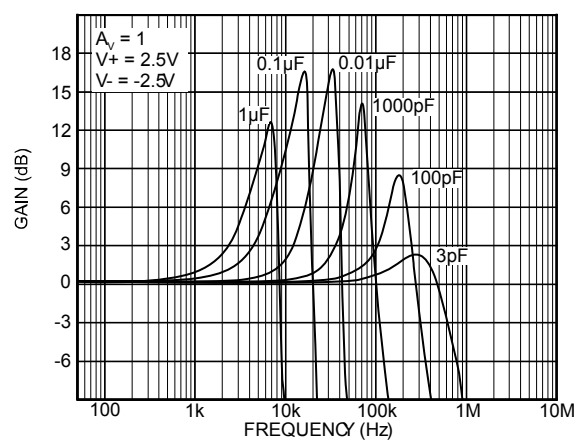
DC Performance Characteristics



AC Performance Characteristics

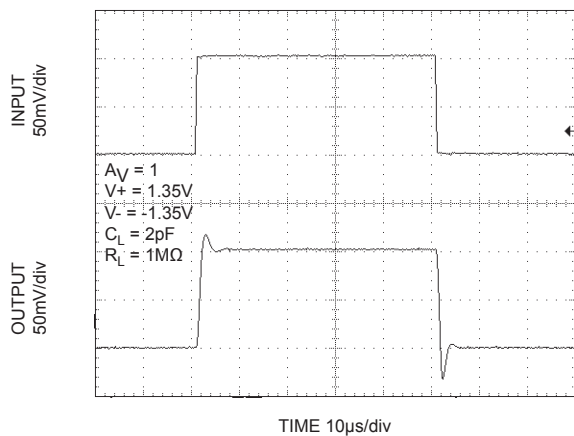


Close-loop Unity Gain Frequency Response

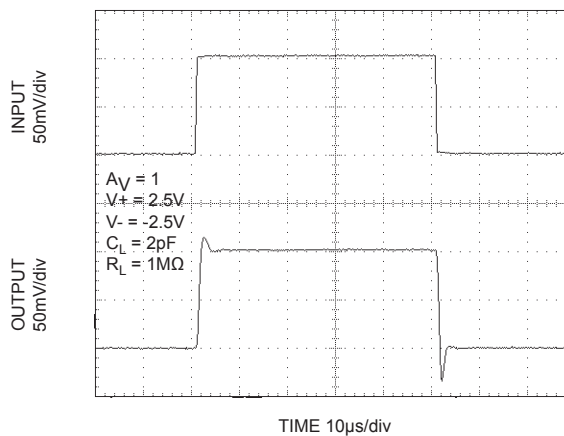


Functional Characteristics

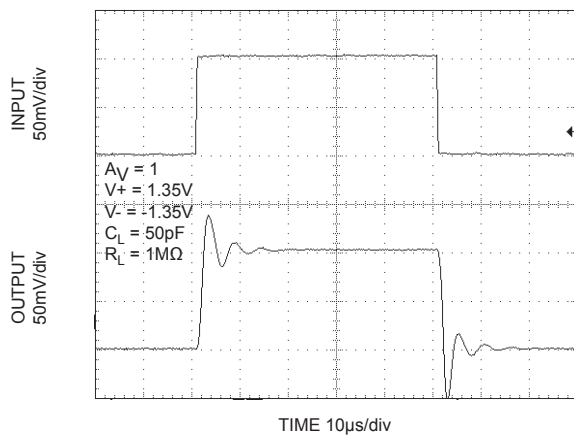
Small Signal Pulse Response
Test Circuit 3: $A_V = 1$



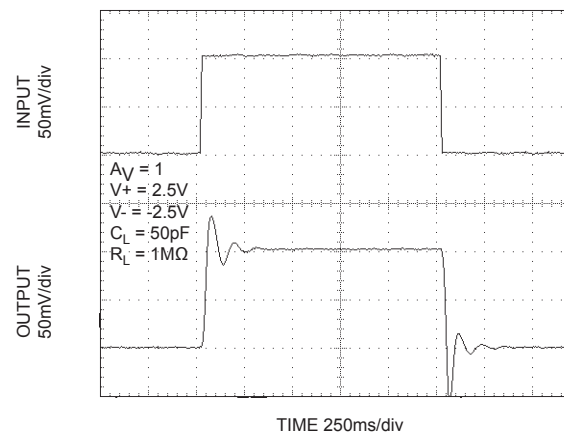
Small Signal Pulse Response
Test Circuit 3: $A_V = 1$



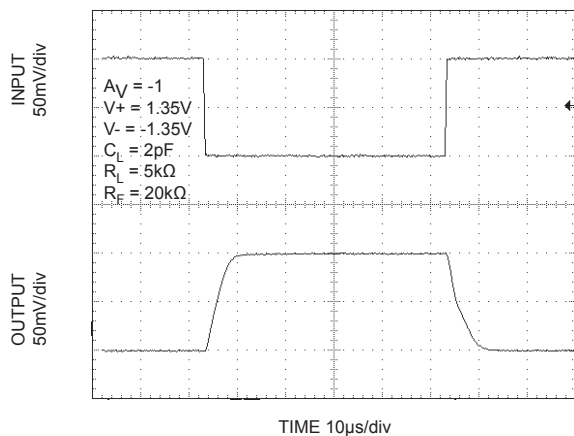
Small Signal Pulse Response
Test Circuit 3: $A_V = 1$



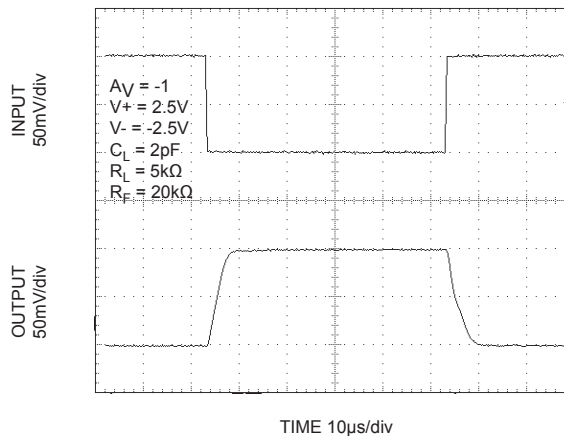
Small Signal Pulse Response
Test Circuit 3: $A_V = 1$



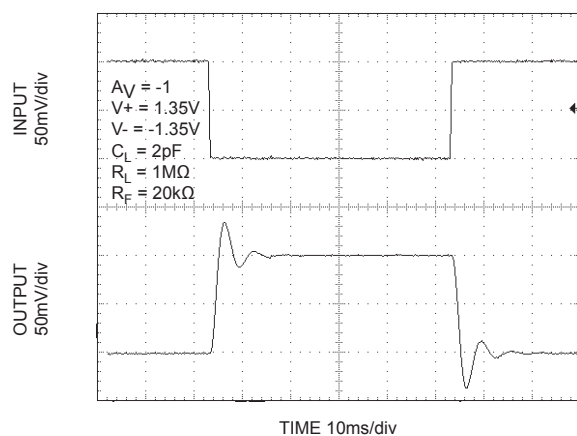
Small Signal Pulse Response
Test Circuit 4: $A_V = -1$



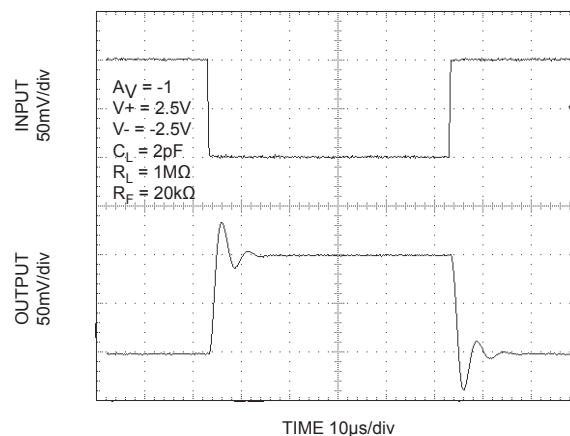
Small Signal Pulse Response
Test Circuit 4: $A_V = -1$



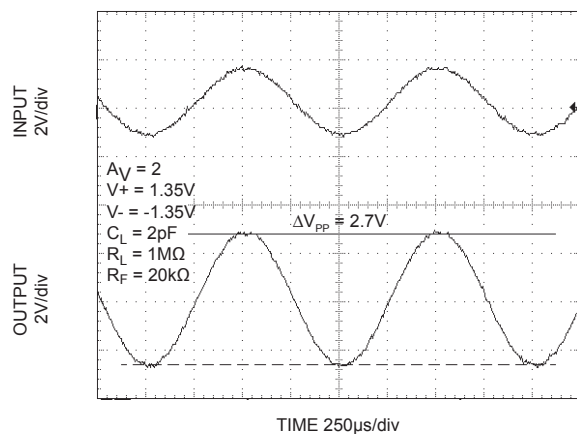
Small Signal Pulse Response
Test Circuit 4: $A_V = -1$



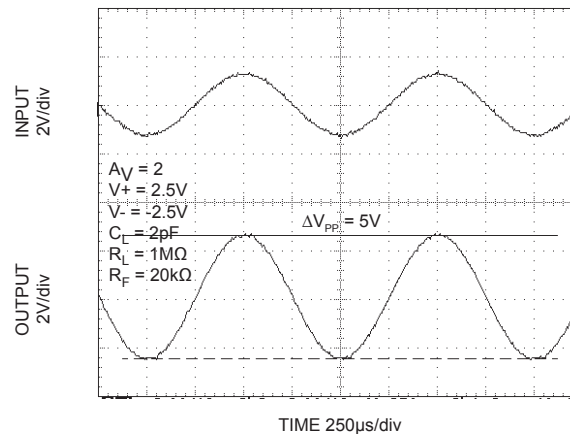
Small Signal Pulse Response
Test Circuit 4: $A_V = -1$



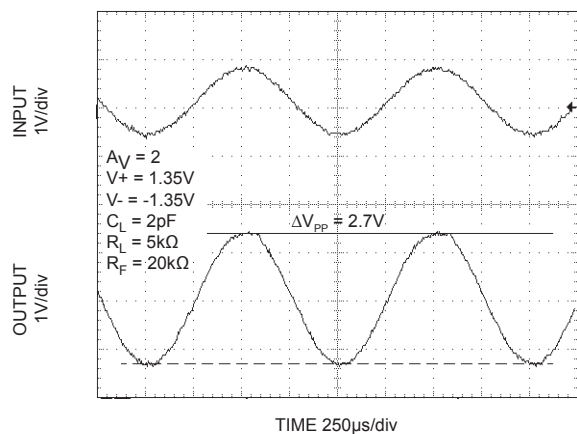
Rail to Rail Output Operation



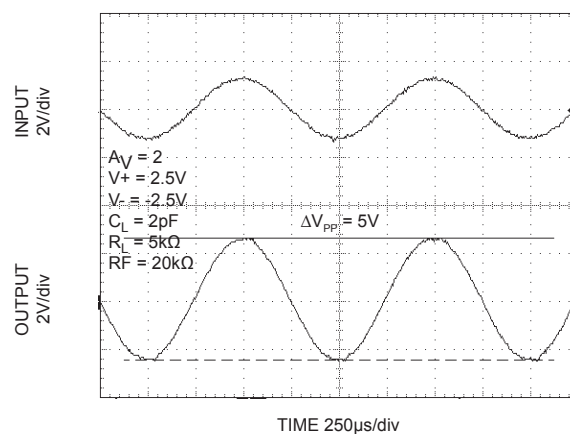
Rail to Rail Output Operation



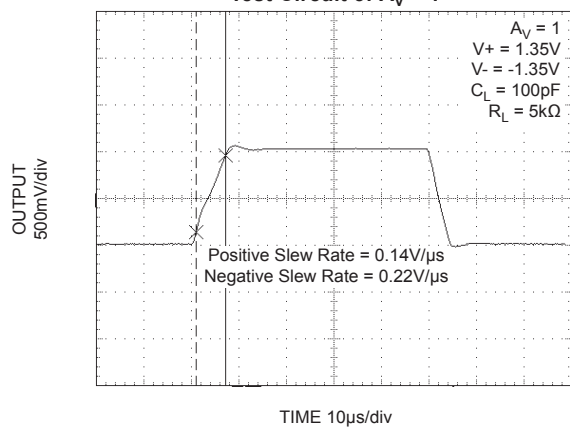
Rail to Rail Output Operation



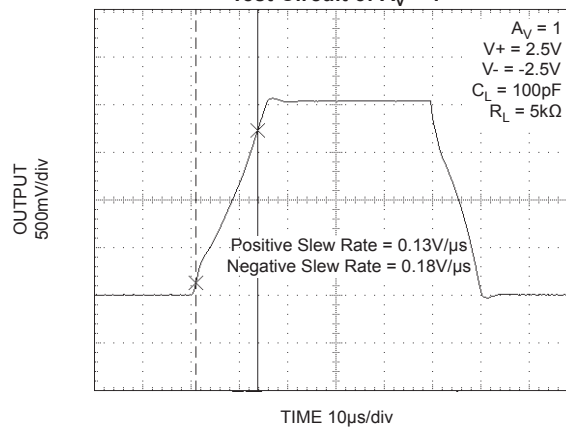
Rail to Rail Output Operation



Large Signal Pulse Response
Test Circuit 3: $A_V = 1$



Large Signal Pulse Response
Test Circuit 3: $A_V = 1$

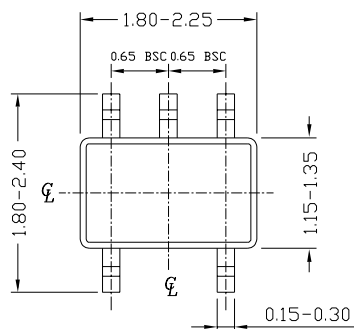


Applications Information

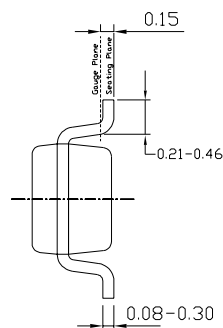
Power Supply Bypassing

Regular supply bypassing techniques are recommended. A 10 μ F capacitor in parallel with a 0.1 μ F capacitor on both the positive and negative supplies are ideal. For best performance all bypassing capacitors should be located as close to the op amp as possible and all capacitors should be low ESL (equivalent series inductance), ESR (equivalent series resistance). Surface-mount ceramic capacitors are ideal.

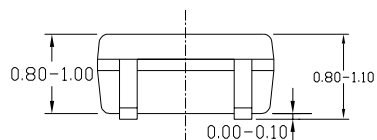
Package Information



TOP VIEW



END VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.

SC70-5

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