

9322

93L22

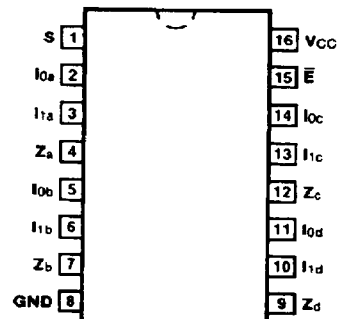
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The '22 quad 2-input digital multiplexers consist of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output.

- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED OUTPUTS

ORDERING CODE: See Section 9

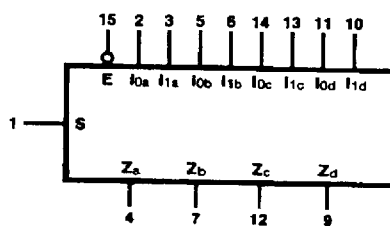
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ \text{C to } +70^\circ \text{C}$	$V_{CC} = +5.0 \text{ V}, \pm 10\%$, $T_A = -55^\circ \text{C to } +125^\circ \text{C}$	
Plastic DIP (P)	A	9322PC, 93L22PC		9B
Ceramic DIP (D)	A	9322DC, 93L22DC	9322DM, 93L22DM	6B
Flatpak (F)	A	9322FC, 93L22FC	9322FM, 93L22FM	4L

CONNECTION DIAGRAM
PINOUT A

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
S	Common Select Input	1.0/1.0	0.5/0.25
E	Enable Input (Active LOW)	1.0/1.0	0.5/0.25
I0a — I0d I1a — I1d	Multiplexer Inputs	1.0/1.0	0.5/0.25
Za — Zd	Multiplexer Outputs	20/10	10/5.0 (3.0)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '22 quad 2-input multiplexer provides the ability to select four bits of either data or control from two sources, in one package. The Enable input ($\bar{E}$) is active LOW. When not activated all outputs (Z_n) are LOW regardless of all other inputs.

The '22 quad 2-input multiplexer is the logical implementation of a four-pole, two position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$$\begin{aligned} Z_a &= E \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) & Z_b &= E \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ Z_c &= E \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) & Z_d &= E \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

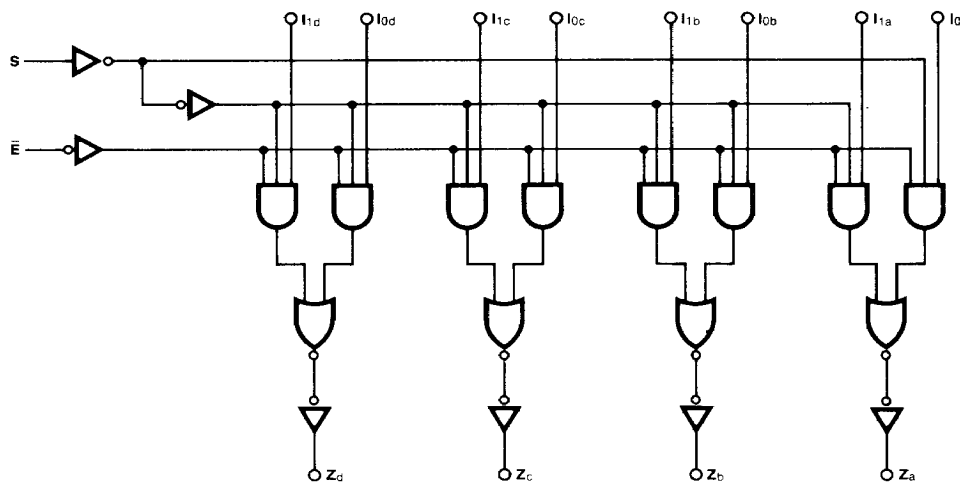
A common use of the '22 is the moving of data from a group of registers to four common output busses. The particular register from which the data comes is determined by the state of the select input. A less obvious use is as a function generator. The '22 can generate four functions of two variables with one variable common. This is useful for implementing random gating functions.

TRUTH TABLE

INPUTS				OUTPUT
$\bar{E}$	S	I_{0n}	I_{1n}	Z_n
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)							
SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
I _{OS}	Output Short Circuit Current	-20	-70			mA	V _{CC} = Max, V _{OUT} = 0 V
I _{CC}	Power Supply Current		47		13.2	mA	V _{CC} = Max
AG CHARACTERISTICS: V _{CC} = +5.0 V, T _A = +25° C (See Section 3 for waveforms and load configurations)							
SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω		C _L = 15 pF			
		Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay S to Z _n		23 27		36 49	ns	Figs. 3-1, 3-20
t _{PLH} t _{PHL}	Propagation Delay I ₀ or I ₁ to Z _n		14 14		22 30	ns	Figs. 3-1, 3-5
t _{PLH} t _{PHL}	Propagation Delay Ē to Z _n		20 21		27 27	ns	Figs. 3-1, 3-4