Zero Drift, Digitally Programmable Instrumentation Amplifier

Data Sheet **AD8231-EP**

FEATURES

Digitally/pin-programmable gain
- **G = 1, 2, 4, 8, 16, 32, 64, or 128**

Specified from −55°C to +125°C
- **50 nV/°C maximum input offset drift**
- **10 ppm/°C maximum gain drift**

Excellent dc performance
- **80 dB minimum CMR, G = 1**
- **15 μV maximum input offset voltage**
- **500 pA maximum bias current**
- **0.7 μV p-p noise (0.1 Hz to 10 Hz)**

Good ac performance
- **2.7 MHz bandwidth, G = 1**
- **1.1 V/μs slew rate**

Rail-to-rail output
Shutdown/multiplex
Extra op amp
Single-supply range: 3 V to 6 V
Dual-supply range: ±1.5 V to ±3 V

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

FUNCTIONAL BLOCK DIAGRAM

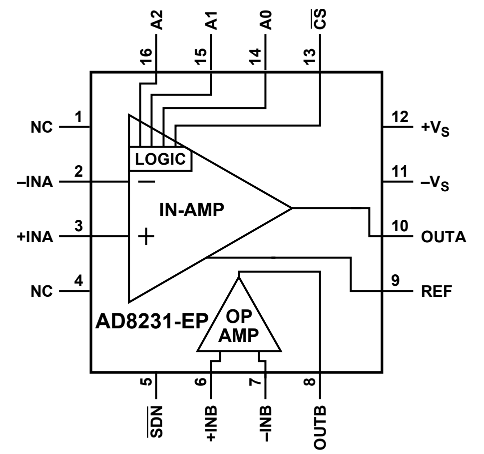

Figure 1.

Table 1. Instrumentation and Difference Amplifiers by Category

High Performance	Low Cost	High Voltage	Mil Grade	Low Power	Digital Gain
AD8221	AD623[1]	AD628	AD620	AD627[1]	AD8231[1]
AD8220[1]	AD8553[1]	AD629	AD621		AD8250
AD8222			AD524		AD8251
AD8224[1]			AD526		AD8555[1]
			AD624		AD8556[1]
					AD8557[1]

[1] Rail-to-rail output.

GENERAL DESCRIPTION

The AD8231-EP is a low drift, rail-to-rail, instrumentation amplifier with software-programmable gains of 1, 2, 4, 8, 16, 32, 64, or 128. The gains are programmed via digital logic or pin strapping.

The AD8231-EP is ideal for applications that require precision performance over a wide temperature range, such as industrial temperature sensing and data logging. Because the gain setting resistors are internal, maximum gain drift is only 10 ppm/°C for gains of 1 to 32. Because of the auto-zero input stage, maximum input offset is 15 μV and maximum input offset drift is just 50 nV/°C. CMRR is 80 dB for G = 1, increasing to 110 dB at higher gains.

The AD8231-EP also includes an uncommitted op amp that can be used for additional gain, differential signal driving, or filtering. Like the in-amp, the op amp has an auto-zero architecture, rail-to-rail input, and rail-to-rail output.

The AD8231-EP includes a shutdown feature that reduces current to a maximum of 1 μA. In shutdown, both amplifiers also have a high output impedance, which allows easy multiplexing of multiple amplifiers without additional switches.

The AD8231-EP is specified over the military temperature range of −55°C to +125°C. It is available in a 4 mm × 4 mm 16-lead LFCSP.

Additional application and technical information can be found in the AD8231 data sheet.

Rev. A **Document Feedback**

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REVISION HISTORY

11/2017—Rev. 0 to Rev. A

Changed CP-16-4 to CP-16-17 ... Throughout
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 18

5/2011—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, V_{REF} = 2.5 V, G = 1, R_L = 10 kΩ, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER					
Offset Voltage	V_{OS} RTI = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}			4	15	µV
Average Temperature Drift	T_A = −55°C to +125°C		0.01	0.05	µV/°C
Output Offset, V_{OSO}			15	30	µV
Average Temperature Drift	T_A = −55°C to +125°C		0.05	0.5	µV/°C
Input Currents					
Input Bias Current			250	500	pA
	T_A = −55°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −55°C to +125°C			0.5	nA
Gains	1, 2, 4, 8, 16, 32, 64, or 128				
Gain Error					
G = 1				0.05	%
G = 2 to 128				0.8	%
Gain Drift	T_A = −55°C to +125°C				
G = 1 to 32			3	10	ppm/°C
G = 64			4	20	ppm/°C
G = 128			10	30	ppm/°C
Linearity	0.2 V to 4.8 V, 10 kΩ load		3		ppm
	0.2 V to 4.8 V, 2 kΩ load		5		ppm
CMRR					
G = 1		80			dB
G = 2		86			dB
G = 4		92			dB
G = 8		98			dB
G = 16		104			dB
G = 32		110			dB
G = 64		110			dB
G = 128		110			dB
Noise	$e_n = \sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$, V_{IN+}, V_{IN-} = 2.5 V				
Input Voltage Noise, e_{ni}	f = 1 kHz		32		nV/√Hz
	f = 1 kHz, T_A = −55°C		27		nV/√Hz
	f = 1 kHz, T_A = 125°C		39		nV/√Hz
	f = 0.1 Hz to 10 Hz		0.7		µV p-p
Output Voltage Noise, e_{no}	f = 1 kHz		58		nV/√Hz
	f = 1 kHz, T_A = −55°C		50		nV/√Hz
	f = 1 kHz, T_A = 125°C		70		nV/√Hz
	f = 0.1 Hz to 10 Hz		1.1		µV p-p
Current Noise	f = 10 Hz		20		fA/√Hz
Other Input Characteristics					
Common-Mode Input Impedance			10‖5		GΩ‖pF
Power Supply Rejection Ratio		100	115		dB
Input Operating Voltage Range		0.05		4.95	V
Reference Input					
Input Impedance			28		kΩ
Voltage Range		−0.2		+5.2	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Dynamic Performance					
Bandwidth					
G = 1			2.7		MHz
G = 2			2.5		MHz
Gain Bandwidth Product					
G = 4 to 128			7		MHz
Slew Rate			1.1		V/µs
Output Characteristics					
Output Voltage High	R_L = 100 kΩ to ground	4.9	4.94		V
	R_L = 10 kΩ to ground	4.8	4.88		V
Output Voltage Low	R_L = 100 kΩ to 5 V		60	100	mV
	R_L = 10 kΩ to 5 V		80	200	mV
Short-Circuit Current			70		mA
Digital Interface					
Input Voltage Low	T_A = −55°C to +125°C			1.0	V
Input Voltage High	T_A = −55°C to +125°C	4.0			V
Setup Time to $\overline{CS}$ High	T_A = −55°C to +125°C	50			ns
Hold Time after $\overline{CS}$ High	T_A = −55°C to +125°C	20			ns
OPERATIONAL AMPLIFIER					
Input Characteristics					
Offset Voltage, V_{OS}			5	15	µV
Temperature Drift	T_A = −55°C to +125°C		0.01	0.06	µV/°C
Input Bias Current			250	500	pA
	T_A = −55°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −55°C to +125°C			0.5	nA
Input Voltage Range		0.05		4.95	V
Open-Loop Gain		100	120		V/mV
Common-Mode Rejection Ratio		100	120		dB
Power Supply Rejection Ratio		100	110		dB
Voltage Noise Density			20		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		0.4		µV p-p
Dynamic Performance					
Gain Bandwidth Product			1		MHz
Slew Rate			0.5		V/µs
Output Characteristics					
Output Voltage High	R_L = 100 kΩ to ground	4.9	4.96		V
	R_L = 10 kΩ to ground	4.8	4.92		V
Output Voltage Low	R_L = 100 kΩ to 5 V		60	100	mV
	R_L = 10 kΩ to 5 V		80	200	mV
Short-Circuit Current			70		mA
BOTH AMPLIFIERS					
Power Supply					
Quiescent Current			4	5	mA
Quiescent Current (Shutdown)			0.01	1	µA

V_S = 3.0 V, V_{REF} = 1.5 V, T_A = 25°C, G = 1, R_L = 10 kΩ, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER					
Offset Voltage	V_{OS} RTI = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}			4	15	µV
Average Temperature Drift			0.01	0.05	µV/°C
Output Offset, V_{OSO}			15	30	µV
Average Temperature Drift			0.05	0.5	µV/°C
Input Currents					
Input Bias Current			250	500	pA
	T_A = −55°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −55°C to +125°C			0.5	nA
Gains	1, 2, 4, 8, 16, 32, 64, or 128				
Gain Error					
G = 1				0.05	%
G = 2 to 128				0.8	%
Gain Drift	T_A = −55°C to +125°C				
G = 1 to 32			3	10	ppm/°C
G = 64			4	20	ppm/°C
G = 128			10	30	ppm/°C
CMRR					
G = 1		80			dB
G = 2		86			dB
G = 4		92			dB
G = 8		98			dB
G = 16		104			dB
G = 32		110			dB
G = 64		110			dB
G = 128		110			dB
Noise	$e_n = \sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$ V_{IN+}, V_{IN-} = 2.5 V, T_A = 25°C				
Input Voltage Noise, e_{ni}	f = 1 kHz		40		nV/√Hz
	f = 1 kHz, T_A = −55°C		35		nV/√Hz
	f = 1 kHz, T_A = 125°C		48		nV/√Hz
	f = 0.1 Hz to 10 Hz		0.8		µV p-p
Output Voltage Noise, e_{no}	f = 1 kHz		72		nV/√Hz
	f = 1 kHz, T_A = −55°C		62		nV/√Hz
	f = 1 kHz, T_A = 125°C		83		nV/√Hz
	f = 0.1 Hz to 10 Hz		1.4		µV p-p
Current Noise	f = 10 Hz		20		fA/√Hz
Other Input Characteristics					
Common-Mode Input Impedance			10‖5		GΩ‖pF
Power Supply Rejection Ratio		100	115		dB
Input Operating Voltage Range		0.05		2.95	V
Reference Input					
Input Impedance			28		kΩ‖pF
Voltage Range		−0.2		+3.2	V

Parameter	Conditions	Min	Typ	Max	Unit
Dynamic Performance					
Bandwidth					
G = 1			2.7		MHz
G = 2			2.5		MHz
Gain Bandwidth Product					
G = 4 to 128			7		MHz
Slew Rate			1.1		V/µs
Output Characteristics					
Output Voltage High	R_L = 100 kΩ to ground	2.9	2.94		V
	R_L = 10 kΩ to ground	2.8	2.88		V
Output Voltage Low	R_L = 100 kΩ to 3 V		60	100	mV
	R_L = 10 kΩ to 3 V		80	200	mV
Short-Circuit Current			40		mA
Digital Interface					
Input Voltage Low	T_A = −55°C to +125°C			0.7	V
Input Voltage High	T_A = −55°C to +125°C	2.3			V
Setup Time to $\overline{CS}$ High	T_A = −55°C to +125°C	60			ns
Hold Time after $\overline{CS}$ High	T_A = −55°C to +125°C	20			ns
OPERATIONAL AMPLIFIERS					
Input Characteristics					
Offset Voltage, V_{OS}			5	15	µV
Temperature Drift	T_A = −55°C to +125°C		0.01	0.06	µV/°C
Input Bias Current			250	500	pA
	T_A = −55°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −55°C to +125°C			0.5	nA
Input Voltage Range		0.05		2.95	V
Open-Loop Gain		100	120		V/mV
Common-Mode Rejection Ratio		100	120		dB
Power Supply Rejection Ratio		100	110		dB
Voltage Noise Density			27		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		0.6		µV p-p
Dynamic Performance					
Gain Bandwidth Product			1		MHz
Slew Rate			0.5		V/µs
Output Characteristics					
Output Voltage High	R_L = 100 kΩ to ground	2.9	2.96		V
	R_L = 10 kΩ to ground	2.8	2.82		V
Output Voltage Low	R_L = 100 kΩ to 3 V		60	100	mV
	R_L = 10 kΩ to 3 V		80	200	mV
Short-Circuit Current			40		mA
BOTH AMPLIFIERS					
Power Supply					
Quiescent Current			3.5	4.5	mA
Quiescent Current (Shutdown)			0.01	1	µA

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Output Short-Circuit Current	Indefinite[1]
Input Voltage (Common-Mode)	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Differential Input Voltage	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Storage Temperature Range	−65°C to +150°C
Operational Temperature Range	−55°C to +125°C
Package Glass Transition Temperature	130°C
ESD (Human Body Model)	1.5 kV
ESD (Charged Device Model)	1.5 kV
ESD (Machine Model)	0.2 kV

[1] For junction temperatures between 105°C and 130°C, short-circuit operation beyond 1000 hours can impact part reliability.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 5.

Thermal Pad	θ_{JA}	Unit
Soldered to Board	54	°C/W
Not Soldered to Board	96	°C/W

The θ_{JA} values in Table 5 assume a 4-layer JEDEC standard board. If the thermal pad is soldered to the board, it is also assumed it is connected to a plane. θ_{JC} at the exposed pad is 6.3°C/W.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8231-EP is limited by the associated rise in junction temperature (T_J) on the die. At approximately 130°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 130°C for an extended period can result in a loss of functionality.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

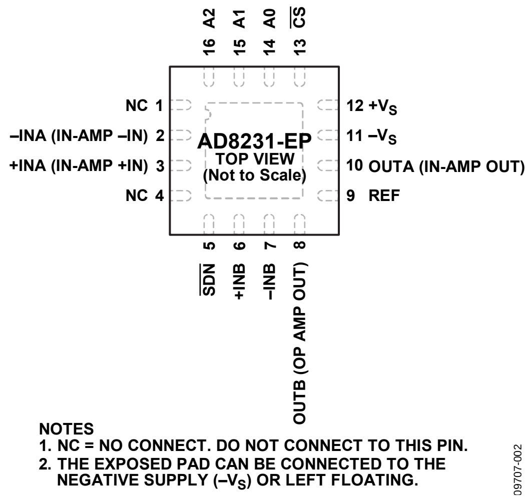

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	NC	No Connect. Do not connect to this pin.
2	−INA (IN-AMP −IN)	Instrumentation Amplifier Negative Input.
3	+INA (IN-AMP +IN)	Instrumentation Amplifier Positive Input.
4	NC	No Connect. Do not connect to this pin.
5	$\overline{\text{SDN}}$	Shutdown.
6	+INB	Operational Amplifier Positive Input.
7	−INB	Operational Amplifier Negative Input.
8	OUTB (OP AMP OUT)	Operational Amplifier Output.
9	REF	Instrumentation Amplifier Reference Pin. It should be driven with a low impedance. Output is referred to this pin.
10	OUTA (IN-AMP OUT)	Instrumentation Amplifier Output.
11	$-V_S$	Negative Power Supply. Connect to ground in single-supply applications.
12	$+V_S$	Positive Power Supply.
13	$\overline{\text{CS}}$	Chip Select. Enables digital logic interface.
14	A0	Gain Setting Bit (LSB).
15	A1	Gain Setting Bit.
16	A2	Gain Setting Bit (MSB).
	EPAD	Exposed Pad. Can be connected to the negative supply ($-V_S$) or left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

INSTRUMENTATION AMPLIFIER PERFORMANCE CURVES

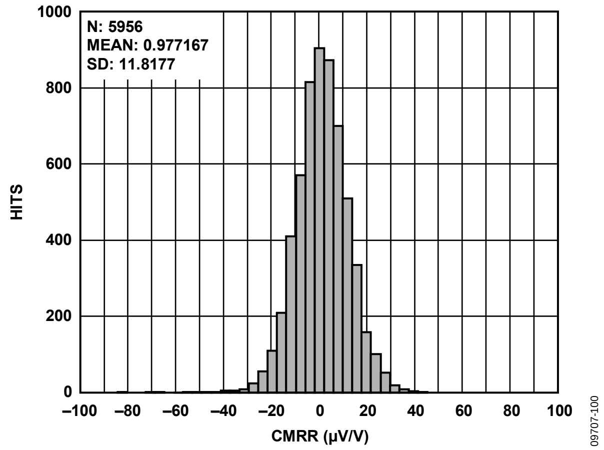

Figure 3. Instrumentation Amplifier CMR Distribution, G = 1

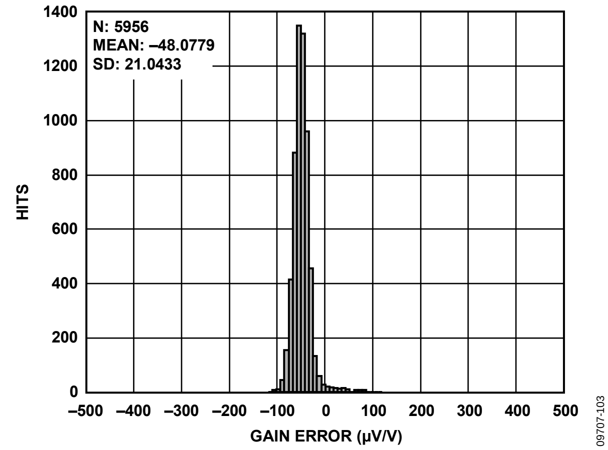

Figure 6. Instrumentation Amplifier Gain Distribution, G = 1

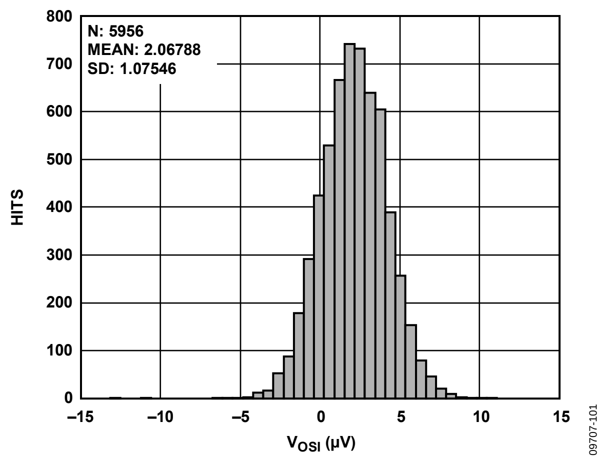

Figure 4. Instrumentation Amplifier Input Offset Voltage Distribution

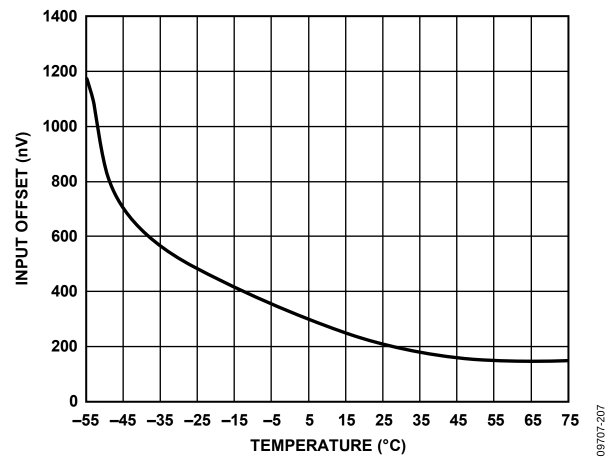

Figure 7. Instrumentation Amplifier Input Offset Voltage Drift, −55°C to +125°C

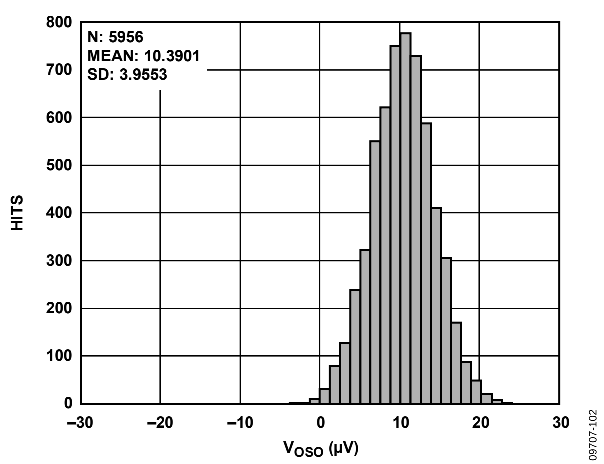

Figure 5. Instrumentation Amplifier Output Offset Voltage Distribution

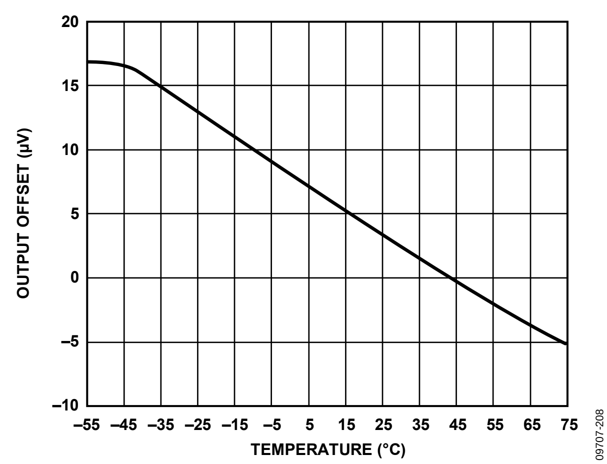

Figure 8. Instrumentation Amplifier Output Offset Drift, −55°C to +125°C

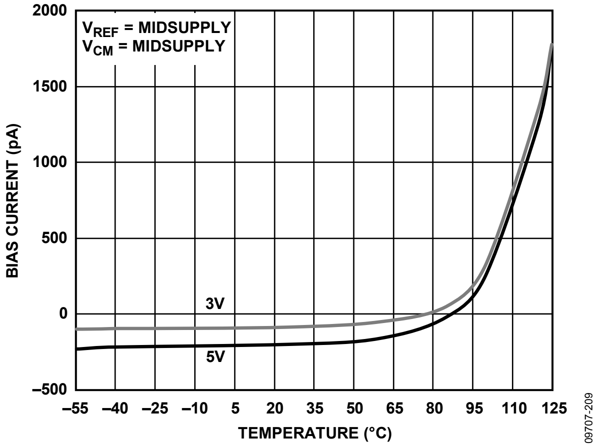

Figure 9. Instrumentation Amplifier Bias Current vs. Temperature

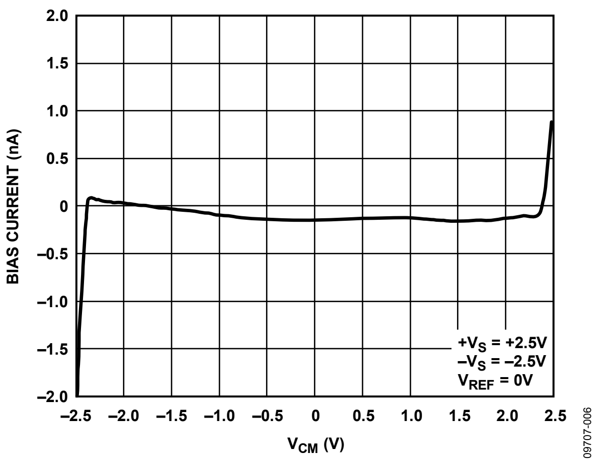

Figure 10. Instrumentation Amplifier Bias Current vs. Common-Mode Voltage, 5 V

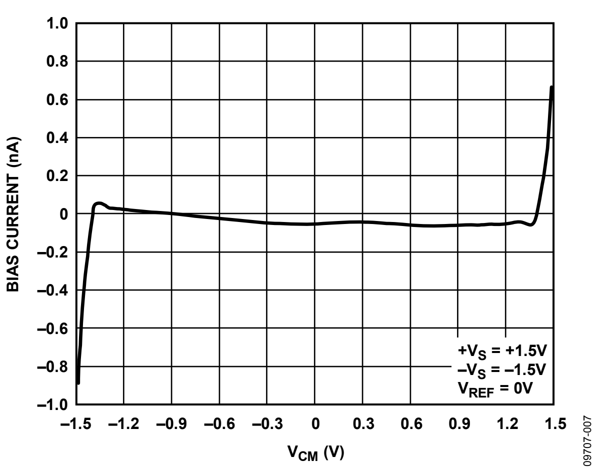

Figure 11. Instrumentation Amplifier Bias Current vs. Common-Mode Voltage, 3 V

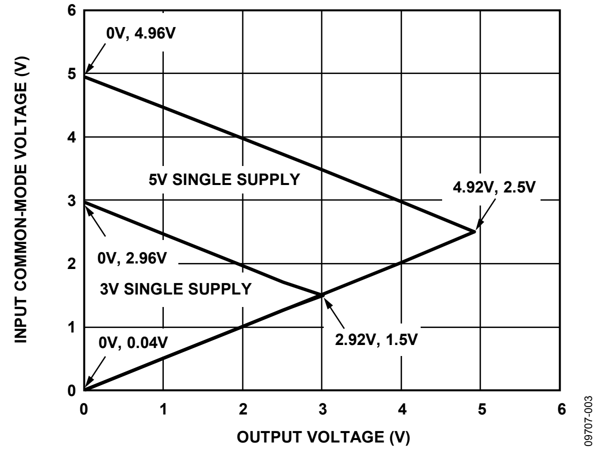

Figure 12. Instrumentation Amplifier Input Common-Mode Range vs. Output Voltage, V_{REF} = 0 V

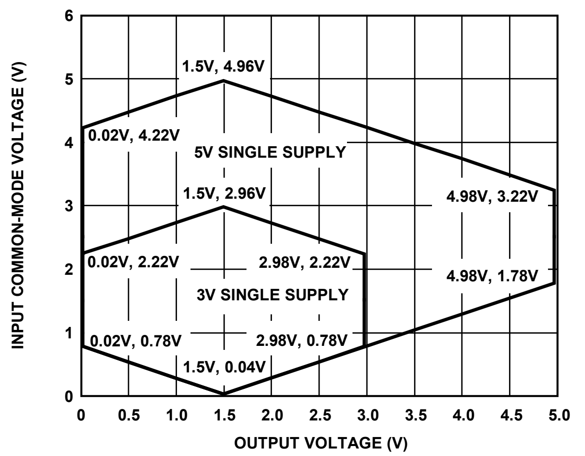

Figure 13. Instrumentation Amplifier Input Common-Mode Range vs. Output Voltage, V_{REF} = 1.5 V

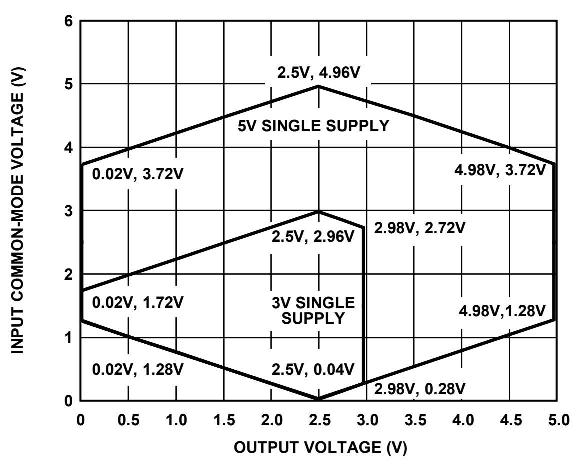

Figure 14. Instrumentation Amplifier Input Common-Mode Range vs. Output Voltage, V_{REF} = 2.5 V

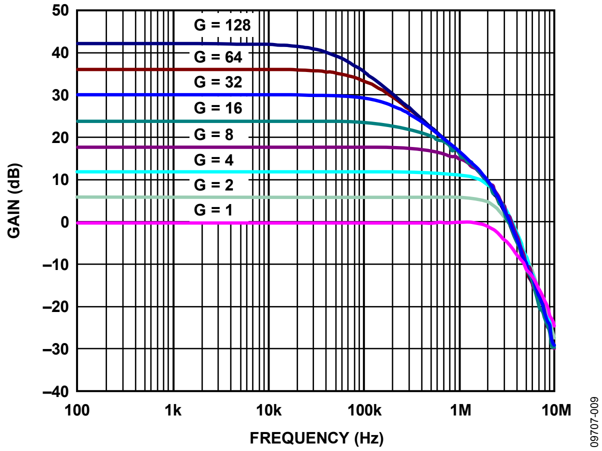

Figure 15. Instrumentation Amplifier Gain vs. Frequency

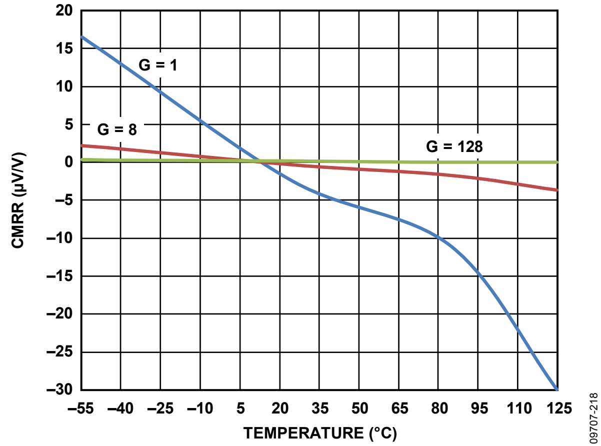

Figure 18. Instrumentation Amplifier CMRR vs. Temperature

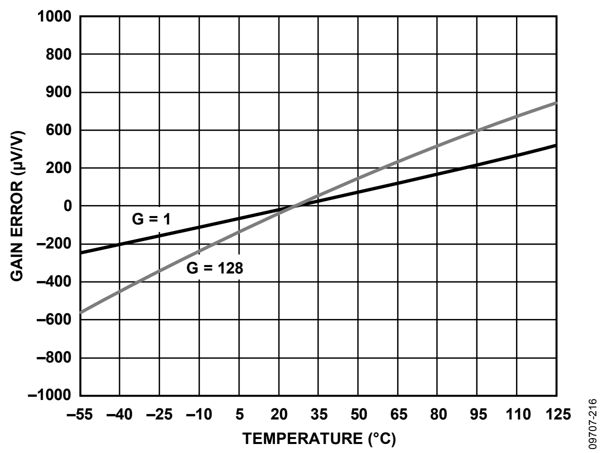

Figure 16. Instrumentation Amplifier Gain Drift vs. Temperature

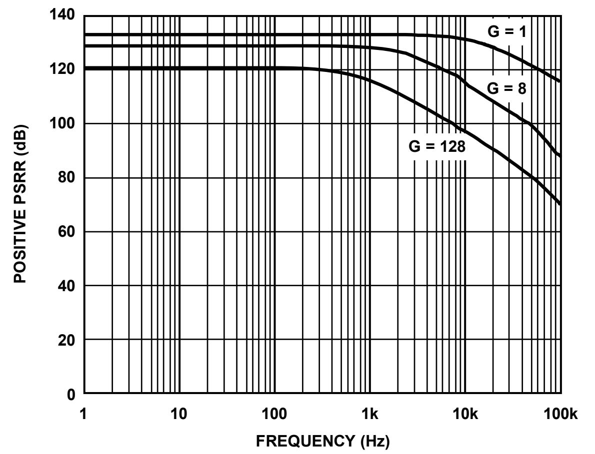

Figure 19. Instrumentation Amplifier Positive PSRR vs. Frequency

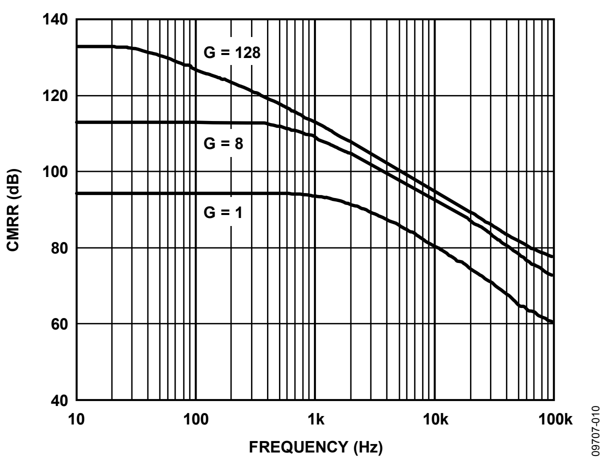

Figure 17. Instrumentation Amplifier CMRR vs. Frequency

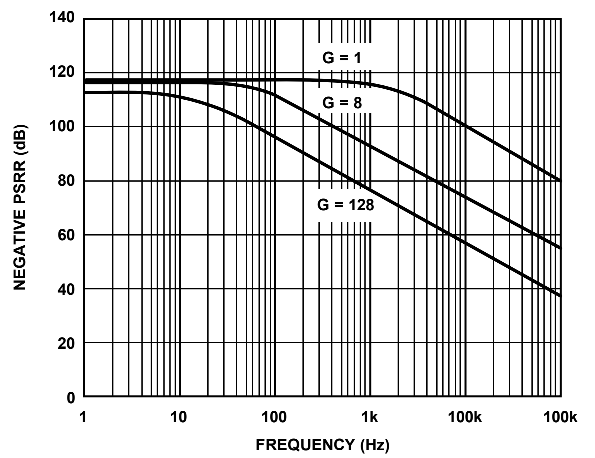

Figure 20. Instrumentation Amplifier Negative PSRR vs. Frequency

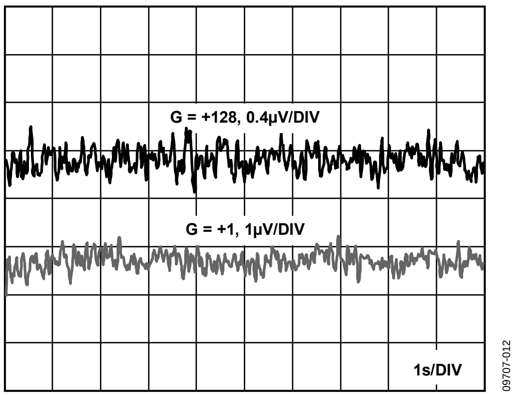

Figure 21. Instrumentation Amplifier 0.1 Hz to 10 Hz Noise

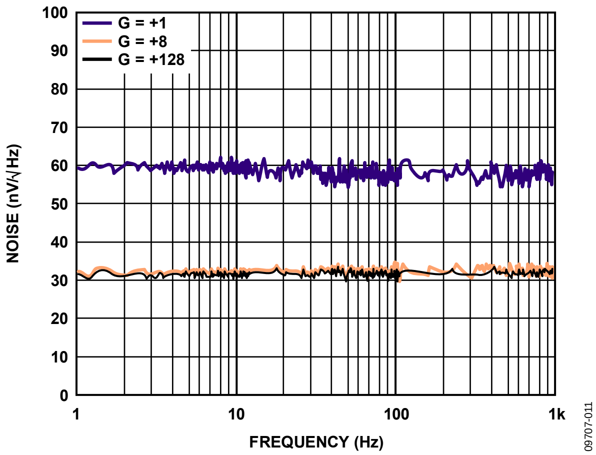

Figure 22. Instrumentation Amplifier Voltage Noise Spectral Density vs. Frequency, 5 V, 1 Hz to 1000 Hz

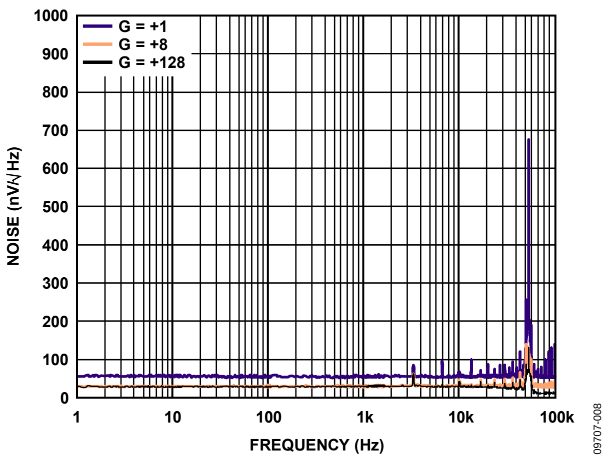

Figure 23. Instrumentation Amplifier Voltage Noise Spectral Density vs. Frequency, 5 V, 1 Hz to 1 MHz

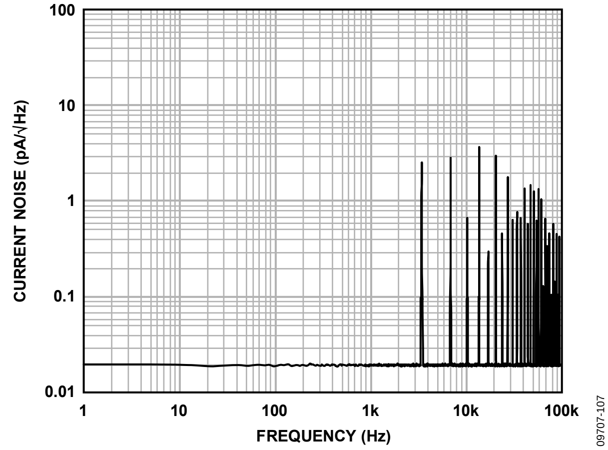

Figure 24. Instrumentation Amplifier Current Noise Spectral Density

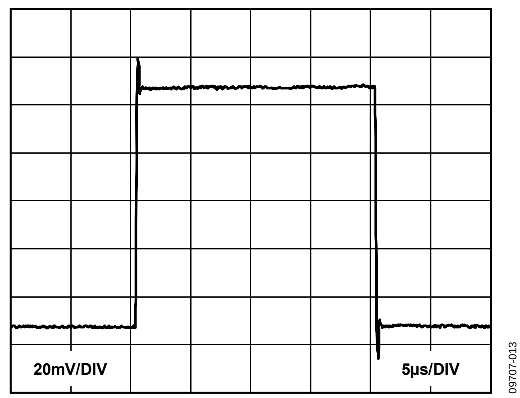

Figure 25. Instrumentation Amplifier Small Signal Pulse Response, G = 1, R_L = 2 kΩ, C_L = 500 pF

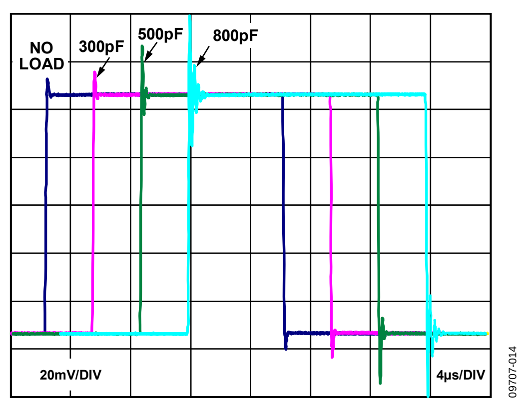

Figure 26. Instrumentation Amplifier Small Signal Pulse Response for Various Capacitive Loads, G = 1

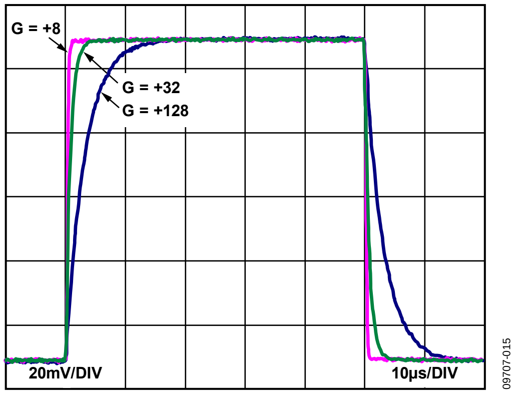

Figure 27. Instrumentation Amplifier Small Signal Pulse Response, G = 4, 16, and 128, R_L = 2 kΩ, C_L = 500 pF

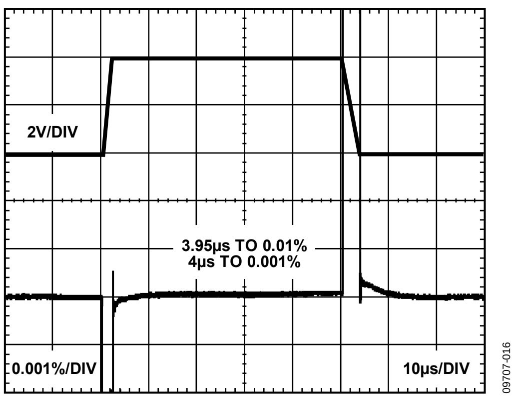

Figure 28. Instrumentation Amplifier Large Signal Pulse Response, G = 1, V_S = 5 V

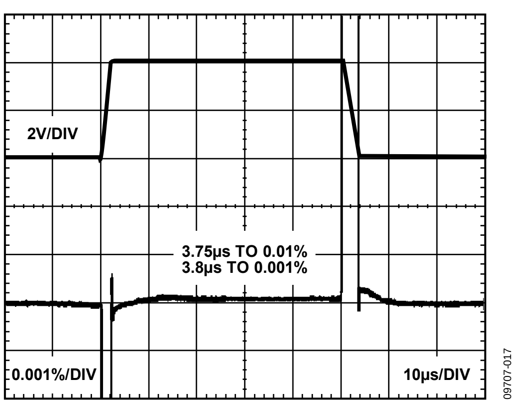

Figure 29. Instrumentation Amplifier Large Signal Pulse Response, G = 8, V_S = 5 V

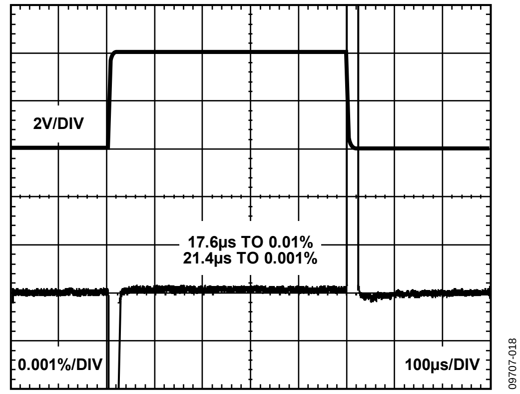

Figure 30. Instrumentation Amplifier Large Signal Pulse Response, G = 128, V_S = 5 V

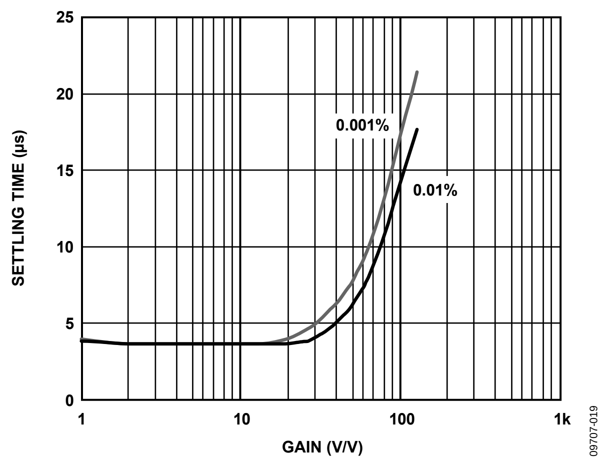

Figure 31. Instrumentation Amplifier Settling Time vs. Gain for a 4 V p-p Step, V_S = 5 V

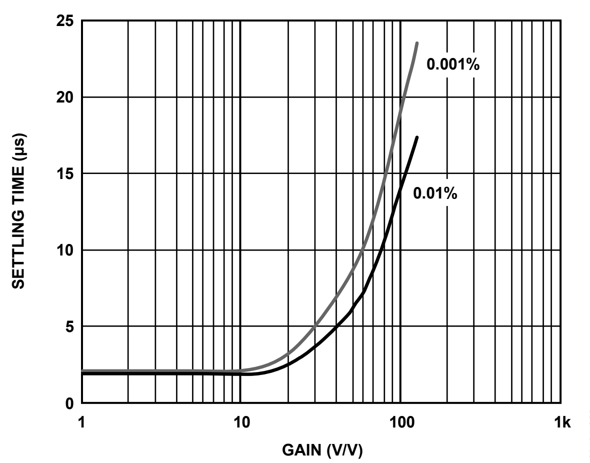

Figure 32. Instrumentation Amplifier Settling Time vs. Gain for a 2 V p-p Step, V_S = 3 V

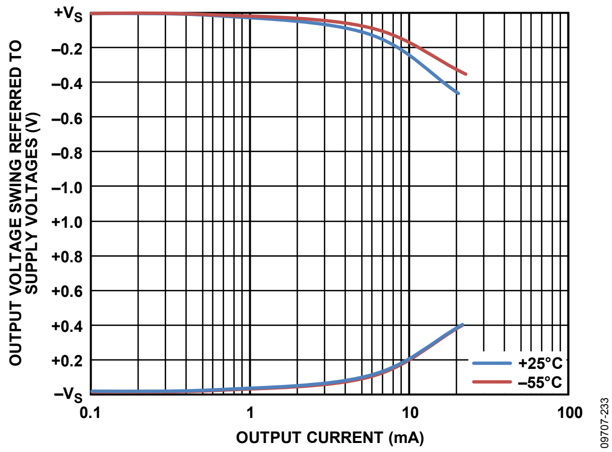

Figure 33. Instrumentation Amplifier Output Voltage Swing vs. Output Current, V_S = 3 V

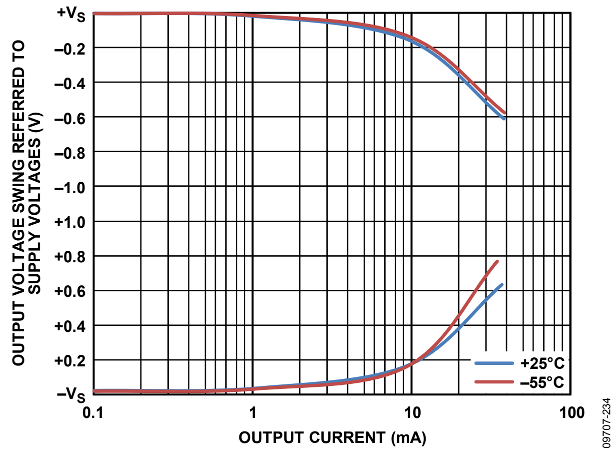

Figure 34. Instrumentation Amplifier Output Voltage Swing vs. Output Current, V_S = 5 V

OPERATIONAL AMPLIFIER PERFORMANCE CURVES

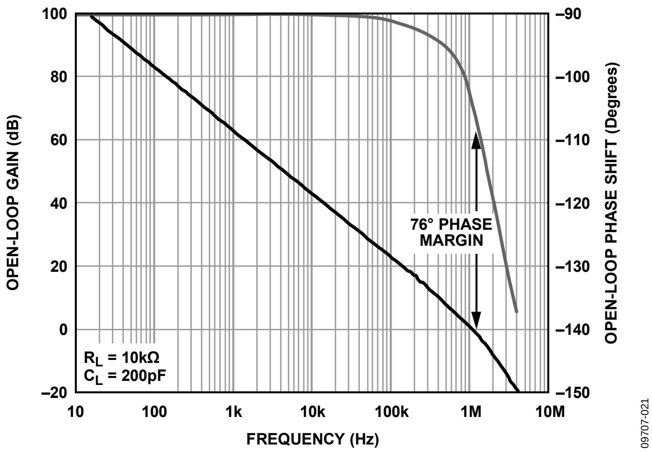

Figure 35. Operational Amplifier Open-Loop Gain and Phase vs. Frequency, V_S = 5 V

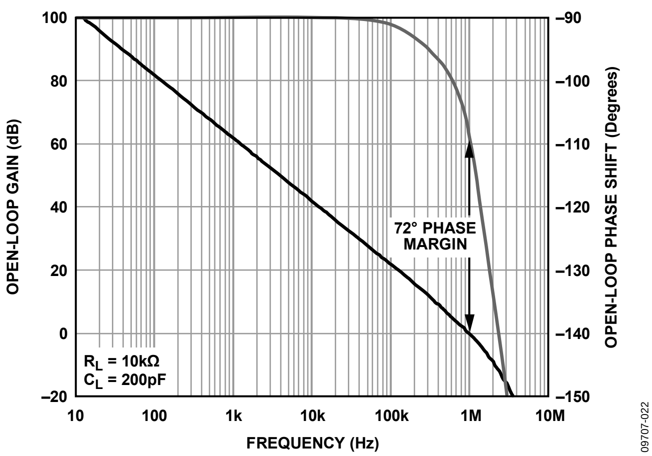

Figure 36. Operational Amplifier Open-Loop Gain and Phase vs. Frequency, V_S = 3 V

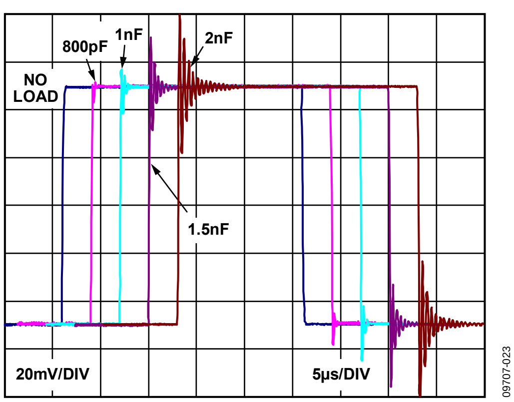

Figure 37. Operational Amplifier Small Signal Response for Various Capacitive Loads, V_S = 5 V

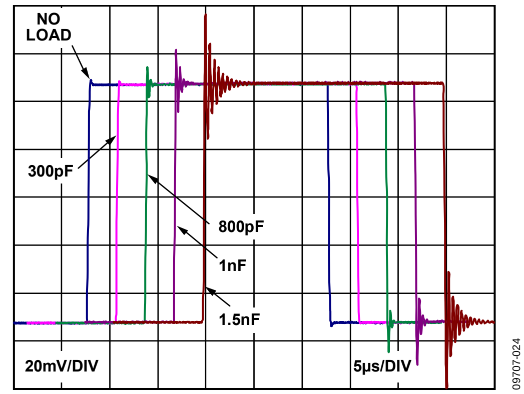

Figure 38. Operational Amplifier Small Signal Response for Various Capacitive Loads, V_S = 3 V

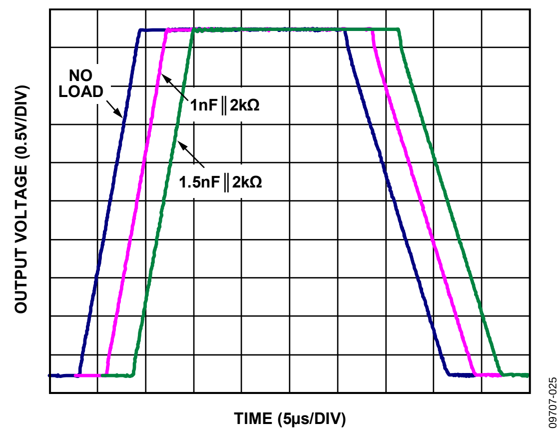

Figure 39. Operational Amplifier Large Signal Transient Response, V_S = 5 V

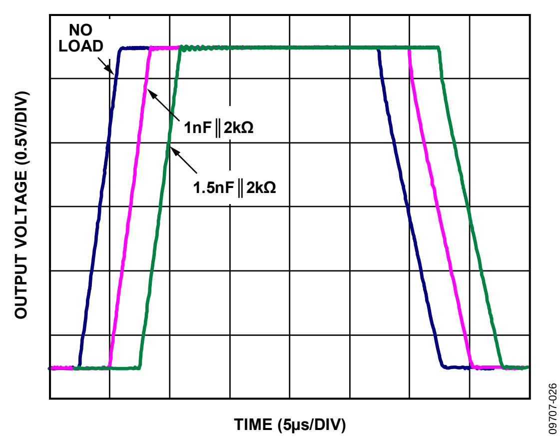

Figure 40. Operational Amplifier Large Signal Transient Response, V_S = 3 V

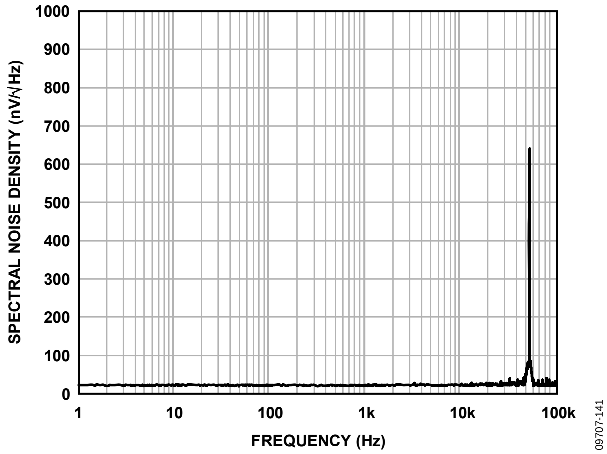

Figure 41. Operational Amplifier Voltage Spectral Noise Density vs. Frequency

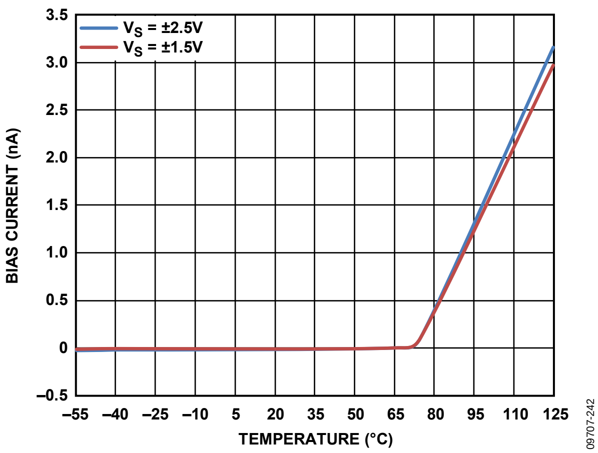

Figure 42. Operational Amplifier Bias Current vs. Temperature

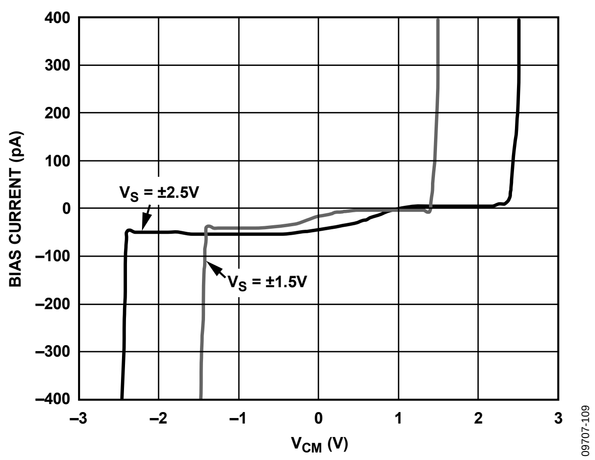

Figure 43. Operational Amplifier Bias Current vs. Common Mode

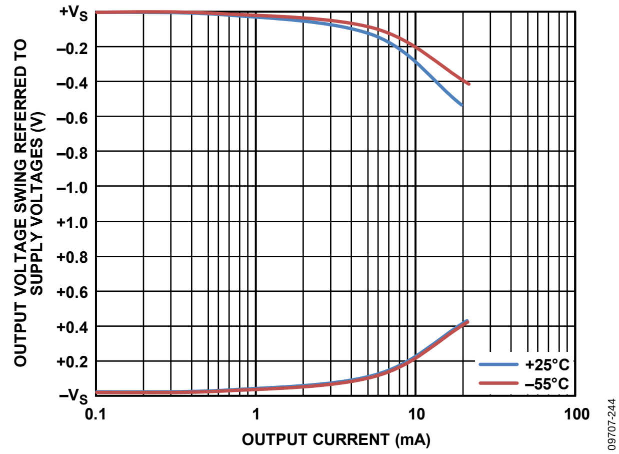

Figure 44. Operational Amplifier Output Voltage Swing vs. Output Current, $V_S = 3$ V

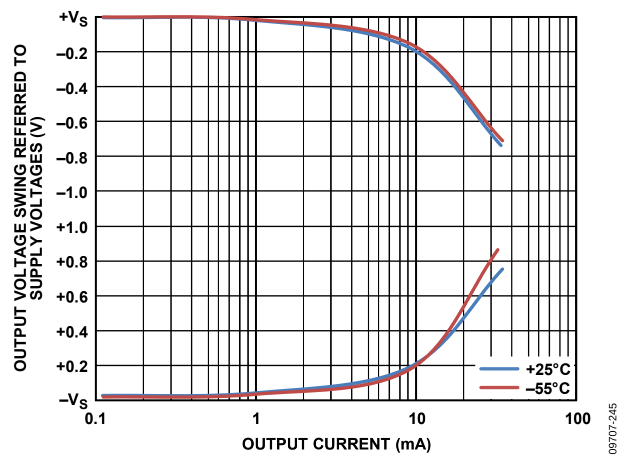

Figure 45. Operational Amplifier Output Voltage Swing vs. Output Current, $V_S = 5$ V

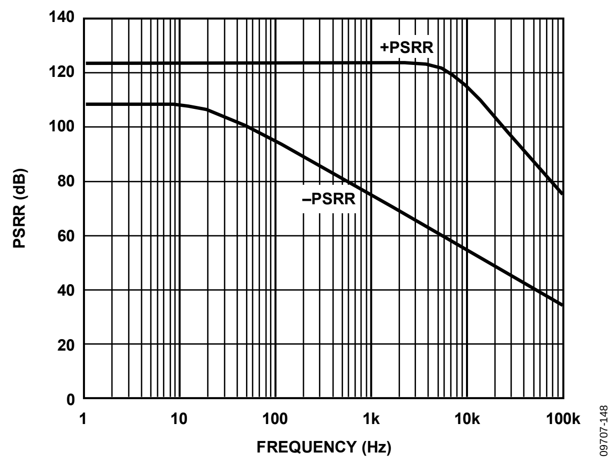

Figure 46. Operational Amplifier Power Supply Rejection Ratio

PERFORMANCE CURVES VALID FOR BOTH AMPLIFIERS

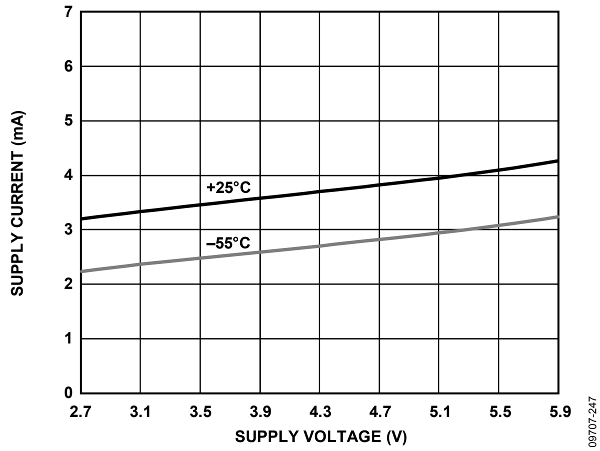

Figure 47. Supply Current vs. Supply Voltage

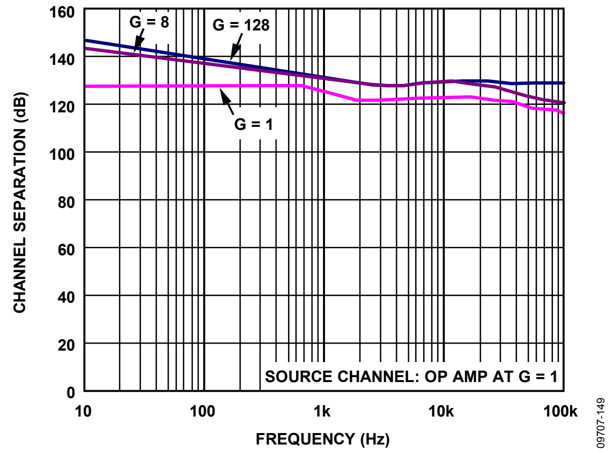

Figure 48. Channel Separation vs. Frequency

OUTLINE DIMENSIONS

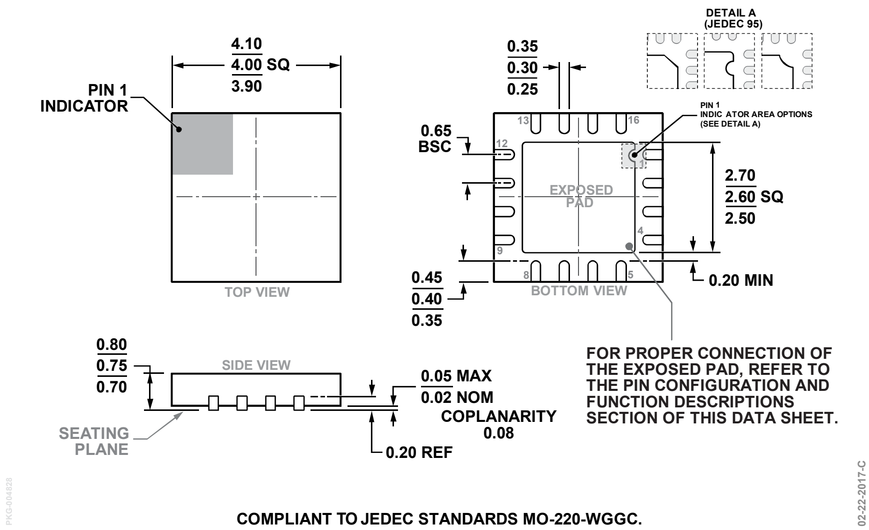

Figure 49. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8231TCPZ-EP-R7	−55°C to +125°C	16-Lead LFCSP, 7" Tape and Reel	CP-16-17

[1] Z = RoHS Compliant Part.

NOTES

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