

# MC100EPT22

## 3.3 V Dual LVTTTL/LVCMOS to Differential LVPECL Translator

### Description

The MC100EPT22 is a dual LVTTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8-lead package and the single gate of the EPT22 makes it ideal for those applications where space, performance, and low power are at a premium. Because the mature MOSAIC 5 process is used, low cost and high speed can be added to the list of features.

### Features

- 420 ps Typical Propagation Delay
- Maximum Frequency = > 1.1 GHz Typical
- Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$  with  $GND = 0\text{ V}$
- PNP LVTTTL Inputs for Minimal Loading
- Q Output Will Default HIGH with Inputs Open
- The 100 Series Contains Temperature Compensation.
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



ON Semiconductor®

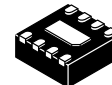
[www.onsemi.com](http://www.onsemi.com)



SOIC-8 NB  
D SUFFIX  
CASE 751-07

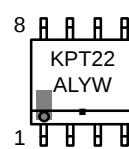


TSSOP-8  
DT SUFFIX  
CASE 948R-02

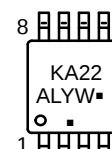


DFN8  
MN SUFFIX  
CASE 506AA

### MARKING DIAGRAMS\*



SOIC-8 NB



TSSOP-8



DFN8

A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
M = Date Code  
■ = Pb-Free Package

(Note: Microdot may be in either location)

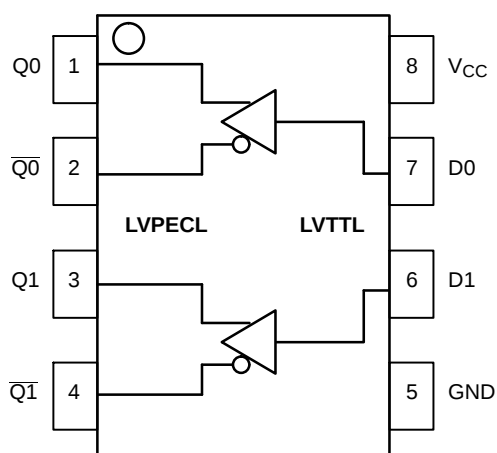
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

| Device          | Package                | Shipping†        |
|-----------------|------------------------|------------------|
| MC100EPT22DG    | SOIC-8 NB<br>(Pb-Free) | 98 Units/Tube    |
| MC100EPT22DR2G  | SOIC-8 NB<br>(Pb-Free) | 2500 Tape & Reel |
| MC100EPT22DTG   | TSSOP-8<br>(Pb-Free)   | 100 Tape & Reel  |
| MC100EPT22DTR2G | TSSOP-8<br>(Pb-Free)   | 2500 Tape & Reel |
| MC100EPT22MNR4G | DFN8<br>(Pb-Free)      | 1000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MC100EPT22



**Table 1. PIN DESCRIPTION**

| PIN                                       | FUNCTION                                                                                                                                                                       |
|-------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Q0, Q1, $\overline{Q0}$ , $\overline{Q1}$ | LVPECL Differential Outputs                                                                                                                                                    |
| D0, D1                                    | LVTTTL Inputs                                                                                                                                                                  |
| V <sub>CC</sub>                           | Positive Supply                                                                                                                                                                |
| GND                                       | Ground                                                                                                                                                                         |
| EP                                        | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 2. ATTRIBUTES**

| Characteristics                                                             | Value                         |
|-----------------------------------------------------------------------------|-------------------------------|
| Internal Input Pulldown Resistor                                            | N/A                           |
| Internal Input Pullup Resistor                                              | N/A                           |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 4 kV<br>> 200 V<br>> 2 kV   |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)               | Pb-Free Pkg                   |
| SOIC-8 NB<br>TSSOP-8<br>DFN8                                                | Level 1<br>Level 3<br>Level 1 |
| Flammability Rating<br>Oxygen Index: 28 to 34                               | UL 94 V-0 @ 0.125 in          |
| Transistor Count                                                            | 164 Devices                   |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                      |                               |

1. For additional information, see Application Note [AND8003/D](#).

# MC100EPT22

**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter                                | Condition 1        | Condition 2                      | Rating      | Unit |
|------------------|------------------------------------------|--------------------|----------------------------------|-------------|------|
| V <sub>CC</sub>  | Power Supply                             | GND = 0 V          |                                  | 6           | V    |
| V <sub>I</sub>   | Input Voltage                            | GND = 0 V          | V <sub>I</sub> ≤ V <sub>CC</sub> | 6 to 0      | V    |
| I <sub>out</sub> | Output Current                           | Continuous Surge   |                                  | 50<br>100   | mA   |
| T <sub>A</sub>   | Operating Temperature Range              |                    |                                  | -40 to +85  | °C   |
| T <sub>stg</sub> | Storage Temperature Range                |                    |                                  | -65 to +150 | °C   |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | SOIC-8 NB<br>SOIC-8 NB           | 190<br>130  | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | Standard Board     | SOIC-8 NB                        | 41 to 44    | °C/W |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | TSSOP-8<br>TSSOP-8               | 185<br>140  | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | Standard Board     | TSSOP-8                          | 41 to 44    | °C/W |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | DFN8<br>DFN8                     | 129<br>84   | °C/W |
| T <sub>sol</sub> | Wave Solder (Pb-Free)                    |                    |                                  | 265         | °C   |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | (Note 1)           | DFN8                             | 35 to 40    | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

**Table 4. TTL INPUT DC CHARACTERISTICS** (V<sub>CC</sub> = 3.3 V, GND = 0 V, T<sub>A</sub> = -40°C to 85°C)

| Symbol           | Characteristic         | Condition                         | Min | Typ | Max  | Unit |
|------------------|------------------------|-----------------------------------|-----|-----|------|------|
| I <sub>IH</sub>  | Input HIGH Current     | V <sub>IN</sub> = 2.7 V           |     |     | 20   | μA   |
| I <sub>IHH</sub> | Input HIGH Current MAX | V <sub>IN</sub> = V <sub>CC</sub> |     |     | 100  | μA   |
| I <sub>IL</sub>  | Input LOW Current      | V <sub>IN</sub> = 0.5 V           |     |     | -0.6 | mA   |
| V <sub>IK</sub>  | Input Clamp Voltage    | I <sub>IN</sub> = -18 mA          |     |     | -1.0 | V    |
| V <sub>IH</sub>  | Input HIGH Voltage     |                                   | 2.0 |     |      | V    |
| V <sub>IL</sub>  | Input LOW Voltage      |                                   |     |     | 0.8  | V    |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 5. PECL OUTPUT DC CHARACTERISTICS** (V<sub>CC</sub> = 3.3 V, GND = 0.0 V (Note 1))

| Symbol          | Characteristic               | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|-----------------|------------------------------|-------|------|------|------|------|------|------|------|------|------|
|                 |                              | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| I <sub>CC</sub> | Power Supply Current         | 32    | 43   | 55   | 35   | 45   | 60   | 37   | 46   | 62   | mA   |
| V <sub>OH</sub> | Output HIGH Voltage (Note 2) | 2155  | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV   |
| V <sub>OL</sub> | Output LOW Voltage (Note 2)  | 1355  | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Output parameters vary 1:1 with V<sub>CC</sub>.
- All loading with 50 Ω to V<sub>CC</sub> - 2.0 V.

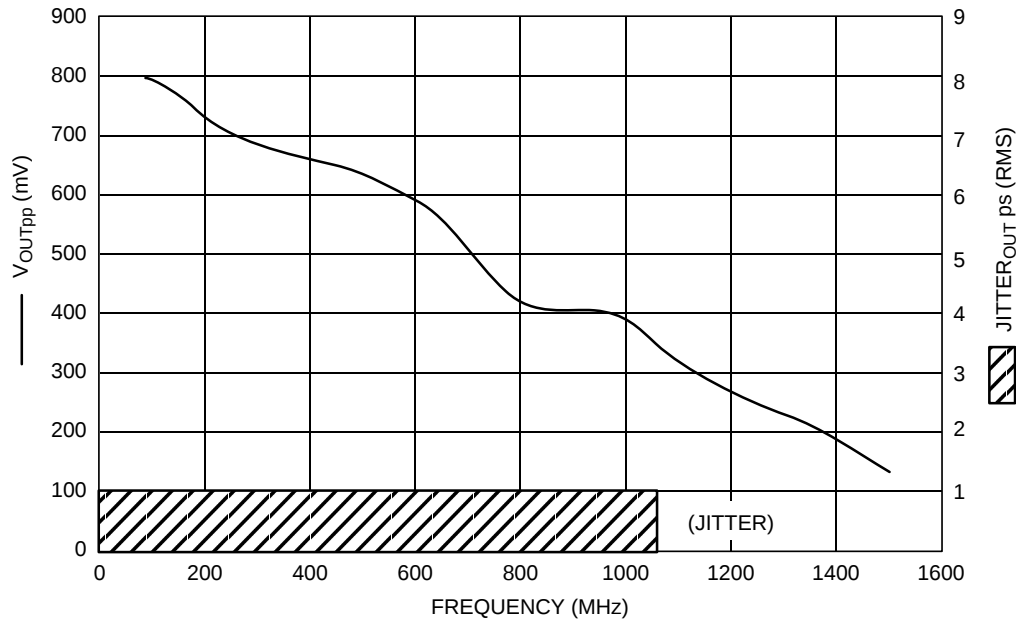
# MC100EPT22

**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ,  $GND = 0.0\text{ V}$  (Note 1))

| Symbol                   | Characteristic                                                                          | -40°C |           |            | 25°C |              |            | 85°C |           |            | Unit |
|--------------------------|-----------------------------------------------------------------------------------------|-------|-----------|------------|------|--------------|------------|------|-----------|------------|------|
|                          |                                                                                         | Min   | Typ       | Max        | Min  | Typ          | Max        | Min  | Typ       | Max        |      |
| $f_{\max}$               | Maximum Frequency (Figure 2)                                                            | 0.8   | 1.1       |            | 0.8  | 1.1          |            | 0.8  | 1.1       |            | GHz  |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to Output Differential                                                | 250   | 400       | 650        | 250  | 420          | 675        | 300  | 500       | 700        | ps   |
| $t_{\text{skew}}$        | Within-Device Skew (Note 2)<br>Device-to-Device Skew (Note 3)                           |       | 50<br>200 | 100<br>400 |      | 50<br>200    | 100<br>425 |      | 50<br>200 | 100<br>400 | ps   |
| $t_{\text{JITTER}}$      | Random Clock Jitter (Figure 2)                                                          |       | 0.2       | < 1        |      | 0.2          | < 1        |      | 0.2       | < 1        | ps   |
| $t_{\text{JIT}(\Phi)}$   | Additive Phase RMS Jitter<br>Integration Range 12 kHz to 20 MHz<br>25 MHz<br>156.25 MHz |       |           |            |      | 0.05<br>0.16 |            |      |           |            | ps   |
| $t_r$<br>$t_f$           | Output Rise/Fall Times<br>Q, $\bar{Q}$ (20%–80%)                                        | 50    | 110       | 200        | 60   | 120          | 220        | 70   | 140       | 250        | ps   |

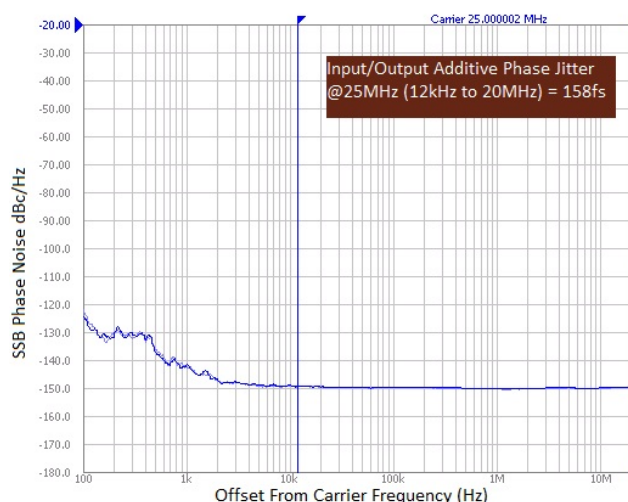
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 2.4 V source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
2. Skew is measured between outputs under identical transitions and conditions on any one device.
3. Device-to-Device Skew for identical transitions at identical  $V_{CC}$  levels.

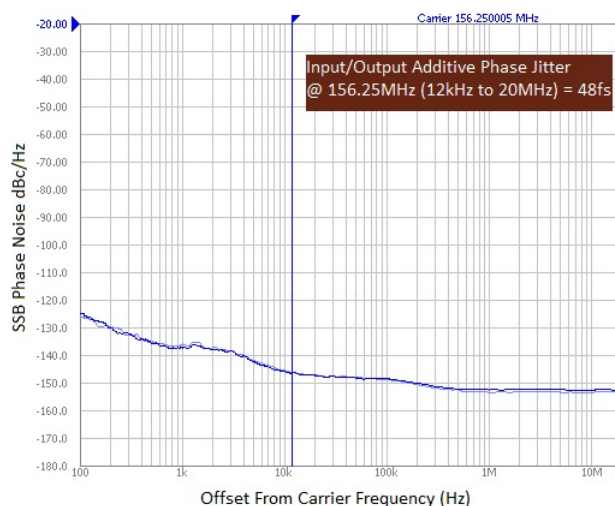


**Figure 2.  $F_{\max}$ /Jitter**

## MC100EPT22



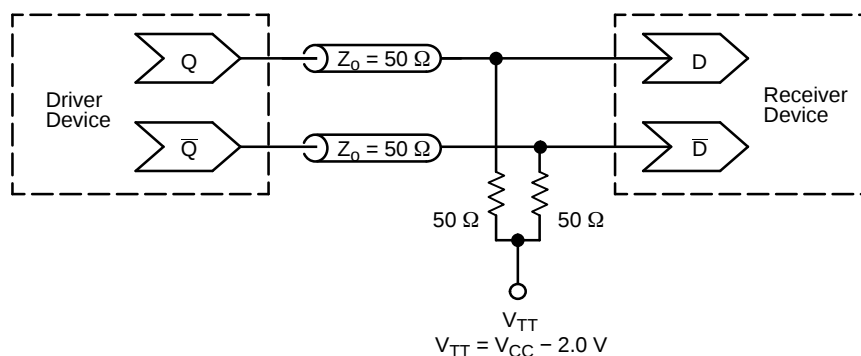
**Figure 3. Typical Phase Noise Plot at  $f_{\text{carrier}} = 25 \text{ MHz}$**



**Figure 4. Typical Phase Noise Plot at  $f_{\text{carrier}} = 156.25 \text{ MHz}$**

The above phase noise plots captured using Agilent E5052A show additive phase noise of the MC100EPT22 device at frequencies 25 MHz and 156.25 MHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the device (integrated

between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 158 fs and 48 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.



**Figure 5. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

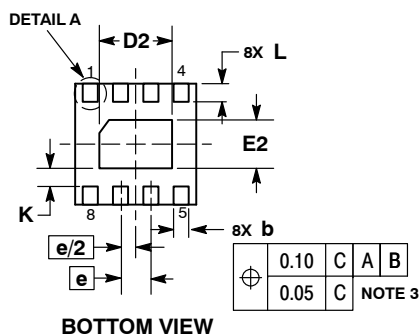
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



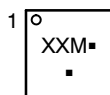
SCALE 4:1

DFN8 2x2, 0.5P  
CASE 506AA  
ISSUE F

DATE 04 MAY 2016

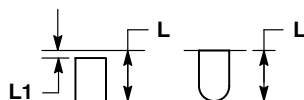


## GENERIC MARKING DIAGRAM\*

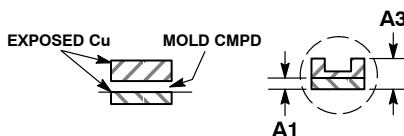


XX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Device

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



DETAIL A  
OPTIONAL  
CONSTRUCTIONS



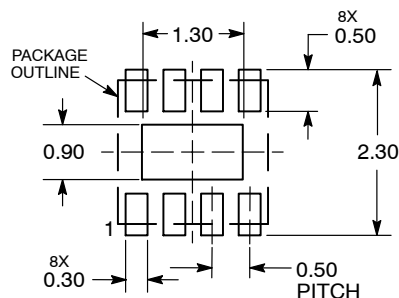
DETAIL B  
ALTERNATE  
CONSTRUCTIONS

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.80 | 1.00 |
| A1          | 0.00 | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.20 | 0.30 |
| D           | 2.00 | BSC  |
| D2          | 1.10 | 1.30 |
| E           | 2.00 | BSC  |
| E2          | 0.70 | 0.90 |
| e           | 0.50 | BSC  |
| K           | 0.30 | REF  |
| L           | 0.25 | 0.35 |
| L1          |      | 0.10 |

## RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |                            |                                                                                                                                                                                  |
|------------------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98AON18658D                | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | DFN8, 2.0X2.0, 0.5MM PITCH | PAGE 1 OF 1                                                                                                                                                                      |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

## GENERIC MARKING DIAGRAM\*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                  |
|------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2                                                                                                                                                                      |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

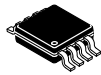
|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
|-------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42564B</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-8 NB</b>   | <b>PAGE 2 OF 2</b>                                                                                                                                                                  |

**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

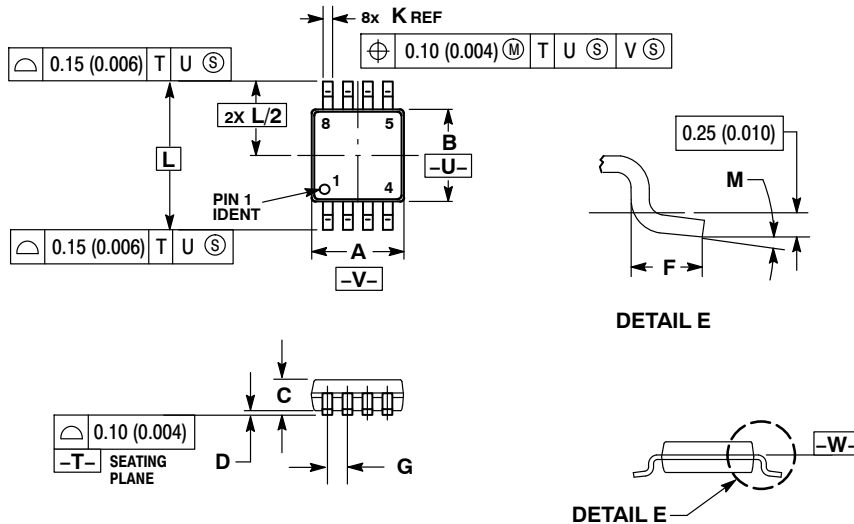
ON Semiconductor®



SCALE 2:1

## TSSOP 8 CASE 948R-02 ISSUE A

DATE 04/07/2000



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

DOCUMENT NUMBER: 98AON00236D

Electronic versions are uncontrolled except when accessed directly from the Document Repository.  
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: TSSOP 8

PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative