RL78/G15
RENESAS MCU

R01DS0420EJ0110
Rev.1.10
Apr 28, 2023

True low-power platform, 54-µA/MHz operating current, T_A = 125°C operation, from 8 to 20 pins, 4 to 8 KB code flash memory, 1 KB RAM, 2.4 to 5.5 V

1. OUTLINE

1.1 Features

Low power consumption technology

- V_{DD} = single power supply voltage of 2.4 to 5.5 V
- HALT mode
- STOP mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.0625 µs: @ 16 MHz operation with high-speed on-chip oscillator) to low speed (1.0 µs: @ 1 MHz operation)
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 1 KB

Code flash memory

- Code flash memory: 4 to 8 KB
- Block size: 1 KB
- Only write after erase is possible
- On-chip debug function
- Self-programming (with no boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 1 KB
- Block size: 512 B
- Unit of rewrites: 32 bits
- Background operation (BGO) is not supported (instructions cannot be executed from the code flash memory while rewriting the data flash memory)
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 2.4 to 5.5 V

High-speed on-chip oscillator

- Select from 16 MHz, 8 MHz, 4 MHz, 2 MHz, and 1 MHz
- Frequency accuracy ±1.0%
  (V_{DD} = 2.4 to 5.5 V, T_A = −20 to +85°C)
  (G: Industrial applications, M: Industrial applications)
- Frequency accuracy ±1.5%
  (V_{DD} = 2.4 to 5.5 V, T_A = −40 to −20°C)
  (G: Industrial applications, M: Industrial applications)
- Frequency accuracy ±2.0%
  (V_{DD} = 2.4 to 5.5 V, T_A = +85 to +125°C)
  (G: Industrial applications, M: Industrial applications)
- Frequency accuracy ±2.0%
  (V_{DD} = 2.4 to 5.5 V, T_A = −40 to +85°C)
  (A: Consumer applications)

Operating ambient temperature

- T_A = −40 to +85°C (A: Consumer applications)
- T_A = −40 to +105°C (G: Industrial applications)
- T_A = −40 to +125°C (M: Industrial applications)

Power management and reset function

- On-chip selectable power-on-reset (SPOR) circuit (Select reset from 3 levels, stop setting is available)

Serial interface

- Simplified SPI (CSI[Note 1]): 1 to 2 channels
- UART: 1 channel
- Simplified I^2C: 1 to 2 channels
- I^2C: 1 channel

Note 1. Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Timer

- 16-bit timer: 8 channels
- 12-bit interval timer: 1 channel
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D converter

- 8/10-bit resolution A/D converter (V_{DD} = 2.4 to 5.5 V)
- Analog input: 3 to 11 channels
- Internal reference voltage (0.815 V (TYP.))

Comparator

- 1 to 2 channels
- Operation mode: High-speed mode, low-speed mode
- External reference voltage or internal reference voltage can be selected as the reference voltage.

I/O port

- I/O port: 6 to 18 (N-ch open drain output [withstand voltage of V_{DD}]: 2 to 9)
- Can be set to N-ch open drain and on-chip pull-up resistor
- External interrupt function: 8 channels
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

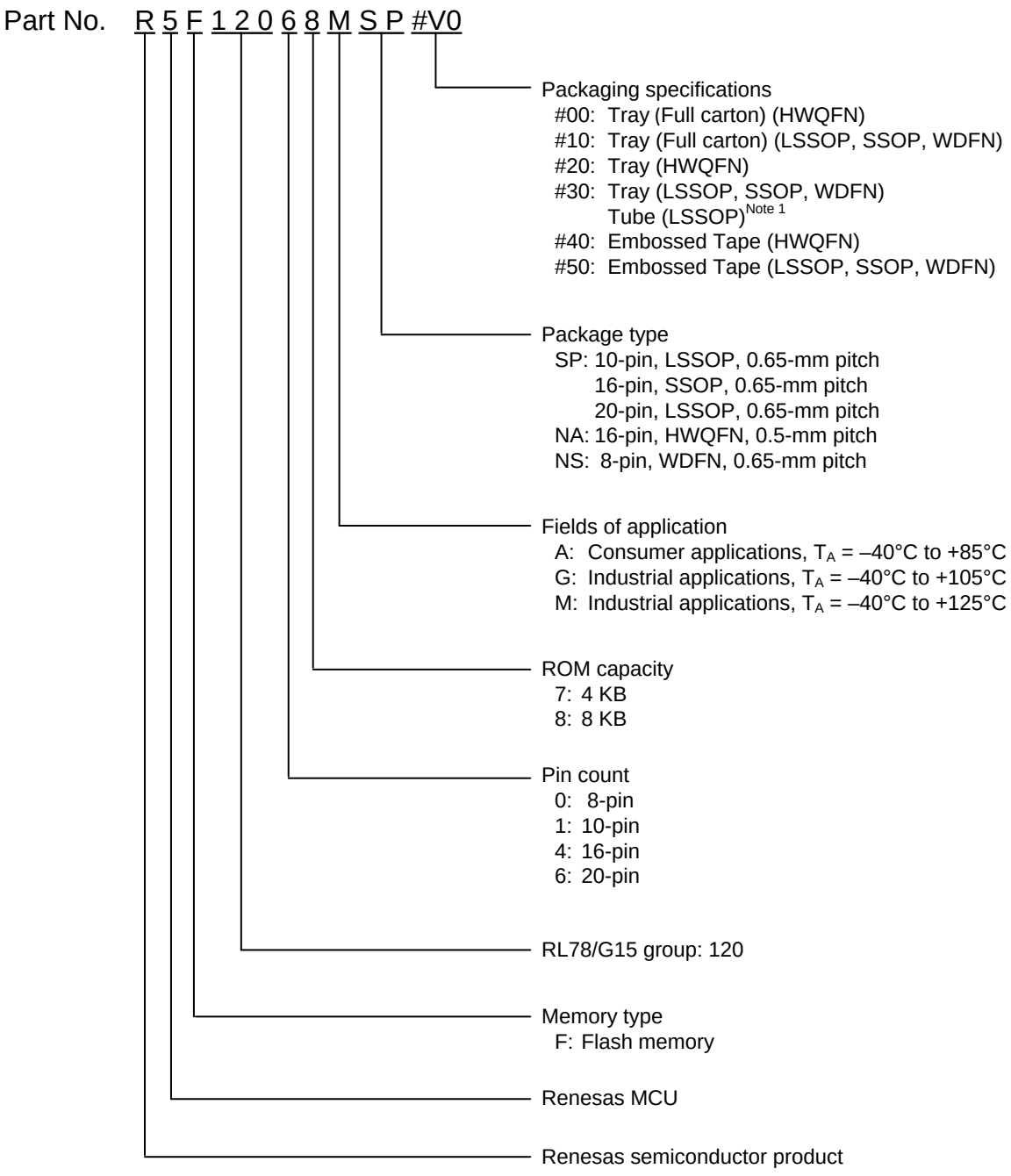
Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G15			
			8 pins	10 pins	16 pins	20 pins
8 KB	1 KB	1 KB	R5F12008	R5F12018	R5F12048	R5F12068
4 KB	1 KB	1 KB	R5F12007	R5F12017	R5F12047	R5F12067

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G15



Note 1. For the 20-pin LSSOP products only, the packaging specification is Tube.

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Fields of Application Note 1	Ordering Part Number		RENESAS Code
			Product Name	Packaging Specifications	
8 pins	8-pin plastic WDFN (3 × 3 mm, 0.65-mm pitch)	A	R5F12008ANS, R5F12007ANS	#10, #30, #50	PWSN0008JG-A
		G	R5F12008GNS, R5F12007GNS		
		M	R5F12008MNS, R5F12007MNS		
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65-mm pitch)	A	R5F12018ASP, R5F12017ASP	#10, #30, #50	PLSP0010JA-A
		G	R5F12018GSP, R5F12017GSP		
		M	R5F12018MSP, R5F12017MSP		
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65-mm pitch)	A	R5F12048ASP, R5F12047ASP	#10, #30, #50	PRSP0016JC-B
		G	R5F12048GSP, R5F12047GSP		
		M	R5F12048MSP, R5F12047MSP		
16 pins	16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)	A	R5F12048ANA, R5F12047ANA	#00, #20, #40	PWQN0016KD-A
		G	R5F12048GNA, R5F12047GNA		
		M	R5F12048MNA, R5F12047MNA		
20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)	A	R5F12068ASP, R5F12067ASP	#30, #50	PLSP0020JB-A
		G	R5F12068GSP, R5F12067GSP		
		M	R5F12068MSP, R5F12067MSP		

Note 1. For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G15**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 8-pin products

- 8-pin plastic WDFN (3 × 3 mm, 0.65-mm pitch)

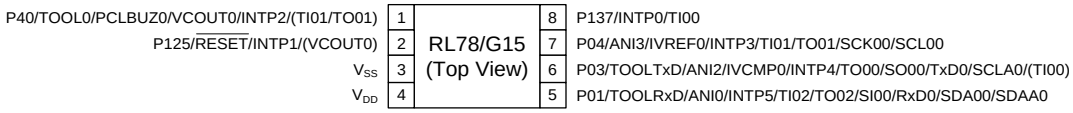


Table 1-2. Multiplexed Functions of 8-pin Products

Pin No.	I/O		Analog		HMI	Timer	Communications Interface	
8WDFN	Digital port	Power supply, system, clock, debug	A/D converter	Comparator	Interrupt function	Timer array unit	Serial array unit	Serial interface IICA
1	P40	TOOL0 PCLBUZ0	—	VCOUT0	INTP2	(TI01/TO01)	—	—
2	P125	$\overline{\text{RESET}}$	—	(VCOUT0)	INTP1	—	—	—
3	—	V_{SS}	—	—	—	—	—	—
4	—	V_{DD}	—	—	—	—	—	—
5	P01	TOOLRxD	ANI0	—	INTP5	TI02/TO02	SI00/RxD0/ SDA00	SDAA0
6	P03	TOOLTxD	ANI2	IVCMP0	INTP4	(TI00) TO00	SO00/TxD0	SCLA0
7	P04	—	ANI3	IVREF0	INTP3	TI01/TO01	SCK00/SCL00	—
8	P137	—	—	—	INTP0	TI00	—	—

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to *Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 3 (PIOR0 to PIOR3)* in *the RL78/G15 User's Manual*.

1.3.2 10-pin products

- 10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65-mm pitch)

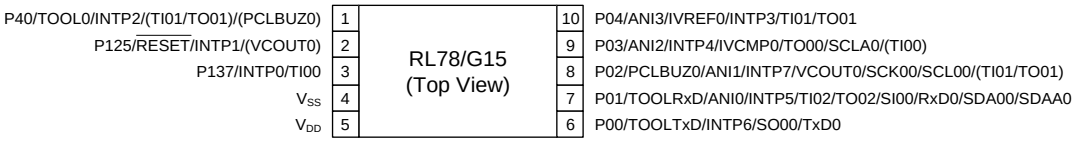


Table 1-3. Multiplexed Functions of 10-pin Products

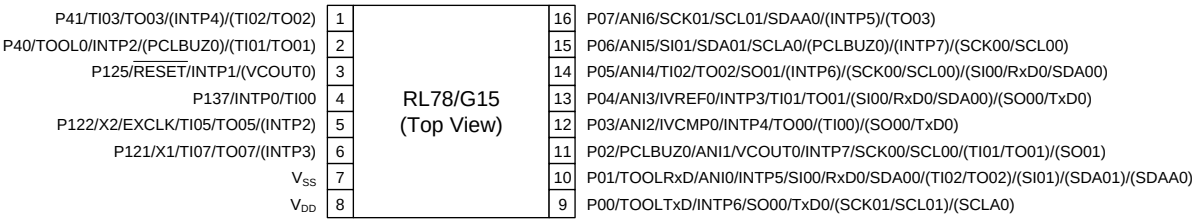
Pin No.	I/O		Analog		HMI	Timer	Communications Interface	
10LSSOP	Digital port	Power supply, system, clock, debug	A/D converter	Comparator	Interrupt function	Timer array unit	Serial array unit	Serial interface IICA
1	P40	TOOL0 (PCLBUZ0)	—	—	INTP2	(TI01/TO01)	—	—
2	P125	$\overline{\text{RESET}}$	—	(VCOUT0)	INTP1	—	—	—
3	P137	—	—	—	INTP0	TI00	—	—
4	—	V_{SS}	—	—	—	—	—	—
5	—	V_{DD}	—	—	—	—	—	—
6	P00	TOOLTxD	—	—	INTP6	—	SO00/TxD0	—
7	P01	TOOLRxD	ANI0	—	INTP5	TI02/TO02	SI00/RxD0/ SDA00	SDAA0
8	P02	PCLBUZ0	ANI1	VCOUT0	INTP7	(TI01/TO01)	SCK00/SCL00	—
9	P03	—	ANI2	IVCMP0	INTP4	(TI00) TO00	—	SCLA0
10	P04	—	ANI3	IVREF0	INTP3	TI01/TO01	—	—

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to *Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 3 (PIOR0 to PIOR3)* in *the RL78/G15 User's Manual*.

1.3.3 16-pin products

- 16-pin plastic SSOP (4.4 × 5.0 mm, 0.65-mm pitch)



- 16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)

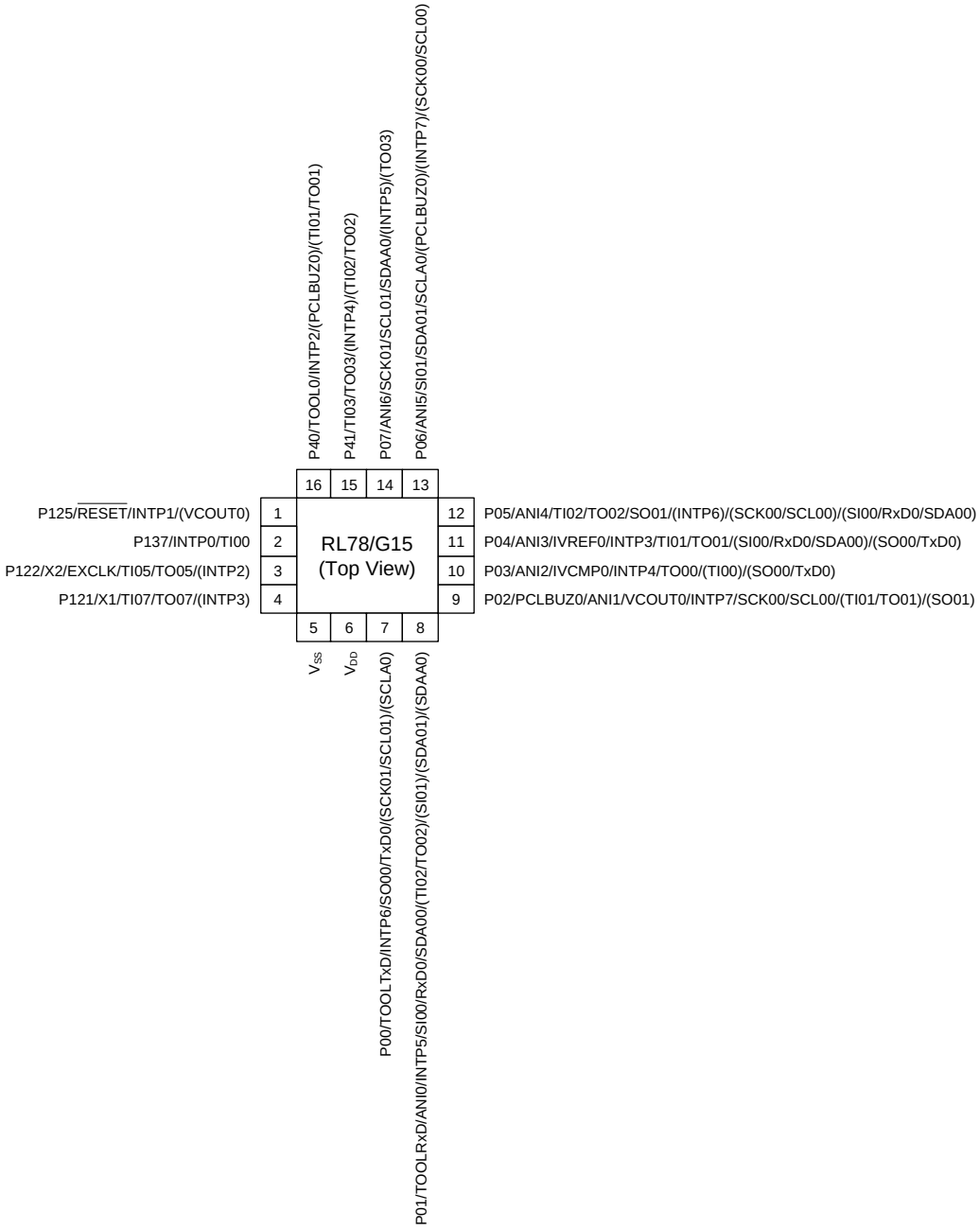


Table 1-4. Multiplexed Functions of 16-pin Products

Pin No.		I/O		Analog		HMI	Timer	Communications Interface	
16SSOP	16HWQFN	Digital port	Power supply, system, clock, debug	A/D converter	Comparator	Interrupt function	Timer array unit	Serial array unit	Serial interface IICA
1	15	P41	—	—	—	(INTP4)	TI03/TO03 (TI02/TO02)	—	—
2	16	P40	TOOL0 (PCLBUZ0)	—	—	INTP2	(TI01/TO01)	—	—
3	1	P125	$\overline{\text{RESET}}$	—	(VCOUT0)	INTP1	—	—	—
4	2	P137	—	—	—	INTP0	TI00	—	—
5	3	P122	X2 EXCLK	—	—	(INTP2)	TI05/TO05	—	—
6	4	P121	X1	—	—	(INTP3)	TI07/TO07	—	—
7	5	—	V_{SS}	—	—	—	—	—	—
8	6	—	V_{DD}	—	—	—	—	—	—
9	7	P00	TOOLTxD	—	—	INTP6	—	SO00/TxD0 (SCK01/SCL01)	(SCLA0)
10	8	P01	TOOLRxD	ANI0	—	INTP5	(TI02/TO02)	SI00/RxD0/ SDA00 (SI01)/(SDA01)	(SDAA0)
11	9	P02	PCLBUZ0	ANI1	VCOUT0	INTP7	(TI01/TO01)	SCK00/SCL00 (SO01)	—
12	10	P03	—	ANI2	IVCMP0	INTP4	(TI00) TO00	(SO00/TxD0)	—
13	11	P04	—	ANI3	IVREF0	INTP3	TI01/TO01	(SI00/RxD0/ SDA00) (SO00/TxD0)	—
14	12	P05	—	ANI4	—	(INTP6)	TI02/TO02	SO01 (SCK00/SCL00) (SI00/RxD0/ SDA00)	—
15	13	P06	(PCLBUZ0)	ANI5	—	(INTP7)	—	SI01/SDA01 (SCK00/SCL00)	SCLA0
16	14	P07	—	ANI6	—	(INTP5)	(TO03)	SCK01/SCL01	SDAA0

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to *Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 3 (PIOR0 to PIOR3)* in *the RL78/G15 User's Manual*.

1.3.4 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)

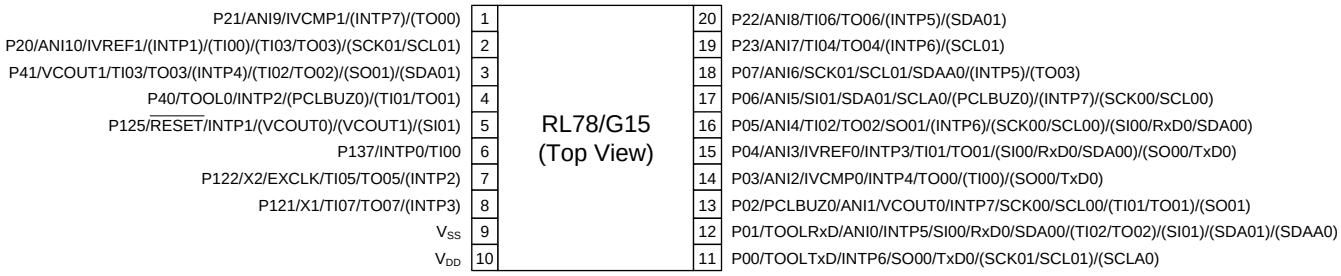


Table 1-5. Multiplexed Functions of 20-pin Products (1/2)

Pin No.	I/O		Analog		HMI	Timer	Communications Interface	
20LSSOP	Digital port	Power supply, system, clock, debug	A/D converter	Comparator	Interrupt function	Timer array unit	Serial array unit	Serial interface IICA
1	P21	—	ANI9	IVCMP1	(INTP7)	(TO00)	—	—
2	P20	—	ANI10	IVREF1	(INTP1)	(TI00) (TI03/TO03)	(SCK01/SCL01)	—
3	P41	—	—	VCOUT1	(INTP4)	TI03/TO03 (TI02/TO02)	(SO01)/(SDA01)	—
4	P40	TOOL0 (PCLBUZ0)	—	—	INTP2	(TI01/TO01)	—	—
5	P125	$\overline{\text{RESET}}$	—	(VCOUT0) (VCOUT1)	INTP1	—	(SI01)	—
6	P137	—	—	—	INTP0	TI00	—	—
7	P122	X2 EXCLK	—	—	(INTP2)	TI05/TO05	—	—
8	P121	X1	—	—	(INTP3)	TI07/TO07	—	—
9		V_{SS}	—	—	—	—	—	—
10		V_{DD}	—	—	—	—	—	—
11	P00	TOOLTxD	—	—	INTP6	—	SO00/TxD0 (SCK01/SCL01)	(SCLA0)
12	P01	TOOLRxD	ANI0	—	INTP5	(TI02/TO02)	SI00/RxD0/SDA00 (SI01)/(SDA01)	(SDAA0)
13	P02	PCLBUZ0	ANI1	VCOUT0	INTP7	(TI01/TO01)	SCK00/SCL00 (SO01)	—
14	P03	—	ANI2	IVCMP0	INTP4	(TI00) TO00	(SO00/TxD0)	—
15	P04	—	ANI3	IVREF0	INTP3	TI01/TO01	(SI00/RxD0/ SDA00) (SO00/TxD0)	—
16	P05	—	ANI4	—	(INTP6)	TI02/TO02	SO01 (SCK00/SCL00) (SI00/RxD0/ SDA00)	—
17	P06	(PCLBUZ0)	ANI5	—	(INTP7)	—	SI01/SDA01 (SCK00/SCL00)	SCLA0
18	P07	—	ANI6	—	(INTP5)	(TO03)	SCK01/SCL01	SDAA0

Table 1-5. Multiplexed Functions of 20-pin Products (2/2)

Pin No.	I/O		Analog		HMI	Timer	Communications Interface	
20LSSOP	Digital port	Power supply, system, clock, debug	A/D converter	Comparator	Interrupt function	Timer array unit	Serial array unit	Serial interface IICA
19	P23	—	ANI7	—	(INTP6)	TI04/TO04	(SCL01)	—
20	P22	—	ANI8	—	(INTP5)	TI06/TO06	(SDA01)	—

Remark 1. For pin identification, see **1.4 Pin Identification**.

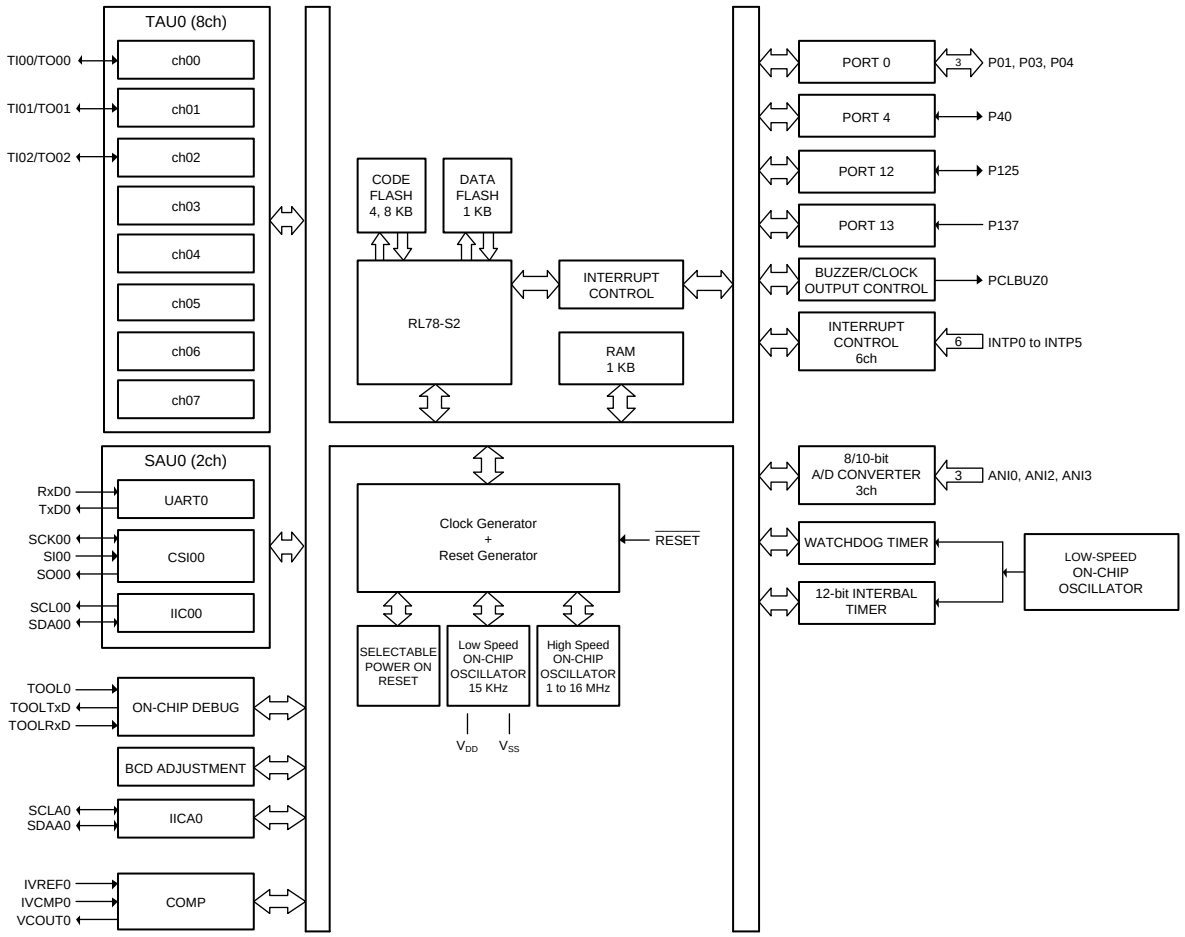
Remark 2. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to *Figure 4-6 Format of Peripheral I/O Redirection Registers 0 to 3 (PIOR0 to PIOR3)* in *the RL78/G15 User's Manual*.

1.4 Pin Identification

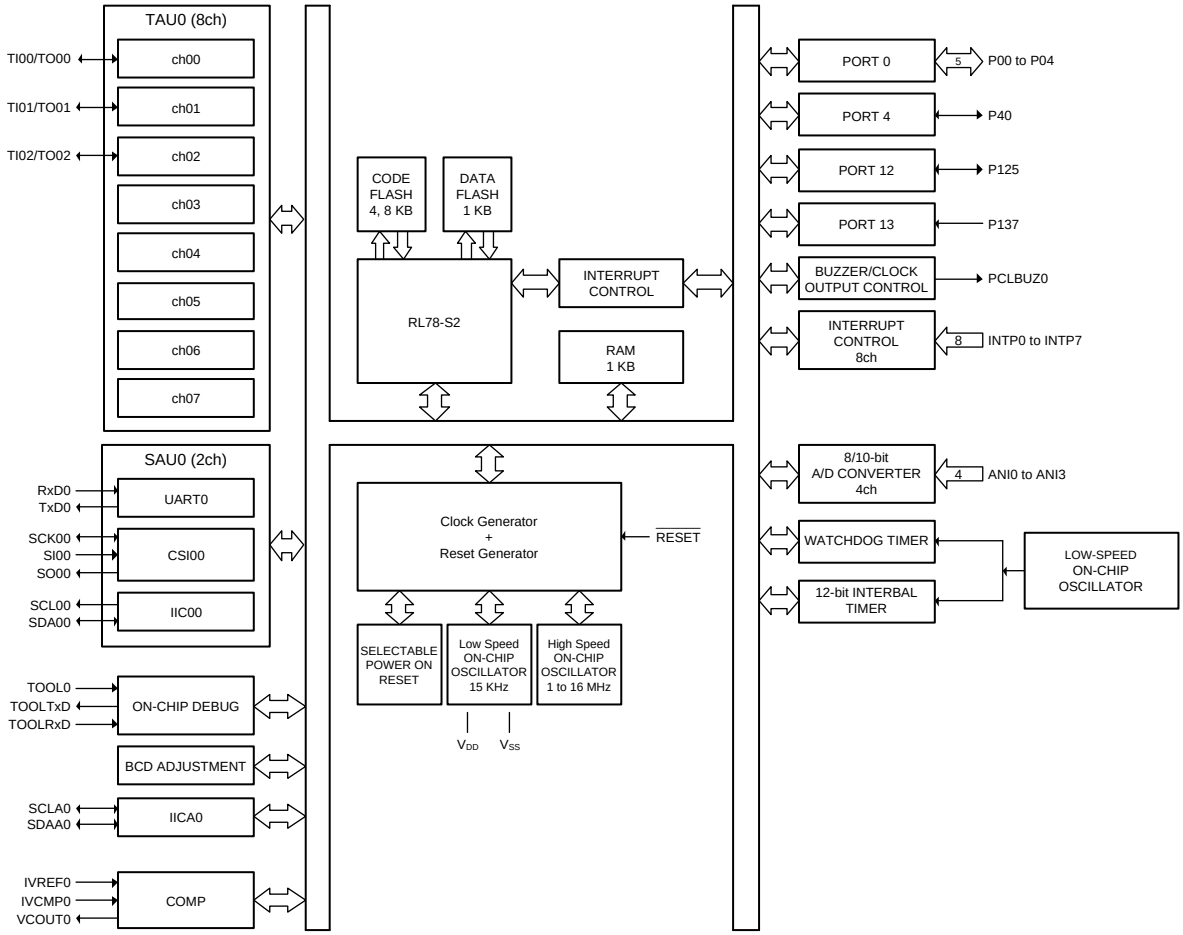
ANI0 to ANI10	: Analog Input
INTP0 to INTP7	: Interrupt Request From Peripherals
P00 to P07	: Port 0
P20 to P23	: Port 2
P40, P41	: Port 4
P121, P122, P125	: Port 12
P137	: Port 13
PCLBUZ0	: Programmable Clock Output/Buzzer Output
EXCLK	: External Clock Input
X1, X2	: Crystal Oscillator (Main System Clock)
IVCMP0, IVCMP1	: Comparator Input
VCOUT0, VCOUT1	: Comparator Output
IVREF0, IVREF1	: Comparator Reference Input
$\overline{\text{RESET}}$	: Reset
RxD0	: Receive Data
SCK00, SCK01	: Serial Clock Input/Output
SCL00, SCL01, SCLA0	: Serial Clock Output
SDA00, SDA01, SDAA0	: Serial Data Input/Output
SI00, SI01	: Serial Data Input
SO00, SO01	: Serial Data Output
TI00 to TI07	: Timer Input
TO00 to TO07	: Timer Output
TOOL0	: Data Input/Output for Tool
TOOLRxD, TOOLTxD	: Data Input/Output for External Device
TxD0	: Transmit Data
V_{DD}	: Power Supply
V_{SS}	: Ground

1.5 Block Diagram

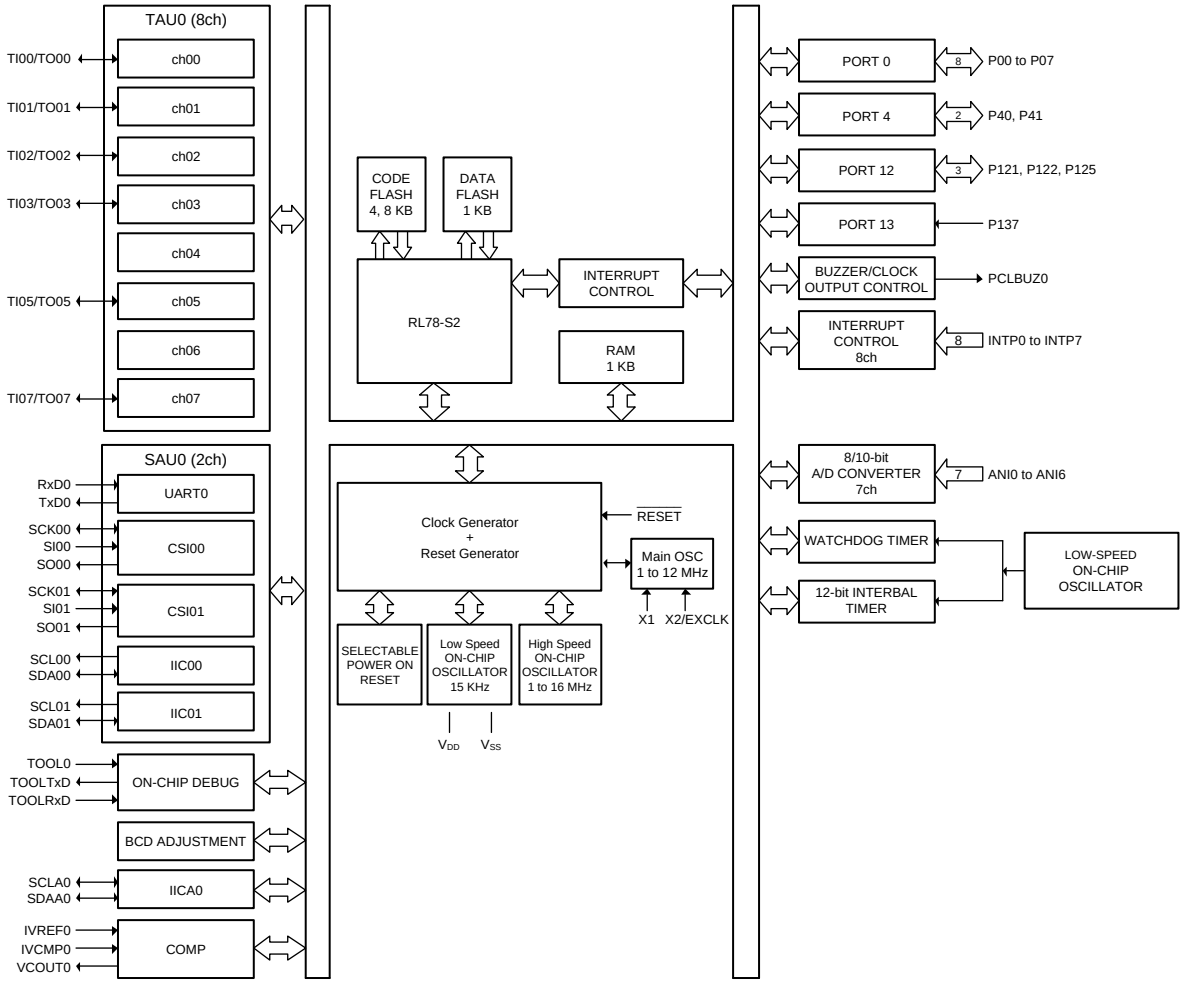
1.5.1 8-pin products



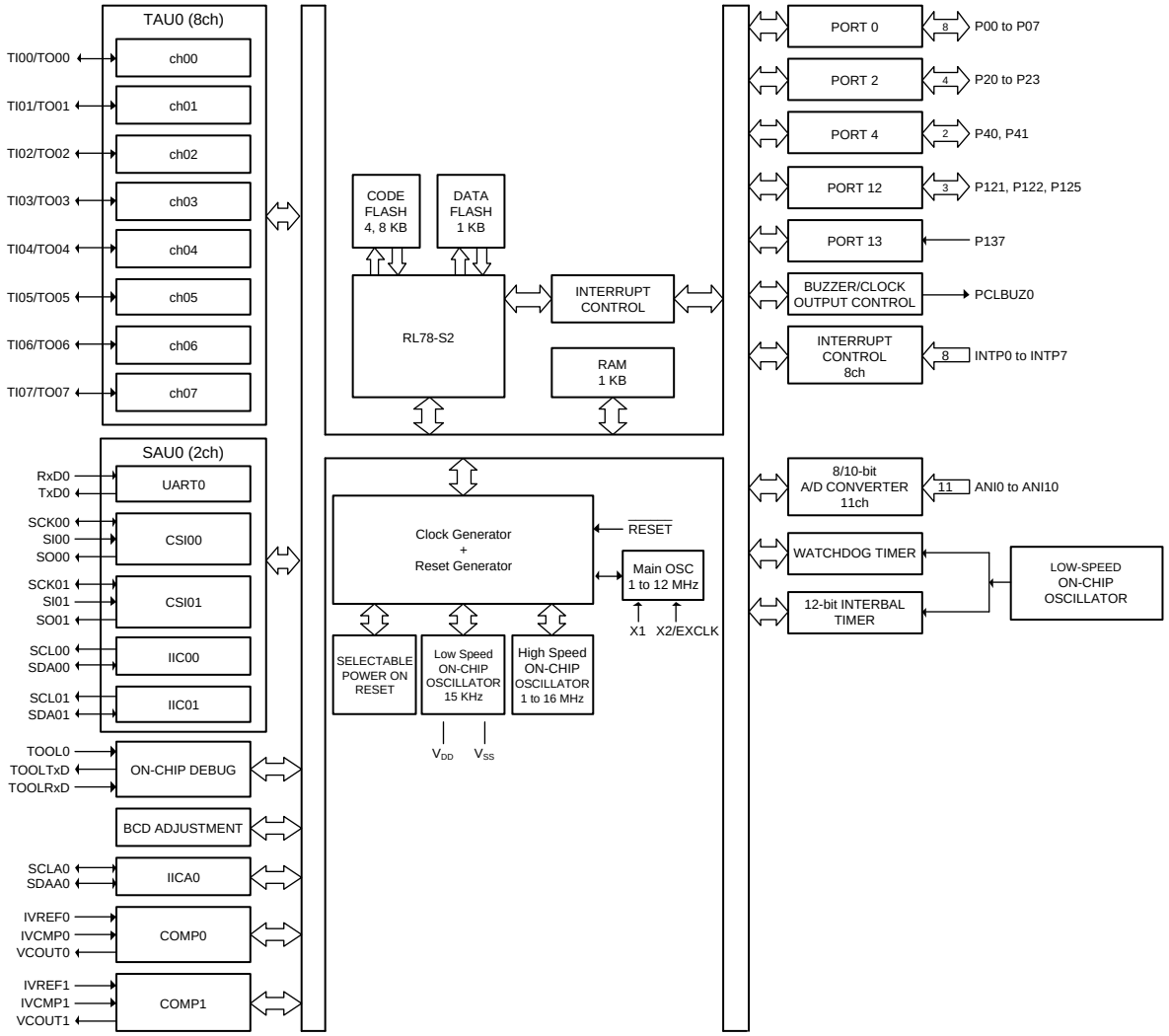
1.5.2 10-pin products



1.5.3 16-pin products



1.5.4 20-pin products



1.6 Outline of Functions

This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		8-pin		10-pin		16-pin		20-pin	
		R5F12007	R5F12008	R5F12017	R5F12018	R5F12047	R5F12048	R5F12067	R5F12068
Code flash memory		4 KB	8 KB	4 KB	8 KB	4 KB	8 KB	4 KB	8 KB
Data flash memory		1 KB							
RAM		1 KB							
Main system clock	High-speed system clock	—		—		X1, X2 (crystal/ceramic) oscillation: 1 to 12 MHz: VDD = 2.4 to 5.5 V External main system clock input (EXCLK): 1 to 16 MHz: VDD = 2.4 to 5.5 V			
	High-speed on-chip oscillator	1 to 16 MHz (VDD = 2.4 to 5.5 V)							
Low-speed on-chip oscillator clock		15 kHz (TYP.)							
General-purpose registers		(8-bit register × 8) × 4 banks							
Minimum instruction execution time		0.0625 μs (16 MHz operation)							
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.							
I/O port	Total	6		8		14		18	
	CMOS I/O	5		7		13		17	
	CMOS input	1							
Timer	16-bit timer	8 channels							
	Watchdog timer	1 channel							
	12-bit interval timer	1 channel							
	Timer output	3 channels (PWM outputs: 2)Note 1		3 channels (PWM outputs: 2)Note 1		6 channels (PWM outputs: 4)Note 1		8 channels (PWM outputs: 7)Note 1	
Clock output/buzzer output		1							
		Up to 10 MHz (peripheral hardware clock: f_{MAIN} = 10 MHz operation)							
Comparator		1 channel		1 channel		1 channel		2 channels	
8/10-bit resolution A/D converter		3 channels		4 channels		7 channels		11 channels	
Serial interface		Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART: 1 channel				Simplified SPI (CSINote 2): 2 channels/simplified I²C: 2 channels/UART: 1 channel			
	I²C bus	1 channel							
Number of Vectored interrupt sources	Internal	8		10		16		19	
	External	6		8		8		8	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by selectable power-on-reset • Internal reset by illegal instruction executionNote 3 • Internal reset by data retention lower limit voltage • Internal reset by illegal-memory access							
Selectable power-on-reset circuit		• Detection voltage Rising edge (V_{SPOR}): 2.25 V/2.68 V/3.02 V/4.45 V (MAX.) Falling edge (V_{SPDR}): 2.20 V/2.62 V/2.96 V/4.37 V (MAX.)							

(2/2)

Item	8-pin		10-pin		16-pin		20-pin	
	R5F12007	R5F12008	R5F12017	R5F12018	R5F12047	R5F12048	R5F12067	R5F12068
On-chip debug function	Provided							
Power supply voltage	V_{DD} = 2.4 to 5.5 V							
Operating ambient temperature	T_A = −40 to +85°C (A: Consumer applications), T_A = −40 to +105°C (G: Industrial applications), T_A = −40 to +125°C (M: Industrial applications)							

Note 1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see *6.9.3 Operation as multiple PWM output function* in *the RL78/G15 User's Manual*).

Note 2. Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Note 3. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.

★ 2. ELECTRICAL SPECIFICATIONS (T_A = −40 to +85°C)

This chapter describes the electrical specifications of A: Consumer applications (T_A = −40 to +85°C).

Caution 1. **The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

Caution 2. **The pins mounted depend on the product. Refer to *2.1 Port Function*, for the port functions, and *2.2.1 Functions for each product*, for the other functions, in *the RL78/G15 User's Manual*.**

★

2.1 Absolute Maximum Ratings

[T_A = 25°C]

Item	Symbol	Condition		Rating	Unit
Supply voltage	V_{DD}			−0.5 to +6.5	V
Input voltage	V_{I1}			−0.3 to V_{DD} + 0.3[Note 1]	V
Output voltage	V_{O1}			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin		−40	mA
		Total of all pins	P20 to P23, P40, P41, P121, P122, P125	−70	mA
		−170mA	P00 to P07	−100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins	P20 to P23, P40, P41, P121, P122, P125	100	mA
		170mA	P00 to P07	100	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note 1. This must be no greater than 6.5 V.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any item. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Remark 2. The reference voltage is V_{SS}.

2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Resonator	Condition	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx)Note 1	Ceramic resonator/ crystal resonator	2.4 V ≤ V_{DD} ≤ 5.5 V	1		12	MHz

Note 1. Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to *5.4 System Clock Oscillator* in *the RL78/G15 User's Manual*.

2.2.2 On-chip oscillator characteristics

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequencyNote 1, Note 2	f_{IH}		1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		T_A = −40 to +85°C	−2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			−15		+15	%

Note 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (00C2H).

Note 2. The listed values only indicate the characteristics of the oscillators. Refer to **2.4 AC Characteristics** for instruction execution time.

★

2.3 DC Characteristics

2.3.1 Pin characteristics

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

(1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00 to P07, P20 to P23, P40, P41, P121, P122, P125				−10.0 Note 2	mA
		Total of P20 to P23, P40, P41, P121, P122, P125 (when duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			−65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−14.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			−10.5	mA
		Total of P00 to P07 (when duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			−65.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−12.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			−9.0	mA
		Total of all pins (when duty ≤ 70% Note 3)				−105.0	mA
Output current, low Note 4	I_{OL1}	Per pin for P00 to P07, P20 to P23, P40, P41, P121, P122, P125				20.0 Note 2	mA
		Total of P20 to P23, P40, P41, P121, P122, P125 (when duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			85.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			21.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			4.2	mA
		Total of P00 to P07 (when duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			85.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			18.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			3.6	mA
		Total of all pins (when duty ≤ 70% Note 3)				145.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the V_{DD} pin to an output pin.

Note 2. The value for maximum total current must not be exceeded.

Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (I_{OH} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OH} = –10.0 mA
  Total output current from the listed pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA
- Total output current from the listed pins = (I_{OL} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OL} = 10.0 mA
  Total output current from the listed pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the V_{SS} pin.

Caution P00, P01, P03 to P07, P22, and P41 do not output high level in N-ch open-drain mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}			0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}			0		0.2 V_{DD}	V
Output voltage, high Note 1	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V	I_{OH} = −10 mA	V_{DD} − 1.5			V
			I_{OH} = −3.0 mA	V_{DD} − 0.7			V
		2.7 V ≤ V_{DD} ≤ 5.5 V	I_{OH} = −2.0 mA	V_{DD} − 0.6			V
		2.4 V ≤ V_{DD} ≤ 5.5 V	I_{OH} = −1.5 mA	V_{DD} − 0.5			V
Output voltage, low Note 2	V_{OL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 20 mA			1.3	V
			I_{OL} = 8.5 mA			0.7	V
		2.7 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 3.0 mA			0.6	V
			I_{OL} = 1.5 mA			0.4	V
		2.4 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 0.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	P00 to P07, P20 to P23, P40, P41, P125, P137 V_I = V_{DD}				1	μA
	I_{LIH2}	P121, P122 (X1, X2, EXCLK) V_I = V_{DD}	In input port or external clock input			1	μA
			In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P20 to P23, P40, P41, P125, P137 V_I = V_{SS}				−1	μA
	I_{LIL2}	P121, P122 (X1, X2, EXCLK) V_I = V_{SS}	In input port or external clock input			−1	μA
			In resonator connection			−10	μA
On-chip pull-up resistance	R_U	V_I = V_{SS}		10	20	100	kΩ

Note 1. The value under the condition which satisfies the high-level output current (I_{OH1}).

Note 2. The value under the condition which satisfies the low-level output current (I_{OL1}).

Caution The maximum value of V_{IH} of P00, P01, P03 to P07, P22, and P41 is V_{DD} even in N-ch open-drain mode. These pins do not output high level in N-ch open-drain mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.3.2 Supply current characteristics

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		0.87		mA
			Normal operation	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		1.86	2.47	mA
				f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		1.17	1.64	mA
				f_{EX} = 16 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		1.69	2.30	mA
				f_X = 12 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Resonator connection		1.57	2.30	mA
				f_{MX} = 4 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		1.00	1.46	mA
					Resonator connection		1.05	1.53	mA
	I_{DD2}[Note 2]	HALT mode		f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		371	800	µA
				f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		334	630	µA
				f_{EX} = 16 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		207	636	µA
				f_X = 12 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Resonator connection		309	894	µA
				f_{MX} = 4 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		156	452	µA
					Resonator connection		207	599	µA
	I_{DD3}[Note 3]	STOP mode		V_{DD} = 3.0 V			0.62	2.25	µA

★ Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
Regarding the values for main system clock operation, the TYP. value does not include the peripheral operating current. The MAX. value includes the peripheral operating current, but does not include those flowing into the A/D converter, comparator, I/O port, and on-chip pull-up/pull-down resistors.
Regarding the values for subsystem clock operation, the TYP. and MAX. values do not include the peripheral operating current. However, in HALT mode, the current flowing into the RTC is included.
Regarding the values in STOP mode, the TYP. and MAX. values do not include the peripheral operating current.

Note 2. When the HALT instruction is executed from the flash memory.

Note 3. The listed currents do not include the current flowing into the 12-bit interval timer and watchdog timer.

Note 4. When the high-speed subsystem clock is stopped.

Note 5. When the high-speed on-chip oscillator is stopped.

Note 6. 16-pin and 20-pin products only.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 3. The temperature condition of the TYP. value is T_A = 25°C.

Peripheral Functions

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.30		µA
12-bit interval timer operating current	I_{TMKA} Note 1, Note 2, Note 3				0.02		µA
Watchdog timer operating current	I_{WDT} Note 1, Note 4				0.02		µA
A/D converter operating current	I_{ADC} Note 1, Note 5	In conversion at maximum speed	V_{DD} = 5.0 V		1.30	1.90	mA
			V_{DD} = 3.0 V		0.50		mA
Comparator operating current	I_{CMP} Note 1, Note 6	In high-speed mode	V_{DD} = 5.0 V		6.50		µA
		In low-speed mode	V_{DD} = 5.0 V		1.70		µA
Internal reference voltage operating current	I_{VREG} Note 1				10		µA
Self-programming operating current	I_{FSP} Note 1, Note 7				2.0	12.20	mA

Note 1. The current flowing into V_{DD}.

Note 2. When the high-speed on-chip oscillator and high-speed system clock are stopped.

Note 3. This current only flows into the 12-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{TMKA} when the 12-bit interval timer is in operation.

Note 4. This current only flows into the watchdog timer. It does not include the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{WDT} when the watchdog timer is in operation.

Note 5. This current only flows into the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter is operating or in the HALT mode.

Note 6. This current only flows into a single comparator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator is in operation.

Note 7. This current only flows during self-programming.

Remark The temperature condition of the TYP. value is T_A = 25°C.

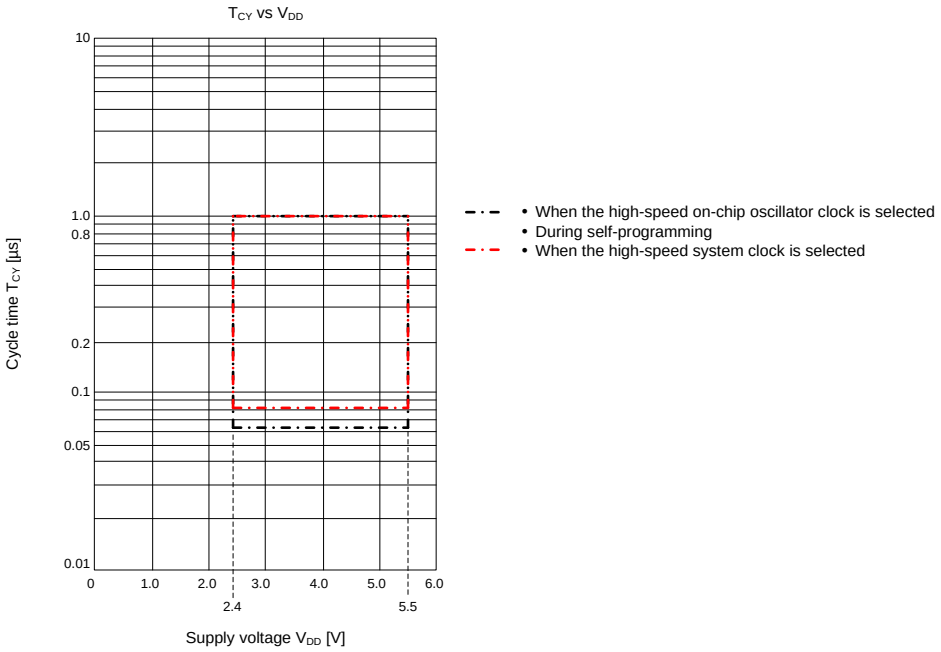
2.4 AC Characteristics

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

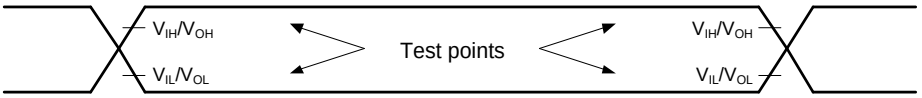
Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	When high-speed on-chip oscillator clock (f_{IH}) is selected	2.4 V ≤ V_{DD} ≤ 5.5 V		0.0625		1.0	µs
		When high-speed system clock (f_{MX}) is selected	2.4 V ≤ V_{DD} ≤ 5.5 V	Square wave input	0.0625		1.0	µs
				Resonator connection	0.0833		1.0	µs
		In the self-programming mode	2.4 V ≤ V_{DD} ≤ 5.5 V		0.0625		1.0	µs
External system clock frequency	f_{EX}	2.4 V ≤ V_{DD} ≤ 5.5 V			1.0		16	MHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.4 V ≤ V_{DD} ≤ 5.5 V			30			ns
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}	Noise filter is not used			1/f_{MCK} + 10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V					8	MHz
		2.7 V ≤ V_{DD} < 4.0 V					5	MHz
		2.4 V ≤ V_{DD} < 2.7 V					4	MHz
PCLBUZ0 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V					10	MHz
		2.7 V ≤ V_{DD} < 4.0 V					5	MHz
		2.4 V ≤ V_{DD} < 2.7 V					4	MHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			µs

Remark f_{MCK}: Timer array unit operating clock frequency
(Operation clock to be set by timer clock select register 0 (TPS0) and the CKS0n1 bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7).)

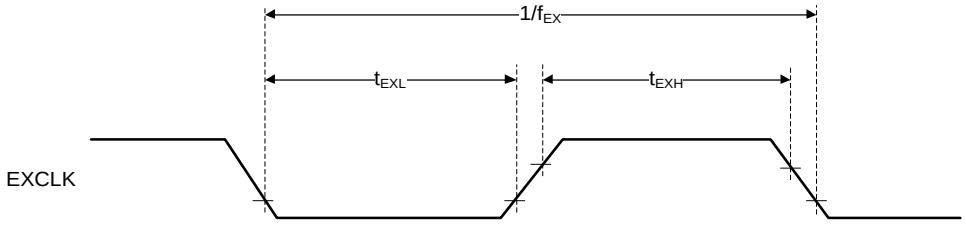
Minimum Instruction Execution Time during Main System Clock Operation



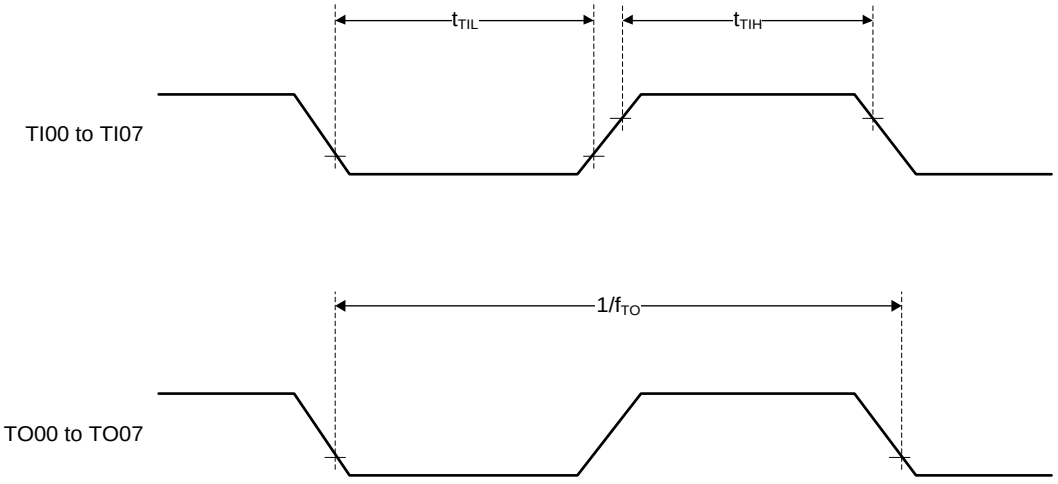
At AC Timing



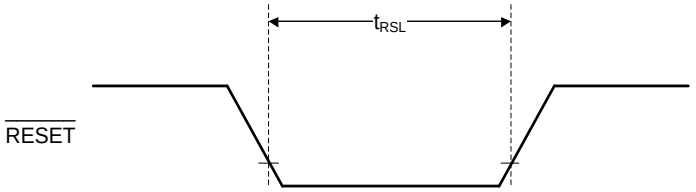
External System Clock Timing



TI/TO Timing

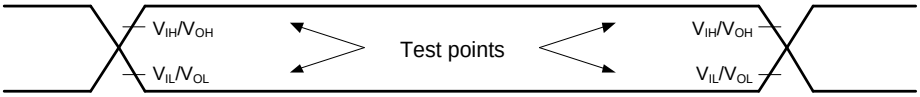


$\overline{\text{RESET}}$ Input Timing



2.5 Serial Interface Characteristics

AC Timing Test Points



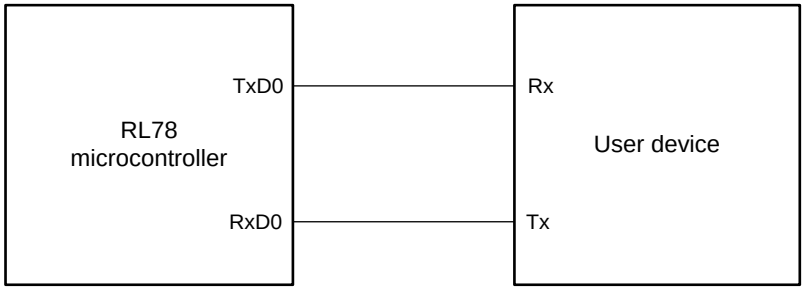
2.5.1 Serial array unit

(1) UART mode

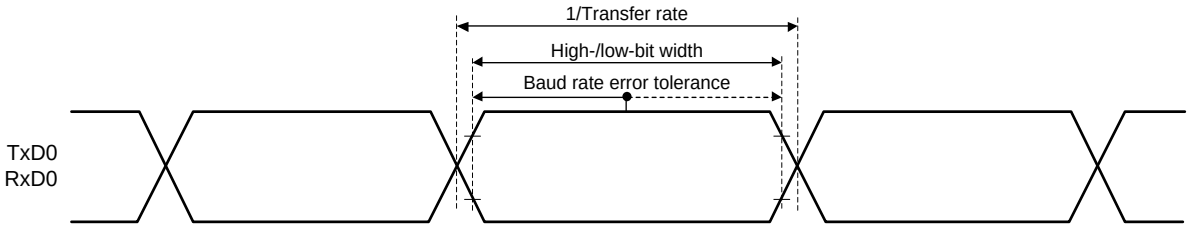
[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 16 MHz			2.6	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by serial clock select register 0 (SPS0) and the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0, 1))

(2) Simplified SPI (CSI) mode (master mode, SCKp... internal clock output)

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.4 V ≤ V_{DD} ≤ 5.5 V	250			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2$ − 18			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2$ − 38			ns
SIp setup time (to SCKp ↑)[Note 1]	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		47			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75			ns
SIp hold time (from SCKp ↑)[Note 1]	t_{KSI1}			19			ns
Delay time from SCKp ↓ to SOp output[Note 2]	t_{KSO1}	C = 30 pF[Note 3]				25	ns

Note 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes “to SCKp ↓” and the SIp hold time becomes “from SCKp ↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

Note 2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes “from SCKp ↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

(3) Simplified SPI (CSI) mode (slave mode, SCKp... external clock input)

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V		$6/f_{MCK}$			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		$6/f_{MCK}$ and also 500			ns
SCKp high-/low-level width	t_{KH2},t_{KL2}	2.4 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY2}/2$ − 18			ns
SIp setup time (to SCKp ↑)[Note 1]	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ + 20			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ + 30			ns
SIp hold time (from SCKp ↑)[Note 1]	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ + 31			ns
Delay time from SCKp ↓ to SOp output[Note 2]	t_{KSO2}	C = 30 pF[Note 3]	2.7 V ≤ V_{DD} ≤ 5.5 V			$2/f_{MCK}$ + 50	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V			$2/f_{MCK}$ + 75	ns

Note 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes “to SCKp ↓” and the SIp hold time becomes “from SCKp ↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

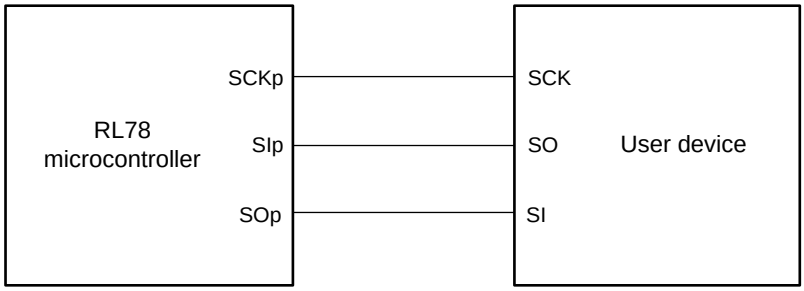
Note 2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes “from SCKp ↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

Note 3. C is the load capacitance of the SOp output lines.

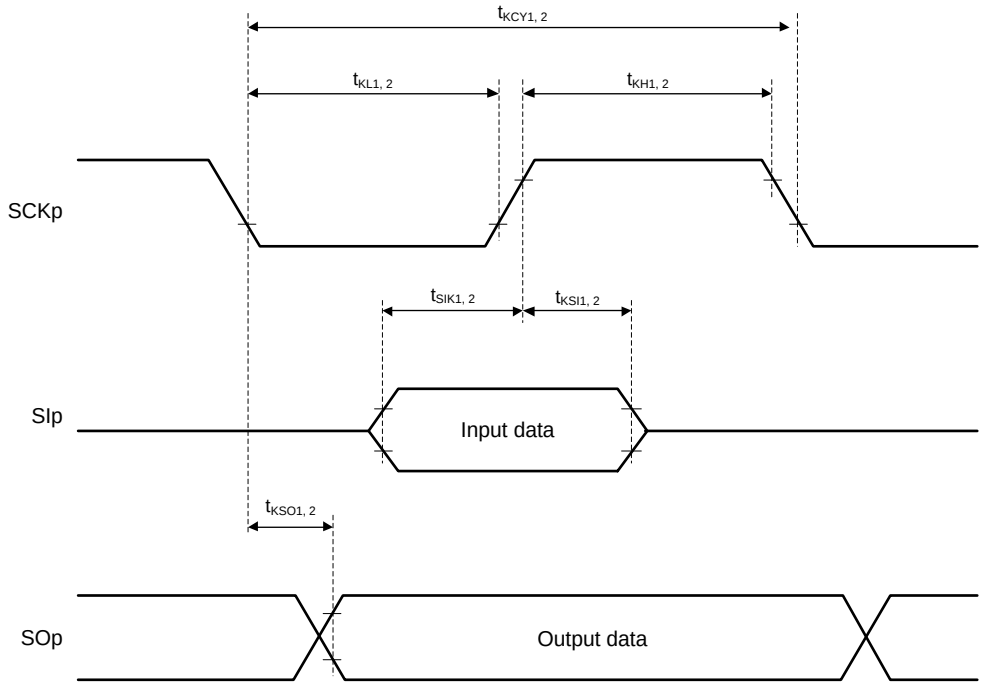
Remark 1. p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by serial clock select register 0 (SPS0) and the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0, 1))

Simplified SPI (CSI) mode connection diagram



Simplified SPI (CSI) mode serial transfer timing
(When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1)



Remark p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

(4) Simplified I²C mode

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

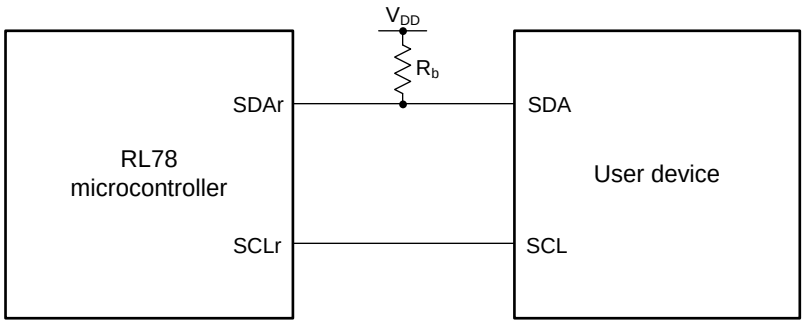
Item	Symbol	Condition	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	C_b = 100 pF, R_b = 3 kΩ	1150		ns
Hold time when SCLr = “H”	t_{HIGH}	C_b = 100 pF, R_b = 3 kΩ	1150		ns
Data setup time (reception)	$t_{SU:DAT}$	C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	C_b = 100 pF, R_b = 3 kΩ	0	355	ns

Note 1. The value must also be no greater than $f_{MCK}/4$.

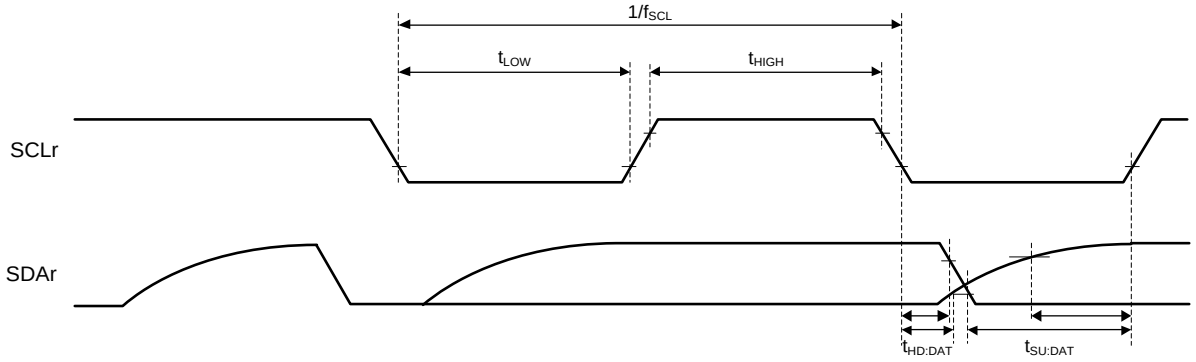
Note 2. Set f_{MCK} so that it will not exceed the hold time when SCLr = “L” or SCLr = “H”.

Caution Select the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin by using port output mode register 0, 2, or 4 (POM0, 2, or 4).

Simplified I²C mode connection diagram



Simplified I^2C mode serial transfer timing



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SCLr, SDAr) load capacitance

Remark 2. r: IIC number (r = 00, 01)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by serial clock select register 0 (SPS0) and the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0, 1))

2.5.2 Serial interface IICA

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	Standard Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz			0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		0.6		µs
Hold time[Note 1]	$t_{HD:STA}$		4.0		0.6		µs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		µs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		µs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		µs
Bus-free time	t_{BUF}		4.7		1.3		µs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

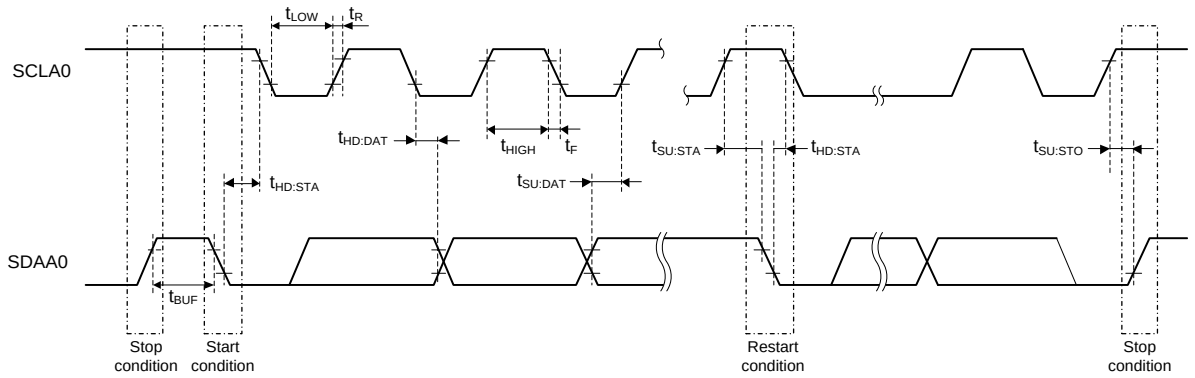
Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ applies to normal transfer and a wait is inserted at the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistance) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 200 pF, R_b = 1.7 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Targets: ANI0 to ANI10, internal reference voltage

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1, Note 2, Note 3	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1	LSB
			V_{DD} = 3 V		±2.3	±4.5	LSB
Conversion time	t_{CONV}	10-bit resolution Targets: ANI0 to ANI10	2.7 V ≤ V_{DD} ≤ 5.5 V	4.25		17	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V Note 5	5.75		23	μs
		10-bit resolution Target: Internal reference voltage Note 6	2.4 V ≤ V_{DD} ≤ 5.5 V	5.75		23	μs
Zero-scale error Note 1, Note 2, Note 3, Note 4	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19	%FSR
			V_{DD} = 3 V			±0.39	%FSR
Full-scale error Note 1, Note 2, Note 3, Note 4	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29	%FSR
			V_{DD} = 3 V			±0.42	%FSR
Integral linearity error Note 1, Note 2, Note 3	ILE	10-bit resolution	V_{DD} = 5 V			±1.8	LSB
			V_{DD} = 3 V			±1.7	LSB
Differential linearity error Note 1, Note 2, Note 3	DLE	10-bit resolution	V_{DD} = 5 V			±1.4	LSB
			V_{DD} = 3 V			±1.5	LSB
Analog input voltage	V_{AIN}	Targets: ANI0 to ANI10		0		V_{DD}	V
		Target: Internal reference voltage Note 6		V_{REG} Note 7			V

Note 1. The TYP. value is an average value at T_A = 25°C. The MAX. value is an average value ±3σ at normal distribution.

Note 2. These values are the results of characteristic evaluation and are not checked for shipment.

Note 3. A quantization error (±1/2 LSB) is not included.

Note 4. Expressed as a ratio (%FSR) relative to the full-scale value.

Note 5. Be sure to set the LV0 bit in A/D converter mode register 0 (ADM0) to 0 when conversion is done in the operating voltage range of 2.4 V ≤ V_{DD} < 2.7 V.

Note 6. Be sure to set the LV0 bit in A/D converter mode register 0 (ADM0) to 0 when the internal reference voltage is selected as the target for conversion.

Note 7. Refer to **2.6.3 Internal reference voltage characteristics**.

Caution 1. Arrange wiring and insert the capacitor so that no noise appears on the power supply/ground line.

Caution 2. Do not allow any pulses that rapidly change such as digital signals to be input/output to/from the pins adjacent to the conversion pin during A/D conversion.

Caution 3. Note that the internal reference voltage cannot be used as the reference voltage of the comparator when the internal reference voltage is selected as the target for A/D conversion.

2.6.2 Comparator characteristics

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage range	I_{VREF}	IVREFn pin input (CnVRF bit = 0)		0		V_{DD} − 1.4	V
		Internal reference voltage (CnVRF bit = 1) Note 1		V_{REG} Note 2			V
	I_{VCMP}	IVCMPn pin input		−0.3		V_{DD} + 0.3	V
Output delay	t_d	V_{DD} = 3.0 V, input slew rate > 50 mV/μs	High-speed mode			0.5	μs
			Low-speed mode		2.0		μs
Operation stabilization wait time	t_{CMP}			100			μs

Note 1. When the internal reference voltage is selected as the reference voltage of the comparator, the internal reference voltage cannot be used as the target for A/D conversion.

Note 2. Refer to **2.6.3 Internal reference voltage characteristics**.

Remark n: Channel number (n = 0, 1)

2.6.3 Internal reference voltage characteristics

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V_{REG}		0.74	0.815	0.89	V
Operation stabilization wait time	t_{AMP}	A/D converter is used (ADS register = 0DH)	5			μs

Caution The internal reference voltage cannot be simultaneously used by the A/D converter and the comparator; only one of them must be selected.

2.6.4 SPOR circuit characteristics

[T_A = −40 to +85°C, V_{SS} = 0 V]

Item		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	Power supply rising	4.08	4.28	4.45	V
		V_{SPDR0}	Power supply falling	4.00	4.20	4.37	V
		V_{SPOR1}	Power supply rising	2.76	2.90	3.02	V
		V_{SPDR1}	Power supply falling	2.70	2.84	2.96	V
		V_{SPOR2}	Power supply rising	2.44	2.57	2.68	V
		V_{SPDR2}	Power supply falling	2.40	2.52	2.62	V
		V_{SPOR3}	Power supply rising		2.16		V
		V_{SPDR3}	Power supply falling		2.11		V
Minimum pulse width[Note 1]		T_{SPW}		300			µs

Note 1. Time required for the reset operation by the SPOR circuit when V_{DD} falls below V_{SPDR}.

Caution Make sure to keep the internal reset state by the SPOR or an external reset until the power supply voltage (V_{DD}) reaches the operating voltage range shown in 2.4 AC Characteristics.

2.6.5 Power supply voltage rising slope characteristics

[T_A = −40 to +85°C, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

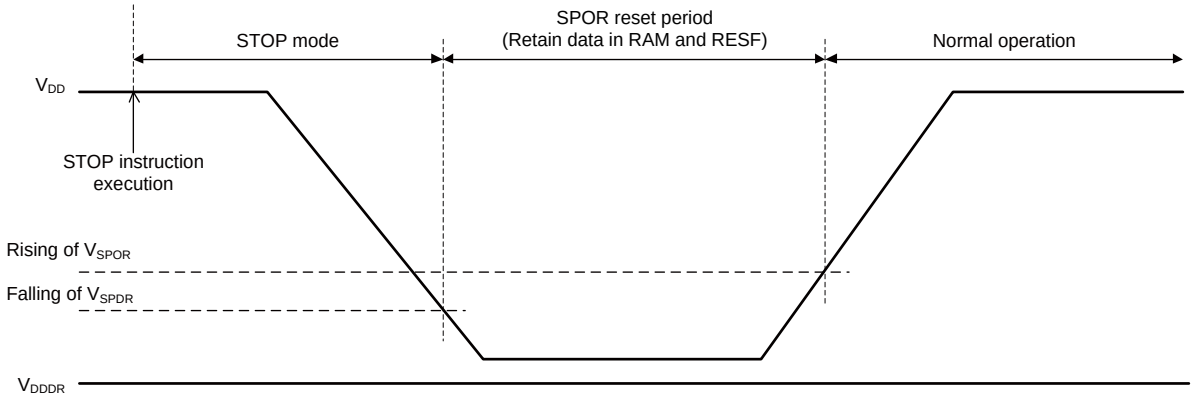
Caution Make sure to keep the internal reset state by the SPOR or an external reset until the power supply voltage (V_{DD}) reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

[T_A = −40 to +85°C, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.9		5.5	V

Caution Data in RAM is retained until the power supply voltage falls below the MIN. value of the data retention power supply voltage (V_{DDDR}). Note that data in the RESF register might not be cleared even if the power supply voltage falls below the MIN. value of the data retention power supply voltage (V_{DDDR}).



2.8 Flash Memory Programming Characteristics

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Number of code flash rewrites Note 1, Note 2	C_{erwr}	Retained for 20 years	T_A = +85°C	1000			Times
Number of data flash rewrites Note 1, Note 2		Retained for 1 year	T_A = +25°C		1,000,000		Times
		Retained for 5 years	T_A = +85°C	100,000			Times
		Retained for 20 years	T_A = +85°C	10,000			Times

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics.

Code flash/data flash self-programming time

★ **[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]**

Item	Symbol	f_{CLK} = 1 MHz			f_{CLK} = 16 MHz			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Writing (4 bytes)	t_{P4}		104	905		53.8	504.9	µs
Block erasure (1 KB)	t_{E1K}		7.9	262.3		5.5	214.1	ms

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2.9 Dedicated Flash Memory Programmer Communication (UART)

[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

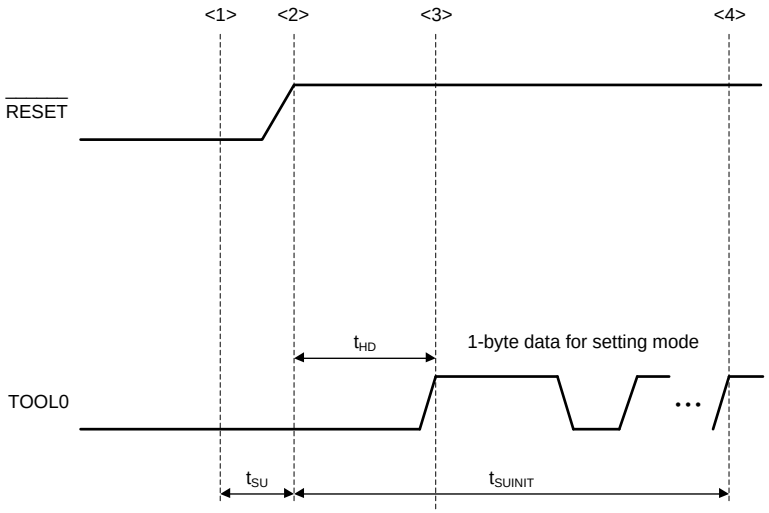
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate				115,200		bps

Remark The transfer rate during flash memory programming is fixed to 115,200 bps.

2.10 Timing of Entry to Flash Memory Programming Mode

★ **[T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	The SPOR reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	The SPOR reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released	t_{HD}	The SPOR reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (the SPOR reset must have been released before that).

<3> The TOOL0 pin is released from the low level.

<4> Setting of entry to the flash memory programming mode by UART reception is completed.

Remark t_{SUINIT}: During this period, the communications for the initial setting must be completed within 100 ms after release from the reset.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released

★ 3. ELECTRICAL SPECIFICATIONS (T_A = −40 to +105°C, T_A = −40 to +125°C)

This chapter describes the electrical specifications of the following target products.

Target product G: Industrial applications T_A = −40 to +105°C

Target product M: Industrial applications T_A = −40 to +125°C

Caution 1. **The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

Caution 2. **The pins mounted depend on the product. Refer to *2.1 Port Function*, for the port functions, and *2.2.1 Functions for each product*, for the other functions, in *the RL78/G15 User's Manual*.**

★

3.1 Absolute Maximum Ratings

[T_A = 25°C]

Item	Symbol	Condition		Rating	Unit
Supply voltage	V_{DD}			−0.5 to +6.5	V
Input voltage	V_{I1}			−0.3 to V_{DD} + 0.3[Note 1]	V
Output voltage	V_{O1}			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin		−40	mA
		Total of all pins	P20 to P23, P40, P41, P121, P122, P125	−70	mA
		−170mA	P00 to P07	−100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins	P20 to P23, P40, P41, P121, P122, P125	100	mA
		170mA	P00 to P07	100	mA
Operating ambient temperature	T_A	G products		−40 to +105	°C
		M products		−40 to +125	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note 1. This must be no greater than 6.5 V.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any item. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Remark 2. The reference voltage is V_{SS}.

3.2 Oscillator Characteristics

3.2.1 X1 oscillator characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Resonator	Condition	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx)Note 1	Ceramic resonator/ crystal resonator	2.4 V ≤ V_{DD} ≤ 5.5 V	1		12	MHz

Note 1. Indicates only permissible oscillator frequency ranges. Refer to **3.4 AC Characteristics** for instruction execution time. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to *5.4 System Clock Oscillator* in *the RL78/G15 User's Manual*.

3.2.2 On-chip oscillator characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequencyNote 1, Note 2	f_{IH}		1		16	MHz
★ High-speed on-chip oscillator clock frequency accuracy		T_A = +85 to +125°C	−1.5		+1.5	%
		T_A = −20 to +85°C	−1.0		+1.0	%
		T_A = −40 to −20°C	−1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			−15		+15	%

Note 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (00C2H).

Note 2. The listed values only indicate the characteristics of the oscillators. Refer to **3.4 AC Characteristics** for instruction execution time.

★

3.3 DC Characteristics

3.3.1 Pin characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

(1/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P07, P20 to P23, P40, P41, P121, P122, P125					−3.0[Note 2]	mA
		Total of P20 to P23, P40, P41, P121, P122, P125 (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V				−25.0	mA
			2.4 V ≤ V_{DD} < 4.0 V				−7.0	mA
		Total of P00 to P07 (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V				−24.0	mA
			2.4 V ≤ V_{DD} < 4.0 V				−6.0	mA
		Total of all pins (when duty ≤ 70%[Note 3])					−40.0	mA
Output current, low[Note 4]	I_{OL1}	Per pin for P00 to P07, P20 to P23, P40, P41, P121, P122, P125					8.5[Note 2]	mA
		Total of P20 to P23, P40, P41, P121, P122, P125 (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V	T_A = −40 to +105°C			50.0	mA
				T_A = −40 to +125°C			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V				10.5	mA
			2.4 V ≤ V_{DD} < 2.7 V				4.2	mA
		Total of P00 to P07 (when duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V	T_A = −40 to +105°C			50.0	mA
				T_A = −40 to +125°C			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V				9.0	mA
			2.4 V ≤ V_{DD} < 2.7 V				3.6	mA
		Total of all pins (when duty ≤ 70%[Note 3])		T_A = −40 to +105°C			80.0	mA
				T_A = −40 to +125°C			60.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the V_{DD} pin to an output pin.

Note 2. The value for maximum total current must not be exceeded.

Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (I_{OH} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OH} = –10.0 mA
  Total output current from the listed pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA
- Total output current from the listed pins = (I_{OL} × 0.7)/(n × 0.01)
  Example when n = 80% and I_{OL} = 10.0 mA
  Total output current from the listed pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the V_{SS} pin.

Caution P00, P01, P03 to P07, P22, and P41 do not output high level in N-ch open-drain mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}			0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}			0		0.2 V_{DD}	V
Output voltage, high Note 1	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V	I_{OH} = −3.0 mA	V_{DD} − 0.7			V
		2.4 V ≤ V_{DD} ≤ 5.5 V	I_{OH} = −1.0 mA	V_{DD} − 0.5			V
Output voltage, low Note 2	V_{OL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 8.5 mA			0.7	V
		2.7 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 1.5 mA			0.5	V
		2.4 V ≤ V_{DD} ≤ 5.5 V	I_{OL} = 0.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	P00 to P07, P20 to P23, P40, P41, P125, P137 V_I=V_{DD}				1	µA
	I_{LIH2}	P121, P122 (X1, X2, EXCLK) V_I = V_{DD}	In input port or external clock input			1	µA
			In resonator connection			10	µA
Input leakage current, low	I_{LIL1}	P00 to P07, P20 to P23, P40, P41, P125, P137 V_I = V_{SS}				−1	µA
	I_{LIL2}	P121, P122 (X1, X2, EXCLK) V_I = V_{SS}	In input port or external clock input			−1	µA
			In resonator connection			−10	µA
On-chip pull-up resistance	R_U	V_I = V_{SS}		10	20	100	kΩ

Note 1. The value under the condition which satisfies the high-level output current (I_{OH1}).

Note 2. The value under the condition which satisfies the low-level output current (I_{OL1}).

Caution The maximum value of V_{IH} of P00, P01, P03 to P07, P22, and P41 is V_{DD} even in N-ch open-drain mode. These pins do not output high level in N-ch open-drain mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

3.3.2 Supply current characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		0.87		mA
			Normal operation	f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		1.86	2.49	mA
				f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		1.17	1.65	mA
				f_{EX} = 16 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		1.69	2.32	mA
				f_X = 12 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Resonator connection		1.57	2.32	mA
				f_{MX} = 4 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		1.00	1.47	mA
					Resonator connection		1.05	1.55	mA
	I_{DD2}[Note 2]	HALT mode		f_{IH} = 16 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		371	811	µA
				f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V, 5.0 V		334	637	µA
				f_{EX} = 16 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		207	647	µA
				f_X = 12 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Resonator connection		309	909	µA
				f_{MX} = 4 MHz[Note 5, Note 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		156	459	µA
					Resonator connection		207	609	µA
	I_{DD3}[Note 3]	STOP mode		V_{DD} = 3.0 V	T_A = +105°C		0.62	3.71	µA
					T_A = +125°C		0.62	7.44	µA

★ Note 1. The listed currents are the total currents flowing into V_{DD}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
Regarding the values for main system clock operation, the TYP. value does not include the peripheral operating current. The MAX. value includes the peripheral operating current, but does not include those flowing into the A/D converter, comparator, I/O port, and on-chip pull-up/pull-down resistors.
Regarding the values for subsystem clock operation, the TYP. and MAX. values do not include the peripheral operating current. However, in HALT mode, the current flowing into the RTC is included.
Regarding the values in STOP mode, the TYP. and MAX. values do not include the peripheral operating current.

Note 2. When the HALT instruction is executed from the flash memory.

Note 3. The listed currents do not include the current flowing into the 12-bit interval timer and watchdog timer.

Note 4. When the high-speed subsystem clock is stopped.

Note 5. When the high-speed on-chip oscillator is stopped.

Note 6. 16-pin and 20-pin products only.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 3. The temperature condition of the TYP. value is T_A = 25°C.

Peripheral Functions

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.30		µA
12-bit interval timer operating current	I_{TMKA} Note 1, Note 2, Note 3				0.02		µA
Watchdog timer operating current	I_{WDT} Note 1, Note 4				0.02		µA
A/D converter operating current	I_{ADC} Note 1, Note 5	In conversion at maximum speed	V_{DD} = 5.0 V		1.30	1.90	mA
			V_{DD} = 3.0 V		0.50		mA
Comparator operating current	I_{CMP} Note 1, Note 6	In high-speed mode	V_{DD} = 5.0 V		6.50		µA
		In low-speed mode	V_{DD} = 5.0 V		1.70		µA
Internal reference voltage operating current	I_{VREG} Note 1				10		µA
Self-programming operating current	I_{FSP} Note 1, Note 7				2.0	12.20	mA

Note 1. The current flowing into V_{DD}.

Note 2. When the high-speed on-chip oscillator and high-speed system clock are stopped.

Note 3. This current only flows into the 12-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{TMKA} when the 12-bit interval timer is in operation.

Note 4. This current only flows into the watchdog timer. It does not include the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{WDT} when the watchdog timer is in operation.

Note 5. This current only flows into the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter is operating or in the HALT mode.

Note 6. This current only flows into a single comparator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator is in operation.

Note 7. This current only flows during self-programming.

Remark The temperature condition of the TYP. value is T_A = 25°C.

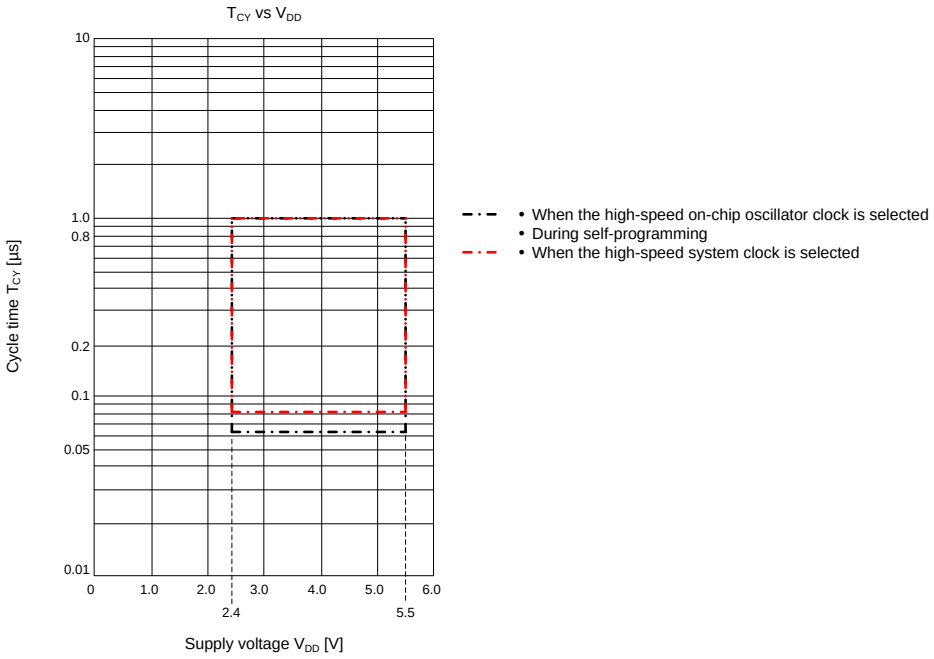
3.4 AC Characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

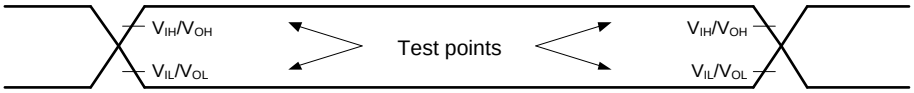
Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	When high-speed on-chip oscillator clock (f_{IH}) is selected	2.4 V ≤ V_{DD} ≤ 5.5 V		0.0625		1.0	µs
		When high-speed system clock (f_{MX}) is selected	2.4 V ≤ V_{DD} ≤ 5.5 V	Square wave input	0.0625		1.0	µs
				Resonator connection	0.0833		1.0	µs
		In the self-programming mode	2.4 V ≤ V_{DD} ≤ 5.5 V		0.0625		1.0	µs
External system clock frequency	f_{EX}	2.4 V ≤ V_{DD} ≤ 5.5 V			1.0		16	MHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.4 V ≤ V_{DD} ≤ 5.5 V			30			ns
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}	Noise filter is not used			1/f_{MCK} + 10			ns
TO00 to TO07 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V					8	MHz
		2.7 V ≤ V_{DD} < 4.0 V					5	MHz
		2.4 V ≤ V_{DD} < 2.7 V					4	MHz
PCLBUZ0 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V					10	MHz
		2.7 V ≤ V_{DD} < 4.0 V					5	MHz
		2.4 V ≤ V_{DD} < 2.7 V					4	MHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			µs

Remark f_{MCK}: Timer array unit operating clock frequency
(Operation clock to be set by timer clock select register 0 (TPS0) and the CKS0n1 bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7).)

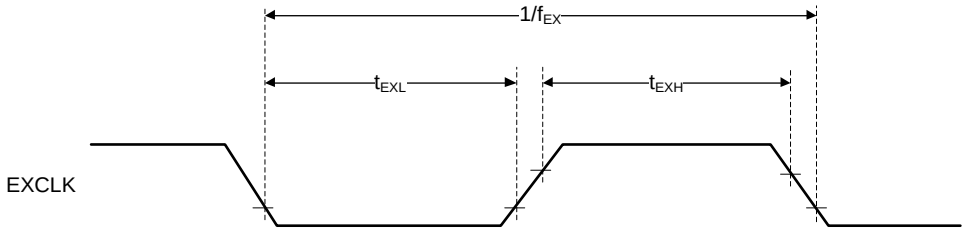
Minimum Instruction Execution Time during Main System Clock Operation



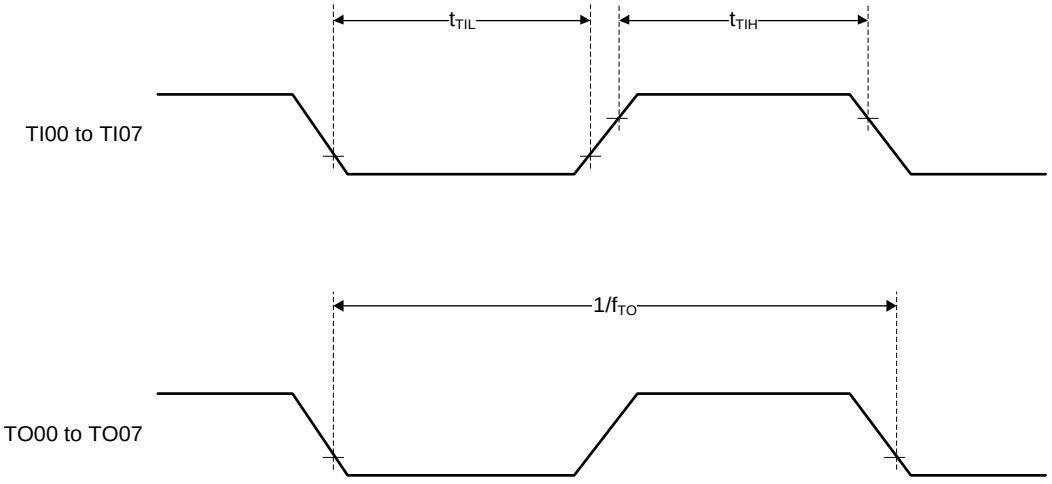
At AC Timing



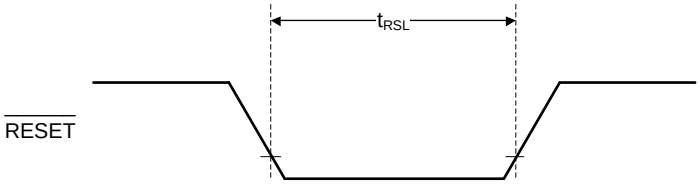
External System Clock Timing



TI/TO Timing

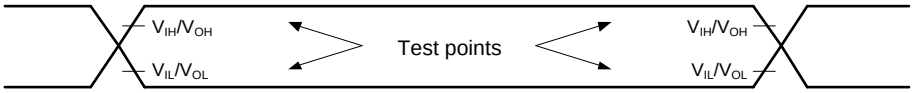


$\overline{\text{RESET}}$ Input Timing



3.5 Serial Interface Characteristics

AC Timing Test Points



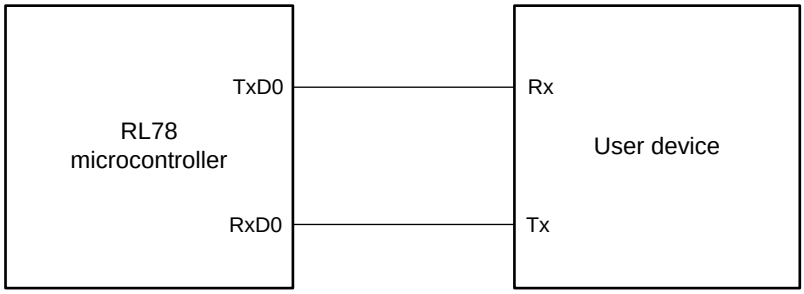
3.5.1 Serial array unit

(1) UART mode

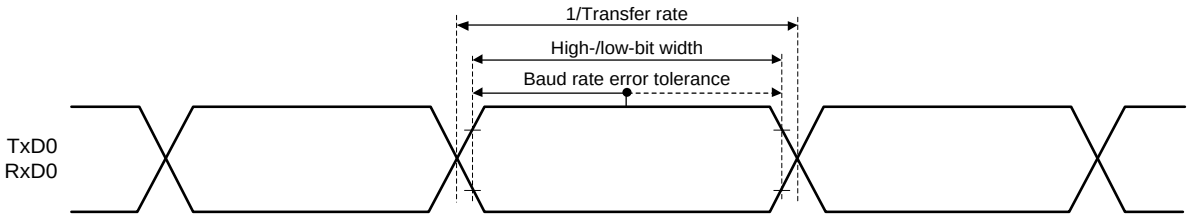
[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/12	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 16 MHz			1.3	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by serial clock select register 0 (SPS0) and the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0, 1))

(2) Simplified SPI (CSI) mode (master mode, SCKp... internal clock output)

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	250			ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	500			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 36$			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 76$			ns
SIp setup time (to SCKp ↑)[Note 1]	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		66			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		113			ns
SIp hold time (from SCKp ↑)[Note 1]	t_{KSI1}			38			ns
Delay time from SCKp ↓ to SOp output[Note 2]	t_{KSO1}	C = 30 pF[Note 3]				66	ns

Note 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes “to SCKp ↓” and the SIp hold time becomes “from SCKp ↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

Note 2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes “from SCKp ↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

(3) Simplified SPI (CSI) mode (slave mode, SCKp... external clock input)

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V		$12/f_{MCK}$			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		$12/f_{MCK}$ and also 1000			ns
SCKp high-/low-level width	t_{KH2},t_{KL2}	2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY2}/2 - 16$			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY2}/2 - 36$			ns
SIp setup time (to SCKp ↑)[Note 1]	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ + 40			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ + 60			ns
SIp hold time (from SCKp ↑)[Note 1]	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ + 62			ns
Delay time from SCKp ↓ to SOp output[Note 2]	t_{KSO2}	C = 30 pF[Note 3]	2.7 V ≤ V_{DD} ≤ 5.5 V			$2/f_{MCK}$ + 66	ns
			2.4V ≤ V_{DD} ≤ 5.5V			$2/f_{MCK}$ + 113	ns

Note 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes “to SCKp ↓” and the SIp hold time becomes “from SCKp ↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

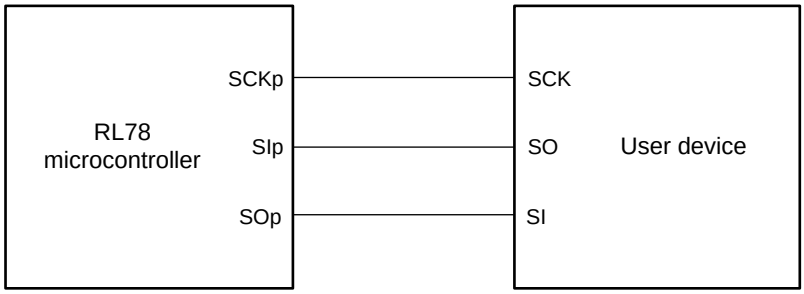
Note 2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes “from SCKp ↓” when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

Note 3. C is the load capacitance of the SOp output lines.

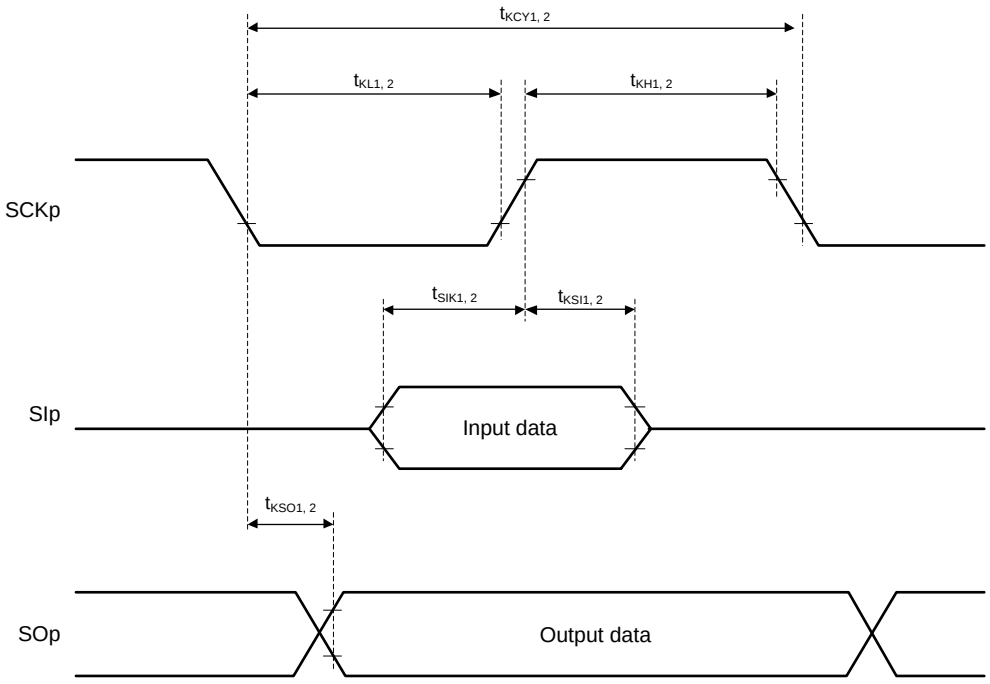
Remark 1. p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by serial clock select register 0 (SPS0) and the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0, 1))

Simplified SPI (CSI) mode connection diagram



Simplified SPI (CSI) mode serial transfer timing
(When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1)



Remark p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

(4) Simplified I²C mode

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

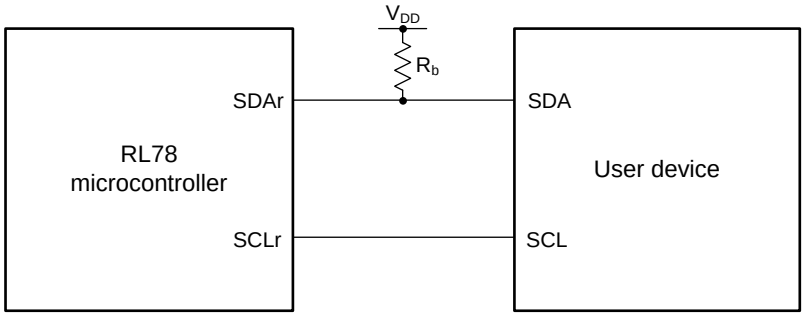
Item	Symbol	Condition	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ		400[Note 1]	kHz
		2.4 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ		100[Note 1]	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	1200		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	1200		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 220[Note 2]		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 580[Note 2]		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	0	770	ns
		2.4 V ≤ V_{DD} ≤ 5.5 V C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Note 1. The value must also be no greater than f_{MCK}/4.

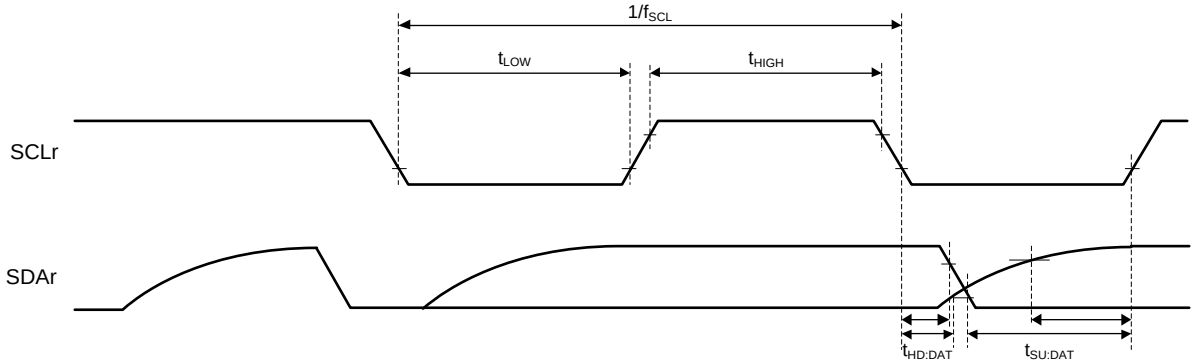
Note 2. Set f_{MCK} so that it will not exceed the hold time when SCLr = “L” or SCLr = “H”.

Caution Select the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin by using port output mode register 0, 2, or 4 (POM0, 2, or 4).

Simplified I²C mode connection diagram



Simplified I^2C mode serial transfer timing



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SCLr, SDAr) load capacitance

Remark 2. r: IIC number (r = 00, 01)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by serial clock select register 0 (SPS0) and the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0, 1))

3.5.2 Serial interface IICA

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	Standard Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz			0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100			kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		0.6		µs
Hold time[Note 1]	$t_{HD:STA}$		4.0		0.6		µs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		µs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		µs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		µs
Bus-free time	t_{BUF}		4.7		1.3		µs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

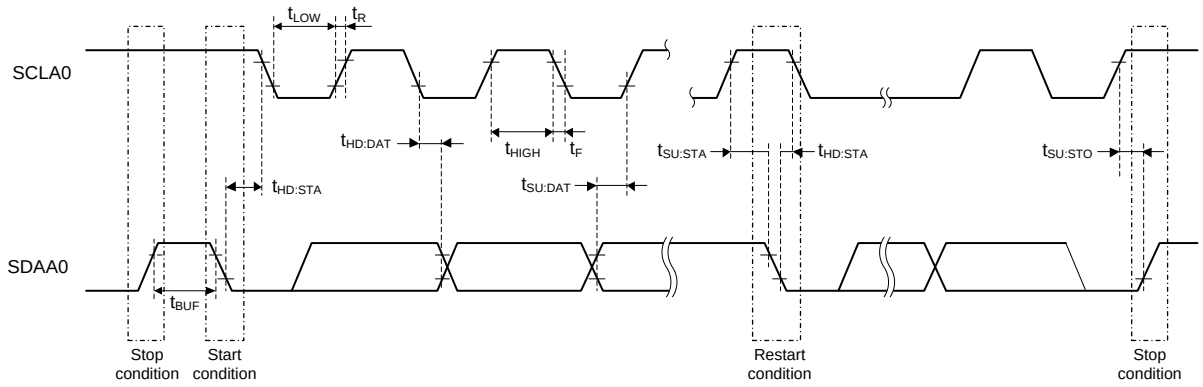
Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ applies to normal transfer and a wait is inserted at the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistance) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 200 pF, R_b = 1.7 kΩ

IICA serial transfer timing



3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Targets: ANI0 to ANI10, internal reference voltage

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1, Note 2, Note 3	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1	LSB
			V_{DD} = 3 V		±2.3	±4.5	LSB
Conversion time	t_{CONV}	10-bit resolution Targets: ANI0 to ANI10	2.7 V ≤ V_{DD} ≤ 5.5 V	4.25		17	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V Note 5	5.75		23	μs
		10-bit resolution Target: Internal reference voltage Note 6	2.4 V ≤ V_{DD} ≤ 5.5 V	5.75		23	μs
Zero-scale error Note 1, Note 2, Note 3, Note 4	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19	%FSR
			V_{DD} = 3 V			±0.39	%FSR
Full-scale error Note 1, Note 2, Note 3, Note 4	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29	%FSR
			V_{DD} = 3 V			±0.42	%FSR
Integral linearity error Note 1, Note 2, Note 3	ILE	10-bit resolution	V_{DD} = 5 V			±1.8	LSB
			V_{DD} = 3 V			±1.7	LSB
Differential linearity error Note 1, Note 2, Note 3	DLE	10-bit resolution	V_{DD} = 5 V			±1.4	LSB
			V_{DD} = 3 V			±1.5	LSB
Analog input voltage	V_{AIN}	Targets: ANI0 to ANI10		0		V_{DD}	V
		Target: Internal reference voltage Note 6		V_{REG} Note 7			V

Note 1. The TYP. value is an average value at T_A = 25°C. The MAX. value is an average value ±3σ at normal distribution.

Note 2. These values are the results of characteristic evaluation and are not checked for shipment.

Note 3. A quantization error (±1/2 LSB) is not included.

Note 4. Expressed as a ratio (%FSR) relative to the full-scale value.

Note 5. Be sure to set the LV0 bit in A/D converter mode register 0 (ADM0) to 0 when conversion is done in the operating voltage range of 2.4 V ≤ V_{DD} < 2.7 V.

Note 6. Be sure to set the LV0 bit in A/D converter mode register 0 (ADM0) to 0 when the internal reference voltage is selected as the target for conversion.

Note 7. Refer to **3.6.3 Internal reference voltage characteristics**.

Caution 1. Arrange wiring and insert the capacitor so that no noise appears on the power supply/ground line.

Caution 2. Do not allow any pulses that rapidly change such as digital signals to be input/output to/from the pins adjacent to the conversion pin during A/D conversion.

Caution 3. Note that the internal reference voltage cannot be used as the reference voltage of the comparator when the internal reference voltage is selected as the target for A/D conversion.

3.6.2 Comparator characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage range	I_{VREF}	IVREFn pin input (CnVRF bit = 0)		0		V_{DD} − 1.4	V
		Internal reference voltage (CnVRF bit = 1) Note 1		V_{REG} Note 2			V
	I_{VCMP}	IVCMPn pin input		−0.3		V_{DD} + 0.3	V
Output delay	t_d	V_{DD} = 3.0 V, input slew rate > 50 mV/μs	High-speed mode			0.5	μs
			Low-speed mode		2.0		μs
Operation stabilization wait time	t_{CMP}			100			μs

Note 1. When the internal reference voltage is selected as the reference voltage of the comparator, the internal reference voltage cannot be used as the target for A/D conversion.

Note 2. Refer to **3.6.3 Internal reference voltage characteristics.**

Remark n: Channel number (n = 0, 1)

3.6.3 Internal reference voltage characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V_{REG}		0.74	0.815	0.89	V
Operation stabilization wait time	t_{AMP}	A/D converter is used (ADS register = 0DH)	5			μs

Caution The internal reference voltage cannot be simultaneously used by the A/D converter and the comparator; only one of them must be selected.

3.6.4 SPOR circuit characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, V_{SS} = 0 V]

Item		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	Power supply rising	4.08	4.28	4.45	V
		V_{SPDR0}	Power supply falling	4.00	4.20	4.37	V
		V_{SPOR1}	Power supply rising	2.76	2.90	3.02	V
		V_{SPDR1}	Power supply falling	2.70	2.84	2.96	V
		V_{SPOR2}	Power supply rising	2.44	2.57	2.68	V
		V_{SPDR2}	Power supply falling	2.40	2.52	2.62	V
		V_{SPOR3}	Power supply rising		2.16		V
		V_{SPDR3}	Power supply falling		2.11		V
Minimum pulse width[Note 1]		T_{SPW}		300			µs

Note 1. Time required for the reset operation by the SPOR circuit when V_{DD} falls below V_{SPDR}.

Caution Make sure to keep the internal reset state by the SPOR or an external reset until the power supply voltage (V_{DD}) reaches the operating voltage range shown in 3.4 AC Characteristics.

3.6.5 Power supply voltage rising slope characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

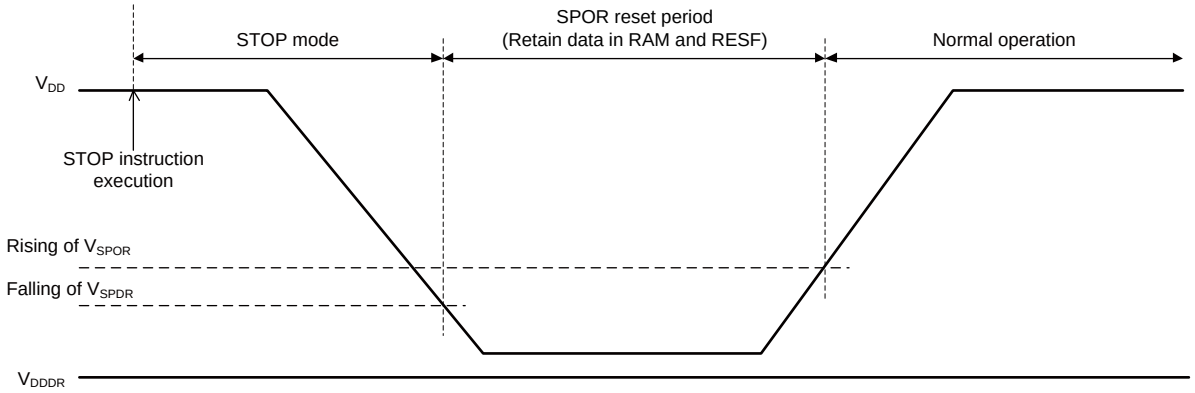
Caution Make sure to keep the internal reset state by the SPOR or an external reset until the power supply voltage (V_{DD}) reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 RAM Data Retention Characteristics

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, V_{SS} = 0 V]

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.9		5.5	V

Caution Data in RAM is retained until the power supply voltage falls below the MIN. value of the data retention power supply voltage (V_{DDDR}). Note that data in the RESF register might not be cleared even if the power supply voltage falls below the MIN. value of the data retention power supply voltage (V_{DDDR}).



3.8 Flash Memory Programming Characteristics

★ **[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]**

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Number of code flash rewrites Note 1, Note 2	C_{erwr}	Retained for 20 years	T_A = +85°C Note 3	1000			Times
Number of data flash rewrites Note 1, Note 2		Retained for 1 year	T_A = +25°C		1,000,000		Times
		Retained for 5 years	T_A = +85°C Note 3	100,000			Times
		Retained for 20 years	T_A = +85°C Note 3	10,000			Times

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics.

★ Note 3. This temperature is the average value at which data are retained.

Code flash/data flash self-programming time

★ **[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]**

Item	Symbol	f_{CLK} = 1 MHz			f_{CLK} = 16 MHz			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Writing (4 bytes)	t_{P4}		104	905		53.8	504.9	µs
Block erasure (1 KB)	t_{E1K}		7.9	262.3		5.5	214.1	ms

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

3.9 Dedicated Flash Memory Programmer Communication (UART)

[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]

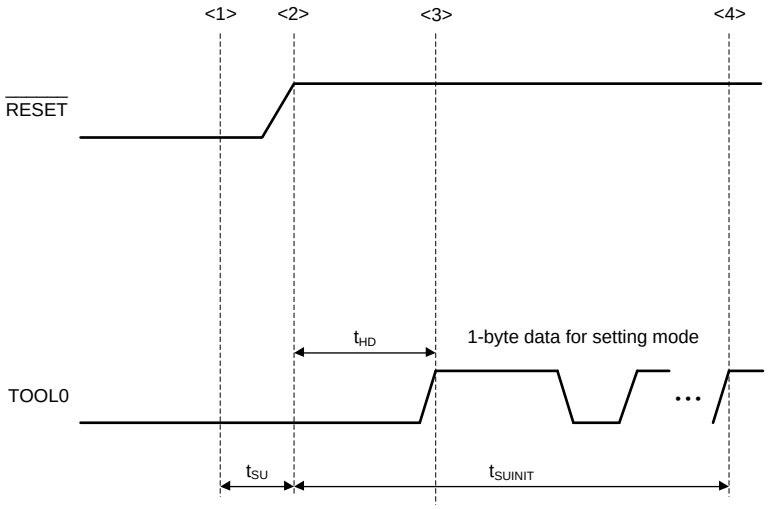
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate				115,200		bps

Remark The transfer rate during flash memory programming is fixed to 115,200 bps.

3.10 Timing of Entry to Flash Memory Programming Mode

★ **[T_A = −40 to +105°C: G products, T_A = −40 to +125°C: M products, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V]**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	The SPOR reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	The SPOR reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released	t_{HD}	The SPOR reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (the SPOR reset must have been released before that).

<3> The TOOL0 pin is released from the low level.

<4> Setting of entry to the flash memory programming mode by UART reception is completed.

Remark t_{SUINIT}: During this period, the communications for the initial setting must be completed within 100 ms after release from the reset.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released

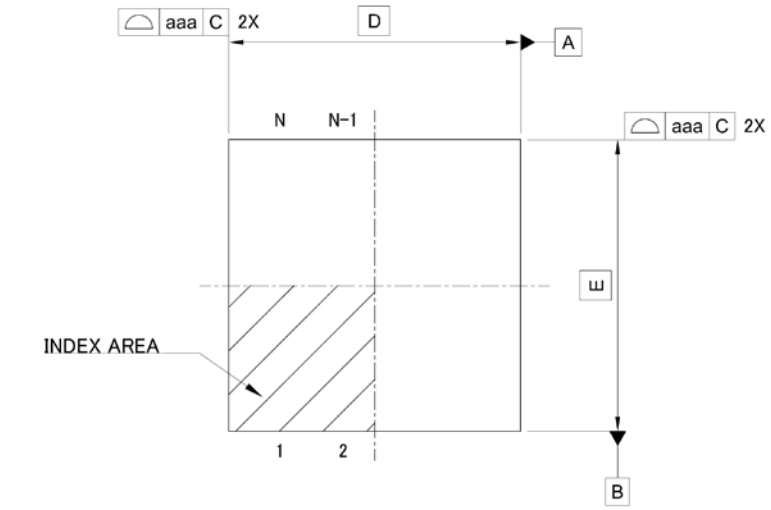
4. PACKAGE DRAWINGS

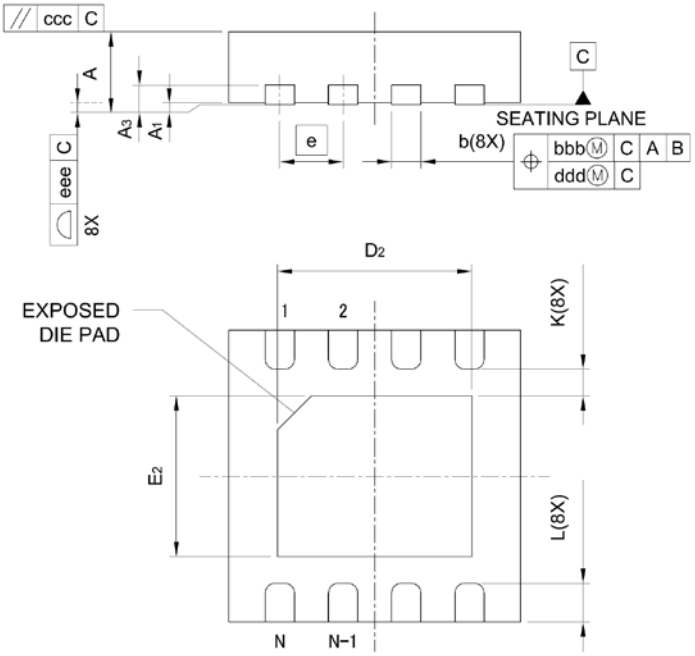
★ 4.1 8-pin products

R5F12008MNS, R5F12008GNS, R5F12008ANS

R5F12007MNS, R5F12007GNS, R5F12007ANS

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWSON8-3x3-0.65	PWSN0008JG-A	0.02





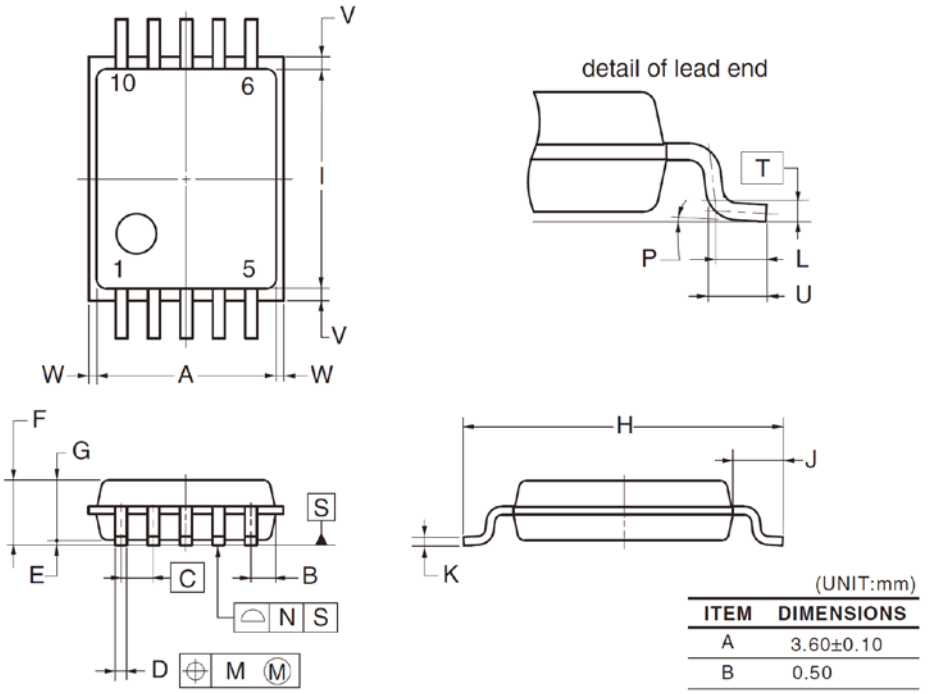
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	—	0.05
A_3		0.203 REF.	
b	0.25	0.30	0.35
D		3.00	
E		3.00	
e		0.65	
N		8	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	1.95	2.00	2.05
E_2	1.60	1.65	1.70
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08

4.2 10-pin products

R5F12018MSP, R5F12018GSP, R5F12018ASP

R5F12017MSP, R5F12017GSP, R5F12017ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



(UNIT:mm)

ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

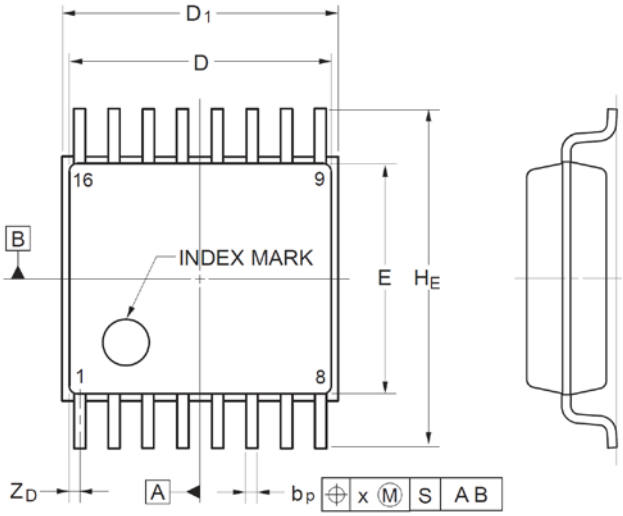
4.3 16-pin products

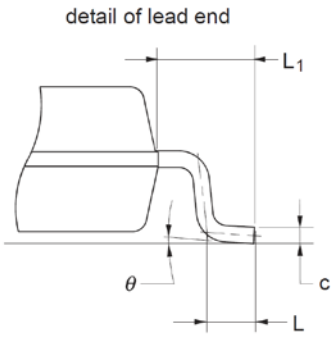
R5F12048MSP, R5F12048GSP, R5F12048ASP

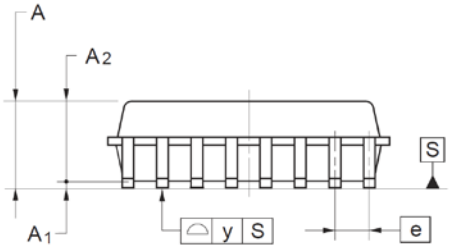
R5F12047MSP, R5F12047GSP, R5F12047ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-B	P16MA-65-FAB-1	0.08

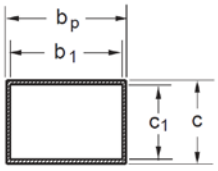
Unit: mm







Terminal cross section

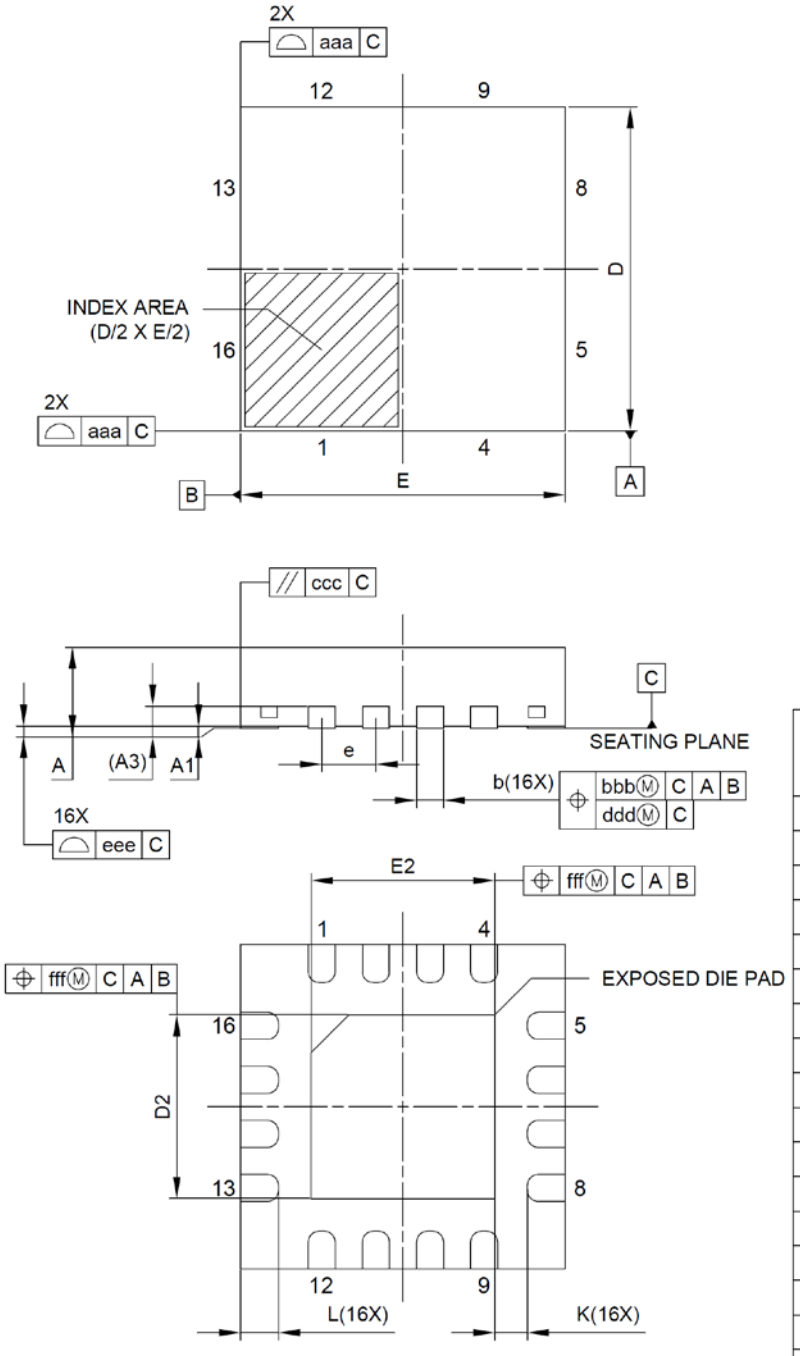


Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	4.85	5.00	5.15
D_1	5.05	5.20	5.35
E	4.20	4.40	4.60
A_2	—	1.50	—
A_1	0.075	0.125	0.175
A	—	—	1.725
b_p	0.17	0.24	0.32
b_1	—	0.22	—
c	0.14	0.17	0.20
c_1	—	0.15	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.225	—
L	0.35	0.50	0.65
L_1	—	1.00	—

R5F12048MNA, R5F12048GNA, R5F12048ANA

R5F12047MNA, R5F12047GNA, R5F12047ANA

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN016-3x3-0.50	PWQN0016KD-A	0.02



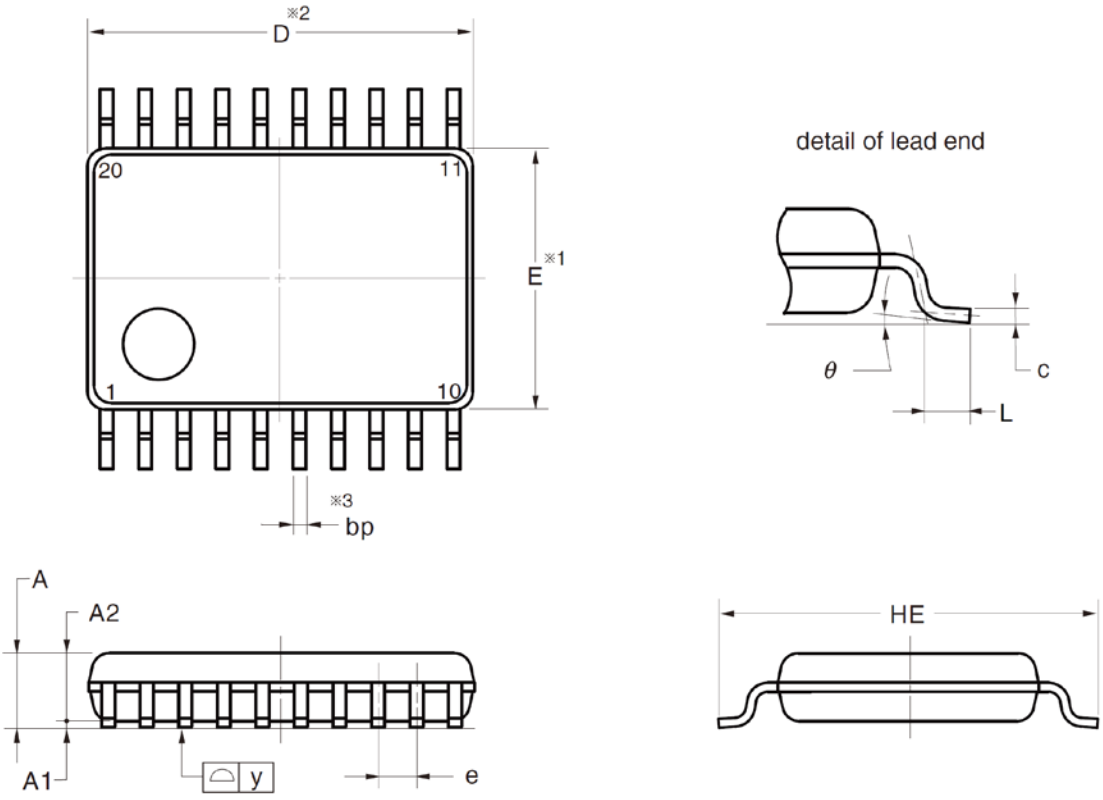
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.20	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
e		0.50 BSC	
L	0.30	0.35	0.40
K	0.20	—	—
D2	1.65	1.70	1.75
E2	1.65	1.70	1.75
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

4.4 20-pin products

R5F12068MSP, R5F12068GSP, R5F12068ASP

R5F12067MSP, R5F12067GSP, R5F12067ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	$0.22^{+0.10}_{-0.05}$
c	$0.15^{+0.05}_{-0.02}$
L	0.50±0.20
y	0.10
θ	0° to 10°

NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

REVISION HISTORY	RL78/G15 Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 17, 2022	—	First edition issued
1.10	Apr 28, 2023	19	2. ELECTRICAL SPECIFICATIONS (T_A = −40 to +85°C): The section title, modified. Caution 3, deleted.
		21	2.2.2 On-chip oscillator characteristics: Note 3, deleted
		24	2.3.2 Supply current characteristics: Note 1, modified
		39	2.8 Flash Memory Programming Characteristics: The condition was added to the code flash/data flash self-programming time
		40	2.10 Timing of Entry to Flash Memory Programming Mode: The condition, added
		41	3. ELECTRICAL SPECIFICATIONS (T_A = −40 to +105°C, T_A = −40 to +125°C): The section title, modified. Caution 3, deleted.
		43	3.2.2 On-chip oscillator characteristics: The MIN. and MAX. values of high-speed on-chip oscillator clock frequency accuracy (T_A = +85 to +125°C), modified. Note 3, deleted.
		46	3.3.2 Supply current characteristics: Note 1, modified
		61	3.8 Flash Memory Programming Characteristics: The condition in the table, modified. Note 3, added. The condition was added to the code flash/data flash self-programming time.
		62	3.10 Timing of Entry to Flash Memory Programming Mode: The condition, added
		63	4.1 8-pin products: The description, deleted. The package drawing, added.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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