1. Overview

1.1 Features

The M16C/6C Group microcomputer (MCU) incorporates the M16C/60 Series CPU core and flash memory, employing sophisticated instructions for a high level of efficiency. This MCU has 1 MB of address space and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

This MCU consumes low power, and supports operating modes that allow additional power control. The MCU also uses an anti-noise configuration to reduce emissions of electromagnetic noise and is designed to withstand electromagnetic interference (EMI). By integrating many of the peripheral functions, including the multifunction timer and serial interface, the number of system components has been reduced.

1.1.1 Applications

This MCU can be used in personal computer peripherals (USB compatible products), audio components, cameras, televisions, household appliances, office equipment, communication devices, mobile devices, industrial equipment, and other applications.

Note: This product has been designed and developed for the purpose of being used in consumer products. It cannot be used with products that require a high level of quality such as automotive electronics.

1.2 Specifications

The M16C/6C Group is available in a 100-pin package. Table 1.1 and Table 1.2 list Specifications.

Table 1.1 Specifications (1/2)

Item	Function	Description
CPU	Central processing unit	M16C/60 Series core (multiplier: 16 bit × 16 bit → 32 bit, multiply and accumulate instruction: 16 bit × 16 bit + 32 bit → 32 bit) • Number of basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC1 = VCC2 = 2.7 to 5.5 V) • Operating modes: Single-chip, memory expansion, and microprocessor
Memory	ROM, RAM, data flash	See Table 1.3 “Product List”
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 selectable)
Clock	Clock generator	• 5 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ±10%), PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop/restart detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 • Power saving features: Wait mode, stop mode • Real-time clock
External Bus Expansion	Bus memory expansion	• Address space: 1 MB • External bus interface: 0 to 3 waits inserted, 4 chip select outputs, 3 V and 5 V interfaces • Bus format: Separate bus or multiplexed bus selectable, data bus width (8 bits), number of address buses selectable (12, 16, or 20)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 85 (selectable pull-up resistors) • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 13 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 8, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15-bit timer × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 55 • Transfer modes: 2 (single transfer, repeat transfer)

Table 1.2 Specifications (2/2)

Item	Function	Description
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer functions	• Three-phase inverter control (timer A1, timer A2, timer A4, timer B2) • On-chip dead time timer
	Real-time clock	Count: seconds, minutes, hours, days of the week
	Timer S (Input capture/output compare)	• Input base timer: 16 bits X 1 • I/O: 8 channels • Time measurement register, Waveform generation register: 16 bits X 8
Serial Interface	UART0 to UART5	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus, special mode 2 SIM (UART2)
Multi-master I^2C-bus Interface		1 channel

USB Functions		• Full speed (12 Mbps, USB 2.0 compliant)
		• Transfer type: Control IN/OUT, Bulk IN x 2, Bulk OUT x 2, Interrupt IN x 2
		• FIFO size: 584 bytes
		  • Setup 8 bytes
		  • Control IN 16 bytes
		  • Control OUT 16 bytes
		  • Interrupt IN 16 bytes: 2 channels
		  • Bulk IN 64 bytes x 2: 2 channels
		  • Bulk OUT 64 bytes x 2: 2 channels

A/D Converter		10-bit resolution × 26 channels (2 circuits), including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2 circuits
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		• Program and erase power supply voltage: 2.7 to 5.5 V • Program and erase cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-chip debug, on-board flash rewrite, address match interrupt × 4
Operation Frequency/Supply Voltage		32 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		Described in Electrical Characteristics
Operating Temperature		-20°C to 85°C, -40°C to 85°C (1)
Package		100-pin QFP: PRQP0100JD-B (Previous package code: 100P6F-A) 100-pin LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A)

Notes:
1. See Table 1.3 “Product List” for the operating temperature.

1.3 Product List

Table 1.3 lists Product List. Figure 1.1 shows Part No., with Memory Size and Package, and Figure 1.2 shows Marking Diagram (Top View).

Table 1.3 Product List As of July 2012

Part No.	ROM Capacity			RAM Capacity	Package Code	Remarks
	Program ROM 1	Program ROM 2	Data flash			
R5F36CAMNFA	512 KB	16 KB	4 KB × 2 blocks	31 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36CAMNFB					PLQP0100KB-A	
R5F36CAMDFA					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36CAMDFB					PLQP0100KB-A	
R5F36CAKNFA	384 KB	16 KB	4 KB × 2 blocks	31 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36CAKNFB					PLQP0100KB-A	
R5F36CAKDFA					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36CAKDFB					PLQP0100KB-A	
R5F36CAENFA	256 KB	16 KB	4 KB × 2 blocks	20 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36CAENFB					PLQP0100KB-A	
R5F36CAEDFA					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36CAEDFB					PLQP0100KB-A	
R5F36CA6NFA	128 KB	16 KB	4 KB × 2 blocks	12 KB	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36CA6NFB					PLQP0100KB-A	
R5F36CA6DFA					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36CA6DFB					PLQP0100KB-A	

(D): Under development
(P): Planning
Previous package codes are as follows:
PRQP0100JD-B: 100P6F-A
PLQP0100KB-A: 100P6Q-A

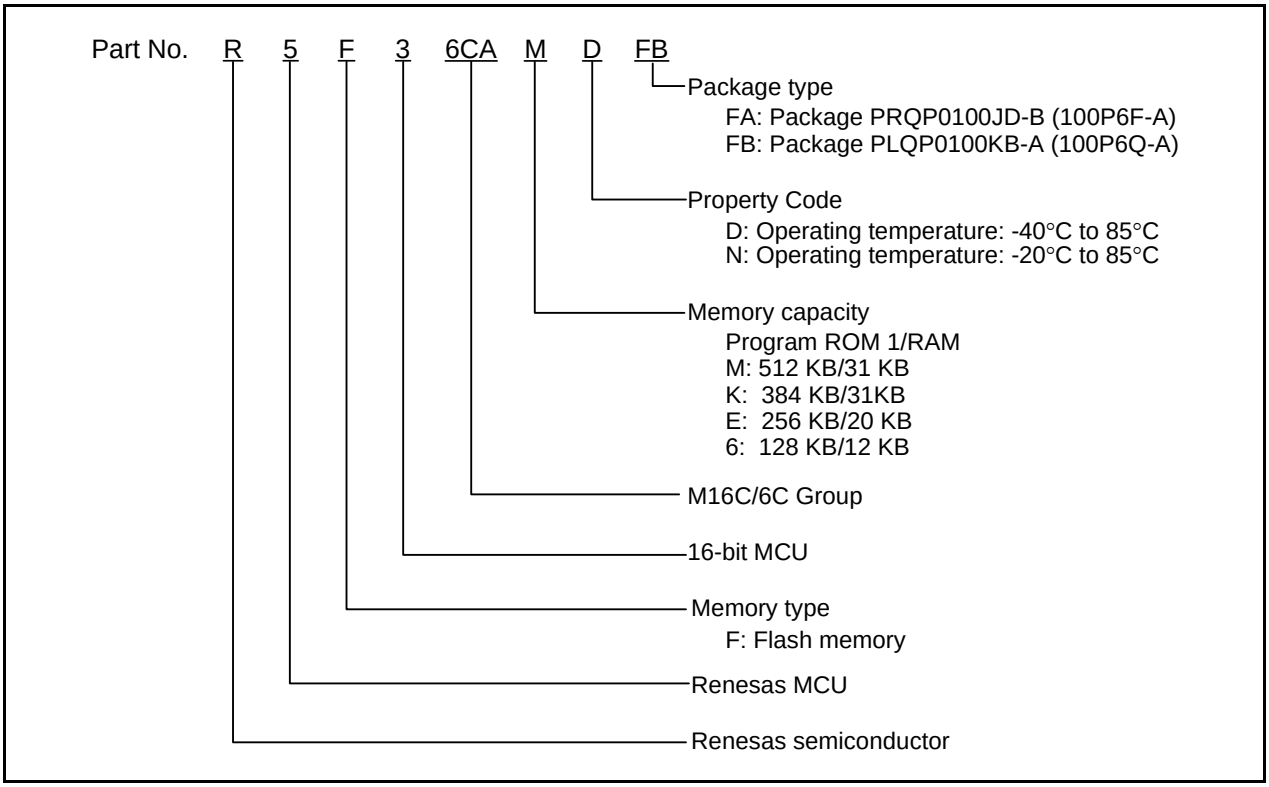


Figure 1.1 Part No., with Memory Size and Package

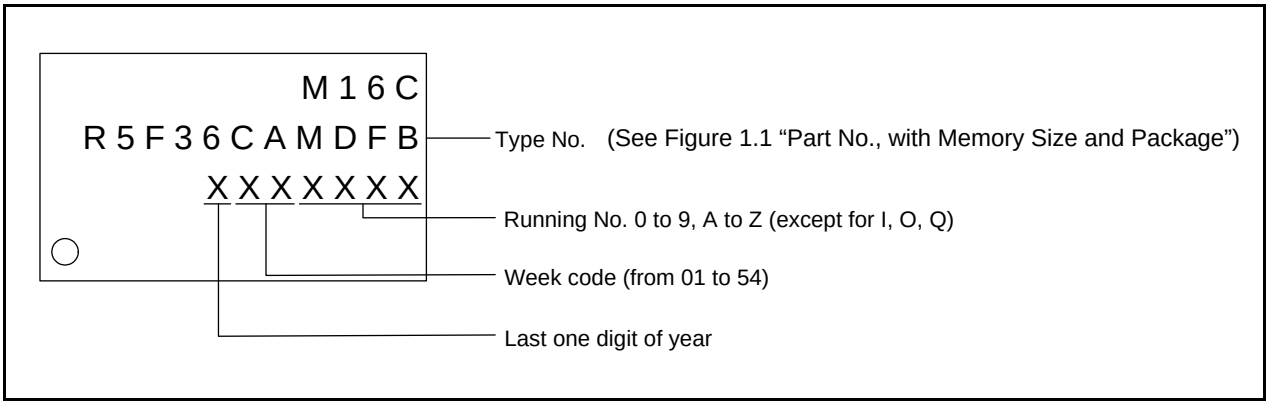
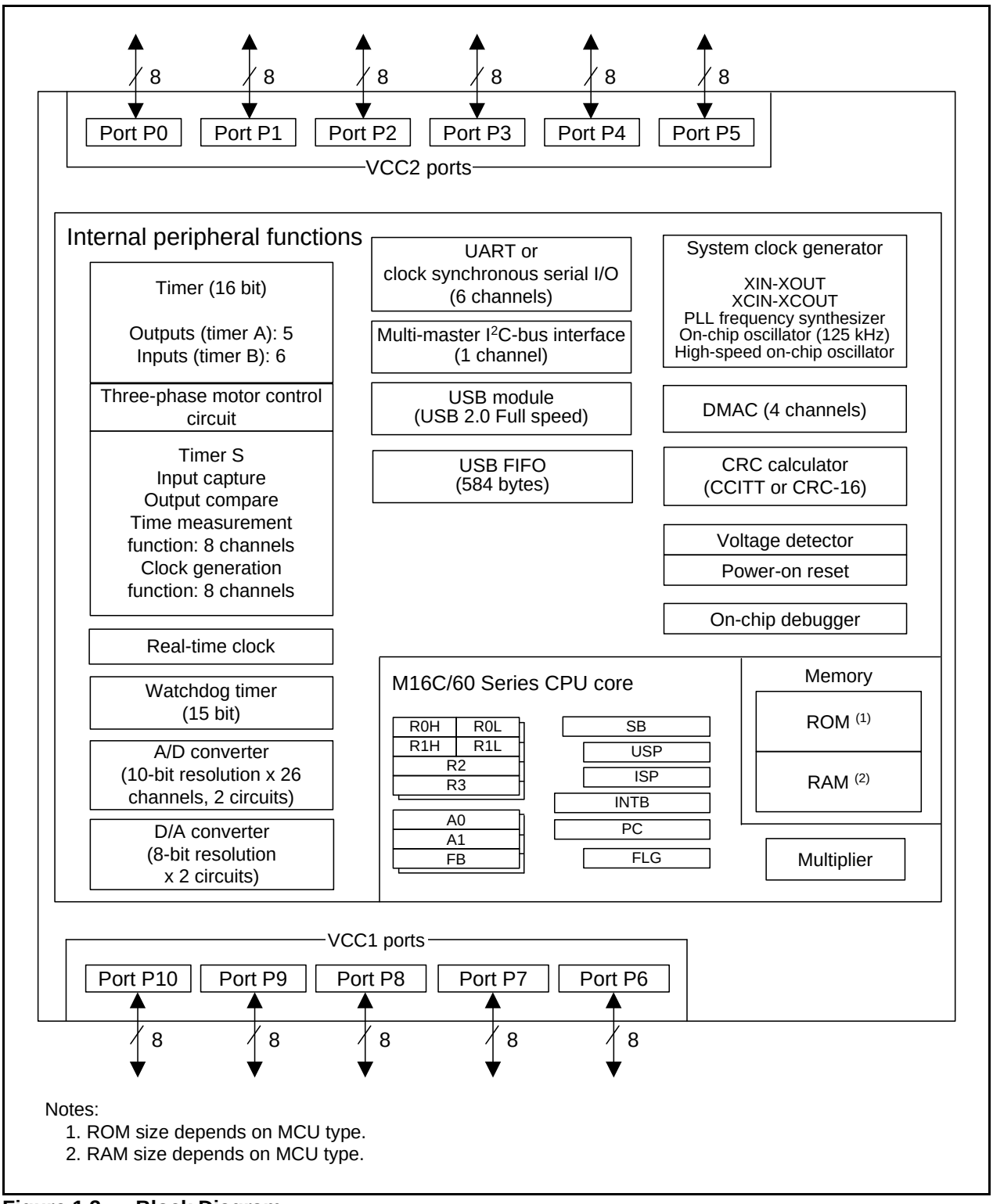


Figure 1.2 Marking Diagram (Top View)

1.4 Block Diagram

Figure 1.3 shows Block Diagram.

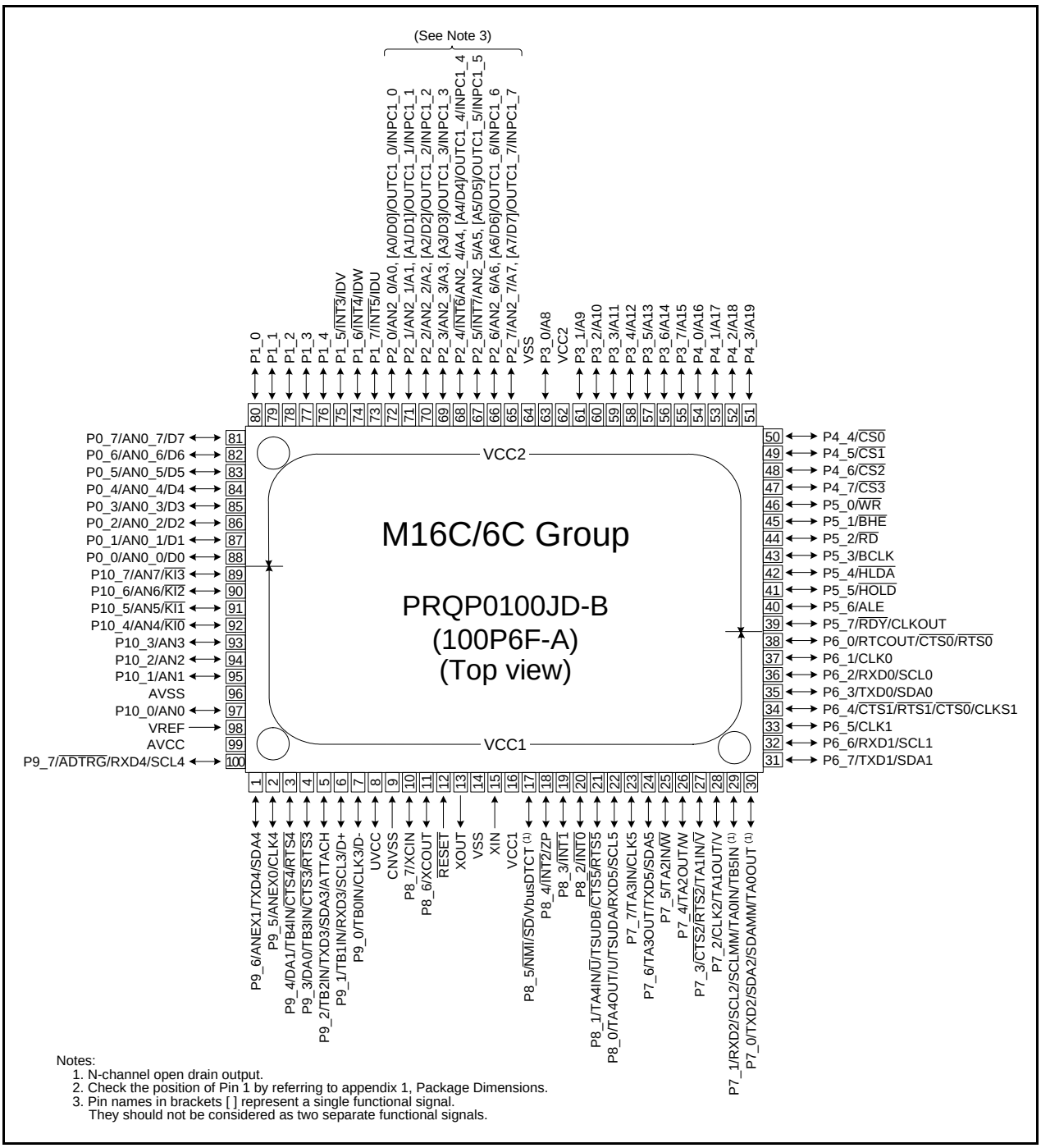


Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.3 Block Diagram

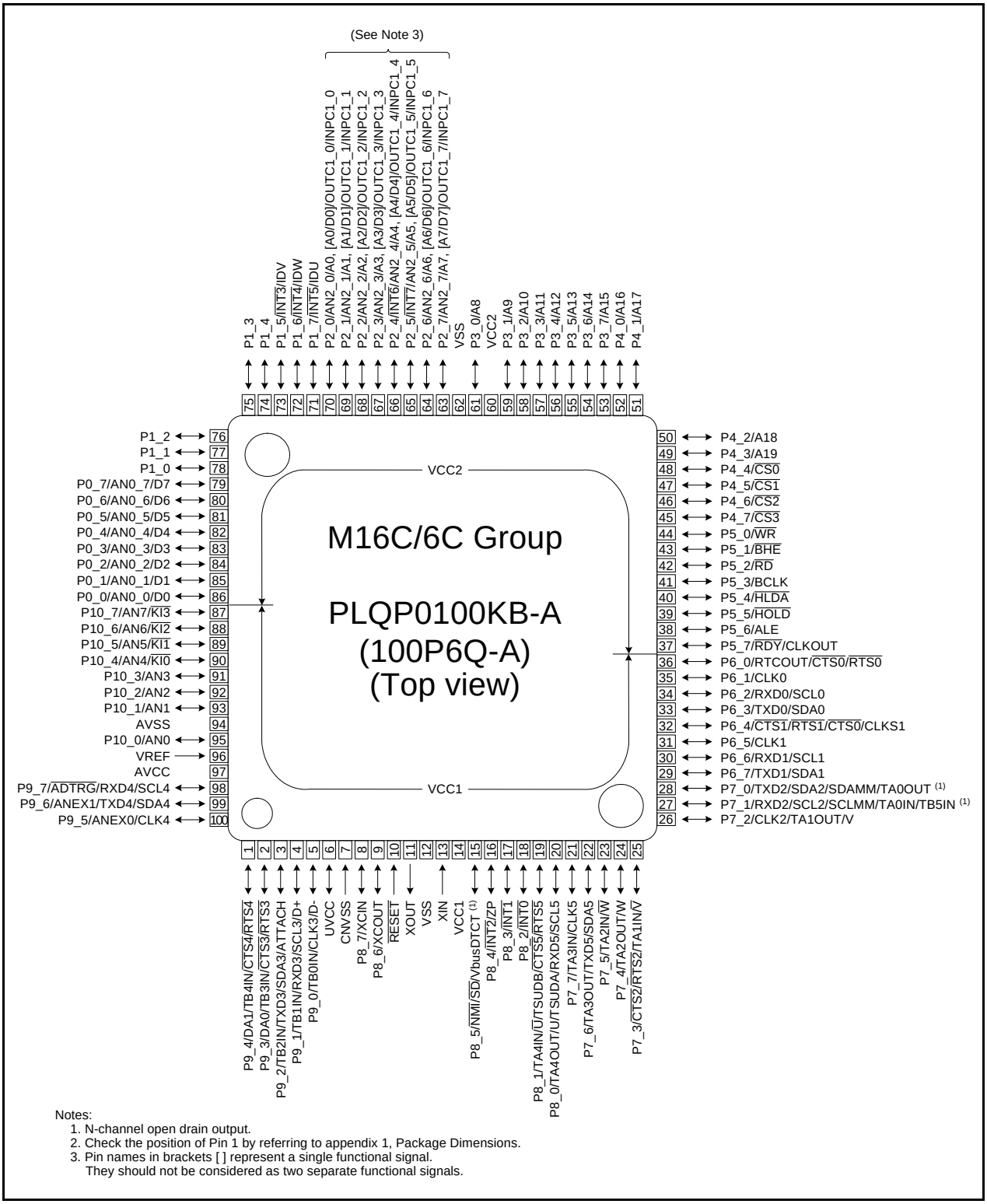
1.5 Pin Assignment

Figure 1.4 and Figure 1.5 show Pin Assignment. Table 1.4 and Table 1.5 list Pin Names.



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

Figure 1.4 Pin Assignment



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal.
They should not be considered as two separate functional signals.

Figure 1.5 Pin Assignment

Table 1.4 Pin Names (1/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface, USB	A/D converter, D/A converter	
1	99		P9_6			TXD4/SDA4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN	CTS4/RTS4	DA1	
4	2		P9_3		TB3IN	CTS3/RTS3	DA0	
5	3		P9_2		TB2IN	TXD3/SDA3/ATTACH		
6	4		P9_1		TB1IN	RXD3/SCL3/D+		
7	5		P9_0		TB0IN	CLK3/D-		
8	6					UVCC		
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$	VbusDTCT		
18	16		P8_4	$\overline{\text{INT2}}$	ZP			
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1		TA4IN/$\overline{\text{U}}$/TSUDB	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$		
22	20		P8_0		TA4OUT/U/TSUDA	RXD5/SCL5		
23	21		P7_7		TA3IN	CLK5		
24	22		P7_6		$\overline{\text{TA3OUT}}$	TXD5/SDA5		
25	23		P7_5		TA2IN/$\overline{\text{W}}$			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
30	28		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/ CLKS1		
35	33		P6_3			TXD0/SDA0		
36	34		P6_2			RXD0/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0		RTCOUT	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
39	37		P5_7					$\overline{\text{RDY}}$/CLKOUT
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLDA}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{BHE}}$
46	44		P5_0					$\overline{\text{WR}}$
47	45		P4_7					$\overline{\text{CS3}}$
48	46		P4_6					$\overline{\text{CS2}}$
49	47		P4_5					$\overline{\text{CS1}}$
50	48		P4_4					$\overline{\text{CS0}}$

Table 1.5 Pin Names (2/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface, USB	A/D converter, D/A converter	
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8
64	62	VSS						
65	63		P2_7		OUTC1_7/INPC1_7		AN2_7	A7, [A7/D7]
66	64		P2_6		OUTC1_6/INPC1_6		AN2_6	A6, [A6/D6]
67	65		P2_5	$\overline{INT7}$	OUTC1_5/INPC1_5		AN2_5	A5, [A5/D5]
68	66		P2_4	$\overline{INT6}$	OUTC1_4/INPC1_4		AN2_4	A4, [A4/D4]
69	67		P2_3		OUTC1_3/INPC1_3		AN2_3	A3, [A3/D3]
70	68		P2_2		OUTC1_2/INPC1_2		AN2_2	A2, [A2/D2]
71	69		P2_1		OUTC1_1/INPC1_1		AN2_1	A1, [A1/D1]
72	70		P2_0		OUTC1_0/INPC1_0		AN2_0	A0, [A0/D0]
73	71		P1_7	$\overline{INT5}$	IDU			
74	72		P1_6	$\overline{INT4}$	IDW			
75	73		P1_5	$\overline{INT3}$	IDV			
76	74		P1_4					
77	75		P1_3					
78	76		P1_2					
79	77		P1_1					
80	78		P1_0					
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	$\overline{KI3}$			AN7	
90	88		P10_6	$\overline{KI2}$			AN6	
91	89		P10_5	$\overline{KI1}$			AN5	
92	90		P10_4	$\overline{KI0}$			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7			RXD4/SCL4	$\overline{ADTRG}$	

1.6 Pin Functions

Table 1.6 Pin Functions (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2). Input 0 V to VSS.(1)
Analog power supply input	AVCC, AVSS	I	VCC1	This is the power supply for the A/D converter. Connect the AVCC pin to VCC1, and connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor modes. Connect the CNVSS pin to VSS via a resistor.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with a separate bus.
	A0 to A19	O	VCC2	Outputs address bits A0 to A19.
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with an 8-bit multiplexed bus.
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area.
	$\overline{\text{WR}}$ $\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Outputs $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ signals. • Data is written to an external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low.
	ALE	O	VCC2	Outputs an ALE signal to latch the address.
	$\overline{\text{HOLD}}$	I	VCC2	$\overline{\text{HOLD}}$ input is unavailable. Connect the $\overline{\text{HOLD}}$ pin to VCC2 via a resistor (pull-up).
	$\overline{\text{HLDA}}$	O	VCC2	In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	The MCU bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to the external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

Note:
1. VCC means VCC1 unless otherwise noted.

Table 1.7 Pin Functions (2/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Main clock input	XIN	I	VCC1	I/O for the main clock oscillator. Connect a ceramic resonator or crystal between pins XIN and XOUT. (1) Input an external clock to XIN pin and leave XOUT pin open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O for a sub clock oscillator. Connect a crystal between XCIN pin and XCOUT pin. (1) Input an external clock to XCIN pin and leave XCOUT pin open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs the BCLK signal.
Clock output	CLKOUT	O	VCC2	Outputs a clock with the same frequency as fC, f1, f8, or f32.
$\overline{INT}$ interrupt input	$\overline{INT0}$ to $\overline{INT2}$	I	VCC1	Input for the $\overline{INT}$ interrupt.
	$\overline{INT3}$ to $\overline{INT7}$	I	VCC2	
$\overline{NMI}$ interrupt input	$\overline{NMI}$	I	VCC1	Input for the $\overline{NMI}$ interrupt.
Key input interrupt input	$\overline{KI0}$ to $\overline{KI3}$	I	VCC1	Input for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O for timers A0 to A4 (TA0OUT is N-channel open drain output).
	TA0IN to TA4IN	I	VCC1	Input for timers A0 to A4.
	ZP	I	VCC1	Input for Z-phase.
Timer B	TB0IN to TB5IN	I	VCC1	Input for timers B0 to B5.
Three-phase motor control timer	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	VCC1	Output for the three-phase motor control timer.
	$\overline{SD}$	I	VCC1	Forced cutoff input.
	IDU, IDV, IDW	I	VCC2	Input for the position data.
Real-time clock output	RTCOUT	O	VCC1	Output for the real-time clock.
Timer S	INPC1_0 to INPC1_7	I	VCC2	Input for the time measurement function.
	OUTC1_0 to OUTC1_7	O	VCC2	Output for the waveform generation function.
	TSUDA, TSUDB	I	VCC1	Input for two-phase pulse.
Serial interface UART0 to UART5	$\overline{CTS0}$ to $\overline{CTS5}$	I	VCC1	Input pins to control data transmission.
	$\overline{RTS0}$ to $\overline{RTS5}$	O	VCC1	Output pins to control data reception.
	CLK0 to CLK5	I/O	VCC1	Transmit/receive clock I/O.
	RXD0 to RXD5	I	VCC1	Serial data input.
	TXD0 to TXD5	O	VCC1	Serial data output. (2)
	CLKS1	O	VCC1	Output for the transmit/receive clock multiple-pin output function.
UART0 to UART5 I^2C mode	SDA0 to SDA5	I/O	VCC1	Serial data I/O.(2)
	SCL0 to SCL5	I/O	VCC1	Transmit/receive clock I/O.(2)

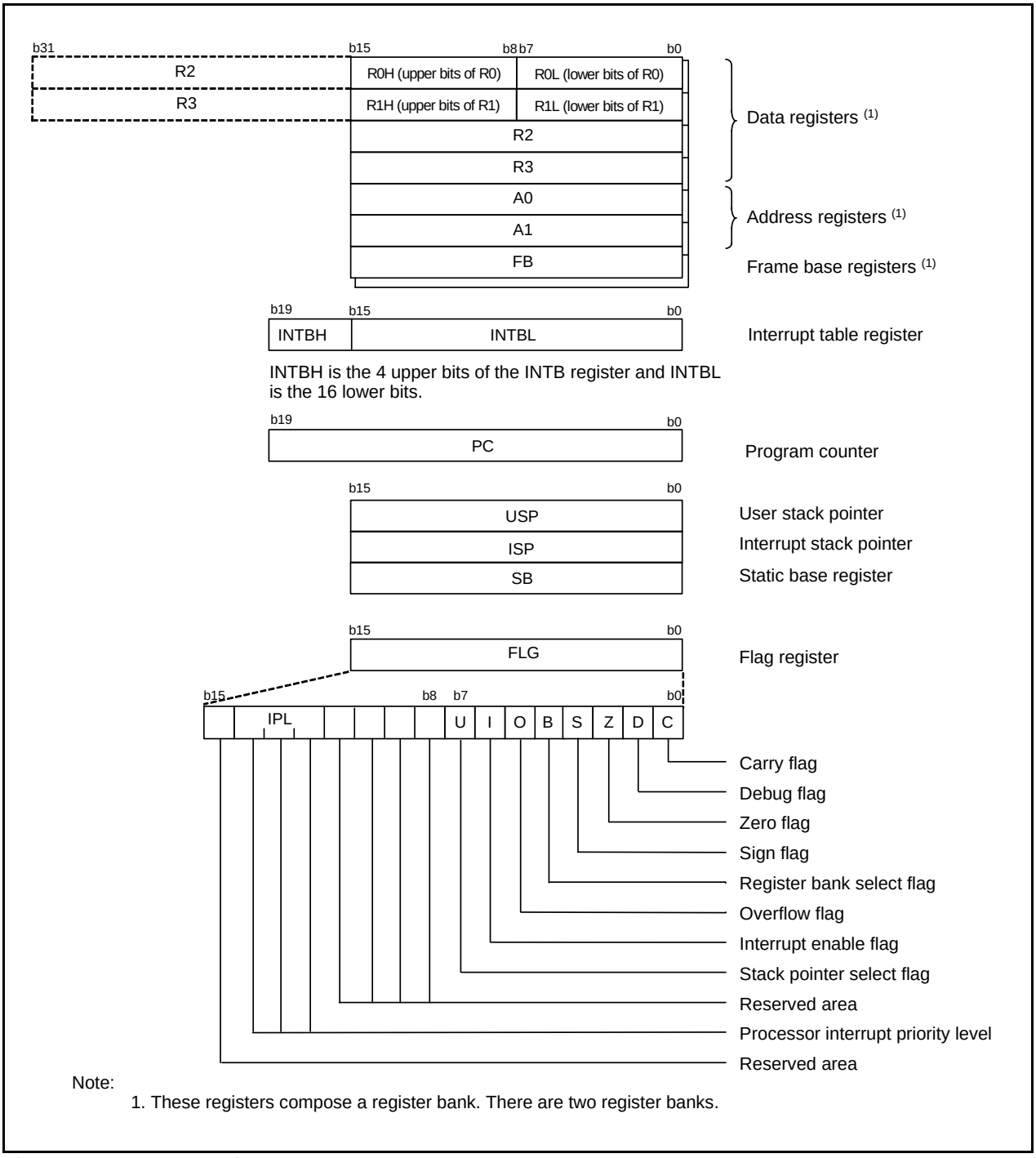
Notes:
1. Contact the manufacturer of crystal/ceramic resonator regarding the oscillation characteristics.
2. TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi, SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins. (i = 0, 1, 3 to 5)

Table 1.8 Pin Functions (3/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Multi-master I^2C-bus interface	SDAMM	I/O	VCC1	Serial data I/O (N-channel open drain output).
	SCLMM	I/O	VCC1	Transmit/receive clock I/O (N-channel open drain output).
USB module	ATTACH	O	UVCC	Output used for D+ 1.5 kΩ pull-up
	VbusDTCT	I	UVCC	Input the power supply signal from a host PC
	UVCC	I/O		Input power supply for pins ATTACH, D+, and D-
	D+	I/O	UVCC	USB D+ input/output
	D-	I/O	UVCC	USB D- input/output
Reference voltage input	VREF	I	VCC1	Reference voltage input for the A/D and D/A converters.
A/D converter	AN0 to AN7	I	VCC1	Analog input.
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC2	
	$\overline{\text{ADTRG}}$	I	VCC1	External trigger input.
	ANEX0, ANEX1	I	VCC1	Extended analog input.
D/A converter	DA0, DA1	O	VCC1	Output for the D/A converter.
I/O ports	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. A direction register determines whether each pin is used as an input port or an output port. A pull-up resistor may be enabled or disabled for input ports in 4-bit units.
	P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_7 P10_0 to P10_7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. However, P7_0, P7_1, and P8_5 are N-channel open drain output ports. No pull-up resistor is provided. P8_5 is an input port for verifying the $\overline{\text{NMI}}$ pin level and shares a pin with $\overline{\text{NMI}}$.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of 13 compose a register bank, and there are two register banks.



Note:
1. These registers compose a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic, and logic operations. R0 and R1 can be split into upper (R0H/R1H) and lower (R0L/R1L) bits to be used separately as 8-bit data registers. R0 can be combined with R2, and R3 can be combined with R1 and be used as 32-bit data registers R2R0 and R3R1, respectively.

2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic, and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register that is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The USP and ISP stack pointers (SP) are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise, it becomes 0.

2.8.4 Sign Flag (S Flag)

The S flag becomes 1 when an arithmetic operation results in a negative value. Otherwise, it becomes 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

The O flag becomes 1 when an arithmetic operation results in an overflow. Otherwise, it becomes 0.

2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.
Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.
The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.
If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

2.8.10 Reserved Areas

Only set these bits to 0. The read value is undefined.

3. Address Space

3.1 Address Space

The M16C/6C Group has a 1 MB address space from 00000h to FFFFFh. Figure 3.1 shows the Address Space. Areas that can be accessed vary depending on processor mode and the status of each control bit.

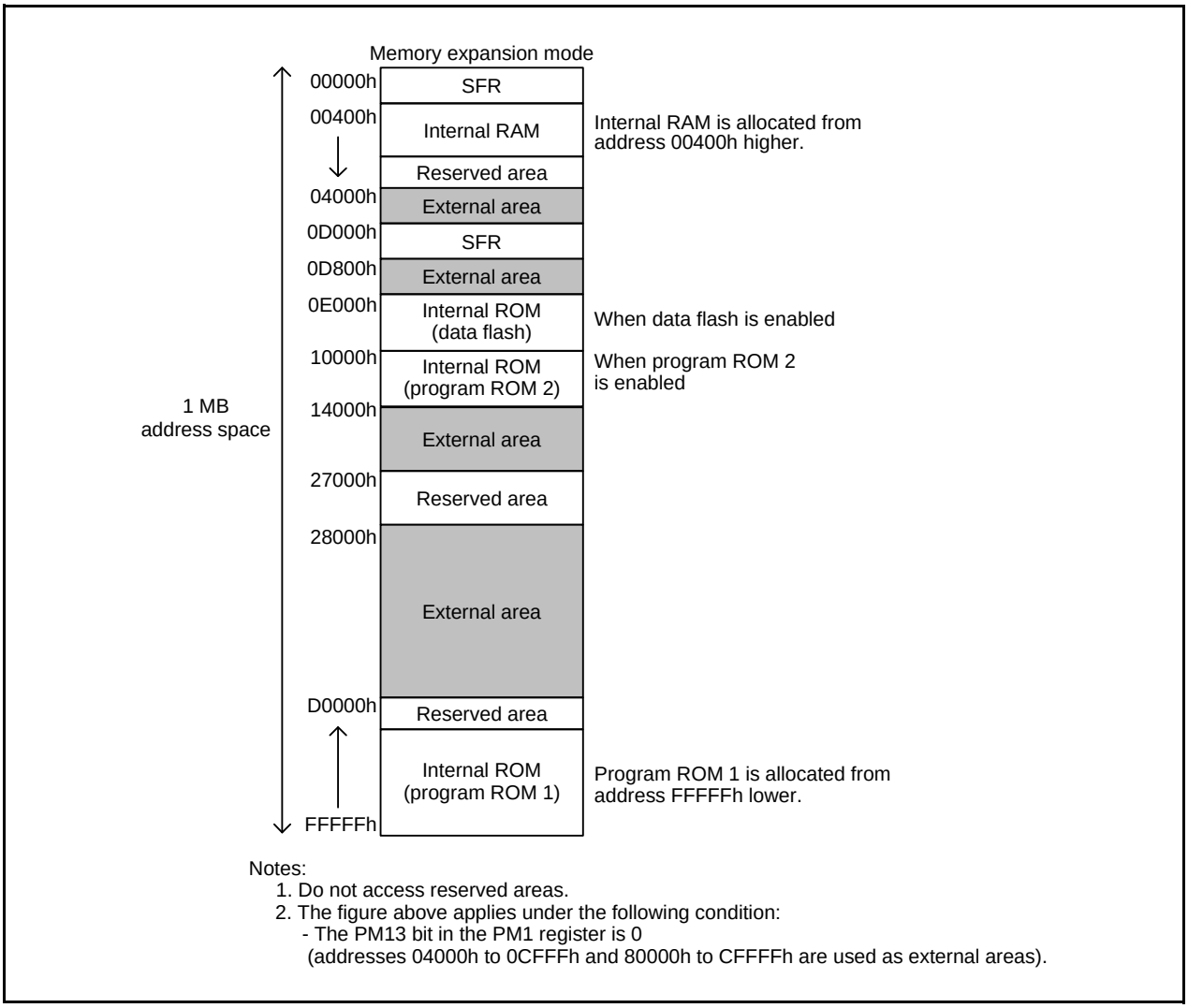


Figure 3.1 Address Space

3.2 Memory Map

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank areas within SFRs are reserved. Do not access these areas.

Internal RAM is allocated from address 00400h and higher, with 10 KB of internal RAM allocated from 00400h to 02BFFh. Internal RAM is used not only for data storage, but also for the stack area when subroutines are called or when an interrupt request is accepted.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is allocated from 0E000h to 0FFFFh. This data flash area is mostly used for data storage, but can also store programs.

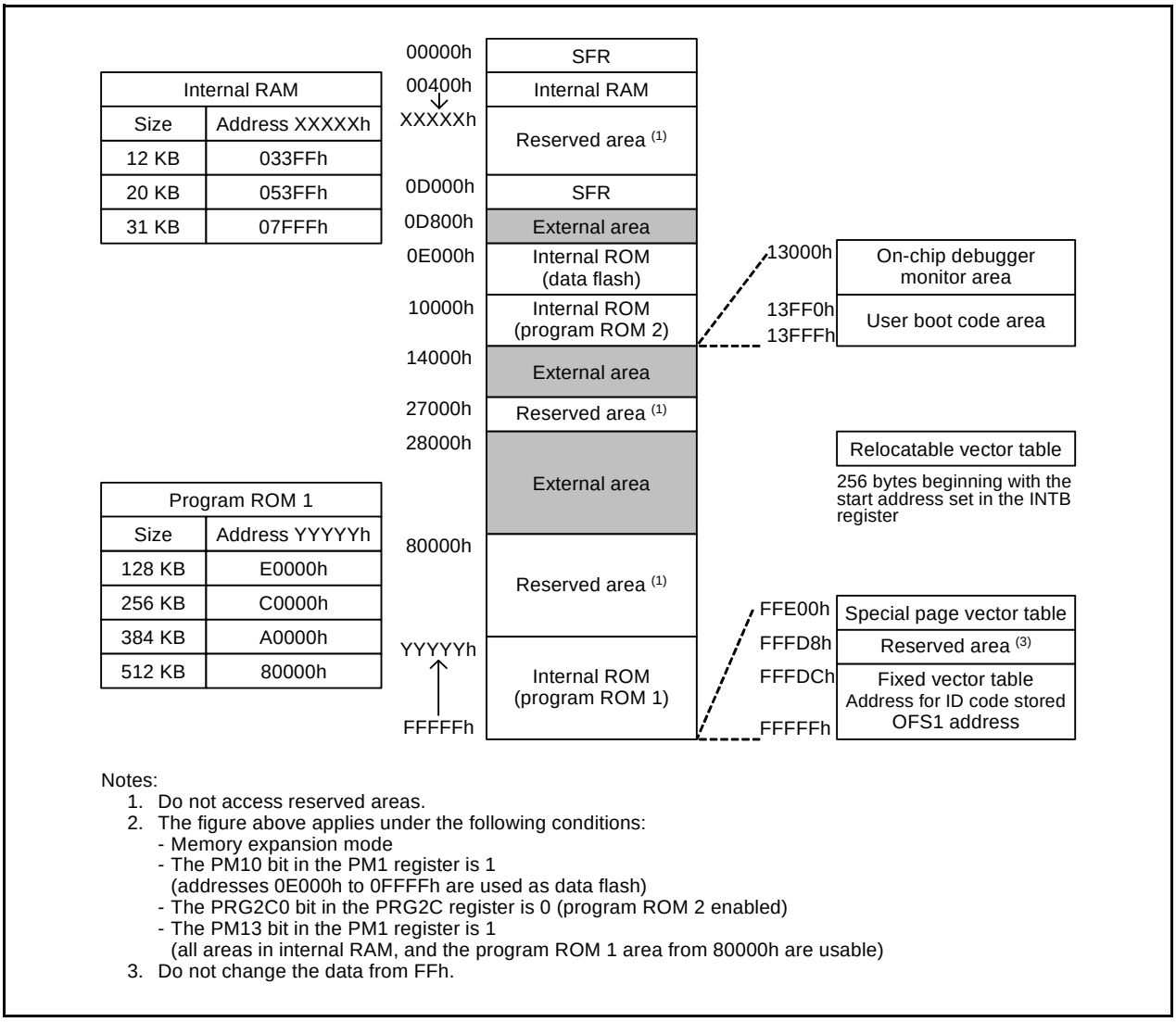
Program ROM 2 is allocated from 10000h to 13FFFh. Program ROM 1 is allocated from FFFFFh and lower, with the 64 KB program ROM 1 area allocated from address F0000h to FFFFFh.

The special page vectors are allocated from FFE00h to FFFD7h. They are used for the JMPS and JSRS instructions. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts is allocated from FFFDCh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

Figure 3.2 shows the Memory Map.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following conditions:
   - Memory expansion mode
   - The PM10 bit in the PM1 register is 1
     (addresses 0E000h to 0FFFFh are used as data flash)
   - The PRG2C0 bit in the PRG2C register is 0 (program ROM 2 enabled)
   - The PM13 bit in the PM1 register is 1
     (all areas in internal RAM, and the program ROM 1 area from 80000h are usable)
3. Do not change the data from FFh.

Figure 3.2 Memory Map

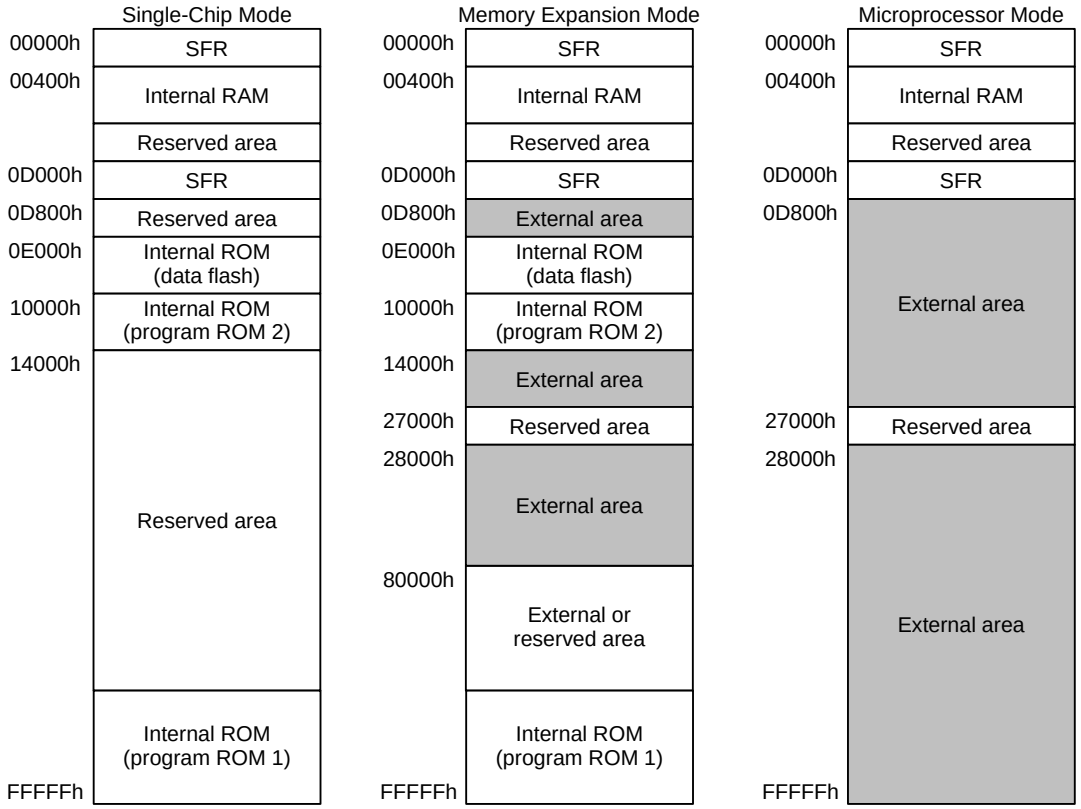
3.3 Accessible Area in Each Mode

Areas that can be accessed vary depending on processor mode and the status of each control bit. Figure 3.3 shows the Accessible Area in Each Mode.

In single-chip mode, the SFRs, internal RAM, and internal ROM can be accessed.

In memory expansion mode, the SFRs, internal RAM, internal ROM, and external areas can be accessed.

In microprocessor mode, the SFRs, internal RAM, and external areas can be accessed. Allocate ROM to the fixed vector table from FFFDCh to FFFFFh.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following conditions:
   Single-chip mode and memory expansion mode
   - The PM10 bit in the PM1 register is 1
     (addresses 0E000h to 0FFFFh are used as data flash)
   - The PRG2C0 bit in the PRG2C register is 0 (program ROM 2 enabled)
   - The PM13 bit in the PM1 register is 1
     (all areas in internal RAM, and the program ROM 1 area from 80000h are usable)re usable).

   Microprocessor mode
   - The PM10 bit is 0 (addresses 0E000h to 0FFFFh are used as the $\overline{CS2}$ area).
   - The PRG2C0 bit is 1 (program ROM 2 disabled).

Figure 3.3 Accessible Area in Each Mode

4. Special Function Registers (SFRs)

4.1 SFRs

An SFR is a control register for a peripheral function.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	Reset Value
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	0000 0000b (2)
0005h	Processor Mode Register 1	PM1	0000 1000b
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h	Chip Select Control Register	CSR	01h
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (3)
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0011h			
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	XX00 001Xb (hardware reset) (4)
0019h	Voltage Detector 2 Flag Register	VCR1	0000 1000b (5)
001Ah	Voltage Detector Operation Enable Register	VCR2	00h (5)
001Bh	Chip Select Expansion Control Register	CSE	00h
001Ch	PLL Control Register 0	PLC0	0001 X010b
001Dh	PLLFCK Control Register	PLCF	00h
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
001Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect the following bits: bits PM01 and PM00 in the PM0 register.
3. Oscillator stop detect reset does not affect bits CM20, CM21, and CM27.
4. The state of bits in the RSTFR register depends on the reset type.
5. This is the reset value after hardware reset. Refer to the explanation of each register for details.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	Reset Value
0020h			
0021h			
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	XXXX XX00b
0023h			
0024h			
0025h			
0026h	Voltage Monitor Function Select Register	VWCE	00h
0027h			
0028h			
0029h			
002Ah	Voltage Monitor 0 Control Register	VW0C	1000 XX10b (2)
002Bh	Voltage Monitor 1 Control Register	VW1C	1000 1010b (2)
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b (2)
002Dh			
002Eh			
002Fh			
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. This is the reset value after hardware reset. Refer to the explanation of each register for details.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h	$\overline{\text{INT7}}$ Interrupt Control Register	INT7IC	XX00 X000b
0043h	$\overline{\text{INT6}}$ Interrupt Control Register	INT6IC	XX00 X000b
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	$\overline{\text{INT5}}$ Interrupt Control Register	INT5IC	XX00 X000b
0049h	$\overline{\text{INT4}}$ Interrupt Control Register	INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register A/D Conversion (A/D1) Interrupt Control Register	KUPIC ADEIC	XXXX X000b
004Eh	A/D Conversion (A/D0) Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	Reset Value
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register	U5BCNIC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register	S5TIC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART4 Bus Collision Detection Interrupt Control Register Real-Time Clock Periodic Interrupt Control Register	U4BCNIC RTCTIC	XXXX X000b
006Fh	UART4 Transmit Interrupt Control Register Real-Time Clock Compare Interrupt Control Register	S4TIC RTCCIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0071h	UART3 Bus Collision Detection Interrupt Control Register	U3BCNIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register	S3TIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0074h			
0075h			
0076h	USB Interrupt 0 Control Register	USBINT0IC	XXXX X000b
0077h	USB Interrupt 1 Control Register	USBINT1IC	XXXX X000b
0078h	USB RESUME Interrupt Control Register	USBRSMIC	XXXX X000b
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register I2C-bus Interface Interrupt Control Register	ICOC1IC IICIC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register SCL/SDA Interrupt Control Register	ICOCH1IC SCLDAIC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b
0080h to 012Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	Reset Value
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
0140h	A/D1 Register 0	AD10	XXXX XXXXb
0141h			0000 00XXb
0142h	A/D1 Register 1	AD11	XXXX XXXXb
0143h			0000 00XXb
0144h	A/D1 Register 2	AD12	XXXX XXXXb
0145h			0000 00XXb
0146h	A/D1 Register 3	AD13	XXXX XXXXb
0147h			0000 00XXb
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h	A/D1 Trigger Control Register	AD1TRGCON	XXXX 00XXb
0153h			
0154h	A/D1 Control Register 2	AD1CON2	0000 X00Xb
0155h			
0156h	A/D1 Control Register 0	AD1CON0	0000 0XXXb
0157h	A/D1 Control Register 1	AD1CON1	0000 X000b
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h to 017Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	Reset Value
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0183h			
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0187h			
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0193h			
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0197h			
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01ADh			
01AEh			
01AFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	Reset Value
01E0h	Timer B3-1 Register	TB31	XXh
01E1h			XXh
01E2h	Timer B4-1 Register	TB41	XXh
01E3h			XXh
01E4h	Timer B5-1 Register	TB51	XXh
01E5h			XXh
01E6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 2	PPWFS2	XXXX X000b
01E7h			
01E8h	Timer B Count Source Select Register 2	TBCS2	00h
01E9h	Timer B Count Source Select Register 3	TBCS3	X0h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0251h			
0252h	UART Clock Select Register	UCLKSEL0	X0h
0253h			
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	Reset Value
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h	UART5 Special Mode Register 4	U5SMR4	00h
0285h	UART5 Special Mode Register 3	U5SMR3	000X 0X0Xb
0286h	UART5 Special Mode Register 2	U5SMR2	X000 0000b
0287h	UART5 Special Mode Register	U5SMR	X000 0000b
0288h	UART5 Transmit/Receive Mode Register	U5MR	00h
0289h	UART5 Bit Rate Register	U5BRG	XXh
028Ah	UART5 Transmit Buffer Register	U5TB	XXh
028Bh			XXh
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
028Eh	UART5 Receive Buffer Register	U5RB	XXh
028Fh			XXh
0290h			
0291h			
0292h			
0293h			
0294h	UART4 Special Mode Register 4	U4SMR4	00h
0295h	UART4 Special Mode Register 3	U4SMR3	000X 0X0Xb
0296h	UART4 Special Mode Register 2	U4SMR2	X000 0000b
0297h	UART4 Special Mode Register	U4SMR	X000 0000b
0298h	UART4 Transmit/Receive Mode Register	U4MR	00h
0299h	UART4 Bit Rate Register	U4BRG	XXh
029Ah	UART4 Transmit Buffer Register	U4TB	XXh
029Bh			XXh
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
029Eh	UART4 Receive Buffer Register	U4RB	XXh
029Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART3 Special Mode Register 4	U3SMR4	00h
02A5h	UART3 Special Mode Register 3	U3SMR3	000X 0X0Xb
02A6h	UART3 Special Mode Register 2	U3SMR2	X000 0000b
02A7h	UART3 Special Mode Register	U3SMR	X000 0000b
02A8h	UART3 Transmit/Receive Mode Register	U3MR	00h
02A9h	UART3 Bit Rate Register	U3BRG	XXh
02AAh	UART3 Transmit Buffer Register	U3TB	XXh
02ABh			XXh
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
02AEh	UART3 Receive Buffer Register	U3RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h	Time Measurement Register 0	G1TM0	XXh
02C1h	Waveform Generation Register 0	G1PO0	XXh
02C2h	Time Measurement Register 1	G1TM1	XXh
02C3h	Waveform Generation Register 1	G1PO1	XXh
02C4h	Time Measurement Register 2	G1TM2	XXh
02C5h	Waveform Generation Register 2	G1PO2	XXh
02C6h	Time Measurement Register 3	G1TM3	XXh
02C7h	Waveform Generation Register 3	G1PO3	XXh
02C8h	Time Measurement Register 4	G1TM4	XXh
02C9h	Waveform Generation Register 4	G1PO4	XXh
02CAh	Time Measurement Register 5	G1TM5	XXh
02CBh	Waveform Generation Register 5	G1PO5	XXh
02CCh	Time Measurement Register 6	G1TM6	XXh
02CDh	Waveform Generation Register 6	G1PO6	XXh
02CEh	Time Measurement Register 7	G1TM7	XXh
02CFh	Waveform Generation Register 7	G1PO7	XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	Reset Value
02D0h	Waveform Generation Control Register 0	G1POCR0	0X00 XX00b
02D1h	Waveform Generation Control Register 1	G1POCR1	0X00 XX00b
02D2h	Waveform Generation Control Register 2	G1POCR2	0X00 XX00b
02D3h	Waveform Generation Control Register 3	G1POCR3	0X00 XX00b
02D4h	Waveform Generation Control Register 4	G1POCR4	0X00 XX00b
02D5h	Waveform Generation Control Register 5	G1POCR5	0X00 XX00b
02D6h	Waveform Generation Control Register 6	G1POCR6	0X00 XX00b
02D7h	Waveform Generation Control Register 7	G1POCR7	0X00 XX00b
02D8h	Time Measurement Control Register 0	G1TMCR0	00h
02D9h	Time Measurement Control Register 1	G1TMCR1	00h
02DAh	Time Measurement Control Register 2	G1TMCR2	00h
02DBh	Time Measurement Control Register 3	G1TMCR3	00h
02DCh	Time Measurement Control Register 4	G1TMCR4	00h
02DDh	Time Measurement Control Register 5	G1TMCR5	00h
02DEh	Time Measurement Control Register 6	G1TMCR6	00h
02DFh	Time Measurement Control Register 7	G1TMCR7	00h
02E0h	Base Timer Register	G1BT	XXh
02E1h			XXh
02E2h	Base Timer Control Register 0	G1BCR0	00h
02E3h	Base Timer Control Register 1	G1BCR1	00h
02E4h	Time Measurement Prescaler Register 6	G1TPR6	00h
02E5h	Time Measurement Prescaler Register 7	G1TPR7	00h
02E6h	Function Enable Register	G1FE	00h
02E7h	Function Select Register	G1FS	00h
02E8h	Base Timer Reset Register	G1BTRR	XXh
02E9h			XXh
02EAh	Count Source Divide Register	G1DV	00h
02EBh			
02ECh	Waveform Output Master Enable Register	G1OER	00h
02EDh			
02EEh	Timer S I/O Control Register 0	G1IOR0	00h
02EFh	Timer S I/O Control Register 1	G1IOR1	00h
02F0h	Interrupt Request Register	G1IR	XXh
02F1h	Interrupt Enable Register 0	G1IE0	00h
02F2h	Interrupt Enable Register 1	G1IE1	00h
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh			
02FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	Reset Value
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			
0310h	Timer B3 Register	TB3	XXh
0311h			XXh
0312h	Timer B4 Register	TB4	XXh
0313h			XXh
0314h	Timer B5 Register	TB5	XXh
0315h			XXh
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0325h			
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	Reset Value
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b
033Fh			
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh			
035Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	Reset Value
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	0000 0000b (2) 0000 0010b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h			
0364h			
0365h			
0366h	Port Control Register	PCR	0000 0XX0b
0367h			
0368h			
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			
0370h			
0371h			
0372h			
0373h			
0374h			
0375h			
0376h			
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h (3)
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h to 038Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
 - 00000000b
 Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detect reset are as follows:
 - 00000000b when bits PM01 and PM00 in the PM0 register are 00b (single-chip mode).
 - 00000010b when bits PM01 and PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).
3. When the CSPROINI bit in the OFS1 address is 0, the reset value is 1000 0000b.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	Reset Value
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h			
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.18 SFR Information (18) (1)

Address	Register	Symbol	Reset Value
03C0h	A/D0 Register 0	AD00	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D0 Register 1	AD01	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D0 Register 2	AD02	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D0 Register 3	AD03	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D0 Register 4	AD04	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D0 Register 5	AD05	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D0 Register 6	AD06	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D0 Register 7	AD07	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h	A/D0 Trigger Control Register	AD0TRGCON	XXXX 00XXb
03D3h			
03D4h	A/D0 Control Register 2	AD0CON2	0000 X00Xb
03D5h			
03D6h	A/D0 Control Register 0	AD0CON0	0000 0XXXb
03D7h	A/D0 Control Register 1	AD0CON1	0000 X000b
03D8h	D/A0 Register	DA0	00h
03D9h			
03DAh	D/A1 Register	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.19 SFR Information (19) (1)

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.20 SFR Information (20) (1)

Address	Register	Symbol	Reset Value
D100h	USB Interrupt Flag Register 0	USBIFR0	00h
D101h	USB Interrupt Flag Register 1	USBIFR1	XXX0 0000b
D102h	USB Interrupt Flag Register 2	USBIFR2	XX00 0110b
D103h	USB Interrupt Flag Register 3	USBIFR3	XX00 0110b
D104h			
D105h			
D106h			
D107h			
D108h	USB Interrupt Enable Register 0	USBIER0	0000 00X0b
D109h	USB Interrupt Enable Register 1	USBIER1	XXX0 0000b
D10Ah	USB Interrupt Enable Register 2	USBIER2	XX00 0000b
D10Bh	USB Interrupt Enable Register 3	USBIER3	XX00 0000b
D10Ch			
D10Dh			
D10Eh			
D10Fh			
D110h	USB Interrupt Select Register 0	USBISR0	00X0 00X0b
D111h	USB Interrupt Select Register 1	USBISR1	XXX0 0000b
D112h	USB Interrupt Select Register 2	USBISR2	XX00 0000b
D113h	USB Interrupt Select Register 3	USBISR3	XX00 0000b
D114h			
D115h			
D116h			
D117h			
D118h			
D119h			
D11Ah			
D11Bh			
D11Ch			
D11Dh			
D11Eh			
D11Fh			
D120h	USB Endpoint 0 IN Data Register	USBEPDR0I	XXh
D121h			
D122h			
D123h			
D124h	USB Endpoint 0 OUT Data Register	USBEPDR0O	00h
D125h			
D126h			
D127h			
D128h	USB Endpoint 0 S Data Register	USBEPDR0S	00h
D129h			
D12Ah			
D12Bh			
D12Ch			
D12Dh			
D12Eh			
D12Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.21 SFR Information (21) (1)

Address	Register	Symbol	Reset Value
D130h	USB Endpoint 1 Data Register	USBEPDR1	00h
D131h			
D132h			
D133h			
D134h	USB Endpoint 2 Data Register	USBEPDR2	XXh
D135h			
D136h			
D137h			
D138h	USB Endpoint 3 Data Register	USBEPDR3	XXh
D139h			
D13Ah			
D13Bh			
D13Ch			
D13Dh			
D13Eh			
D13Fh			
D140h	USB Endpoint 4 Data Register	USBEPDR4	00h
D141h			
D142h			
D143h			
D144h	USB Endpoint 5 Data Register	USBEPDR5	XXh
D145h			
D146h			
D147h			
D148h	USB Endpoint 6 Data Register	USBEPDR6	XXh
D149h			
D14Ah			
D14Bh			
D14Ch			
D14Dh			
D14Eh			
D14Fh			
D150h to D17Fh			
D180h	USB Endpoint 0 OUT Receive Data Size Register	USBEPSZ0O	000X XXXXb
D181h	USB Endpoint 1 Receive Data Size Register	USBEPSZ1	0XXX XXXXb
D182h	USB Endpoint 4 Receive Data Size Register	USBEPSZ4	0XXX XXXXb
D183h			
D184h			
D185h			
D186h			
D187h			
D188h	USB Data Status Register 0	USBDASTS0	XXXX XXX0b
D189h	USB Data Status Register 1	USBDASTS1	XXXX X00Xb
D18Ah	USB Data Status Register 2	USBDASTS2	XXXX X00Xb
D18Bh			
D18Ch			
D18Dh			
D18Eh			
D18Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.22 SFR Information (22) (1)

Address	Register	Symbol	Reset Value
D190h	USB Trigger Register 0	USBTRG0	XXh
D191h	USB Trigger Register 1	USBTRG1	XXh
D192h	USB Trigger Register 2	USBTRG2	XXh
D193h			
D194h			
D195h			
D196h			
D197h			
D198h	USB FIFO Clear Register 0	USBFCLR0	XXh
D199h	USB FIFO Clear Register 1	USBFCLR1	XXh
D19Ah	USB FIFO Clear Register 2	USBFCLR2	XXh
D19Bh			
D19Ch			
D19Dh			
D19Eh			
D19Fh			
D1A0h	USB Endpoint Stall Register 0	USBEPSTL0	XXXX XXX0b
D1A1h	USB Endpoint Stall Register 1	USBEPSTL1	XXXX X000b
D1A2h	USB Endpoint Stall Register 2	USBEPSTL2	XXXX X000b
D1A3h			
D1A4h			
D1A5h			
D1A6h			
D1A7h			
D1A8h			
D1A9h	USB Stall Status Register 1	USBSTLSR1	X000 X000b
D1AAh	USB Stall Status Register 2	USBSTLSR2	X000 X000b
D1ABh			
D1ACh			
D1ADh			
D1AEh			
D1AFh			
D1B0h	USB DMA Transfer Setting Register	USBDMAR	XXX0 0X00b
D1B1h			
D1B2h			
D1B3h			
D1B4h	USB Configuration Value Register	USBCVR	0000 X000b
D1B5h			
D1B6h			
D1B7h			
D1B8h	USB Control Register	USBCTLR	0XX0 0001b
D1B9h			
D1BAh			
D1BBh			
D1BCh			
D1BDh			
D1BEh			
D1BFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

Table 4.23 SFR Information (23) (1)

Address	Register	Symbol	Reset Value
D1C0h	USB Endpoint Information Register	USBEPIR	XXh
D1C1h			
D1C2h			
D1C3h			
D1C4h			
D1C5h			
D1C6h			
D1C7h			
D1C8h			
D1C9h			
D1CAh			
D1CBh			
D1CCh	USB Module Control Register	USBMC	11X1 0000b
D1CDh			
D1CEh			
D1CFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

4.2 Notes on SFRs

4.2.1 Register Settings

Table 4.24 lists Registers with Write-Only Bits (1/2) and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM. Read-modify-write instructions can be used when writing to the no register bits.

Table 4.24 Registers with Write-Only Bits (1/2)

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0289h	UART5 Bit Rate Register	U5BRG
028Bh to 028Ah	UART5 Transmit Buffer Register	U5TB
0299h	UART4 Bit Rate Register	U4BRG
029Bh to 029Ah	UART4 Transmit Buffer Register	U4TB
02A9h	UART3 Bit Rate Register	U3BRG
02ABh to 02AAh	UART3 Transmit Buffer Register	U3TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS

Table 4.25 Registers with Write-Only Bits (2/2)

Address	Register	Symbol
D120h	USB Endpoint 0 IN Data Register	USBEPDR0I
D134h	USB Endpoint 2 Data Register	USBEPDR2
D138h	USB Endpoint 3 Data Register	USBEPDR3
D144h	USB Endpoint 5 Data Register	USBEPDR5
D148h	USB Endpoint 6 Data Register	USBEPDR6
D190h	USB Trigger Register 0	USBTRG0
D191h	USB Trigger Register 1	USBTRG1
D192h	USB Trigger Register 2	USBTRG2
D198h	USB FIFO Clear Register 0	USBFCLR0
D199h	USB FIFO Clear Register 1	USBFCLR1
D19Ah	USB FIFO Clear Register 2	USBFCLR2
D1A0h	USB Endpoint Stall Register 0	USBEPSTL0
D1A1h	USB Endpoint Stall Register 1	USBEPSTL1
D1A2h	USB Endpoint Stall Register 2	USBEPSTL2
D1C0h	USB Endpoint Information Register	USBEPIR

Table 4.26 Read-Modify-Write Instructions

Function	Mnemonic
Transfer	MOV*Dir*
Bit processing	BCLR, BM*Cnd*, BNOT, BSET, BTSTC, and BTSTS
Shifting	ROLC, RORC, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

5. Electrical Characteristics

5.1 Electrical Characteristics (Common to 3 V and 5 V)

5.1.1 Absolute Maximum Rating

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC1}	Supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to 6.5	V
V_{CC2}	Supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to V_{CC1} + 0.1 (1)	V
AV_{CC}	Analog supply voltage		$V_{CC1} = AV_{CC}$	–0.3 to 6.5	V
V_{REF}	Analog reference voltage		$V_{CC1} = AV_{CC}$	–0.3 to V_{CC1} + 0.1 (1)	V
V_I	Input voltage	$\overline{RESET}$, CNVSS, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, UVCC		–0.3 to V_{CC1} + 0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		–0.3 to V_{CC2} + 0.3 (1)	V
		P7_0, P7_1, P8_5		–0.3 to 6.5	V
V_O	Output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XOUT, UVCC		–0.3 to V_{CC1} + 0.3 (1)	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		–0.3 to V_{CC2} + 0.3 (1)	V
		P7_0, P7_1, P8_5		–0.3 to 6.5	V
P_d	Power consumption		–40°C < T_{opr} ≤ 85°C	300	mW
T_{opr}	Operating temperature	When the MCU is operating		–20 to 85/–40 to 85	°C
		Flash program erase	Program area	0 to 60	
			Data area	0 to 60	
T_{stg}	Storage temperature			–65 to 150	°C

Note:
1. Maximum value is 6.5 V.

5.1.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions (1/3)

V_{CC1} = V_{CC2} = 2.7 to 5.5 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter			Standard			Unit
				Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply voltage ($V_{CC1} \geq V_{CC2}$)		USB function is used	3.0	5.0	5.5	V
			USB function is not used	2.7	5.0	5.5	V
AV_{CC}	Analog supply voltage				V_{CC1}		V
UVCC	USB Supply Voltage (When UVCC pin is input)	USB function is used	V_{CC1} = 3.6 to 5.5V	3.0	3.3	3.6	V
			V_{CC1} = 3.0 to 3.6V	3.0	-	V_{CC1}	V
		USB function is not used	V_{CC1} = 2.7 to 5.5V	-	V_{CC1}	-	V
V_{SS}	Supply voltage				0		V
AV_{SS}	Analog supply voltage				0		V
V_{IH}	High input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7		$0.8V_{CC2}$		V_{CC2}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode)		$0.8V_{CC2}$		V_{CC2}	V
		P0_0 to P0_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor modes)		$0.5V_{CC2}$		V_{CC2}	V
		P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		$0.8V_{CC1}$		V_{CC1}	V
		P7_0, P7_1, P8_5		$0.8V_{CC1}$		6.5	V
V_{IL}	Low input voltage	P3_1 to P3_7, P4_0 to P4_7, P5_0 to P5_7		0		$0.2V_{CC2}$	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 (in single-chip mode)		0		$0.2V_{CC2}$	V
		P0_0 to P0_7, P2_0 to P2_7, P3_0 (data input in memory expansion and microprocessor mode)		0		$0.16V_{CC2}$	V
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		0		$0.2V_{CC1}$	V
$I_{OH(sum)}$	High peak output current	Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7				-40.0	mA
		Sum of $I_{OH(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7				-40.0	mA
		Sum of $I_{OH(peak)}$ at P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4				-40.0	mA
		Sum of $I_{OH(peak)}$ at P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7				-40.0	mA
$I_{OH(peak)}$	High peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7				–10.0	mA
$I_{OH(avg)}$	High average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7				–5.0	mA

Note:
1. The average output current is the mean value within 100 ms.

Table 5.3 Recommended Operating Conditions (2/3)

V_{CC1} = V_{CC2} = 2.7 to 5.5 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			80.0	mA
		Sum of $I_{OL(peak)}$ at P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_5			80.0	mA
$I_{OL(peak)}$	Low peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
$I_{OL(avg)}$	Low average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			5.0	mA
$f_{(XIN)}$	Main clock input oscillation frequency	V_{CC1} = 2.7 V to 5.5 V	2		16	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768	50	kHz
$f_{(PLL)}$	PLL clock oscillation frequency	V_{CC1} = 2.7 V to 5.5 V	10		32	MHz
$f_{(BCLK)}$	CPU operation clock		fOCO-S divided by 16		32	MHz
$t_{SU(PLL)}$	PLL frequency synthesizer stabilization wait time	V_{CC1} = 5.0 V			2	ms
		V_{CC1} = 3.0 V			3	ms

Note:
1. The average output current is the mean value within 100 ms.

Table 5.4 Recommended Operating Conditions (3/3)(1)

V_{CC1} = 2.7 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.
The ripple voltage must not exceed $V_{r(VCC1)}$ and/or $dV_{r(VCC1)}/dt$.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$V_{r(VCC1)}$	Allowable ripple voltage	V_{CC1} = 5.0 V			0.5	Vp-p
		V_{CC1} = 3.0 V			0.3	Vp-p
$dV_{r(VCC1)}/dt$	Ripple voltage falling gradient	V_{CC1} = 5.0 V			0.3	V/ms
		V_{CC1} = 3.0 V			0.3	V/ms

Note:
1. The device is operationally guaranteed under these operating conditions.

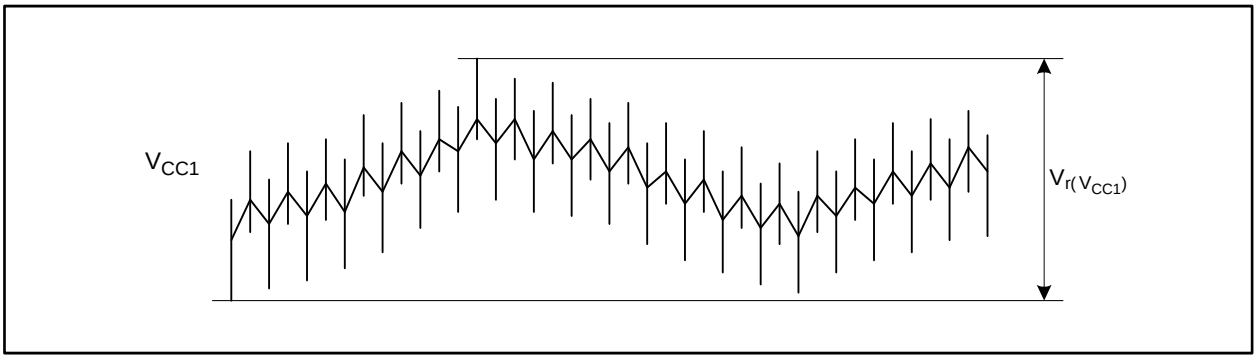


Figure 5.1 Ripple Waveform

5.1.3 A/D Conversion Characteristics

Table 5.5 A/D Conversion Characteristics (1/2) (1, 2)

$AV_{CC} = V_{CC1} = V_{CC2} = V_{REF}$ = 3.0 to 5.5 V, $V_{SS} = AV_{SS}$ = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
-	Resolution		$AV_{CC} = V_{CC1} = V_{CC2} = V_{REF}$				10	Bits
I_{NL}	Integral non-linearity error	10 bits	V_{CC1} = 5.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 3)			±3	LSB
			V_{CC1} = 3.3 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 3)			±3	LSB
			V_{CC1} = 3.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 3)			±3	LSB
-	Absolute accuracy	10 bits	V_{CC1} = 5.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 3)			±3	LSB
			V_{CC1} = 3.3 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 3)			±3	LSB
			V_{CC1} = 3.0 V	AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input, ANEX0, ANEX1 input (Note 3)			±3	LSB

Notes:
1. This applies when using one A/D converter, with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby).
2. Use when $AV_{CC} = V_{CC1} = V_{CC2}$.
3. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.2 “A/D Accuracy Measure Circuit”.

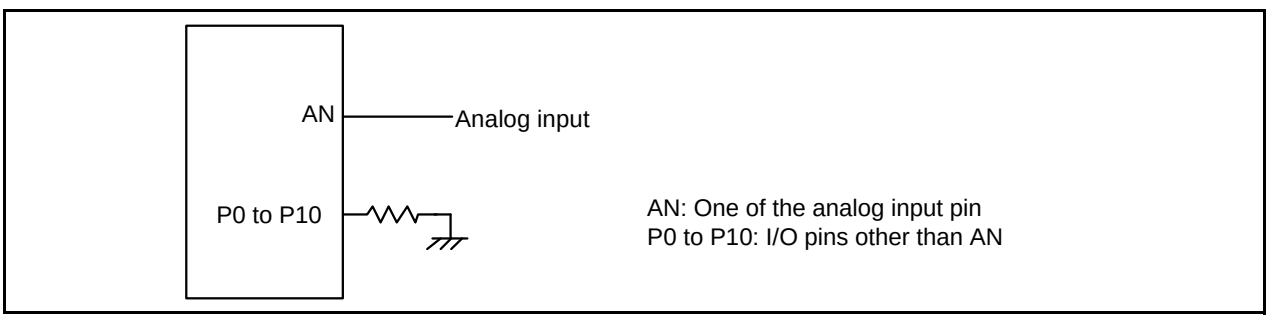


Figure 5.2 A/D Accuracy Measure Circuit

Table 5.6 A/D Conversion Characteristics (2/2) (1, 2)

$AV_{CC} = V_{CC1} = V_{CC2} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
ϕAD	A/D operating clock frequency	4.0 V ≤ V_{REF} ≤ AV_{CC} ≤ 5.5 V	2		25	MHz
		3.2 V ≤ V_{REF} ≤ AV_{CC} ≤ 5.5 V	2		16	MHz
		3.0 V ≤ V_{REF} ≤ AV_{CC} ≤ 5.5 V	2		10	MHz
-	Tolerance level impedance			3		kΩ
D_{NL}	Differential non-linearity error	(5)			±1	LSB
-	Offset error	(5)			±3	LSB
-	Gain error	(5)			±3	LSB
t_{CONV}	10-bit conversion time	V_{CC1} = 5 V, ϕAD = 25 MHz	1.60			µs
t_{SAMP}	Sampling time		0.60			µs
V_{REF}	Reference voltage		3.0		AV_{CC}	V
V_{IA}	Analog input voltage (3), (4)		0		V_{REF}	V

Notes:
1. This applies when using one A/D converter, with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby).
2. Use when $AV_{CC} = V_{CC1} = V_{CC2}$.
3. Do not use A/D converter when $V_{CC1} > V_{CC2}$.
4. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
5. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.2 “A/D Accuracy Measure Circuit”.

5.1.4 D/A Conversion Characteristics

Table 5.7 D/A Conversion Characteristics

$V_{CC1} = AV_{CC} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				2.5	LSB
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		5	6	8.2	kΩ
I_{VREF}	Reference Power Supply Input Current	See Notes 1 and 2			1.5	mA

Notes:
1. This applies when using one D/A converter, with the D/A register for the unused D/A converter set to 00h.
2. The current consumption of the A/D converter is not included. Also, the I_{VREF} of the D/A converter will flow even if the ADSTBY bit in the ADCON1 register is 0 (A/D operation stopped (standby)).

5.1.5 USB Characteristics

Table 5.8 USB Characteristics

V_{CC1} = 3.0 to 5.5 V, UVCC = 3.0 to 3.6 V, at T_{opr} = -20°C to 85°C / -40°C to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{IH}	Input Characteristics	High Input Voltage	Figure 5.3, Figure 5.4	2.0	-	-	V
V_{IL}		Low Input Voltage		-	-	0.8	V
V_{DI}		Differential Input Sensitivity		0.2	-	-	V
V_{CM}		Differential Common Mode Range		0.8	-	2.5	V
V_{OH}	Output Characteristics	High Output Voltage	Figure 5.3, Figure 5.4 I_{OH} = 200 µA	2.8	-	-	V
V_{OL}		Low Output Voltage	Figure 5.3, Figure 5.4 I_{OL} = 2 mA	-	-	0.3	V
V_{CRS}		Crossover Voltage	Figure 5.3, Figure 5.4	1.3	-	2.0	V
t_R		Rise Time	Figure 5.3, Figure 5.4	4.0	-	20.0	ns
t_F		Fall Time	Figure 5.3, Figure 5.4	4.0	-	20.0	ns
t_{RFM}		Rise Time / Fall Time Matching	Figure 5.3, Figure 5.4 (t_R/t_F)	90.0	-	111.1	%
Z_{DRV}		Output Resistance	Figure 5.3, Figure 5.4 Includes R_S = 27 Ω	28.0	-	44.0	W
UV_{CC}	UVCC Output Voltage	V_{CC1} = 4.0 to 5.5V, PXXCON = VDDUSBE = 1		3.0	3.3	3.6	V
		PXXCON = 0		-	V_{CC1}	-	V
I_{susp}	Consumption current of the Internal Power Supply for USB		V_{CC1} = 4.0 to 5.5 V UV_{CC} to V_{SS} 0.33 µF V_{CC1} to V_{SS} 0.1 µF		50		µA

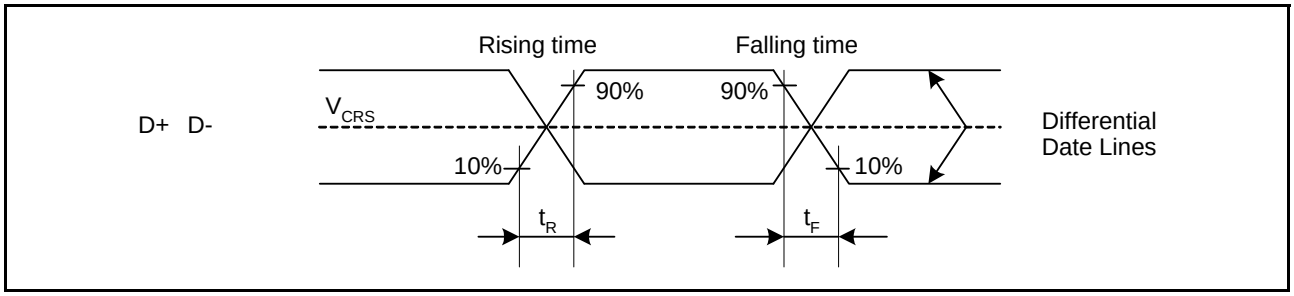


Figure 5.3 Data Signal Timing Diagram

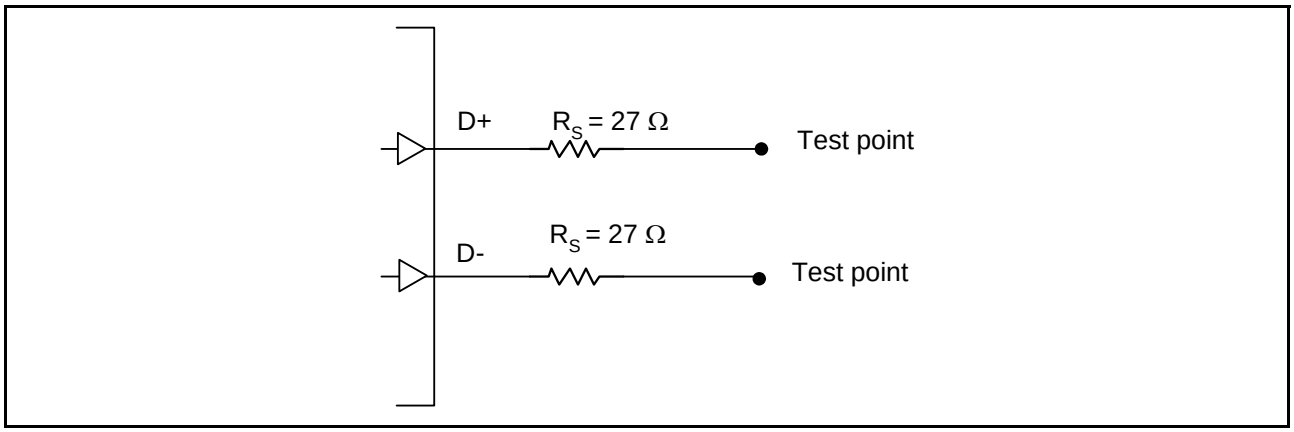


Figure 5.4 Load Condition

5.1.6 Flash Memory Electrical Characteristics

Table 5.9 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				10 (1)	MHz
f(SLOW_R)	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC(32.768)	35	kHz
-	Data flash read	2.7 V ≤ V_{CC1} ≤ 3.0 V			16 (2)	MHz
		3.0 V < V_{CC1} ≤ 5.5 V			20 (2)	MHz

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

Table 5.10 Flash Memory (Program ROM 1, 2) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = 0°C to 60°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	1,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		150	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		70	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage	T_{opr}= -20°C to 85°C/-40°C to 85°C	2.7		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles:
   The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.11 Flash Memory (Data Flash) Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1), (3), (4)	V_{CC1} = 3.3 V, T_{opr} = 25°C	10,000 (2)			times
-	2 word program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		300	4000	µs
-	Lock bit program time	V_{CC1} = 3.3 V, T_{opr} = 25°C		140	3000	µs
-	Block erase time	V_{CC1} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact a Renesas Electronics sales office.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

5.1.7 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 5.12 Voltage Detector 0 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)	When V_{CC1} is falling.	1.60	1.90	2.20	V
	Voltage detection level Vdet0_2 (1)	When V_{CC1} is falling.	2.70	2.85	3.15	V
-	Voltage detector 0 response time (3)	When V_{CC1} falls from 5 V to (Vdet0_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC25 = 1, V_{CC1} = 5.0 V		1.5		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (2)				100	µs

Notes:
1. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
3. Time from when passing the V_{det0} until when a voltage monitor 0 reset is generated.

Table 5.13 Voltage Detector 1 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1	When V_{CC} is falling	2.95	3.25	3.55	V
-	Hysteresis width when V_{CC1} of voltage detector 1 is rising			0.15		V
-	Voltage detector 1 response time (2)	When V_{CC1} falls from 5 V to (Vdet1_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC26 = 1, V_{CC1} = 5.0 V		1.7		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)				100	µs

Notes:
1. Necessary time until the voltage detector operates when setting to 1 again after setting the VC26 bit in the VCR2 register to 0.
2. Time from when passing the V_{det1} until when a voltage monitor 1 reset is generated.

Table 5.14 Voltage Detector 2 Electrical Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	When V_{CC1} is falling	3.70	4.00	4.30	V
-	Hysteresis width at the rising of V_{CC1} in voltage detector 2			0.15		V
-	Voltage detector 2 response time (2)	When V_{CC1} falls from 5 V to (Vdet2_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC27 = 1, V_{CC1} = 5.0 V		1.7		µA
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)				100	µs

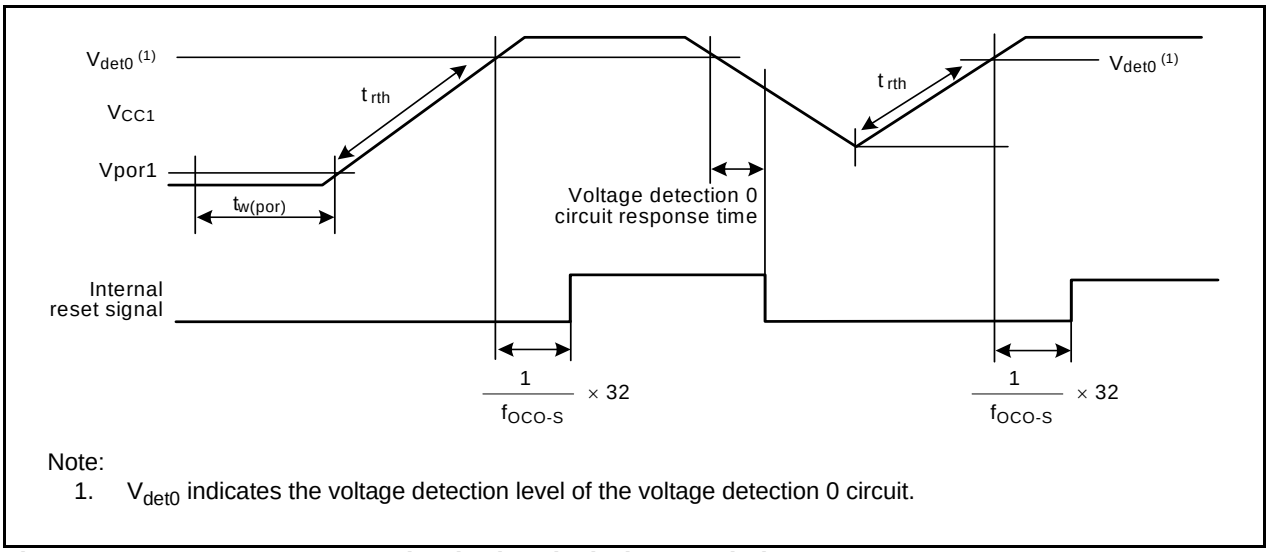
Notes:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.
2. Time from when passing the V_{det2} until when a voltage monitor 2 reset is generated.

Table 5.15 Power-On Reset Circuit

The measurement condition is V_{CC1} = 2.0 to 5.5 V, T_{opr} = -20°C to 85°C/ -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Voltage at which power-on reset enabled (1)				0.5	V
t_{rth}	External power V_{CC1} rise gradient		2.0		50000	mV/ms
$t_{w(por)}$	Time necessary to enable power-on reset		300			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0. Also, set the VDSEL1 bit to 0 (Vdet0_2).



Note:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit.

Figure 5.5 Power-On Reset Circuit Electrical Characteristics

Table 5.16 Power Supply Circuit Timing Characteristics

The measurement condition is V_{CC1} = 2.7 to 5.5 V and T_{opr} = 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply stability time when power is on (1)				5	ms
$t_{d(R-S)}$	STOP release time				150	µs
$t_{d(W-S)}$	Low power mode wait mode release time				150	µs

Note:
1. Waiting time until the internal power supply generator stabilizes when power is on.

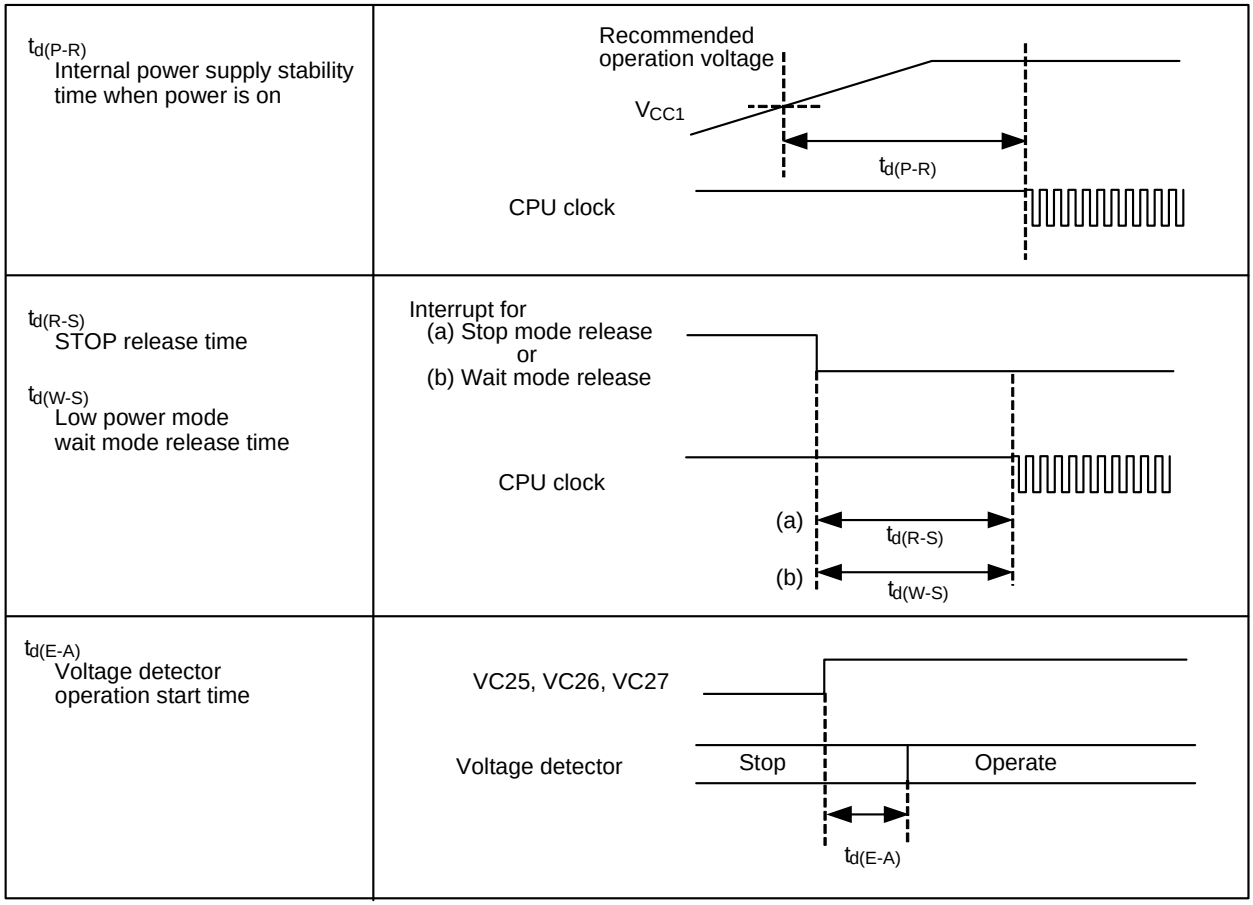


Figure 5.6 Power Supply Circuit Timing Diagram

5.1.8 Oscillator Electrical Characteristics

Table 5.17 40 MHz On-Chip Oscillator Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V, T_{opr} = -20°C to 85°C/-40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO40M}	40 MHz on-chip oscillator frequency	Average frequency in a 10 ms period	36	40	44	MHz
tsu(f_{OCO40M})	Wait time until 40 MHz on-chip oscillator stabilizes				2	ms

Table 5.18 125 kHz On-Chip Oscillator Electrical Characteristics

V_{CC1} = 2.7 to 5.5 V, T_{opr} = –20°C to 85°C/–40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO-S}	125 kHz on-chip oscillator frequency	Average frequency in a 10 ms period	100	125	150	kHz
tsu(f_{OCO-S})	Wait time until 125 kHz on-chip oscillator stabilizes				20	µs

5.2 Electrical Characteristics (V_{CC1} = V_{CC2} = 5 V)

5.2.1 Electrical Characteristics

V_{CC1} = V_{CC2} = 5 V

Table 5.19 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 4.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = –20°C to 85°C/–40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –5 mA	V_{CC1} – 2.0		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –5 mA	V_{CC2} – 2.0		V_{CC2}	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –200 µA	V_{CC1} – 0.3		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –200 µA	V_{CC2} – 0.3		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGH POWER	I_{OH} = –1 mA	V_{CC1} – 2.0		V_{CC1}	V
			LOW POWER	I_{OH} = –0.5 mA	V_{CC1} – 2.0		V_{CC1}	
	High output voltage XCOUT		HIGH POWER	With no load applied		2.6		V
			LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 5 mA			2.0	
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 200 µA			0.45	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 200 µA			0.45	
V_{OL}	Low output voltage XOUT		HIGH POWER	I_{OL} = 1 mA			2.0	V
			LOW POWER	I_{OL} = 0.5 mA			2.0	
	Low output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.20 Electrical Characteristics (2) (1)

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/–40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS5}$, SCL0 to SCL5, SDA0 to SDA5, CLK0 to CLK5, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD5, $\overline{SD}$, SCLMM, SDAMM, ZP, IDU, IDV, IDW		0.5		2.0	V
$V_{T+} - V_{T-}$	Hysteresis	$\overline{RESET}$		0.5		2.5	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS	V_I = 5 V			5.0	µA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS	V_I = 0 V			–5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	V_I = 0 V	30	50	100	kΩ
R_{fXIN}	Feedback resistance XIN				1.5		MΩ
R_{fXCIN}	Feedback resistance XCIN				8		MΩ
V_{RAM}	RAM retention voltage		In stop mode	1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 Vor 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 5\ V$

Table 5.21 Electrical Characteristics (3)

$V_{CC1} = V_{CC2} = 4.2$ to 5.5 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/−40°C to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 32 MHz XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		27.0		mA
			$f_{(BCLK)}$ =32 MHz, A/D conversion (2) XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		27.7		mA
			$f_{(BCLK)}$ = 16 MHz XIN = 16 MHz (square wave) 125 kHz on-chip oscillator stopped		13.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 ($f_{(BCLK)}$ = 10 MHz) 125 kHz on-chip oscillator stopped		17.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped, 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		500.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 kHz In low-power mode FMR22 = FMR23 = 1 On flash memory (1)		160.0		µA
			$f_{(BCLK)}$ = 32 kHz In low-power mode On RAM (1)		45.0		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		21.0		µA
			$f_{(XCIN)}$ = 32 kHz (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		11.0		µA
			$f_{(XCIN)}$ = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		6.0		µA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		2.2		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 5.0 V		30.0		mA

Notes:
1. This indicates the memory in which the program to be executed exists.
2. This applies when using one A/D converter (fAD = 25MHz), with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby).

$V_{CC1} = V_{CC2} = 5\ V$

5.2.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.22 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

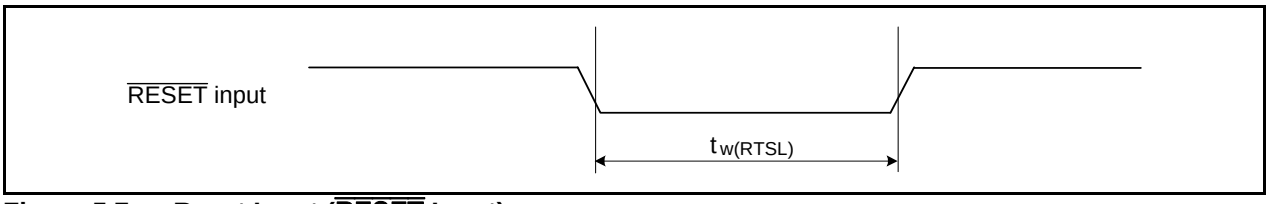


Figure 5.7 Reset Input ($\overline{\text{RESET}}$ Input)

5.2.2.2 External Clock Input

Table 5.23 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 3.0$ to 5.0 V.

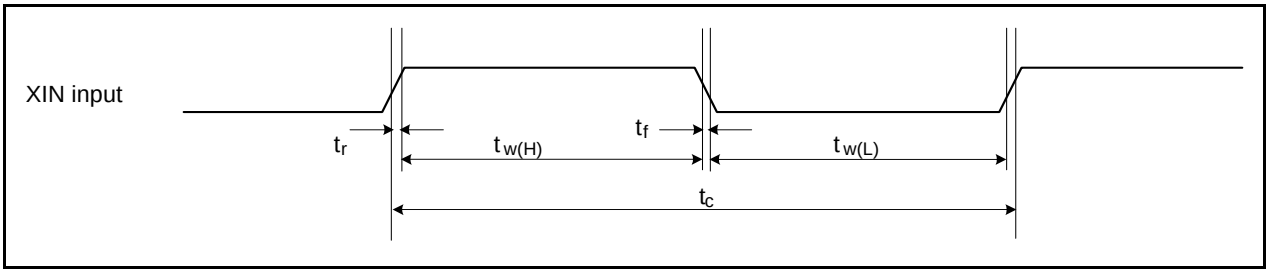


Figure 5.8 External Clock Input (XIN Input)

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.3 Timer A Input

Table 5.24 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

Table 5.25 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

Table 5.26 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

Table 5.27 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

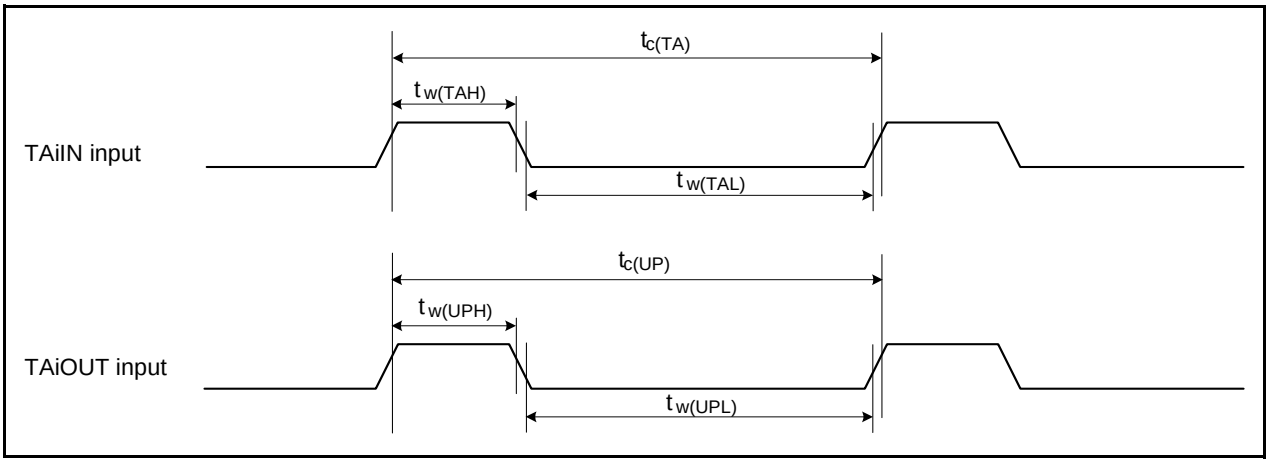


Figure 5.9 Timer A Input

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

Table 5.28 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

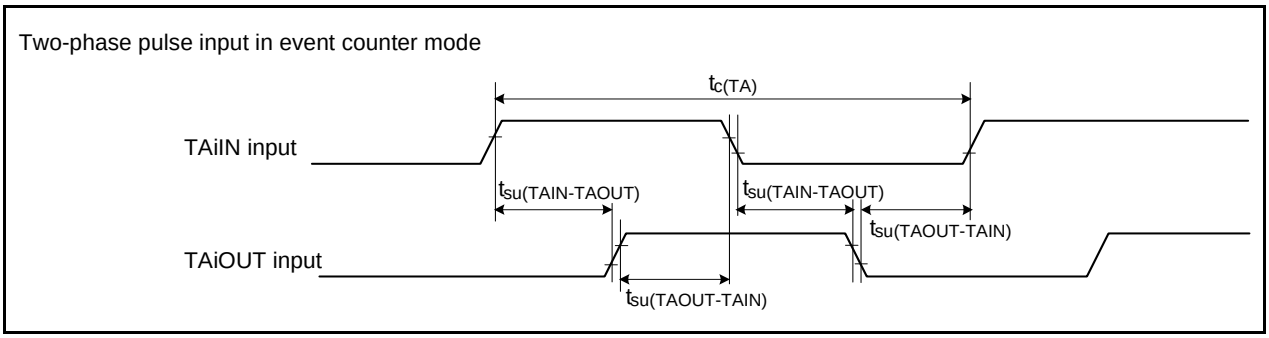


Figure 5.10 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.4 Timer B Input

Table 5.29 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	80		ns

Table 5.30 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

Table 5.31 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

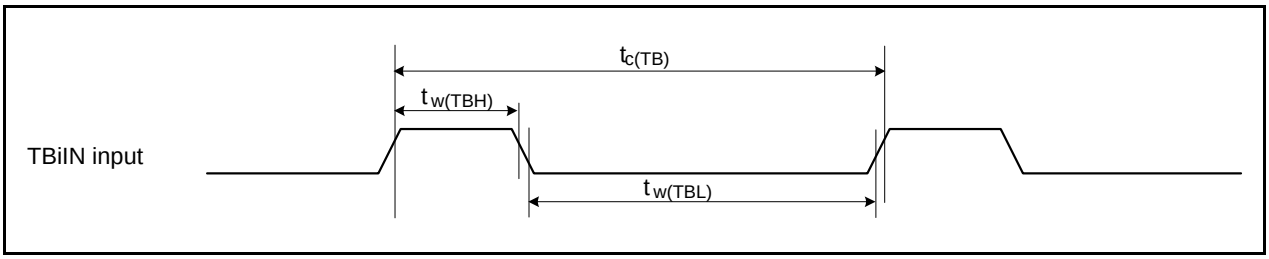


Figure 5.11 Timer B Input

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

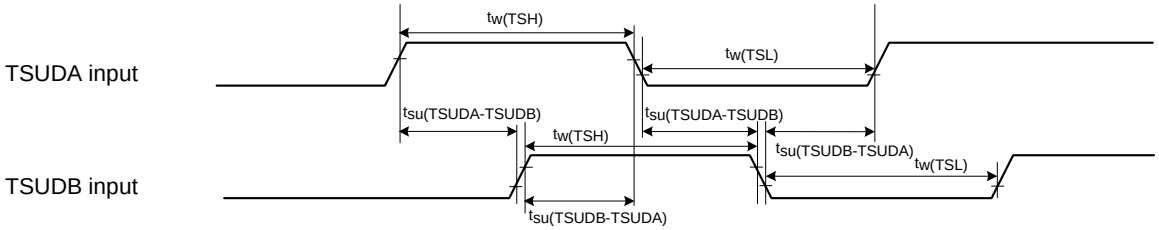
($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to $85°C/-40°C$ to $85°C$ unless otherwise specified)

5.2.2.5 Timer S Input

Table 5.32 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:

1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 5.12 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.6 Serial Interface

Table 5.33 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high pulse width	100		ns
$t_{w(CKL)}$	CLKi input low pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

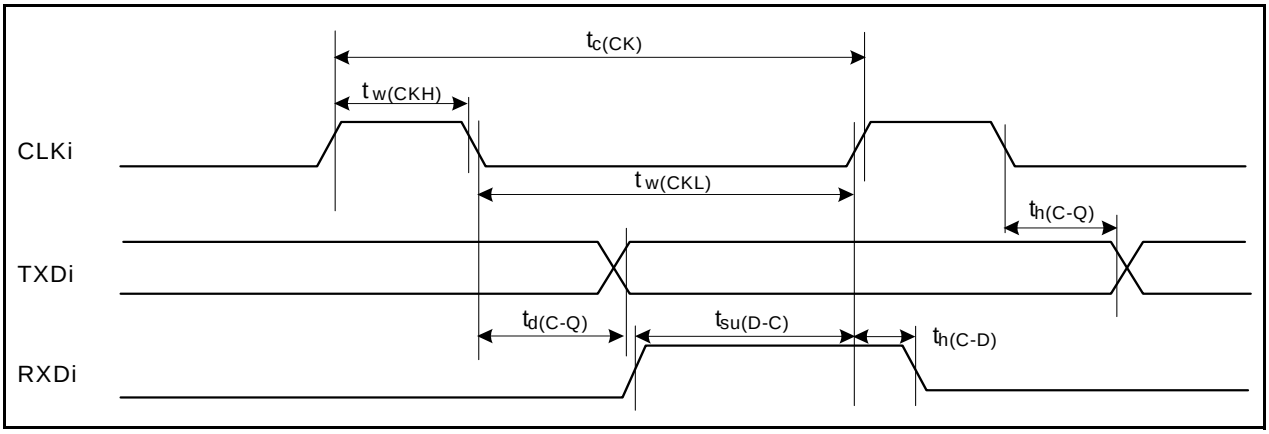


Figure 5.13 Serial Interface

5.2.2.7 External Interrupt $\overline{INTi}$ Input

Table 5.34 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	250		ns

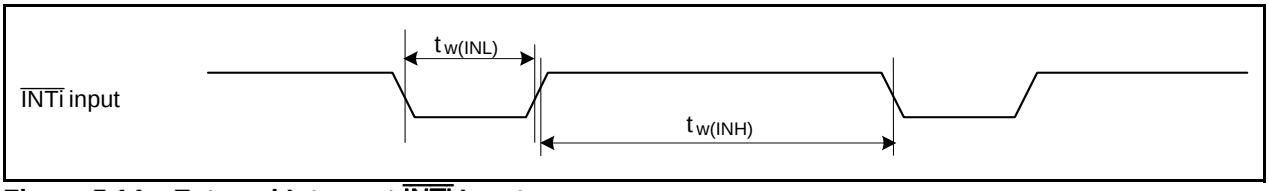


Figure 5.14 External Interrupt $\overline{INTi}$ Input

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.2.8 Multi-master I²C-bus

Table 5.35 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

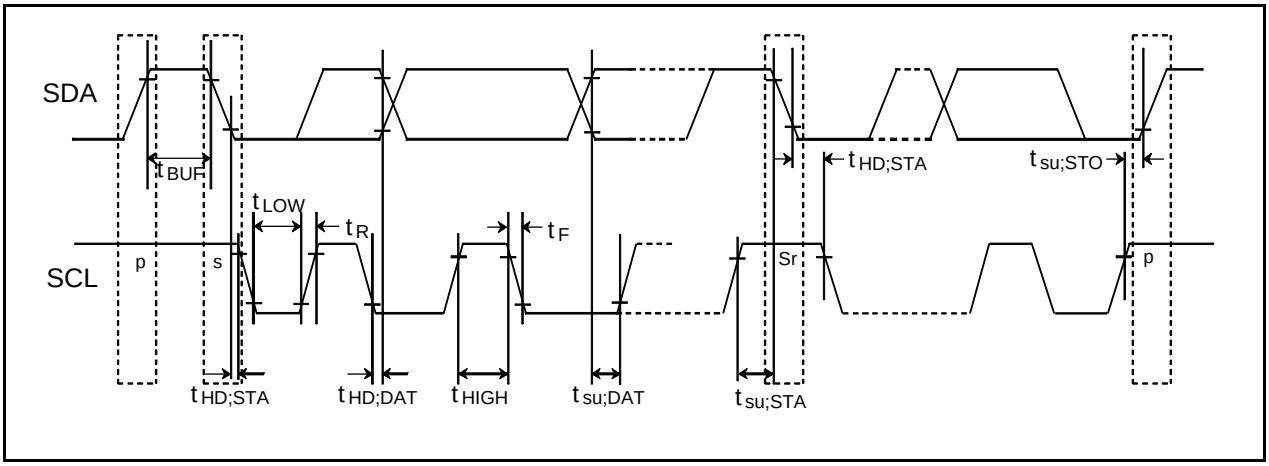


Figure 5.15 Multi-master I²C-bus

$V_{CC1} = V_{CC2} = 5\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.2.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

Table 5.36 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with 1 to 3 waits)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	80		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 45[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 45[ns]$$ n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.

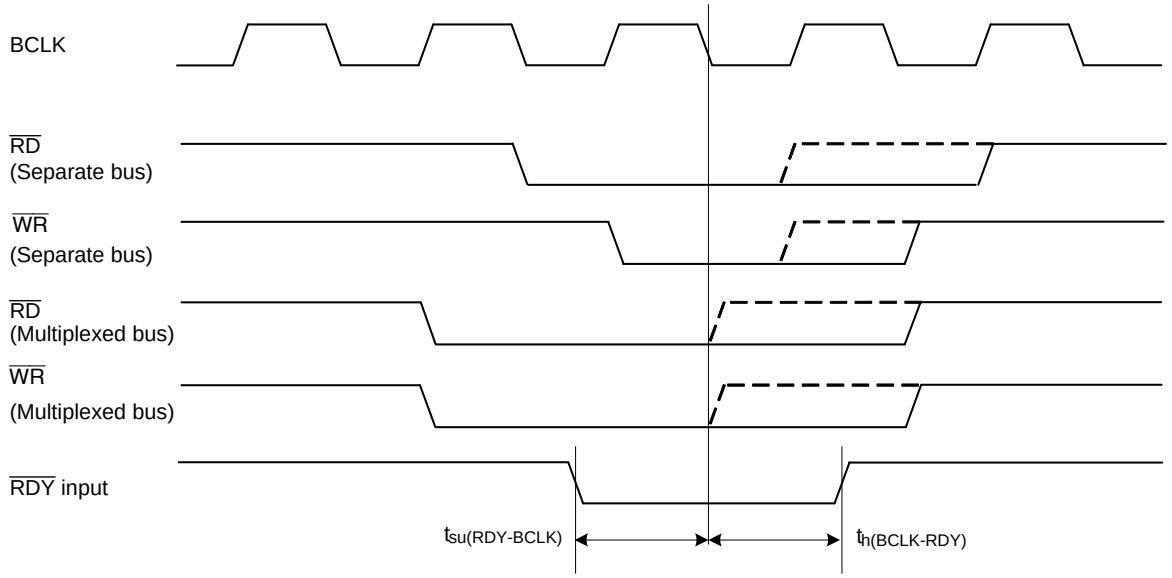
3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 45[ns]$$ n is 2 for 2 waits setting, and 3 for 3 waits setting.

Memory Expansion Mode and Microprocessor Mode

$V_{CC1} = V_{CC2} = 5\ V$

(Effective in wait state setting**)**



Measuring conditions

- $V_{CC1} = V_{CC2} = 5\ V$
- Input timing voltage: $V_{IL} = 1.0\ V$, $V_{IH} = 4.0\ V$
- Output timing voltage: $V_{OL} = 2.5\ V$, $V_{OH} = 2.5\ V$

Figure 5.16 Timing Diagram

$V_{CC1} = V_{CC2} = 5\ V$

5.2.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.1 In No Wait State Setting

Table 5.37 Memory Expansion Mode and Microprocessor Mode (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.17		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

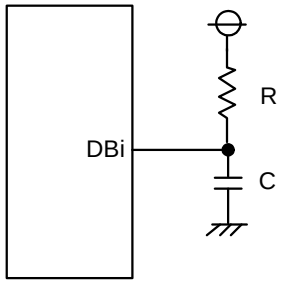
1. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$ $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
   $t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
   = 6.7 ns.



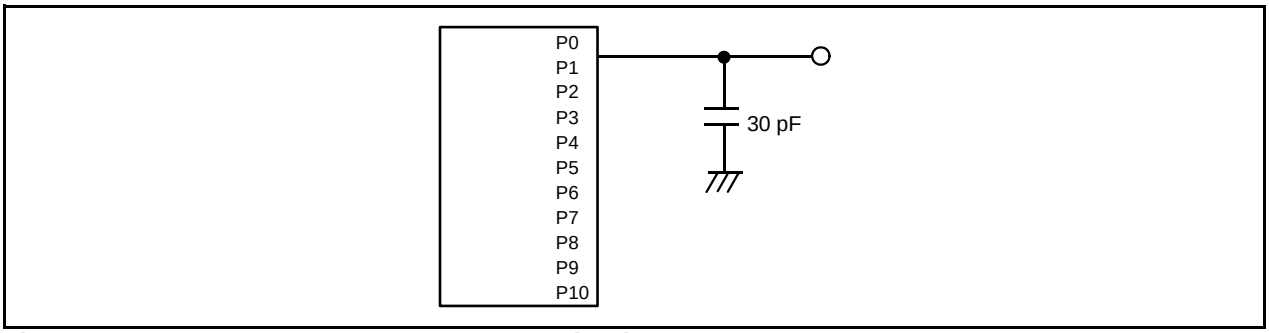
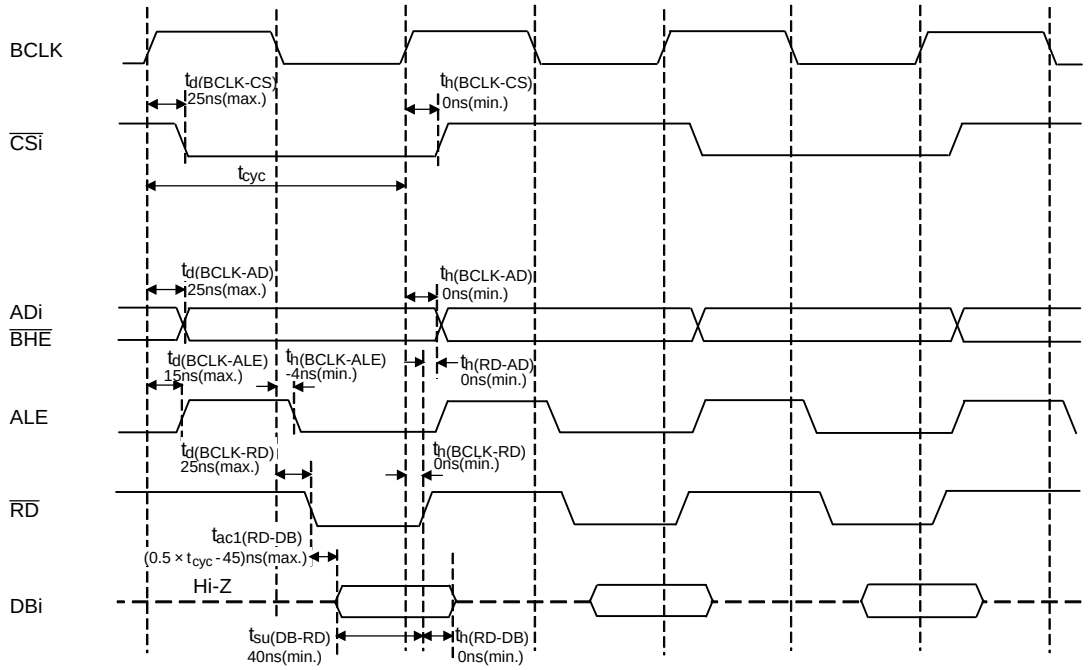


Figure 5.17 Ports P0 to P10 Measurement Circuit

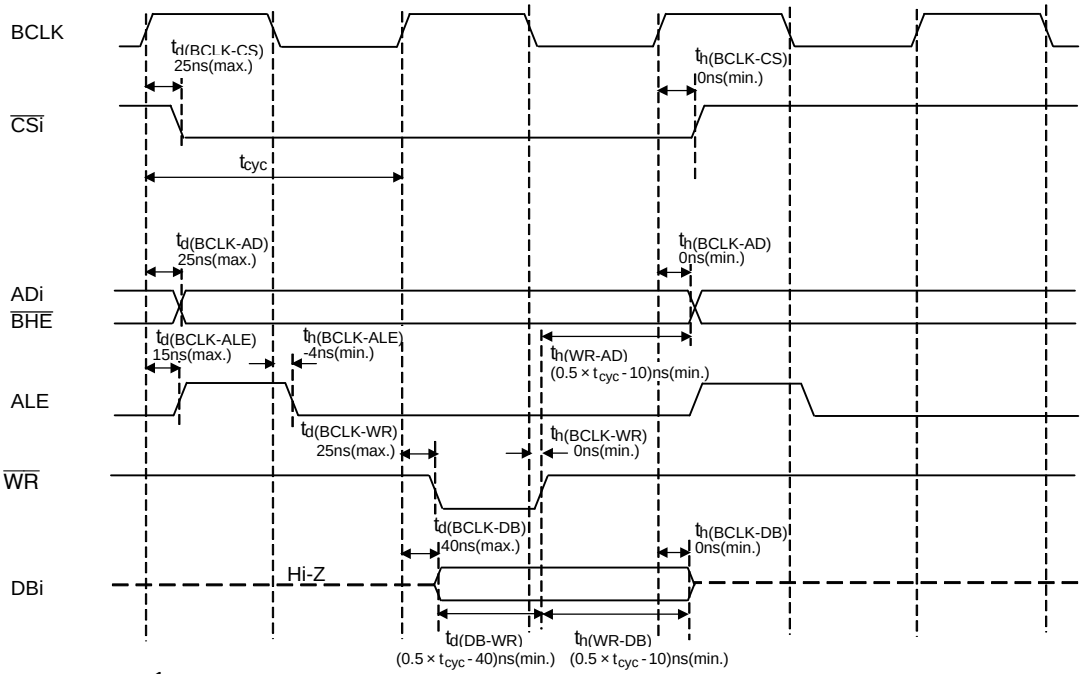
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$V_{CC1} = V_{CC2} = 5V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

Figure 5.18 Timing Diagram

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.2 In 1 to 3 Waits Setting and When Accessing External Area

Table 5.38 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.17		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)(3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

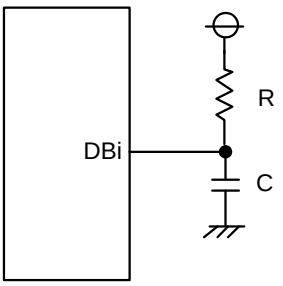
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

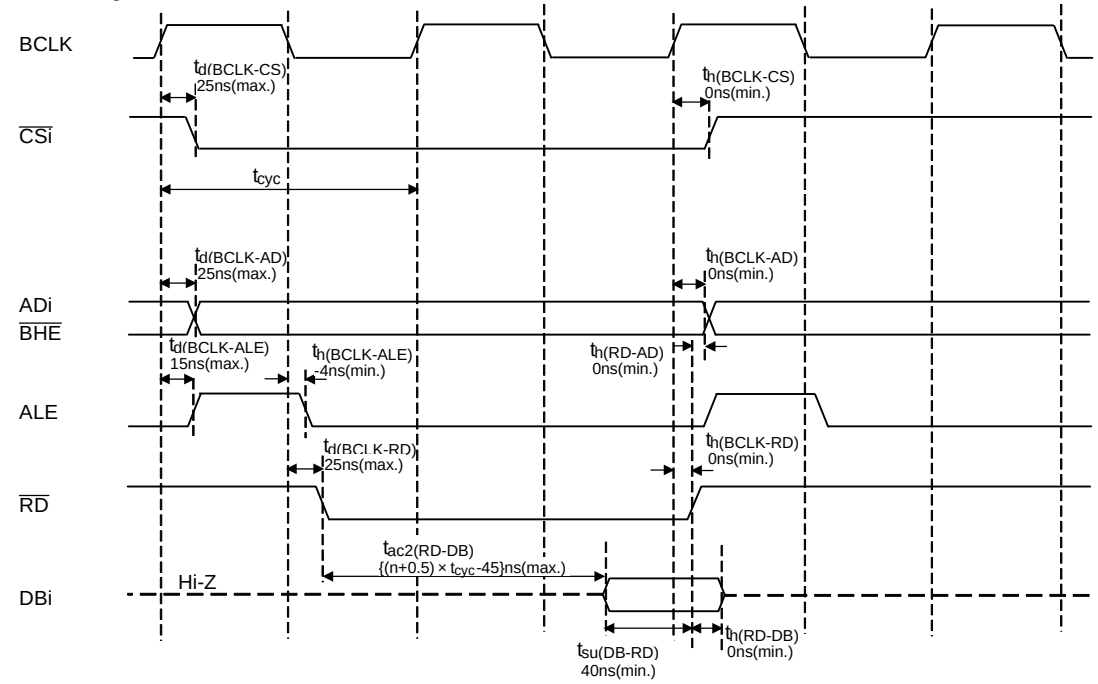
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



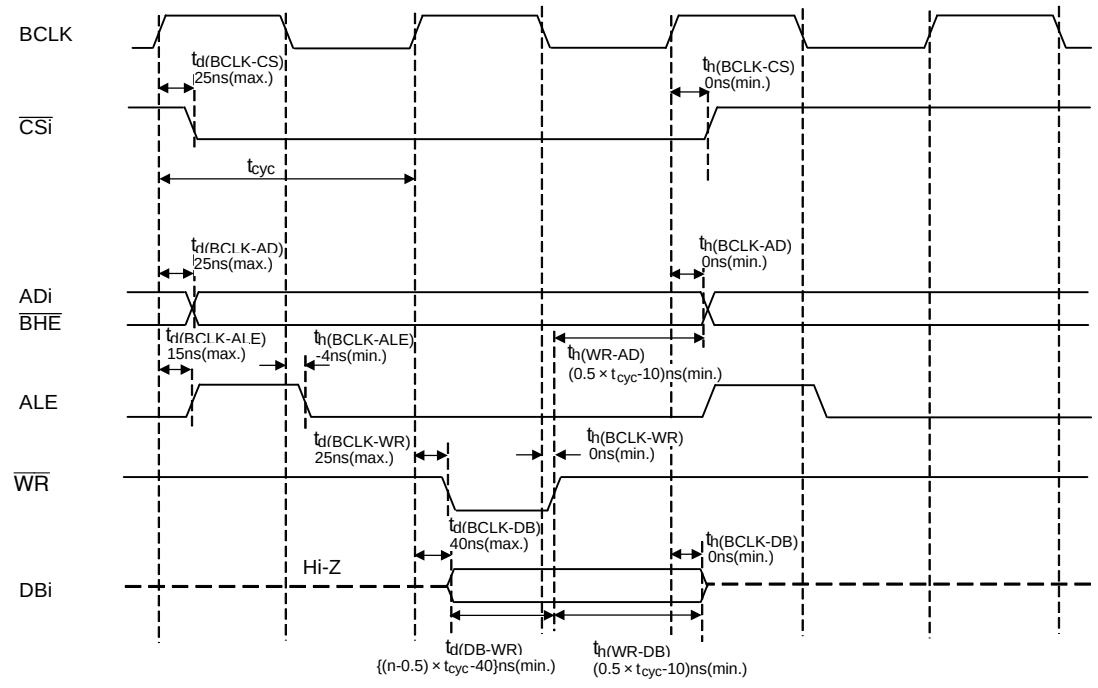
Memory Expansion Mode and Microprocessor Mode
(in 1 to 3 waits setting and when accessing external area)

$V_{CC1} = V_{CC2} = 5V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

n: 1 (when 1 wait)
2 (when 2 waits)
3 (when 3 waits)

Figure 5.19 Timing Diagram

$V_{CC1} = V_{CC2} = 5\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 5$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.2.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.39 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.17		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			15	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of address		0		ns
$t_{dz(RD-AD)}$	Address output floating start time			8	ns

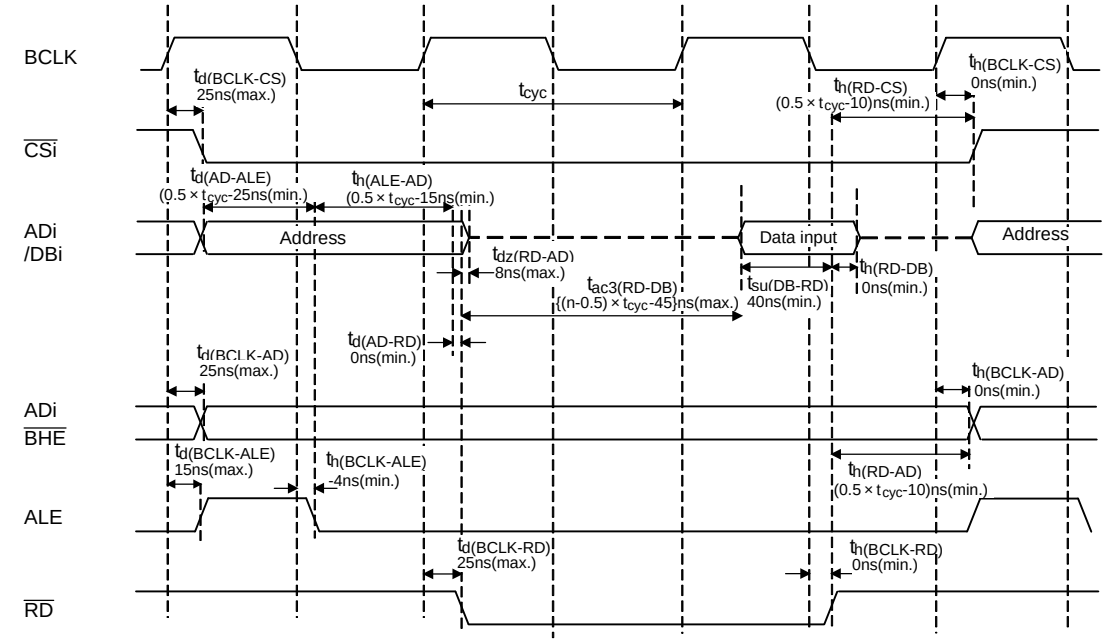
Notes:

1. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$$
2. Calculated according to the BCLK frequency as follows:
$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 40[ns]$$
n is 2 for 2-wait setting, 3 for 3-wait setting.
3. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 25[ns]$$
4. Calculated according to the BCLK frequency as follows:
$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$$
5. When using multiplex bus, set $f_{(BCLK)}$ 12.5 MHz or less.

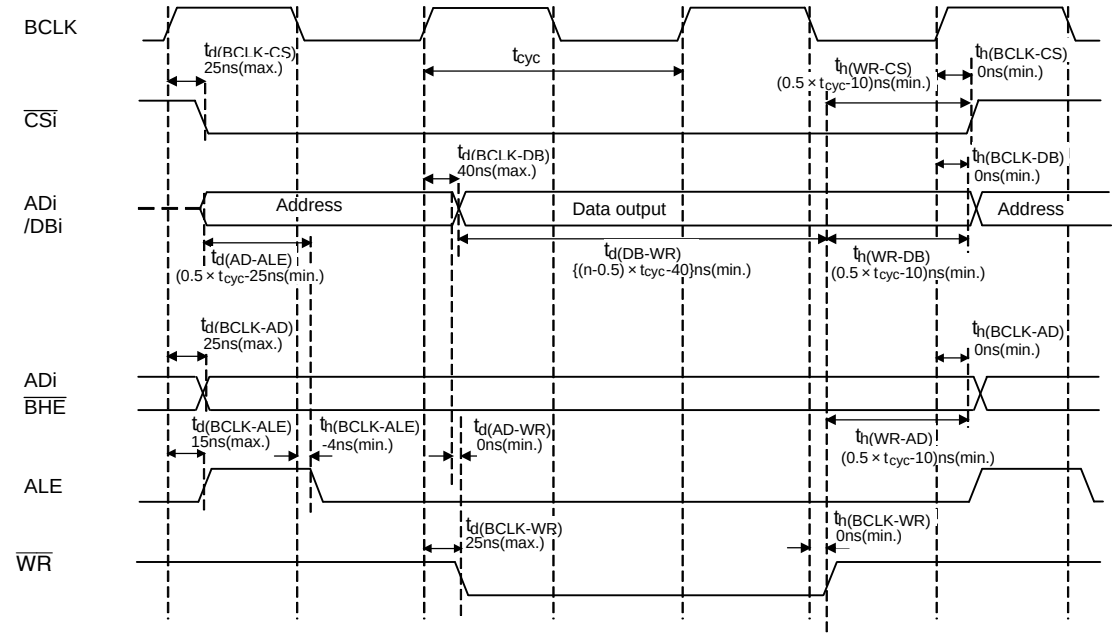
Memory Expansion Mode and Microprocessor Mode
(in 2 or 3 waits setting, and when accessing external area and using multiplexed bus)

$V_{CC1} = V_{CC2} = 5V$

Read timing



Write timing



Measuring conditions

- $V_{CC1} = V_{CC2} = 5V$
- Input timing voltage: $V_{IL} = 0.8$ V, $V_{IH} = 2.0$ V
- Output timing voltage: $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V

n: 2 (when 2 waits)
3 (when 3 waits)

Figure 5.20 Timing Diagram

5.3 Electrical Characteristics (V_{CC1} = V_{CC2} = 3 V)

5.3.1 Electrical Characteristics

VCC1 = VCC2 = 3 V

Table 5.40 Electrical Characteristics (1) [1]

V_{CC1} = V_{CC2} = 2.7 to 3.3 V, V_{SS} = 0 V at T_{opr} = -20°C to 85°C/-40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	High output voltage	P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OH} = –1 mA	V_{CC1} – 0.5		V_{CC1}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OH} = –1 mA	V_{CC2} – 0.5		V_{CC2}	
V_{OH}	High output voltage XOUT		HIGH POWER	I_{OH} = –0.1 mA	V_{CC1} – 0.5		V_{CC1}	V
			LOW POWER	I_{OH} = –50 µA	V_{CC1} – 0.5		V_{CC1}	
	High output voltage XCOUT		HIGH POWER	With no load applied		2.6		V
			LOW POWER	With no load applied		2.2		
V_{OL}	Low output voltage	P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7		I_{OL} = 1 mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7		I_{OL} = 1 mA			0.5	
V_{OL}	Low output voltage XOUT		HIGH POWER	I_{OL} = 0.1 mA			0.5	V
			LOW POWER	I_{OL} = 50 µA			0.5	
	Low output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN to TA4IN, TB0IN to TB5IN, $\overline{INT0}$ to $\overline{INT7}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS5}$, SCL0 to SCL5, SDA0 to SDA5, CLK0 to CLK5, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD5, $\overline{SD}$, SCLMM, SDAMM, ZP, IDU, IDV, IDW			0.2		1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	High input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 3 V			4.0	µA
I_{IL}	Low input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 0 V			–4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7		V_I = 0 V	50	80	150	kΩ
R_{fXIN}	Feedback resistance XIN					3.0		MΩ
R_{fXCIN}	Feedback resistance XCIN					16		MΩ
V_{RAM}	RAM retention voltage			In stop mode	1.8			V

Note:
1. When $V_{CC1} \neq V_{CC2}$, refer to 5 V or 3 V standard depending on the voltage.

$V_{CC1} = V_{CC2} = 3$ V

Table 5.41 Electrical Characteristics (2)

$V_{CC1} = V_{CC2} = 2.7$ to 3.3 V, $V_{SS} = 0$ V at $T_{opr} = -20°C$ to 85°C/–40°C to 85°C, $f_{(BCLK)} = 32$ MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current In single-chip, mode, the output pin are open and other pins are V_{SS}	High-speed mode	$f_{(BCLK)}$ = 32 MHz XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		27.0		mA
			$f_{(BCLK)}$ = 32 MHz (2) XIN = 4 MHz (square wave), PLL multiplied by 8 125 kHz on-chip oscillator stopped		27.7		mA
			$f_{(BCLK)}$ = 16 MHz XIN = 16 MHz (square wave) 125 kHz on-chip oscillator stopped		13.0		mA
		40 MHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator on, divide-by-4 ($f_{(BCLK)}$ = 10 MHz) 125 kHz on-chip oscillator stopped		17.0		mA
		125 kHz on-chip oscillator mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		450.0		µA
		Low-power mode	$f_{(BCLK)}$ = 32 MHz In low-power mode FMR 22 = FMR23 = 1 On flash memory (1)		160.0		µA
			$f_{(BCLK)}$ = 32 MHz In low-power mode On RAM (1)		40.0		µA
		Wait mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator on Peripheral clock operating T_{opr} = 25°C		20.0		µA
			$f_{(XCIN)}$ = 32 MHz (oscillation capacity High) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		8.0		µA
			$f_{(XCIN)}$ = 32 kHz (oscillation capacity Low) 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock operating T_{opr} = 25°C		6.0		µA
		Stop mode	Main clock stopped 40 MHz on-chip oscillator stopped 125 kHz on-chip oscillator stopped Peripheral clock stopped T_{opr} = 25°C		2.0		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 3.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC1} = 3.0 V		30.0		mA

Notes:
1. This indicates the memory in which the program to be executed exists.
2. This applies when using one A/D converter (fAD = 25MHz), with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby).

$V_{CC1} = V_{CC2} = 3\ V$

5.3.2 Timing Requirements (Peripheral Functions and Others)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.42 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

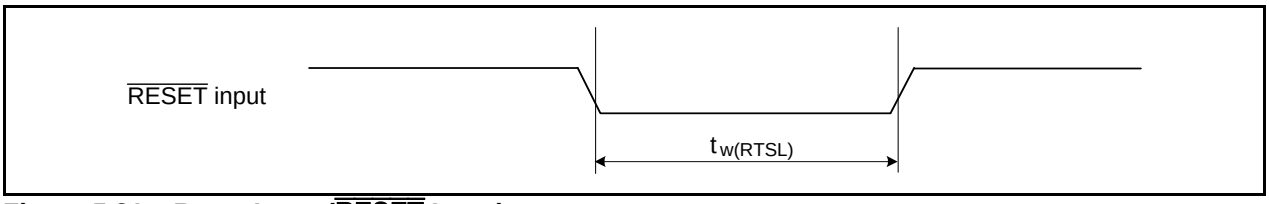


Figure 5.21 Reset Input ($\overline{\text{RESET}}$ Input)

5.3.2.2 External Clock Input

Table 5.43 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is $V_{CC1} = V_{CC2} = 2.7$ to 3.0 V.

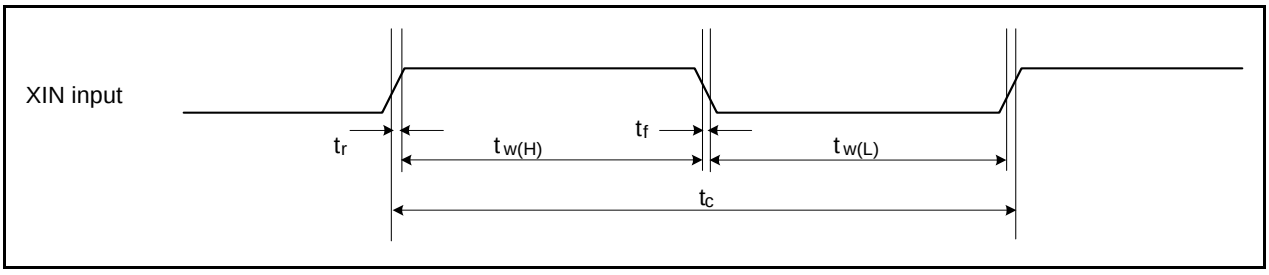


Figure 5.22 External Clock Input (XIN Input)

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.3 Timer A Input

Table 5.44 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

Table 5.45 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

Table 5.46 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

Table 5.47 Timer A Input (External Trigger Input in Pulse Width Modulation Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

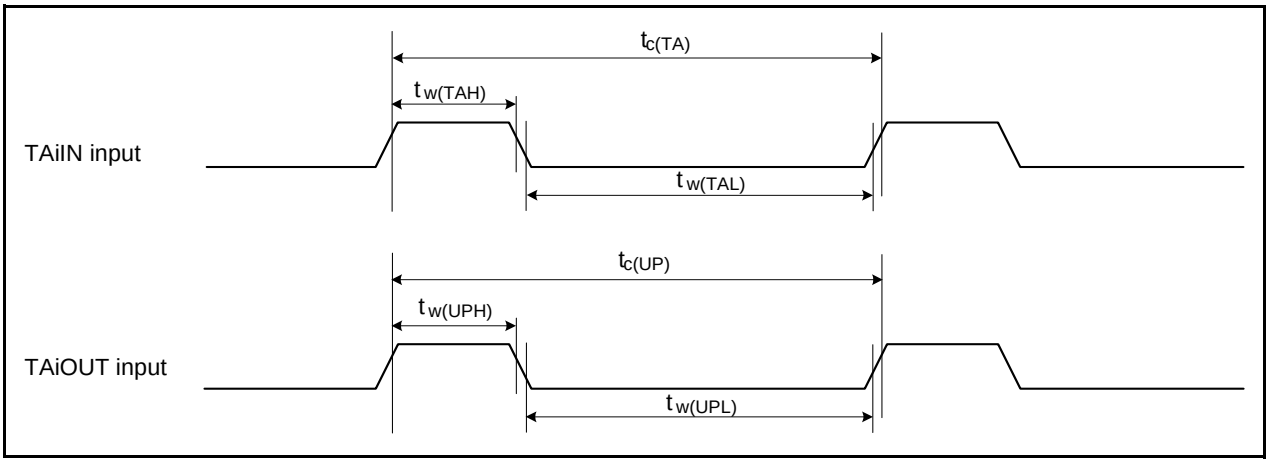


Figure 5.23 Timer A Input

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

Table 5.48 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

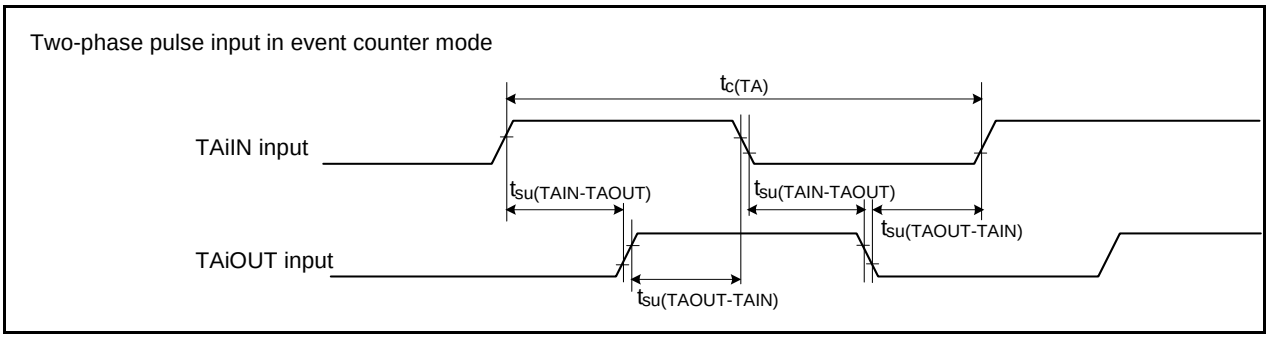


Figure 5.24 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.4 Timer B Input

Table 5.49 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on both edges)	120		ns

Table 5.50 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 5.51 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t^{w(TBL)}$	TBiIN input low pulse width	300		ns

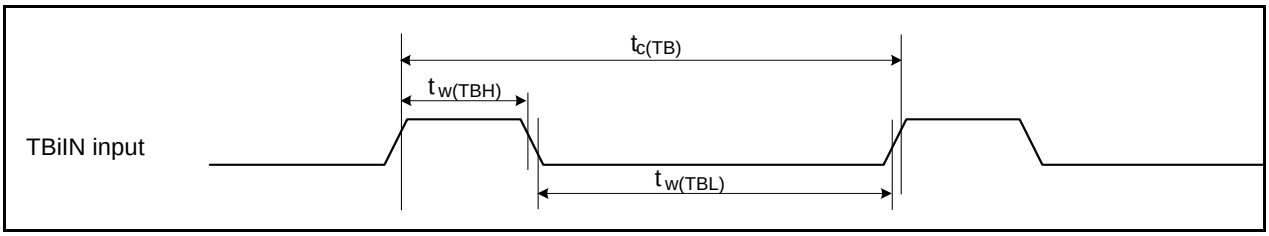


Figure 5.25 Timer B Input

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

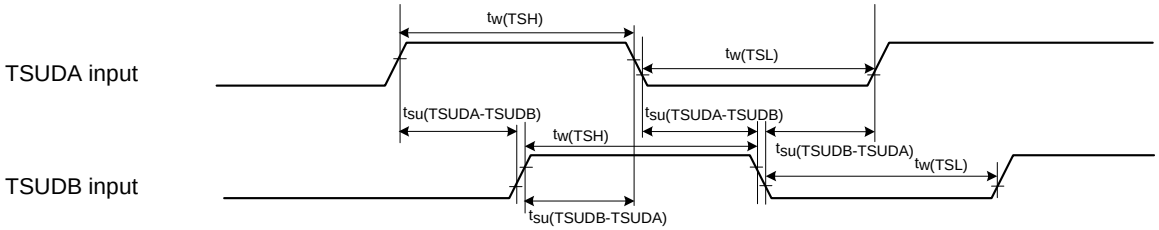
($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.5 Timer S Input

Table 5.52 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:

1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.6 Serial Interface

Table 5.53 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

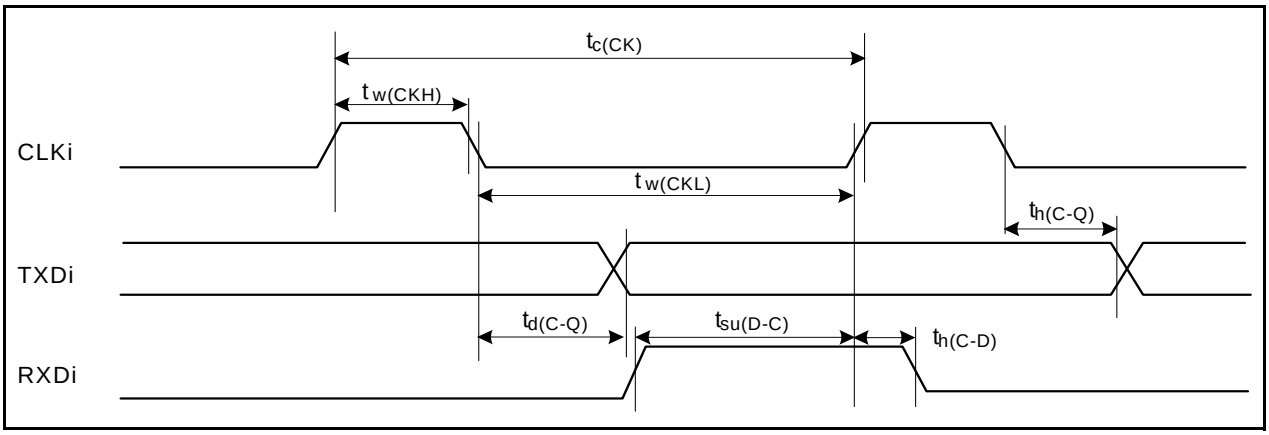


Figure 5.26 Serial Interface

5.3.2.7 External Interrupt $\overline{INTi}$ Input

Table 5.54 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	380		ns

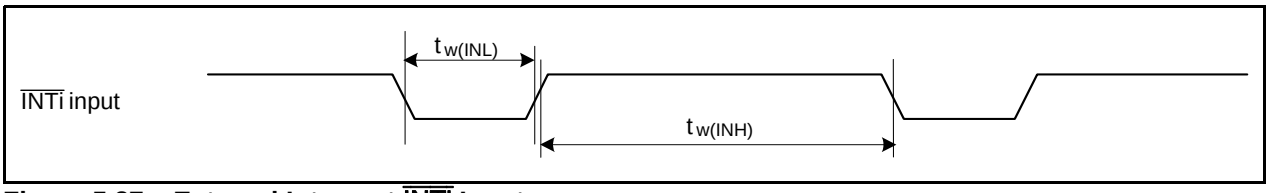


Figure 5.27 External Interrupt $\overline{INTi}$ Input

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.2.8 Multi-master I²C-bus

Table 5.55 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

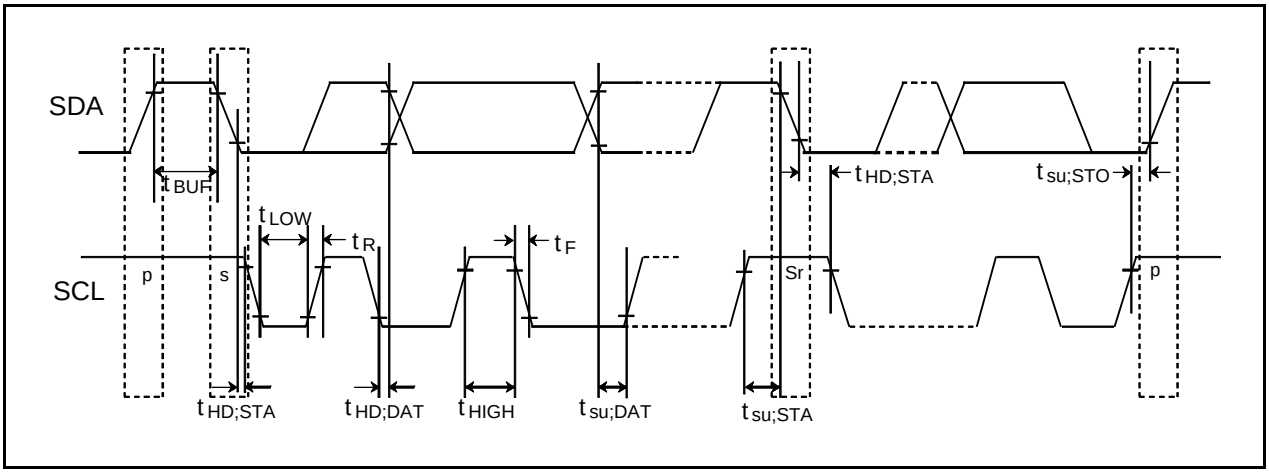


Figure 5.28 Multi-master I²C-bus

$V_{CC1} = V_{CC2} = 3\ V$

Timing Requirements

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.3 Timing Requirements (Memory Expansion Mode and Microprocessor Mode)

Table 5.56 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	50		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	85		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f_{(BCLK)}} - 60[ns]$$

2. Calculated according to the BCLK frequency as follows:

$$\frac{(n + 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns]$$ n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.

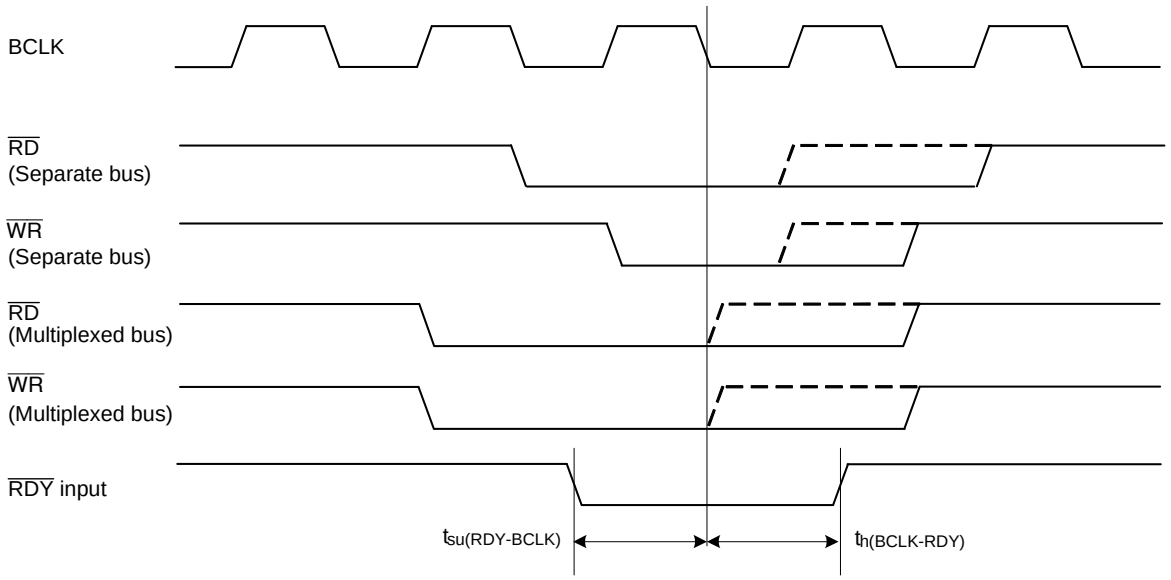
3. Calculated according to the BCLK frequency as follows:

$$\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 60[ns]$$ n is 2 for 2 waits setting, 3 for 3 waits setting.

Memory Expansion Mode and Microprocessor Mode

$V_{CC1} = V_{CC2} = 3$ V

(Effective in wait state setting**)**



Measuring conditions

- $V_{CC1} = V_{CC2} = 3$ V
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

Figure 5.29 Timing Diagram

$V_{CC1} = V_{CC2} = 3\ V$

5.3.4 Switching Characteristics (Memory Expansion Mode and Microprocessor Mode)

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at T_{opr} = -20°C to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.1 In No Wait State Setting

Table 5.57 Memory Expansion and Microprocessor Modes (in No Wait State Setting)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.30		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

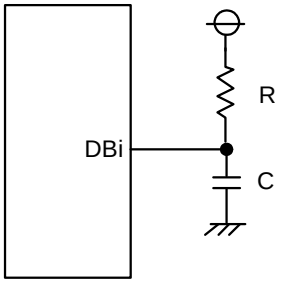
1. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$ $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

   $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$

3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
   Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
   Hold time of data bus is expressed in
   $t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
   by a circuit of the right figure.
   For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ,
   hold time of output low level is
   $t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
   = 6.7 ns.



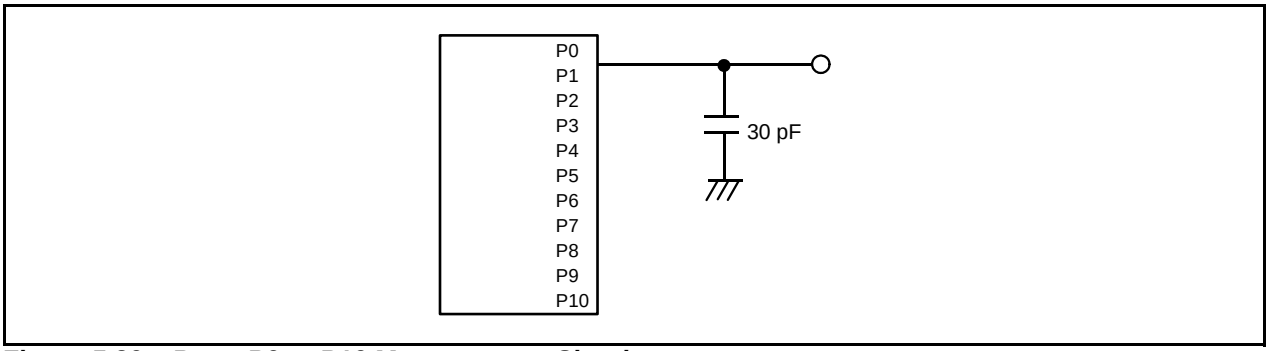
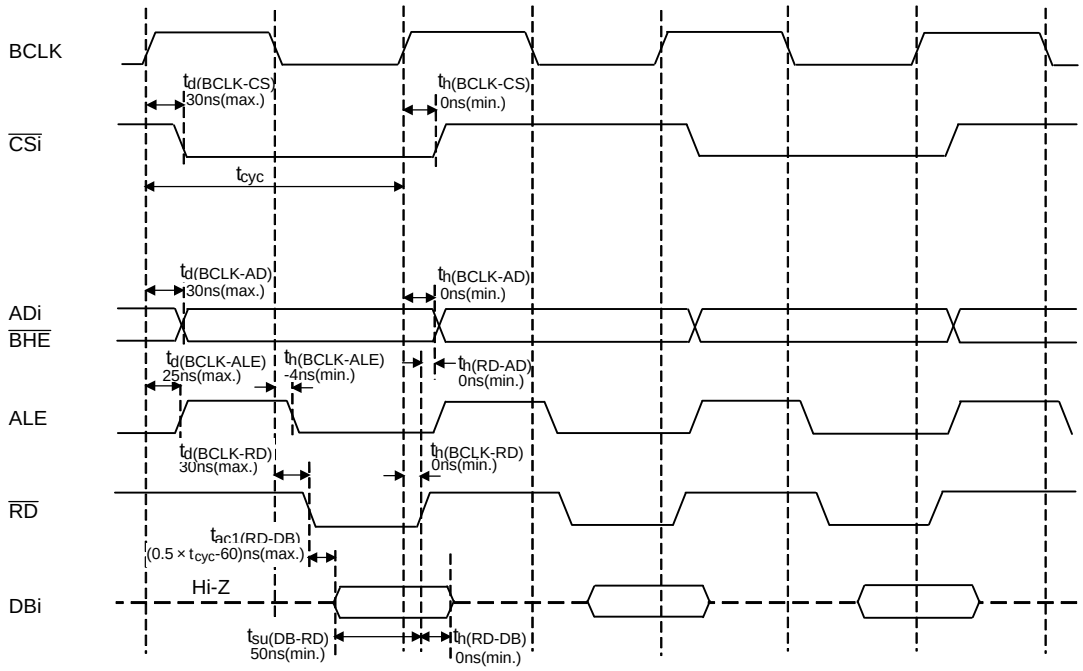


Figure 5.30 Ports P0 to P10 Measurement Circuit

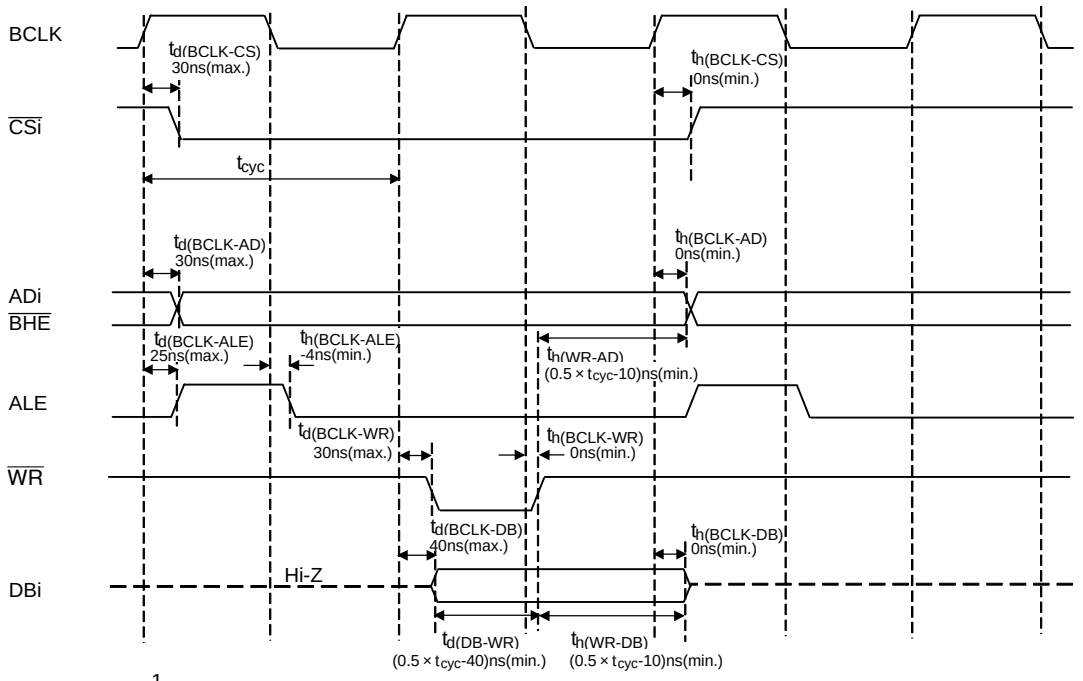
Memory Expansion Mode and Microprocessor Mode
(in no wait state setting)

$V_{CC1} = V_{CC2} = 3V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

Figure 5.31 Timing Diagram

$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.2 In 1 to 3 Waits Setting and When Accessing External Area

Table 5.58 Memory Expansion Mode and Microprocessor Mode (in 1 to 3 Waits Setting and When Accessing External Area)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.30		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		-4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK) (3)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR) (3)		(Note 2)		ns

Notes:

1. Calculated according to the BCLK frequency as follows:

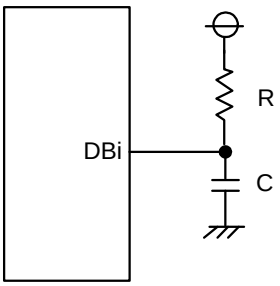
$$\frac{(n-0.5)\times 10^9}{f_{(BCLK)}} - 40[ns]$$

n is 1 for 1 wait setting, 2 for 2 waits setting and 3 for 3 waits setting.
When n = 1, $f_{(BCLK)}$ is 12.5 MHz or less.

2. Calculated according to the BCLK frequency as follows:

$$\frac{0.5\times 10^9}{f_{(BCLK)}} - 10[ns]$$

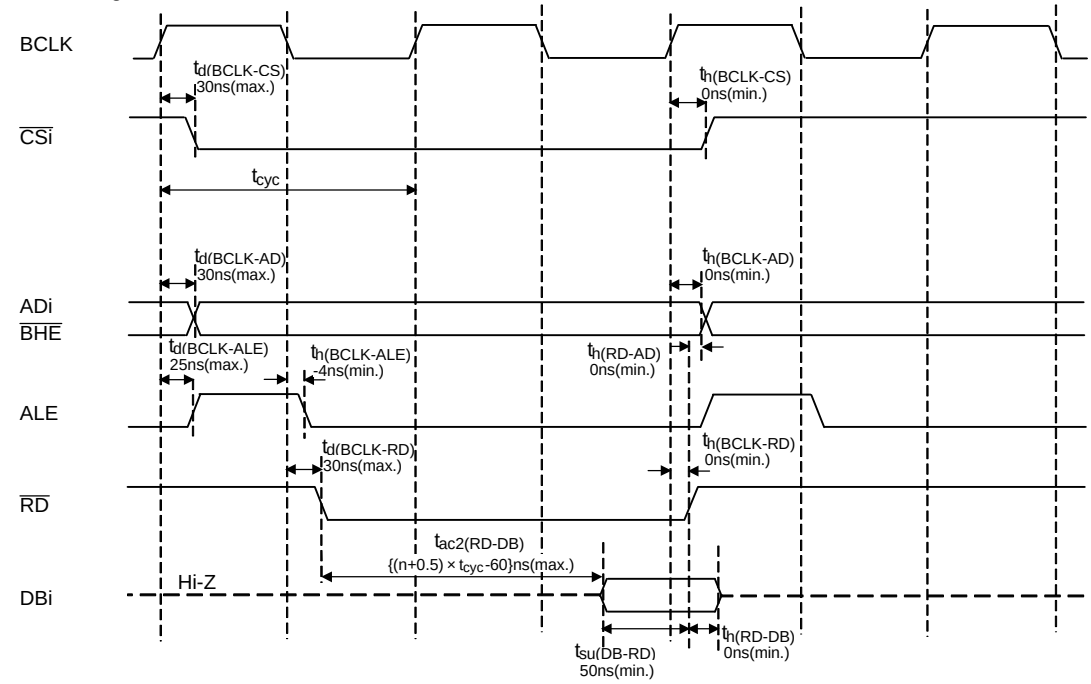
3. This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in
$t = -CR \times \ln(1 - V_{OL}/V_{CC2})$
by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30 pF, R = 1 kΩ, hold time of output low level is
$t = -30\ pF \times 1\ k\Omega \times \ln(1 - 0.2V_{CC2}/V_{CC2})$
= 6.7 ns.



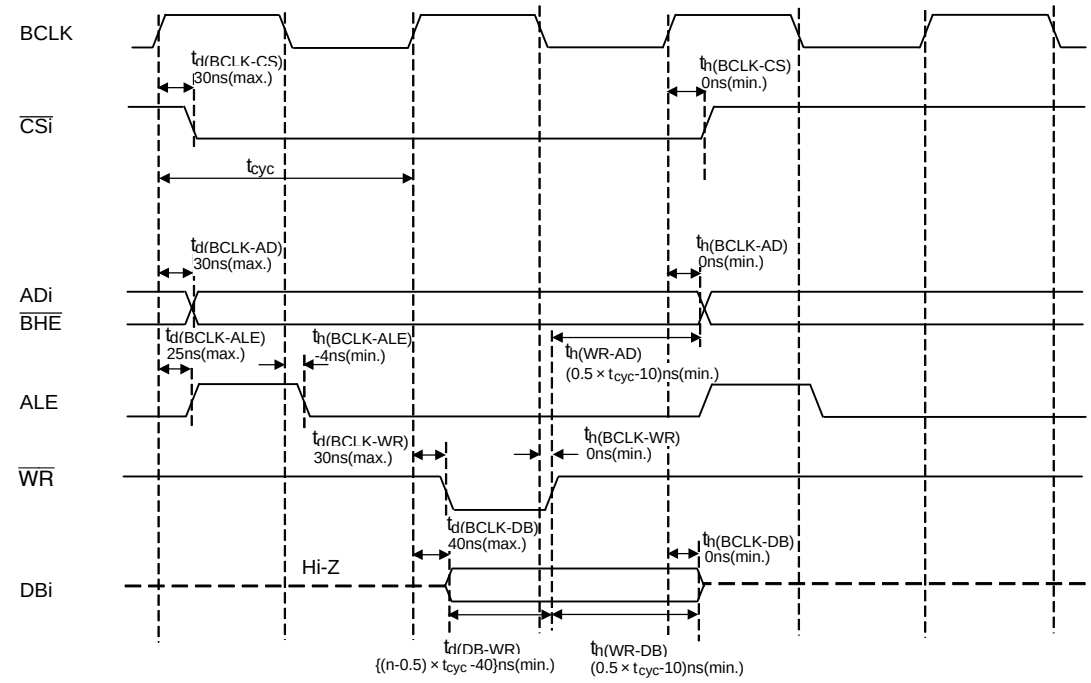
Memory Expansion Mode and Microprocessor Mode
(in 1 to 3 waits setting and when accessing external area)

$V_{CC1} = V_{CC2} = 3V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

n: 1 (when 1 wait)
2 (when 2 waits)
3 (when 3 waits)

Figure 5.32 Timing Diagram

$V_{CC1} = V_{CC2} = 3\ V$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3$ V, $V_{SS} = 0$ V, at $T_{opr} = -20°C$ to 85°C/-40°C to 85°C unless otherwise specified)

5.3.4.3 In 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus

Table 5.59 Memory Expansion Mode and Microprocessor Mode (in 2 or 3 Waits Setting, and When Accessing External Area and Using Multiplexed Bus) (5)

Symbol	Parameter	Measuring Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	See Figure 5.30		50	ns
$t_{h(BCLK-AD)}$	Address output hold time (in relation to BCLK)		0		ns
$t_{h(RD-AD)}$	Address output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			50	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (in relation to BCLK)		0		ns
$t_{h(RD-CS)}$	Chip select output hold time (in relation to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			40	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			40	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (in relation to BCLK)			50	ns
$t_{h(BCLK-DB)}$	Data output hold time (in relation to BCLK)		0		ns
$t_{d(DB-WR)}$	Data output delay time (in relation to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (in relation to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (in relation to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (in relation to BCLK)		–4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (in relation to Address)		(Note 3)		ns
$t_{h(AD-ALE)}$	ALE signal output hold time (in relation to Address)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of address		0		ns
$t_{dz(RD-AD)}$	Address output floating start time			8	ns

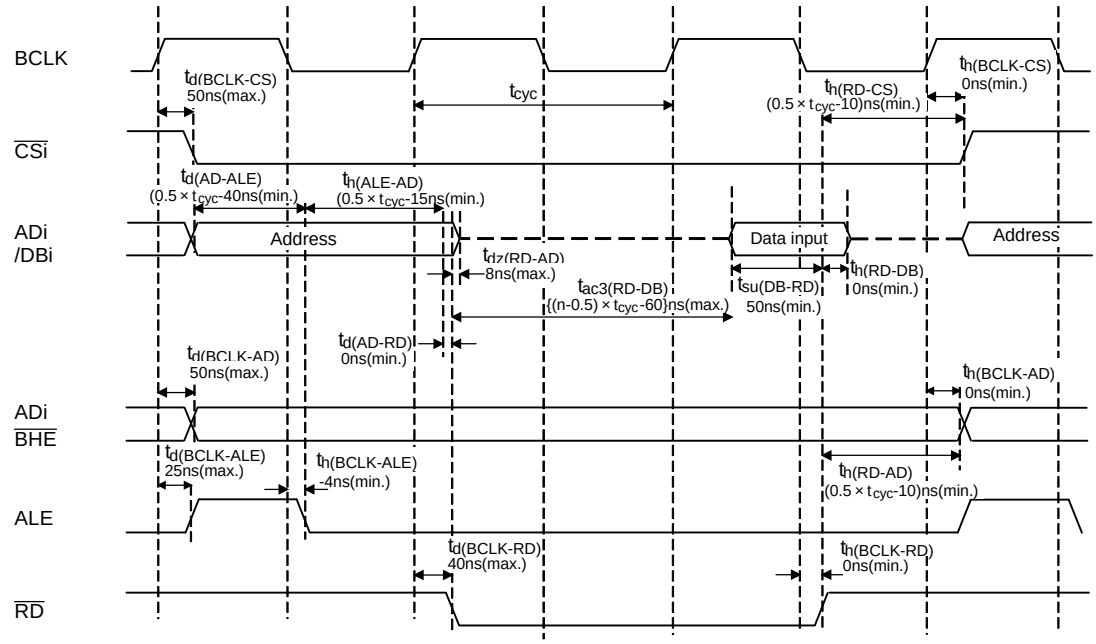
Notes:

1. Calculated according to the BCLK frequency as follows: $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 10[ns]$
2. Calculated according to the BCLK frequency as follows:
   $\frac{(n - 0.5) \times 10^9}{f_{(BCLK)}} - 50[ns]$ n is 2 for 2 waits setting, 3 for 3 waits setting.
3. Calculated according to the BCLK frequency as follows: $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 40[ns]$
4. Calculated according to the BCLK frequency as follows: $\frac{0.5 \times 10^9}{f_{(BCLK)}} - 15[ns]$
5. When using multiplexed bus, set $f_{(BCLK)}$ 12.5 MHz or less.

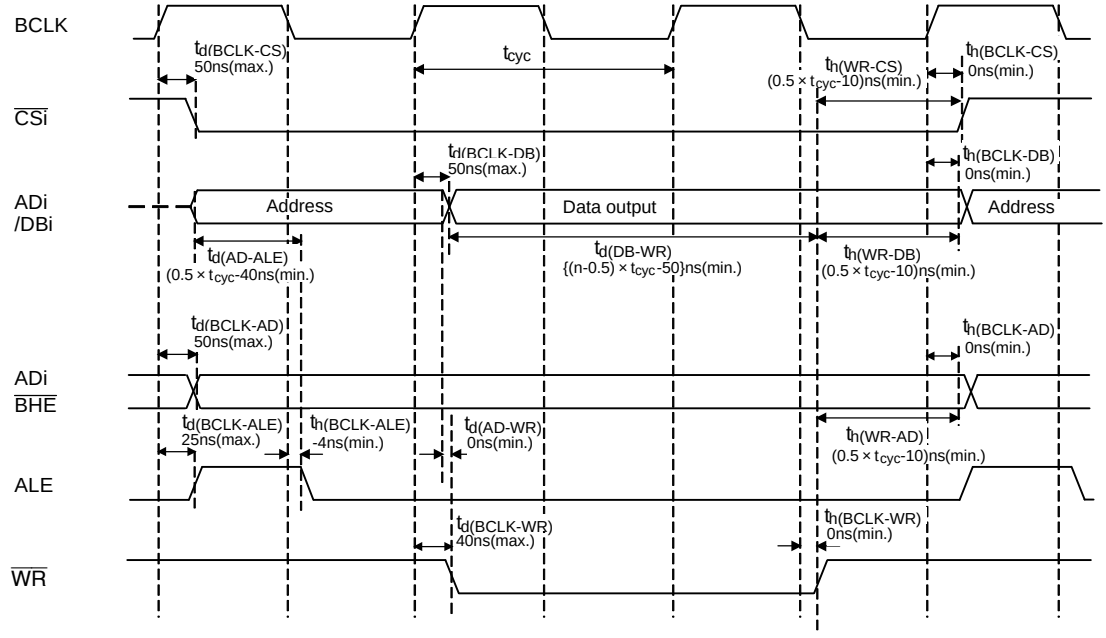
Memory Expansion Mode and Microprocessor Mode
(in 2 or 3 waits setting, and when accessing external area and using multiplexed bus)

$V_{CC1} = V_{CC2} = 3V$

Read timing



Write timing



$$t_{cyc} = \frac{1}{f_{(BCLK)}}$$

Measuring conditions

- $V_{CC1} = V_{CC2} = 3V$
- Input timing voltage: $V_{IL} = 0.6$ V, $V_{IH} = 2.4$ V
- Output timing voltage: $V_{OL} = 1.5$ V, $V_{OH} = 1.5$ V

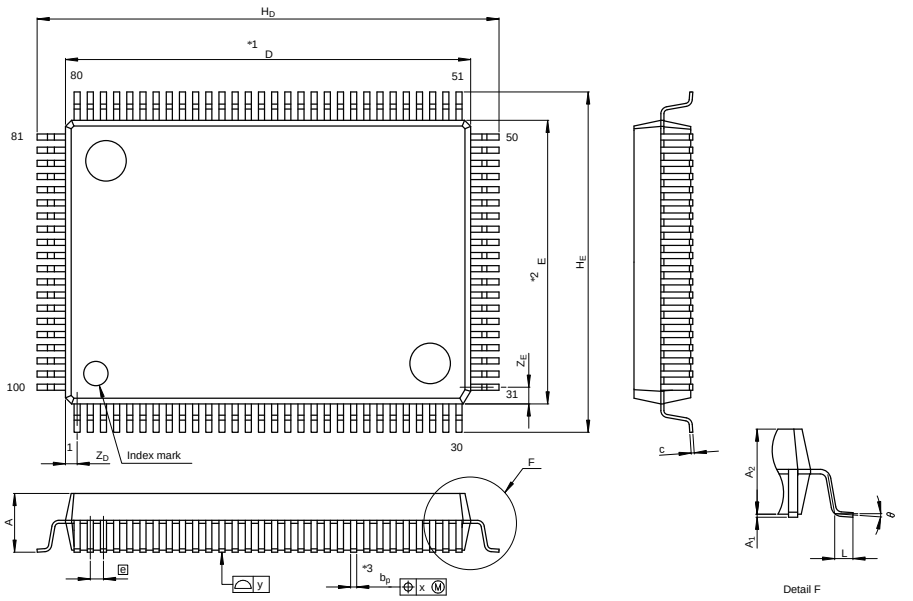
n: 2 (when 2 waits)
3 (when 3 waits)

Figure 5.33 Timing Diagram

Appendix 1. Package Dimensions

The information on the latest package dimensions or packaging may be obtained from “Packages“ on the Renesas Electronics website.

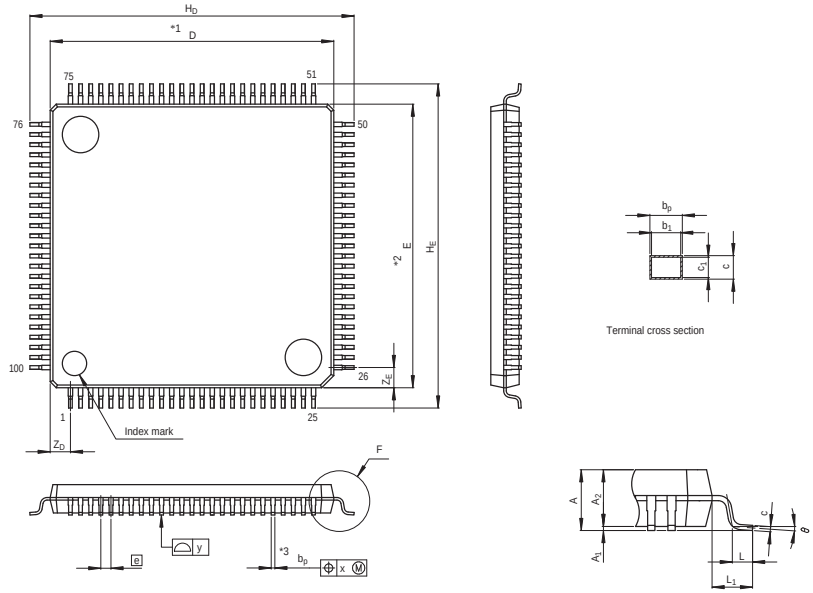
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	M16C/6C Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Jul 15, 2009	-	First Edition issued.
2.00	Feb 07, 2011	Overall	0004h Processor Mode Register 0: Combined differing reset values into one.
		Overall	0019h Voltage Detector 2 Flag Register: Changed the reset value from “0000 X000b”.
		Overall	001Ah Voltage Detector Operation Enable Register: Changed reset value from “000X 0000b”.
		Overall	002Ah Voltage Monitor 0 Control Register: Changed reset value from “1100 XX10b”.
		Overall	002Bh Voltage Monitor 1 Control Register: Changed reset value from “1000 1X10b”.
		Overall	02B9h I2C0 Status Register 1: Changed reset value from “00h”.
		Overall	0324h Increment/Decrement Flag: Changed name from Up/Down Flag.
		Overall	03DCh D/A Control Register: Changed reset value from “XXXX XX00b”.
		Overall	Changed the UVCC pin from “Input” to “I/O”.
		Overview	
		Chap. 1.	Changed from “INPC10 to INPC17” to “INPC1_0 to INPC1_7” and from “OUTC10 to OUTC17” to “OUTC1_0 to OUTC1_7”.
		1	1.1.1 Applications: Added the note.
		3	Table 1.2 Specifications (2/2): • Changed the value in the Current Consumption row to “Described in Electrical Characteristics”. • Deleted note 1.
		4	Table 1.3 Product List: Changed the development status.
		5	Figure 1.2 Marking Diagram (Top View): Added the detail explanations for the 7-digit date code.
		7, 8	Figure 1.4 Pin Assignment and Figure 1.5 Pin Assignment: Added “/TSUDA” to P8_0 and “/TSUDB” to P8_1.
		9	Table 1.4 Pin Names (1/2): Added “/TSUDB” to P8_1 and “/TSUDA” to P8_0.
		11	Table 1.6 Pin Functions (1/3): • Changed the description of $\overline{\text{CNVSS}}$ pin. • Changed the description of $\overline{\text{HOLD}}$ pin.
		12	Table 1.7 Pin Functions (2/3): Added “TSUDA, TSUDB” to the pin name of Timer S.
		13	Table 1.8 Pin Functions (3/3): Deleted notes 1 and 2.
		Address Space	
		18	Figure 3.2 Memory Map: Added note 1 and 3 to the reserved areas.
		Special Function Registers (SFRs)	
		20	Table 4.1 SFR Information (1): • Deleted “the VCR1 register, the VCR2 register” from note 2. • Deleted notes 5 to 6 and added note 5.
		21	Table 4.2 SFR Information (2): Deleted notes 2 to 6 and added note 2.
		35	Table 4.16 SFR Information (16): Deleted “00000010b” from values after hardware reset in note 2.
		43	4.2.1 Register Settings: Added the description regarding read-modify-write instructions.
		44	Table 4.26 Read-Modify-Write Instructions: Added.
		Electrical Characteristics	
		Chap. 5.	Moved the measuring conditions in note 1 to below the table title.
		Chap. 5.	Reordered figures and tables in 5.2.2 Timing Requirements (Peripheral Functions and Others) and 5.3.2 Timing Requirements (Peripheral Functions and Others).
		45	Table 5.1 Absolute Maximum Ratings: • Changed the Condition of the V_{cc2} row. • Added the V_{REF} row. • Added a row for the data area value to T_{opr} (Flash program erase). • Added the note 1.
		46	Table 5.2 Recommended Operating Conditions (1/3): Added the $I_{OH(sum)}$ row and deleted note 3.
		47	Table 5.3 Recommended Operating Conditions (2/3): Added the $I_{OL(sum)}$ row and deleted note 3.

REVISION HISTORY	M16C/6C Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Feb 07, 2011	49	Table 29.5 A/D Conversion Characteristics (1/2): Added the Measuring Condition of the Resolution row.
		50	Table 5.6 A/D Conversion Characteristics (2/2): Added the note 5.
		52	Table 5.9 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$): Added the Typ. value of the Low current consumption read mode.
		52	Table 5.10 Flash Memory (Program ROM 1, 2) Electrical Characteristics: • Added a condition to the Read voltage row. • Modified note 1. • Deleted the example stated in note 4.
		53	Table 5.11 Flash Memory (Data Flash) Electrical Characteristics: Changed “128 groups” to “256 groups” in note 4.
		54	Table 5.12 Voltage Detector 0 Electrical Characteristics: Added the condition in the V_{det0} row.
		55	Table 5.15 Power-On Reset Circuit: • Added the V_{por1} and $t_{w(por)}$ row. • Deleted the Condition of t_{rth} row. • Added the last line in note 1.
		55	Figure 5.5 Power-On Reset Circuit Electrical Characteristics: • Changed the signal name “0.1 V” to “V_{por1}”. • Deleted note 2.
		57	Table 5.17 40 MHz On-Chip Oscillator Electrical Characteristics: Changed the Condition in the f_{OCO40M} row.
		59	Table 5.20 Electrical Characteristics (2): Added “ZP, IDU, IDV, IDW” to the V_{T+} - V_{T-} row.
		60	Table 5.21 Electrical Characteristics (3): Added the During flash memory program row and During flash memory erase row.
		65, 83	5.2.2.5 and 5.3.2.5 Timer S Input: Added.
		67, 85	5.2.2.8 and 5.3.2.8 Multi-master I^2C-bus: Added.
		68	Table 5.36 Memory Expansion Mode and Microprocessor Mode: Changed $\overline{RDY}$ input setup time from 30.
		68 to 75, 86 to 93	Table 5.36 to Table 5.39 and Table 5.56 to Table 5.59 Memory Expansion Mode and Microprocessor Mode: Deleted the following: • $\overline{HOLD}$ input setup time • $\overline{HOLD}$ input hold time • $\overline{HLDA}$ output delay time
		69, 87	Figure 5.16 and Figure 5.29 Timing Diagram: Deleted lower figure (Common to wait state and no wait state settings).
		77	Table 5.40 Electrical Characteristics (1): Added “ZP, IDU, IDV, IDW” to the V_{T+} - V_{T-} row.
		78	Table 5.41 Electrical Characteristics (2): Added the During flash memory program row and During flash memory erase row.
		86	Table 5.56 Memory Expansion Mode and Microprocessor Mode: Changed $\overline{RDY}$ input setup time from 40.
2.10	Jul 31, 2011	**Electrical Characteristics**	
		Vcc = 5 V	
		61	Table 5.21 Electrical Characteristics (3): Changed the Measuring Condition column of 40 MHz on-chip oscillator for the 40 MHz on-chip oscillator mode in the I_{CC}.
		Vcc = 3 V	
		79	Table 5.41 Electrical Characteristics (2): Changed the Measuring Condition column of 40 MHz on-chip oscillator for the 40 MHz on-chip oscillator mode in the I_{CC}.

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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