

8 BIT SHIFT REGISTER WITH OUTPUT REGISTER

- HIGH SPEED: $t_{PD} = 4.2ns$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 mA$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2V$ to $5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 594
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.8V$ (MAX.)

DESCRIPTION

The 74VHC594 is an high speed CMOS 8-BIT SHIFT REGISTERS fabricated with sub-micron silicon gate C²MOS technology.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (SCLR, RCLR) are provided for both the shift register and the storage register.



Table 1: Order Codes

| PACKAGE | T & R |
|---------|---------------|
| SOP | M74VHC594RMTR |
| TSSOP | M74VHC594TTR |

A serial (QH') output is provided for cascading purposes. Both the shift register and storage register use positive-edge triggered clocks. If the clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

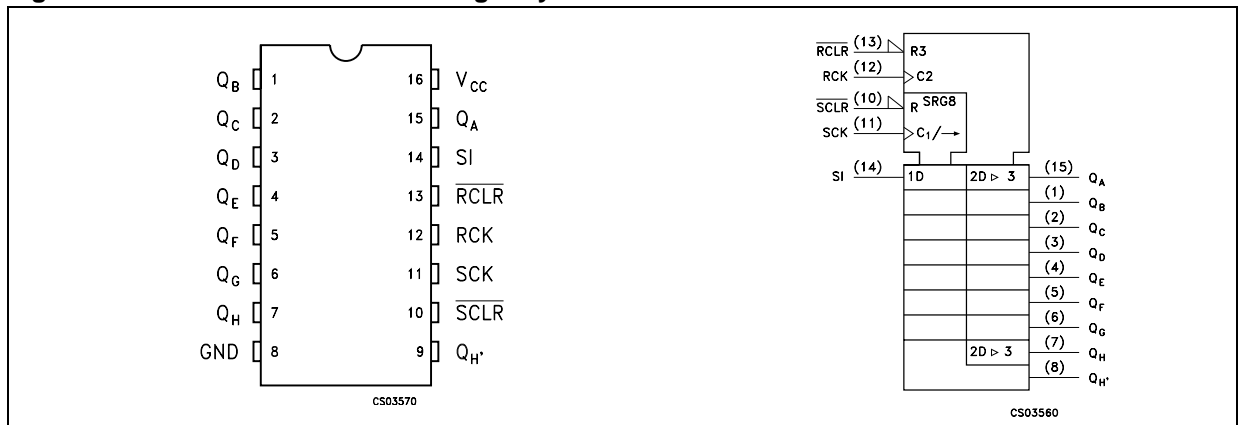


Figure 2: Input Equivalent Circuit

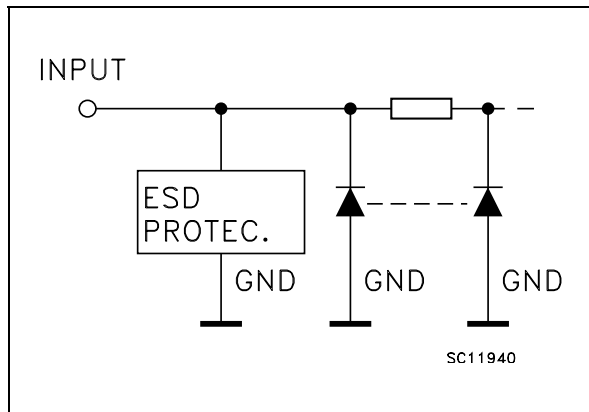


Table 2: Pin Description

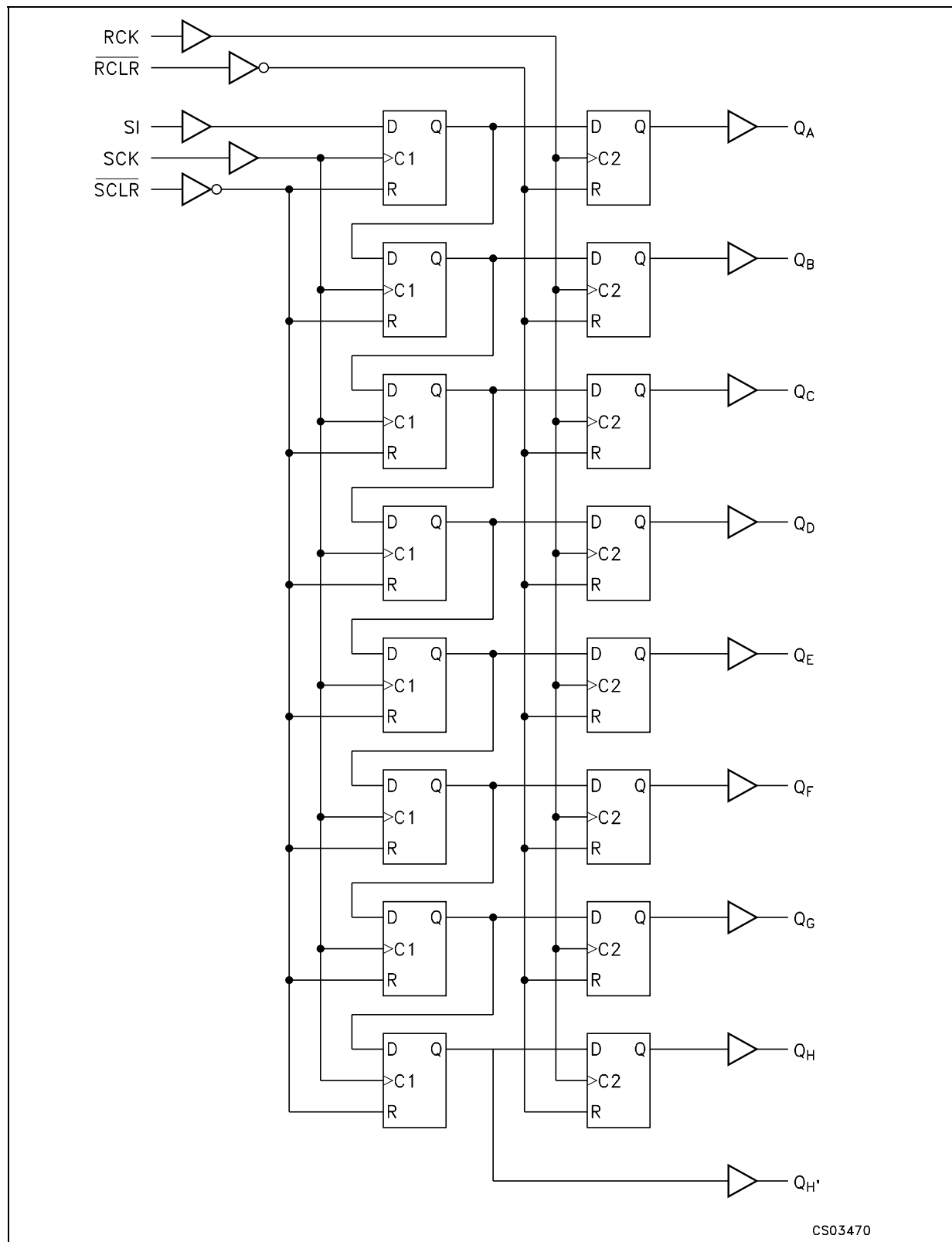
| PIN N° | SYMBOL | NAME AND FUNCTION |
|-------------------------|-----------------|------------------------------|
| 1, 2, 3, 4, 5, 6, 7, 15 | QA to QH | Data Outputs |
| 9 | QH' | Serial Data Output |
| 10 | SCLR | Shift Register Clear Input |
| 11 | SCK | Shift Register Clock Input |
| 13 | RCLR | Storage Register Clear Input |
| 14 | SI | Serial Data Input |
| 12 | RCK | Storage Register Clock Input |
| 8 | GND | Ground (0V) |
| 16 | V _{CC} | Positive Supply Voltage |

Table 3: Truth Table

| INPUTS | | | | | OUTPUTS |
|--------|-----|------|-----|------|--|
| SI | SCK | SCLR | RCK | RCLR | |
| X | X | L | X | X | SHIFT REGISTER IS CLEAR |
| L | | H | X | X | FIRST STAGE OF SHIFT REGISTER GOES LOW OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY |
| H | | H | X | X | FIRST STAGE OF SHIFT REGISTER GOES HIGH OTHER STAGES STORE THE DATA OF PREVIOUS STAGE, RESPECTIVELY |
| L | | H | X | X | SHIFT REGISTER STATE IS NOT CHANGED |
| X | X | X | X | L | STORAGE REGISTER IS CLEARED |
| X | X | X | | H | SHIFT REGISTER DATA IS STORED IN THE STORAGE REGISTER |
| X | X | X | | H | STORAGE REGISTER STATE IS NOT CHANGED |

X: Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Figure 4: Timing Chart

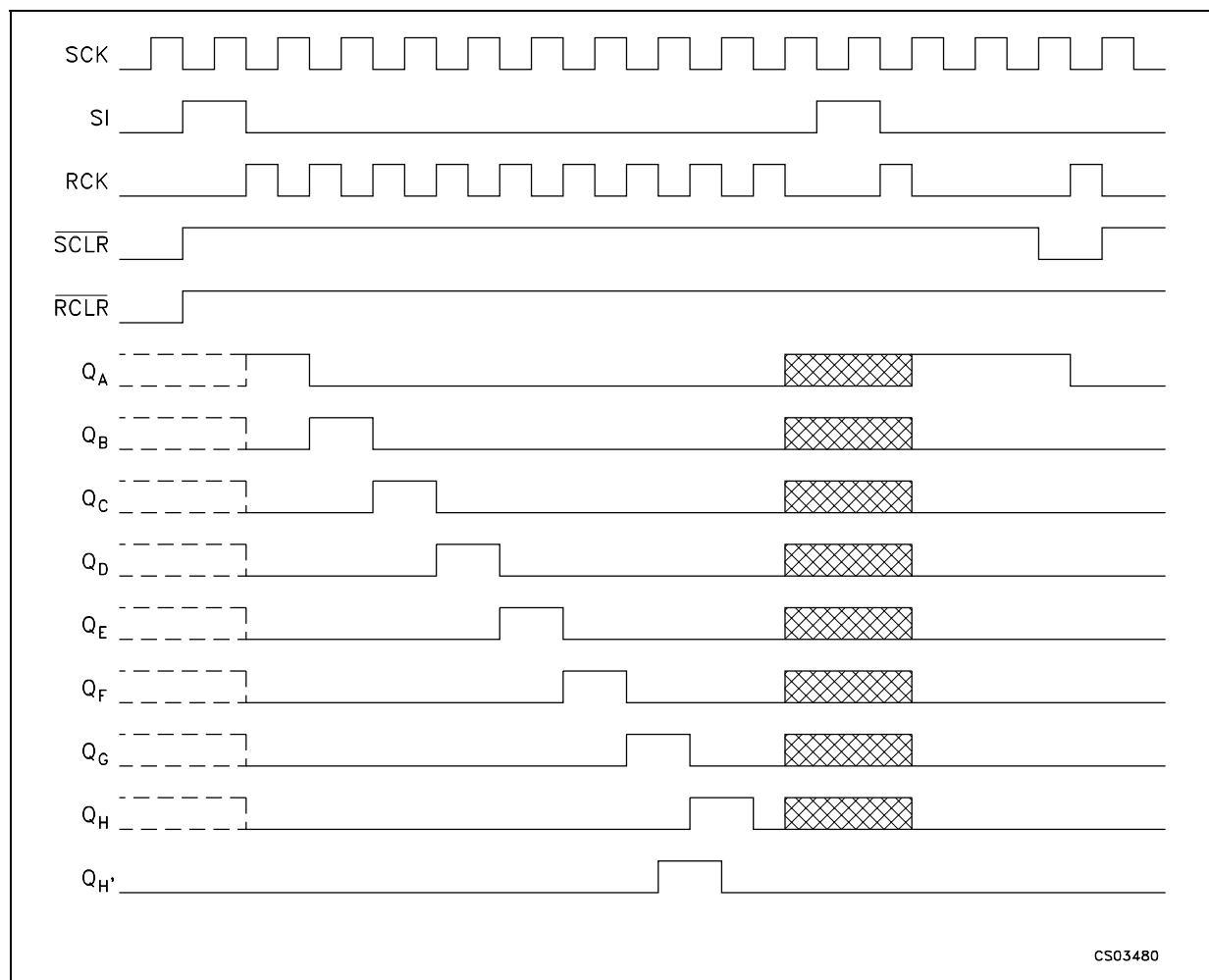


Table 4: Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-----------------------|-------------------------------|------------------------|-------------|
| V_{CC} | Supply Voltage | -0.5 to +7.0 | V |
| V_I | DC Input Voltage | -0.5 to +7.0 | V |
| V_O | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | - 20 | mA |
| I_{OK} | DC Output Diode Current | ± 20 | mA |
| I_O | DC Output Current | ± 25 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current | ± 50 | mA |
| T_{stg} | Storage Temperature | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature (10 sec) | 300 | $^{\circ}C$ |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5: Recommended Operating Conditions

| Symbol | Parameter | Value | Unit |
|----------|--|---------------------|------|
| V_{CC} | Supply Voltage | 2 to 5.5 | V |
| V_I | Input Voltage | 0 to 5.5 | V |
| V_O | Output Voltage | 0 to V_{CC} | V |
| T_{op} | Operating Temperature | -55 to 125 | °C |
| dt/dv | Input Rise and Fall Time (note 1) ($V_{CC} = 3.3 \pm 0.3V$) ($V_{CC} = 5.0 \pm 0.5V$) | 0 to 100 0 to 20 | ns/V |

1) V_I from 30% to 70% of V_{CC}

Table 6: DC Specifications

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|-----------|---------------------------|-----------------|-------------------------|--------------------------|------|-------------|-------------|-------------|--------------|-------------|---------------|
| | | V_{CC} (V) | | $T_A = 25^\circ\text{C}$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V_{IH} | High Level Input Voltage | 2.0 | | 1.5 | | | 1.5 | | 1.5 | | V |
| | | 3.0 to 5.5 | | $0.7V_{CC}$ | | | $0.7V_{CC}$ | | $0.7V_{CC}$ | | |
| V_{IL} | Low Level Input Voltage | 2.0 | | | | 0.5 | | 0.5 | | 0.5 | V |
| | | 3.0 to 5.5 | | | | $0.3V_{CC}$ | | $0.3V_{CC}$ | | $0.3V_{CC}$ | |
| V_{OH} | High Level Output Voltage | 2.0 | $I_O = -50 \mu\text{A}$ | 1.9 | 2.0 | | 1.9 | | 1.9 | | V |
| | | 3.0 | $I_O = -50 \mu\text{A}$ | 2.9 | 3.0 | | 2.9 | | 2.9 | | |
| | | 4.5 | $I_O = -50 \mu\text{A}$ | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | 3.0 | $I_O = -4 \text{ mA}$ | 2.58 | | | 2.48 | | 2.4 | | |
| | | 4.5 | $I_O = -8 \text{ mA}$ | 3.94 | | | 3.8 | | 3.7 | | |
| V_{OL} | Low Level Output Voltage | 2.0 | $I_O = 50 \mu\text{A}$ | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | 3.0 | $I_O = 50 \mu\text{A}$ | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 | $I_O = 50 \mu\text{A}$ | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 3.0 | $I_O = 4 \text{ mA}$ | | | 0.36 | | 0.44 | | 0.55 | |
| | | 4.5 | $I_O = 8 \text{ mA}$ | | | 0.36 | | 0.44 | | 0.55 | |
| I_I | Input Leakage Current | 0 to 5.5 | $V_I = 5.5V$ or GND | | | ± 0.1 | | ± 1 | | ± 1 | μA |
| I_{off} | Power Off Leakage Current | 0 | $V_I = 0$ to 5V | | | ± 0.1 | | ± 5 | | ± 5 | μA |
| I_{CC} | Quiescent Supply Current | 5.5 | $V_I = V_{CC}$ or GND | | | 4 | | 40 | | 40 | μA |

Table 7: AC Electrical Characteristics (Input $t_r = t_f = 3\text{ns}$)

| Symbol | Parameter | Test Condition | | | Value | | | | | | Unit |
|------------------------|-------------------------------------|---------------------|---------------|--------------------------|-------|------|-----------------------------|------|------------------------------|------|------|
| | | V_{CC} (V) | C_L (pF) | $T_A = 25^\circ\text{C}$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| t_{PLH} t_{PHL} | Propagation Delay Time (RCK - Qn) | 3.3 ^(*) | 15 | | 4.9 | 8.2 | 1.0 | 8.8 | 1.0 | 8.8 | ns |
| | | 3.3 ^(*) | 50 | | 8.1 | 11.9 | 1.0 | 13.1 | 1.0 | 13.1 | |
| | | 5.0 ^(**) | 15 | | 4.2 | 6.5 | 1.0 | 6.9 | 1.0 | 6.9 | |
| | | 5.0 ^(**) | 50 | | 6.7 | 8.9 | 1.0 | 9.7 | 1.0 | 9.7 | |
| t_{PLH} t_{PHL} | Propagation Delay Time (SCK - QH') | 3.3 ^(*) | 15 | | 5.5 | 9.2 | 1.0 | 9.9 | 1.0 | 9.9 | ns |
| | | 3.3 ^(*) | 50 | | 8.4 | 12.5 | 1.0 | 13.9 | 1.0 | 13.9 | |
| | | 5.0 ^(**) | 15 | | 4.1 | 7.2 | 1.0 | 7.6 | 1.0 | 7.6 | |
| | | 5.0 ^(**) | 50 | | 6.0 | 9.2 | 1.0 | 10.1 | 1.0 | 10.1 | |
| t_{PHL} | Propagation Delay Time (RCLR) - Qn) | 3.3 ^(*) | 15 | | 6.0 | 9.8 | 1.0 | 10.6 | 1.0 | 10.6 | ns |
| | | 3.3 ^(*) | 50 | | 9.0 | 13.1 | 1.0 | 14.4 | 1.0 | 14.4 | |
| | | 5.0 ^(**) | 15 | | 4.5 | 7.6 | 1.0 | 8.2 | 1.0 | 8.2 | |
| | | 5.0 ^(**) | 50 | | 6.6 | 10.0 | 1.0 | 10.7 | 1.0 | 10.7 | |
| t_{PLH} t_{PHL} | Propagation Delay Time (SCLR - QH') | 3.3 ^(*) | 15 | | 5.6 | 9.2 | 1.0 | 10.0 | 1.0 | 10.0 | ns |
| | | 3.3 ^(*) | 50 | | 8.5 | 12.4 | 1.0 | 14.0 | 1.0 | 14.0 | |
| | | 5.0 ^(**) | 15 | | 4.1 | 7.1 | 1.0 | 7.6 | 1.0 | 7.6 | |
| | | 5.0 ^(**) | 50 | | 6.0 | 9.2 | 1.0 | 10.1 | 1.0 | 10.1 | |
| f_{MAX} | Maximum Clock Frequency | 3.3 ^(*) | 15 | | 80 | 120 | | 70 | | 70 | MHz |
| | | 3.3 ^(*) | 50 | | 55 | 105 | | 50 | | 50 | |
| | | 5.0 ^(**) | 15 | | 135 | 170 | | 115 | | 115 | |
| | | 5.0 ^(**) | 50 | | 120 | 140 | | 95 | | 95 | |
| $t_{W(H)}$ | Minimum Pulse Width (SCK, RCK) | 3.3 ^(*) | | | 5.5 | | | 5.5 | | 5.5 | ns |
| | | 5.0 ^(**) | | | 5.0 | | | 5.0 | | 5.0 | |
| $t_{W(L)}$ | Minimum Pulse Width (SCLR, RCLR) | 3.3 ^(*) | | | 5.0 | | | 5.0 | | 5.0 | ns |
| | | 5.0 ^(**) | | | 5.2 | | | 5.2 | | 5.2 | |
| t_s | Minimum Set-Up Time (SI - CCK) | 3.3 ^(*) | | | 3.5 | | | 3.5 | | 3.5 | ns |
| | | 5.0 ^(**) | | | 3.0 | | | 3.0 | | 3.0 | |
| t_s | Minimum Set - Up Time (SCK, RCK) | 3.3 ^(*) | | | 8.0 | | | 8.5 | | 8.5 | ns |
| | | 5.0 ^(**) | | | 5.0 | | | 5.0 | | 5.0 | |
| t_s | Minimum Set - Up Time (SCRL - RCK) | 3.3 ^(*) | | | 8.0 | | | 9.0 | | 9.0 | ns |
| | | 5.0 ^(**) | | | 5.0 | | | 5.0 | | 5.0 | |
| t_h | Minimum Hold Time | 3.3 ^(*) | | | 1.5 | | | 1.5 | | 1.5 | ns |
| | | 5.0 ^(**) | | | 2.0 | | | 2.0 | | 2.0 | |
| t_{REM} | Minimum Clear-Removal Time | 3.3 ^(*) | | | | 3.0 | | | 3.0 | | ns |
| | | 5.0 ^(**) | | | | 2.5 | | | 2.5 | | |

(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$ (**) Voltage range is $5.0\text{V} \pm 0.5\text{V}$

Table 8: Capacitive Characteristics

| Symbol | Parameter | Test Condition | Value | | | | | | Unit | |
|------------------|--|----------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| C _{IN} | Input Capacitance | | | 7 | | | | | | pF |
| C _{OUT} | Output Capacitance | | | 9 | | | | | | pF |
| C _{PD} | Power Dissipation Capacitance (note 1) | | | 70 | | | | | | pF |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

Table 9: Dynamic Switching Characteristics

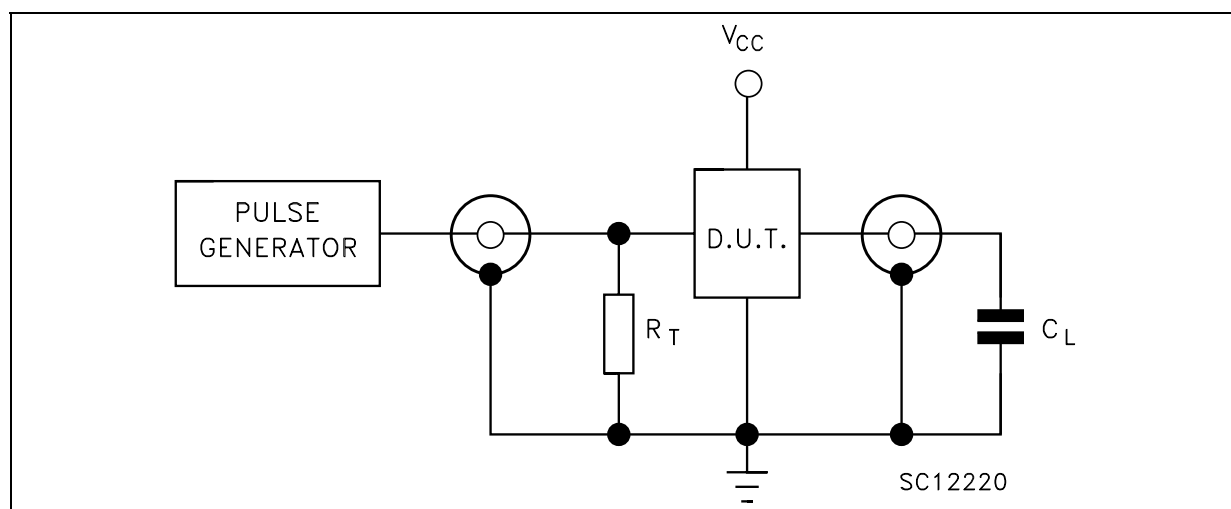
| Symbol | Parameter | V _{CC} (V) | Test Condition | Value | | | | | | Unit | |
|------------------|--|---------------------|------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V _{OLP} | Dynamic Low Voltage Quiet Output (note 1, 2) | 5.0 | C _L = 50 pF | | 0.9 | 1.2 | | | | | V |
| V _{OLV} | | | | -0.9 | -1.2 | | | | | | |
| V _{IHD} | Dynamic High Voltage Input (note 1, 3) | 5.0 | | 3.5 | | | | | | V | |
| V _{ILD} | Dynamic Low Voltage Input (note 1, 3) | 5.0 | | | | 1.5 | | | | | V |

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Figure 5: Test Circuit



C_L = 15/50pF or equivalent (includes jig and probe capacitance)

R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 6: Waveform - Propagation Delays, Setup And Hold Times (f=1MHz; 50% duty cycle)

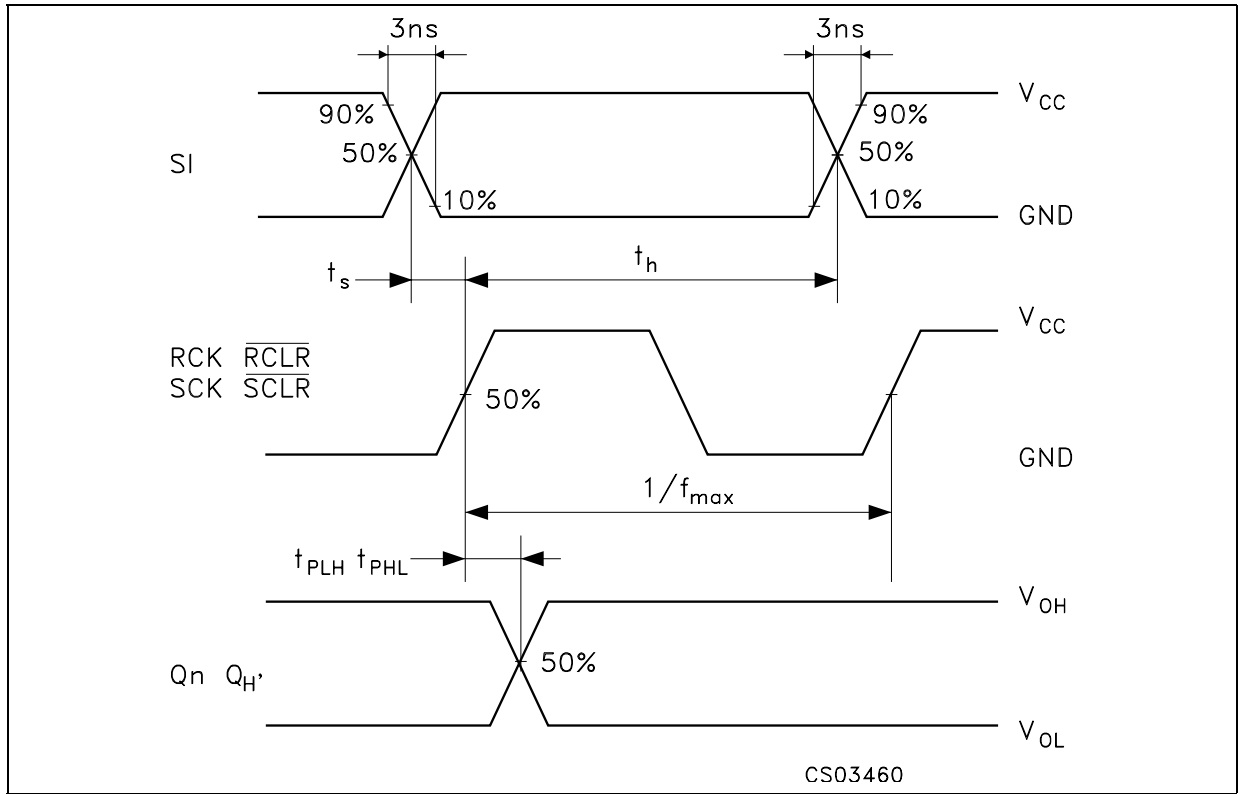
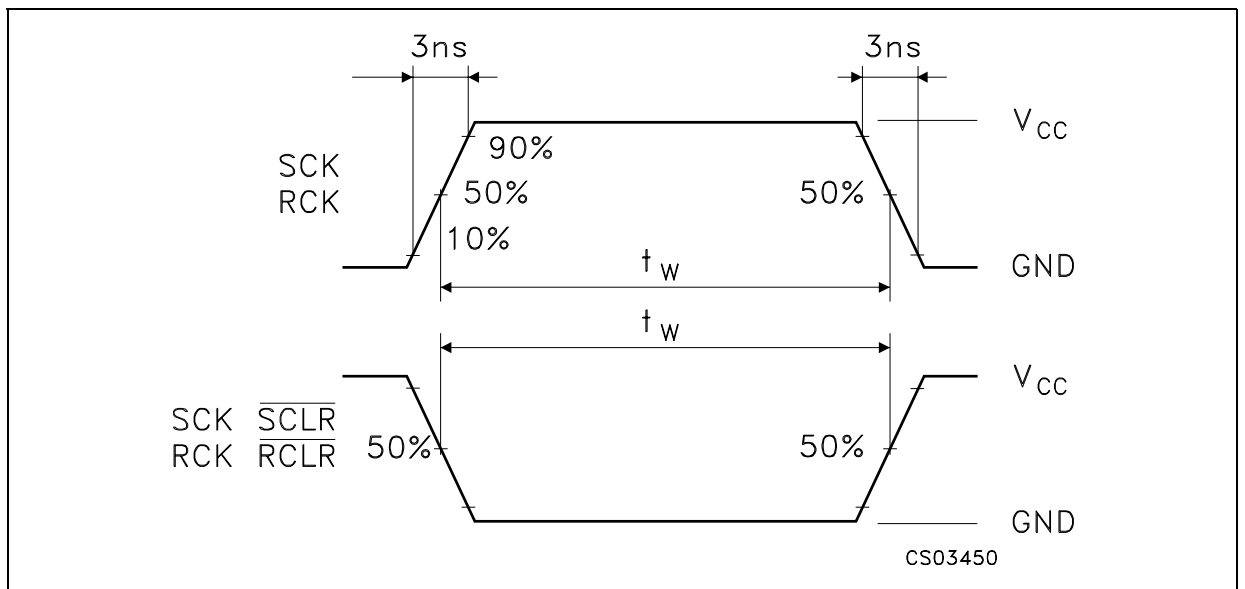
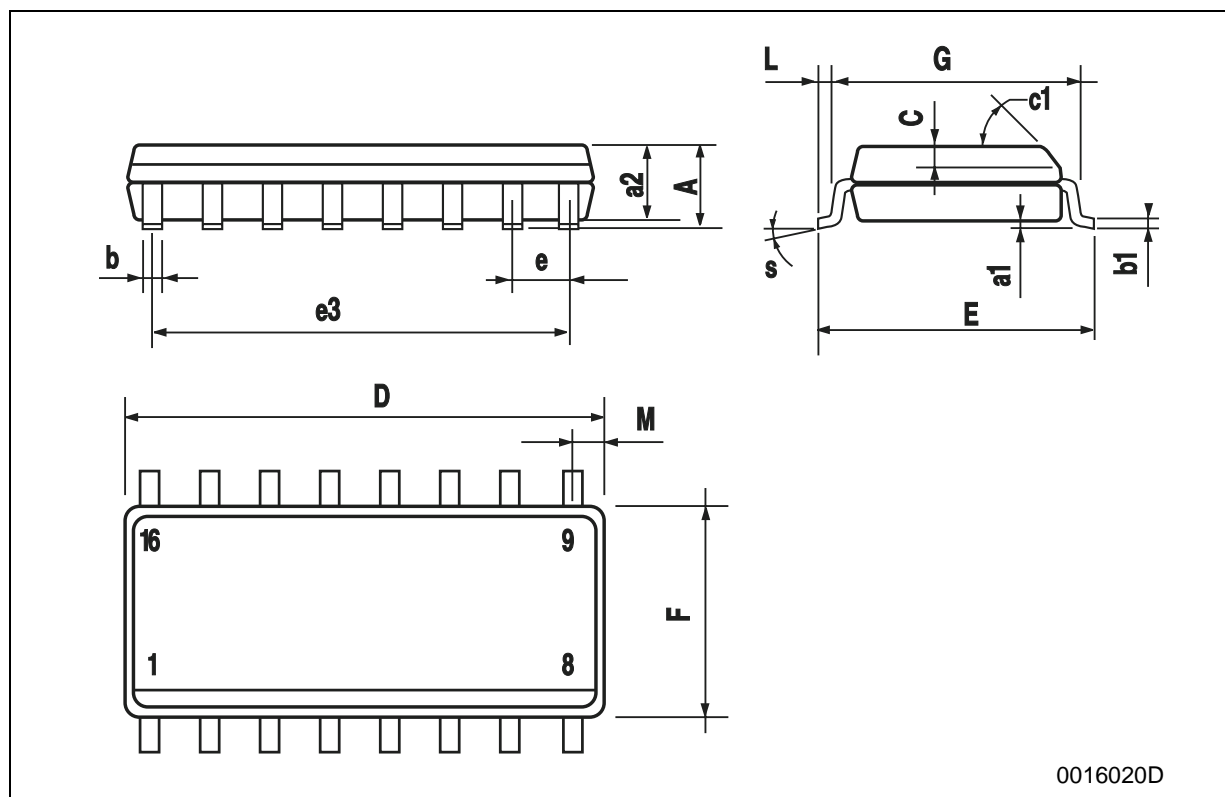


Table 10: Waveform 2: Pulse Width (f=1MHz; 50% duty cycle)



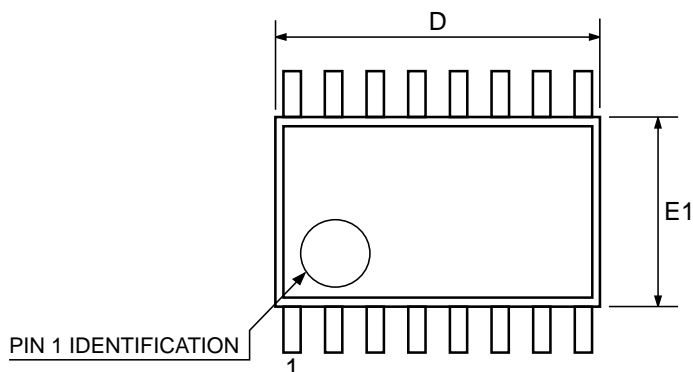
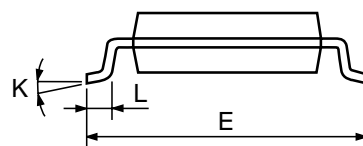
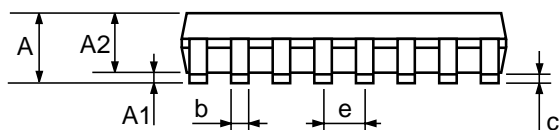
SO-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.64 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 9.8 | | 10 | 0.385 | | 0.393 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8° (max.) | | | | | |



TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|----------|------|-------|------------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0079 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



0080338D

Tape & Reel SO-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.45 | | 6.65 | 0.254 | | 0.262 |
| Bo | 10.3 | | 10.5 | 0.406 | | 0.414 |
| Ko | 2.1 | | 2.3 | 0.082 | | 0.090 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |



Tape & Reel TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|------|-------|------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.7 | | 6.9 | 0.264 | | 0.272 |
| Bo | 5.3 | | 5.5 | 0.209 | | 0.217 |
| Ko | 1.6 | | 1.8 | 0.063 | | 0.071 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |

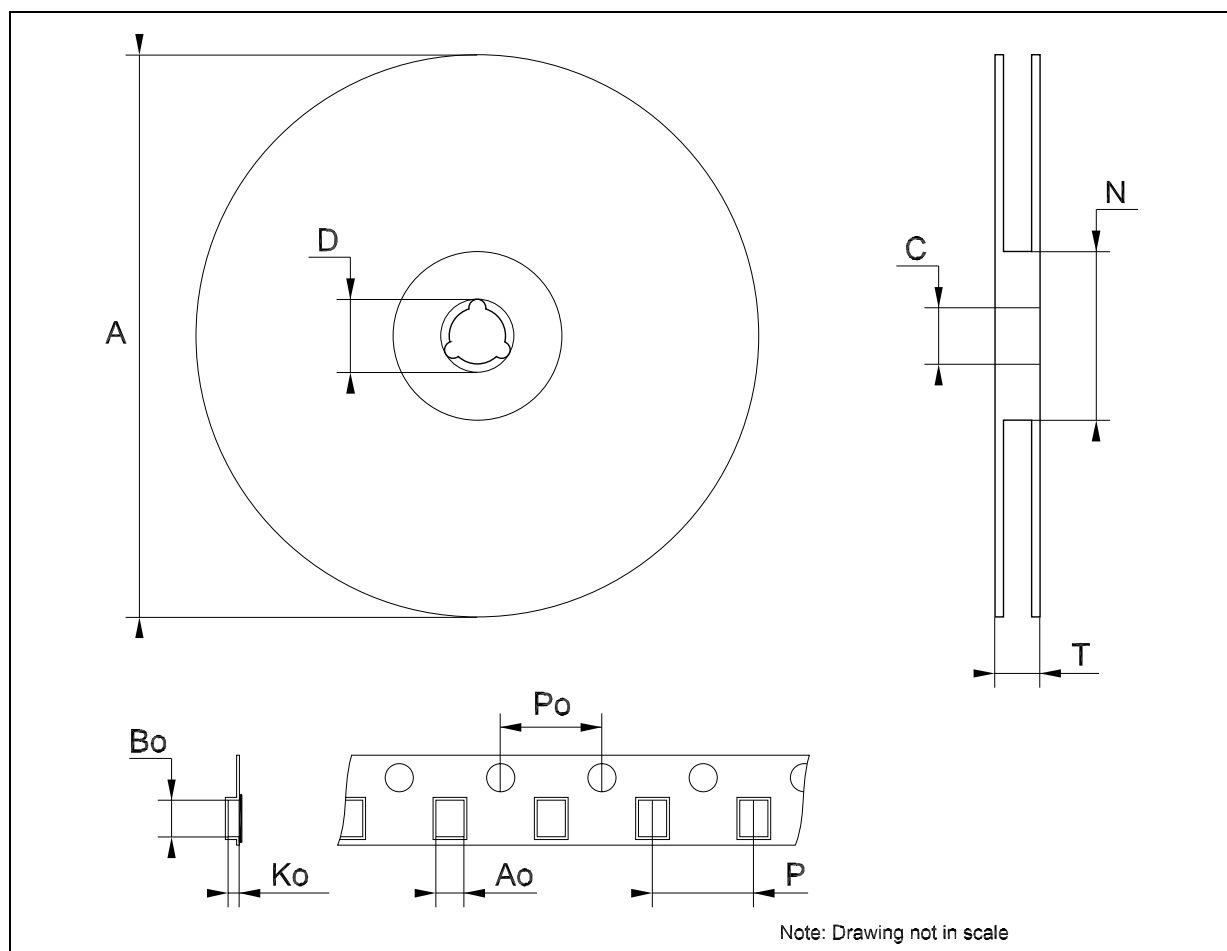


Table 11: Revision History

| Date | Revision | Description of Changes |
|-------------|----------|--------------------------------|
| 12-Nov-2004 | 5 | Order Codes Revision - pag. 1. |

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