

**AK4565****Low Power 20bit CODEC with built-in ALC****GENERAL DESCRIPTION**

The AK4565 is a low power voltage, 20bit CODEC. The recording feature includes four stereo inputs selector which switches among microphone and line inputs etc. And the input PGA has an ALC function, making it suitable for microphone application. The AK4565 has a dedicated power supply pin for digital I/F, which can support I/O level down to 1.5V. The AK4565 can be powered-down partly and is suitable for portable application.

**FEATURES**

1. Resolution: 20bits
2. Recording Functions
  - Four Stereo Inputs Selector
  - Input PGA (Programmable Gain Amplifier) with ALC (Automatic Level Control)
  - FADEIN / FADEOUT
  - Digital HPF for DC-offset cancellation ( $f_c=3.7\text{Hz}@f_s=48\text{kHz}$ )
3. Playback Function
  - Digital De-emphasis Filter ( $t_c = 50/15\mu\text{s}$ ,  $f_s=32\text{k}$ ,  $44.1\text{k}$  and  $48\text{kHz}$ )
4. Power Management
5. CODEC
  - Single-ended Inputs/Outputs
  - Input / Output Level:  $1.5\text{Vpp}@V_{\text{REF}}=2.5\text{V}$  ( $= 0.6 \times V_{\text{REF}}$ )
  - S/(N+D): 83dB(ADC), 86dB(DAC) @ $V_{\text{REF}}=2.5\text{V}$
  - DR, S/N: 87dB(ADC), 91dB(DAC) @ $V_{\text{REF}}=2.5\text{V}$
6. Master Clock: 256fs/384fs
7. Sampling Rate: 8kHz ~ 50kHz
8. Audio Data Interface Format: MSB-First, 2's compliment
  - ADC: 20bit MSB justified,  $I^2\text{S}$
  - DAC: 20bit MSB justified, 16/20bit LSB justified,  $I^2\text{S}$
9.  $\mu\text{P}$  Interface: 4-wire
10. Power Supply
  - CODEC, IPGA: 2.3 ~ 3.6V (typ.2.5V)
  - Digital I/F: 1.5 ~ 3.6V(yp.2.5V)
11. Power Supply Current
  - ALL Power ON: 12.5mA
  - IPGA + ADC: 8mA
  - DAC: 5.5mA
12.  $T_a = -40 \sim 85^\circ\text{C}$
13. Package: 28pin VSOP
14. AK4563A pin-compatible

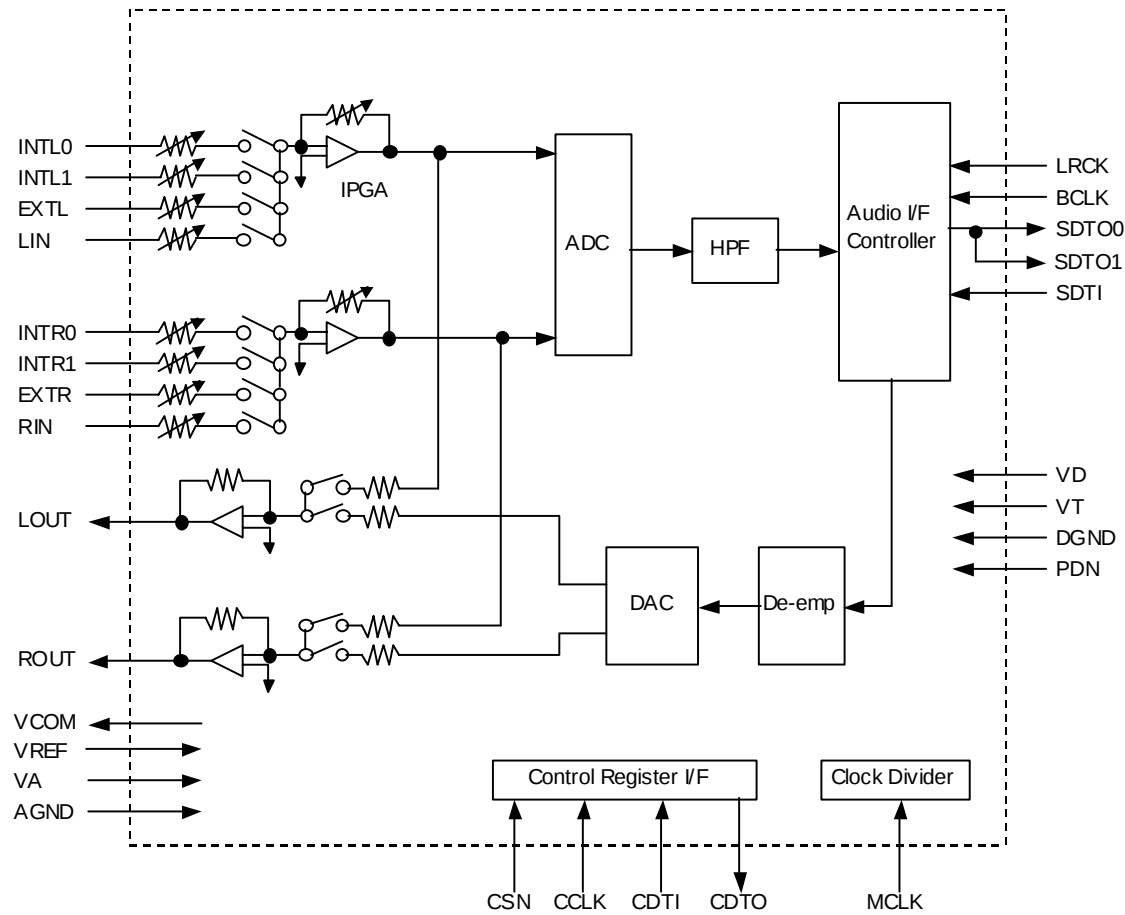


Figure 1. AK4565 Block Diagram

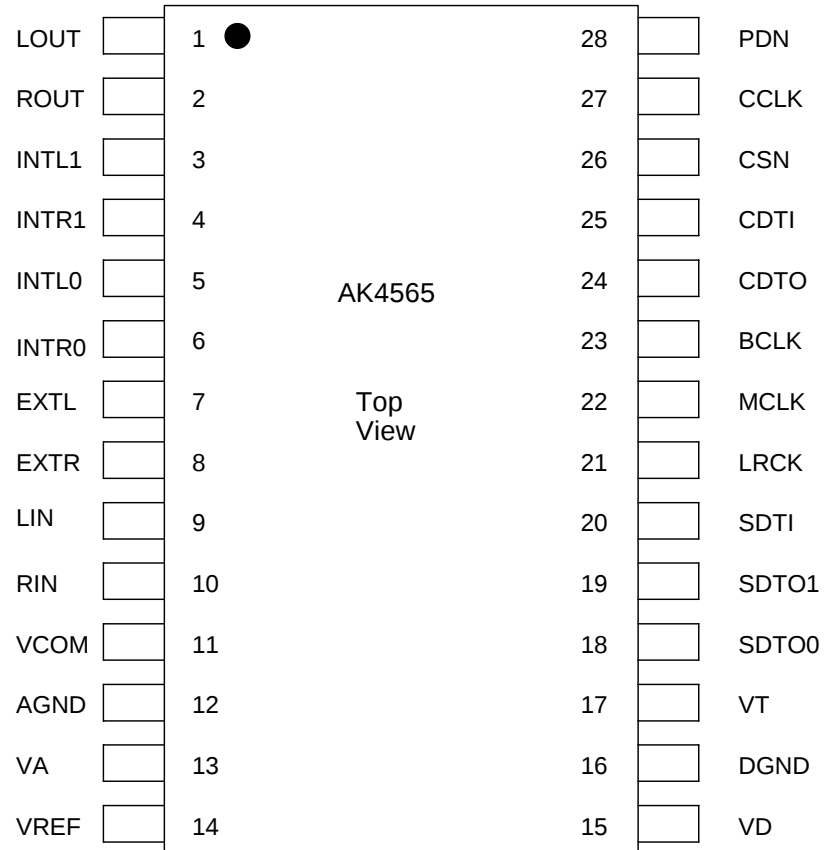
## ■ Ordering Guide

AK4565VF  
AKD4565

-40 ~ +85°C  
Evaluation board for AK4565

28pin VSOP (0.65mm pitch)

## ■ Pin Layout



| PIN / FUNCTION |          |     |                                                                                                                                            |
|----------------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------|
| No.            | Pin Name | I/O | Function                                                                                                                                   |
| 1              | LOUT     | O   | Lch Analog Output Pin                                                                                                                      |
| 2              | ROUT     | O   | Rch Analog Output Pin                                                                                                                      |
| 3              | INTL1    | I   | Lch INT #1 Input Pin                                                                                                                       |
| 4              | INTR1    | I   | Rch INT #1 Input Pin                                                                                                                       |
| 5              | INTL0    | I   | Lch INT #0 Input Pin                                                                                                                       |
| 6              | INTR0    | I   | Rch INT #0 Input Pin                                                                                                                       |
| 7              | EXTL     | I   | Lch EXT Input Pin                                                                                                                          |
| 8              | EXTR     | I   | Rch EXT Input Pin                                                                                                                          |
| 9              | LIN      | I   | Lch Line Input Pin                                                                                                                         |
| 10             | RIN      | I   | Rch Line Input Pin                                                                                                                         |
| 11             | VCOM     | O   | Common Voltage Output Pin, $0.45 \times V_A$<br>Bias voltage of ADC inputs and DAC outputs                                                 |
| 12             | AGND     | -   | Analog Ground Pin                                                                                                                          |
| 13             | VA       | -   | Analog Power Supply Pin, +2.3 ~ 3.6V                                                                                                       |
| 14             | VREF     | I   | ADC & DAC Voltage Reference Input Pin, $V_A$<br>Used as a voltage reference of ADC & DAC. VREF is connected externally to filtered $V_A$ . |
| 15             | VD       | -   | Digital Power Supply Pin, +2.3 ~ 3.6V                                                                                                      |
| 16             | DGND     | -   | Digital Ground Pin                                                                                                                         |
| 17             | VT       | -   | Digital I/F Power Supply Pin, +1.5 ~ 3.6V                                                                                                  |
| 18             | SDTO0    | O   | Audio Serial Data #0 Output Pin                                                                                                            |
| 19             | SDTO1    | O   | Audio Serial Data #1 Output Pin                                                                                                            |
| 20             | SDTI     | I   | Audio Serial Data Input Pin                                                                                                                |
| 21             | LRCK     | I   | Input/Output Channel Clock Pin                                                                                                             |
| 22             | MCLK     | I   | Master Clock Input Pin                                                                                                                     |
| 23             | BCLK     | I   | Audio Serial Data Clock Pin                                                                                                                |
| 24             | CDTO     | O   | Control Data Output Pin                                                                                                                    |
| 25             | CDTI     | I   | Control Data Input Pin                                                                                                                     |
| 26             | CSN      | I   | Chip Select Pin                                                                                                                            |
| 27             | CCLK     | I   | Control Data Clock Pin                                                                                                                     |
| 28             | PDN      | I   | Power Down & Reset Pin, "L": Power Down & Reset, "H": Normal Operation                                                                     |

Note: All digital input pins should not be left floating.

**ABSOLUTE MAXIMUM RATING**

(AGND, DGND=0V; Note 1)

| Parameter                              |                        | Symbol       | min  | max      | Units |
|----------------------------------------|------------------------|--------------|------|----------|-------|
| Power Supply                           | Analog (VA pin)        | VA           | -0.3 | 4.6      | V     |
|                                        | Digital 1 (VD pin)     | VD           | -0.3 | 4.6      | V     |
|                                        | Digital 2 (VT pin)     | VT           | -0.3 | 4.6      | V     |
|                                        | DGND – AGND   (Note 2) | $\Delta$ GND | -    | 0.3      | V     |
| Input Current, Any Pin Except Supplies |                        | IIN          | -    | $\pm 10$ | mA    |
| Analog Input Voltage (Note 3)          |                        | VINA         | -0.3 | VA+0.3   | V     |
| Digital Input Voltage (Note 4)         |                        | VIND         | -0.3 | VT+0.3   | V     |
| Ambient Temperature                    |                        | Ta           | -40  | 85       | °C    |
| Storage Temperature                    |                        | Tstg         | -65  | 150      | °C    |

Note 1. All voltages with respect to ground.

Note 2. AGND and DGND must be connected to the same analog plane.

Note 3. INTL0, INTR0, INTL1, INTR1, EXTL, EXTR, LIN, RIN and VREF pins

Note 4. PDN, MCLK, BCLK, LRCK, SDTI, CSN, CCLK and CDTI pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**

(AGND, DGND=0V; Note 1)

| Parameter         |                                              | Symbol | min           | typ | max | Units |
|-------------------|----------------------------------------------|--------|---------------|-----|-----|-------|
| Power Supply      | Analog (VA pin)                              | VA     | 2.3           | 2.5 | 3.6 | V     |
|                   | Digital 1 (VD pin) (Note 5)                  | VD     | 2.3 or VA-0.3 | 2.5 | VA  | V     |
|                   | Digital 2 (VT pin)                           | VT     | 1.5           | 2.5 | VD  | V     |
| Reference Voltage | Analog Reference Voltage (VREF pin) (Note 6) | VREF   | -             | -   | VA  | V     |

Note 1. All voltages with respect to ground.

Note 5. Minimum value is the higher between 2.3V and “VA-0.3”V.

Note 6. VREF and VA should be the same voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHARACTERISTICS

(Ta=25°C; VA, VD, VT=2.5V; fs=48kHz; Signal Frequency =1kHz; Measurement frequency = 10Hz ~ 20kHz; Unless otherwise specified)

| Parameter                                                                            | min           | typ           | max         | Units           |
|--------------------------------------------------------------------------------------|---------------|---------------|-------------|-----------------|
| Input PGA Characteristics (IPGA):                                                    |               |               |             |                 |
| Input Voltage<br>(INTL1-0, INTR1-0, EXTL, EXTR, LIN and RIN pins) (Note 7)           | 1.35          | 1.5           | 1.65        | V <sub>pp</sub> |
| Input Resistance: MIC (INTL1-0, INTR1-0, EXTL and EXTR pins)<br>LINE (LIN, RIN pins) | 6.5<br>80     | 10<br>125     | 14.5<br>176 | kΩ              |
| Step Size                                                                            | MIC           | LINE          |             |                 |
|                                                                                      | +28dB ~ -8dB  | +6dB ~ -30dB  |             |                 |
|                                                                                      | -8dB ~ -16dB  | -30dB ~ -38dB |             |                 |
|                                                                                      | -16dB ~ -32dB | -38dB ~ -54dB |             |                 |
|                                                                                      | -32dB ~ -40dB | -54dB ~ -62dB |             |                 |
|                                                                                      | -40dB ~ -52dB | -62dB ~ -74dB |             |                 |
|                                                                                      | 0.1           | 0.5           | 0.9         | dB              |
|                                                                                      | 0.1           | 1             | 1.9         | dB              |
|                                                                                      | 0.1           | 2             | 3.9         | dB              |
|                                                                                      | -             | 2             | -           | dB              |
|                                                                                      | -             | 4             | -           | dB              |
| ADC Analog Input Characteristics: (Note 8)                                           |               |               |             |                 |
| Resolution                                                                           |               |               | 20          | Bits            |
| S/(N+D) (-2dBFS)                                                                     | 74            | 83            |             | dB              |
| D-Range (-60dBFS, A-weighted)                                                        | 81            | 87            |             | dB              |
| S/N (A-weighted)                                                                     | 81            | 87            |             | dB              |
| Interchannel Isolation (Note 9)                                                      | 85            | 100           |             | dB              |
| Interchannel Gain Mismatch                                                           |               | 0.2           | 0.5         | dB              |
| DAC Analog Output Characteristics: Measured by LOUT/ROUT                             |               |               |             |                 |
| Resolution                                                                           |               |               | 20          | Bits            |
| S/(N+D) (0dBFS)                                                                      | 77            | 86            |             | dB              |
| D-Range (-60dBFS, A-weighted)                                                        | 85            | 91            |             | dB              |
| S/N (A-weighted)                                                                     | 85            | 91            |             | dB              |
| Interchannel Isolation                                                               | 85            | 100           |             | dB              |
| Interchannel Gain Mismatch                                                           |               | 0.2           | 0.5         | dB              |
| Output Voltage (Note 10)                                                             | 1.35          | 1.5           | 1.65        | V <sub>pp</sub> |
| Load Resistance                                                                      | 10            |               |             | kΩ              |
| Load Capacitance                                                                     |               |               | 20          | pF              |
| Power Supplies                                                                       |               |               |             |                 |
| Power Supply Current: VA+VD+VT                                                       |               |               |             |                 |
| Normal Operation (PDN= “H”)                                                          |               |               |             |                 |
| All Power ON (PM3=“0”, PM2=PM1=PM0=“1”)                                              |               | 12.5          | 19          | mA              |
| IPGA + ADC (PM3=PM2=“0”, PM1=PM0=“1”)                                                | -             | 8.0           | -           | mA              |
| DAC (PM3=“0”, PM2= “1”, PM1=PM0=“0”)                                                 | -             | 5.5           | -           | mA              |
| Power-down mode (PDN= “L”) (Note 11)                                                 |               | 10            | 100         | μA              |

Note 7. Full-scale voltage of analog inputs when IPGA is set 0dB. Its voltage is proportional to VREF.  $V_{in} = 0.6 \times V_{REF}$ .

Note 8. ADC measurements are input from INTL0/INTR0, INTL1/INTR1, EXTL/EXTR or LIN/RIN and routed through IPGA. The gain of IPGA is set 0dB.

The internal HPF cancels the offset of IPGA and ADC.

Note 9. This value is interchannel isolation between INTL0 and INTR0, between INTL1 and INTR1, between EXTL and EXTR, or between LIN and RIN.

Note 10. Analog output voltage is proportional to VREF.  $V_{out} = 0.6 \times V_{REF}$ .

Note 11. All digital input pins except for PDN pin are held at VT or DGND. PDN pin is held at DGND.

| FILTER CHARACTERISTICS                                                  |         |        |      |      |       |       |
|-------------------------------------------------------------------------|---------|--------|------|------|-------|-------|
| (Ta=25°C; VA, VD=2.3 ~ 3.6V; VT=1.5~ 3.6V; fs=48kHz; De-emphasis = OFF) |         |        |      |      |       |       |
| Parameter                                                               |         | Symbol | min  | typ  | max   | Units |
| ADC Digital Filter (Decimation LPF):                                    |         |        |      |      |       |       |
| Passband (Note 12)                                                      | ±0.1dB  | PB     | 0    |      | 18.9  | kHz   |
|                                                                         | -1.0dB  |        | -    | 21.8 | -     | kHz   |
|                                                                         | -3.0dB  |        | -    | 23.0 | -     | kHz   |
| Stopband (Note 12)                                                      |         | SB     | 29.4 |      |       | kHz   |
| Passband Ripple                                                         |         | PR     |      |      | ±0.1  | dB    |
| Stopband Attenuation                                                    |         | SA     | 65   |      |       | dB    |
| Group Delay (Note 13)                                                   |         | GD     | -    | 17.0 | -     | 1/fs  |
| Group Delay Distortion                                                  |         | ΔGD    |      | 0    |       | μs    |
| ADC Digital Filter (HPF):                                               |         |        |      |      |       |       |
| Frequency Response (Note 12)                                            | -3.0dB  | FR     | -    | 3.7  | -     | Hz    |
|                                                                         | -0.56dB |        | -    | 10   | -     | Hz    |
|                                                                         | -0.15dB |        | -    | 20   | -     | Hz    |
| DAC Digital Filter:                                                     |         |        |      |      |       |       |
| Passband (Note 12)                                                      | ±0.1dB  | PB     | 0    |      | 21.7  | kHz   |
|                                                                         | -6.0dB  |        | -    | 24.0 | -     | kHz   |
| Stopband (Note 12)                                                      |         | SB     | 26.2 |      |       | kHz   |
| Passband Ripple                                                         |         | PR     |      |      | ±0.06 | dB    |
| Stopband Attenuation                                                    |         | SA     | 43   |      |       | dB    |
| Group Delay (Note 13)                                                   |         | GD     | -    | 14.8 | -     | 1/fs  |
| Group Delay Distortion                                                  |         | ΔGD    |      | 0    |       | μs    |
| DAC Digital Filter + Analog Filter:                                     |         |        |      |      |       |       |
| Frequency Response: 0 ~ 20.0kHz                                         |         | FR     |      | ±0.5 |       | dB    |

Note 12. The passband and stopband frequencies scale with fs.

For example, ADC: PB=0.454 x fs(@-1.0dB), DAC: PB=0.454 x fs(@-0.1dB).

Note 13. The calculated delay time caused by digital filtering. This time is from the input of an analog signal to setting the 20bit data of both channels to the output register of the ADC and includes the group delay of the HPF.

For DAC, this time is from setting the 20bit data of both channels on input register to the output of analog signal.

**DC CHARACTERISTICS**

(Ta=25°C; VA, VD=2.3 ~ 3.6V, VT=1.5 ~ 3.6V)

| Parameter                              | Symbol | Min    | typ | max   | Units |
|----------------------------------------|--------|--------|-----|-------|-------|
| Input High Level Voltage               | VIH    | 80%VT  | -   | -     | V     |
| Input Low Level Voltage                | VIL    | -      | -   | 20%VT | V     |
| Output High Level Voltage: Iout=-400μA | VOH    | VT-0.4 | -   | -     | V     |
| Output Low Level Voltage: Iout=400μA   | VOL    | -      | -   | 0.4   | V     |
| Input Leakage Current                  | Iin    | -      | -   | ±10   | μA    |

**SWITCHING CHARACTERISTICS**

(Ta=25°C; VA, VD=2.3 ~ 3.6V, VT=1.5 ~ 3.6V; CL=20pF)

| Parameter                                         | Symbol | Min          | typ    | max      | Units |
|---------------------------------------------------|--------|--------------|--------|----------|-------|
| <b>Control Clock Frequency</b>                    |        |              |        |          |       |
| Master Clock (MCLK) 256fs: Frequency              | fCLK   | 2.048        | 12.288 | 12.8     | MHz   |
| Pulse Width Low                                   | tCLKL  | 28           |        |          | ns    |
| Pulse Width High                                  | tCLKH  | 28           |        |          | ns    |
| 384fs: Frequency                                  | fCLK   | 3.072        | 18.432 | 19.2     | MHz   |
| Pulse Width Low                                   | tCLKL  | 23           |        |          | ns    |
| Pulse Width High                                  | tCLKH  | 23           |        |          | ns    |
| Channel Selection Clock (LRCK) frequency          | fs     | 8            | 48     | 50       | kHz   |
| Duty                                              |        | 45           | 50     | 55       | %     |
| <b>Audio Interface Timing</b>                     |        |              |        |          |       |
| BCLK Period                                       | tBLK   | 312.5        |        |          | ns    |
| BCLK Pulse Width Low                              | tBLKL  | 130          |        |          | ns    |
| Pulse Width High                                  | tBLKH  | 130          |        |          | ns    |
| BCLK “↓” to LRCK                                  | tBLR   | -tBLKH+50    |        | tBLKL-50 | ns    |
| LRCK to SDTO (MSB) (Except I <sup>2</sup> S mode) | tDLR   |              |        | 80       | ns    |
| BCLK “↓” to SDTO                                  | tDSS   |              |        | 80       | ns    |
| SDTI Hold Time                                    | tSDH   | 50           |        |          | ns    |
| SDTI Setup Time                                   | tSDS   | 50           |        |          | ns    |
| <b>Control Interface Timing</b>                   |        |              |        |          |       |
| CCLK Period                                       | tCCK   | 200(Note 15) |        |          | ns    |
| CCLK Pulse Width Low                              | tCCKL  | 80           |        |          | ns    |
| Pulse Width High 1                                | tCCKH  | 80           |        |          | ns    |
| Pulse Width High 2                                | tCKH2  | 80           |        |          | ns    |
| CDTI Setup Time                                   | tCDS   | 50           |        |          | ns    |
| CDTI Hold Time                                    | tCDH   | 50           |        |          | ns    |
| CSN “H” Time                                      | tCSW   | 150(Note 15) |        |          | ns    |
| CSN “↓” to CCLK “↑”                               | tCSS   | 50(Note 15)  |        |          | ns    |
| CCLK “↑” to CSN “↑”                               | tCSH   | 50           |        |          | ns    |
| CDTO Output Delay Time                            | tDCD   |              |        | 70       | ns    |
| CSN “↑” to CDTO(Hi-Z) (Note 14.)                  | tCCZ   |              |        | 70       | ns    |
| <b>Reset/Calibration Timing</b>                   |        |              |        |          |       |
| PDN Pulse Width                                   | tPDW   | 150          |        |          | ns    |
| PDN “↑” to SDTO0/SDTO1 valid                      | tPDV   |              | 4128   |          | 1/fs  |

Note 14. RL=1kΩ/10% Change (Pulled-up operates for VT.)

Note 15. fs ≥ 22.4kHz.

In the case of fs &lt; 22.4kHz, these three parameters must meet a relationship of

(tCSW + tCSS + 6 × tCCK) > 1/(32 × fs) in addition to these specifications. For example, When tCCK=200ns and tCSS=50ns at fs=8kHz, tCSW(min) is 2657ns. When tCSW=150ns and tCSS=50ns fs=8kHz, tCCK(min) is 618ns.

## ■ Timing Diagram

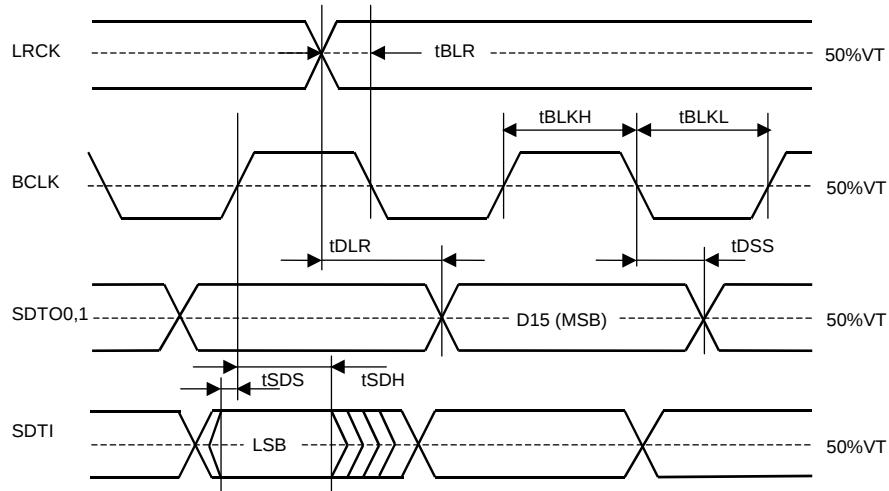


Figure 2. Audio Data Input/Output Timing (Audio I/F Format: No.0)

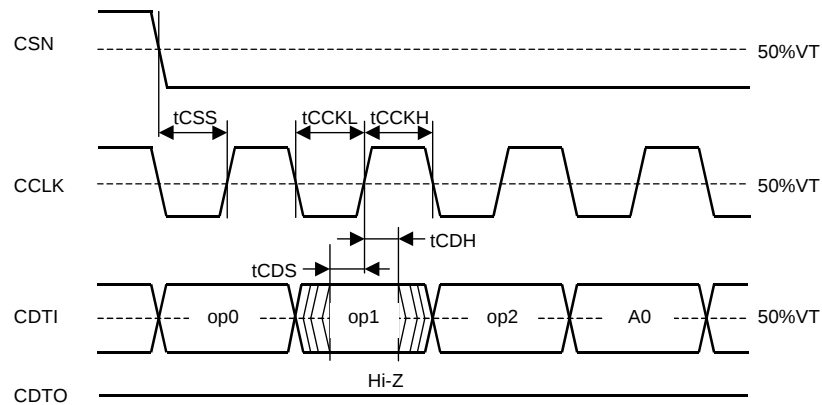


Figure 3. WRITE/READ Command Input Timing

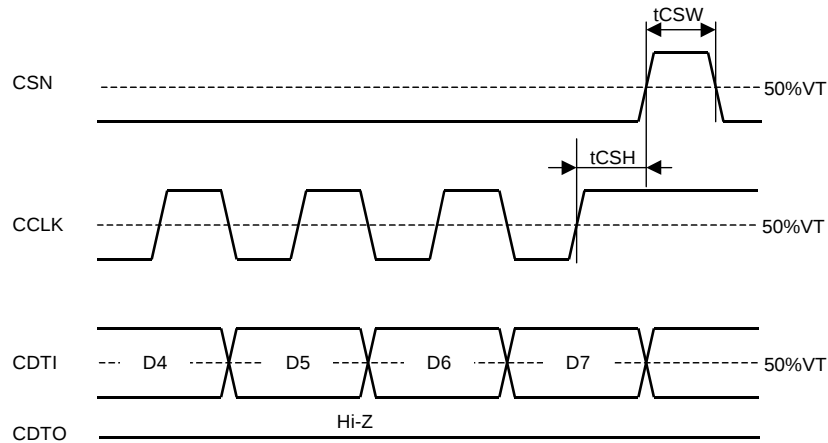


Figure 4. WRITE Data Input Timing

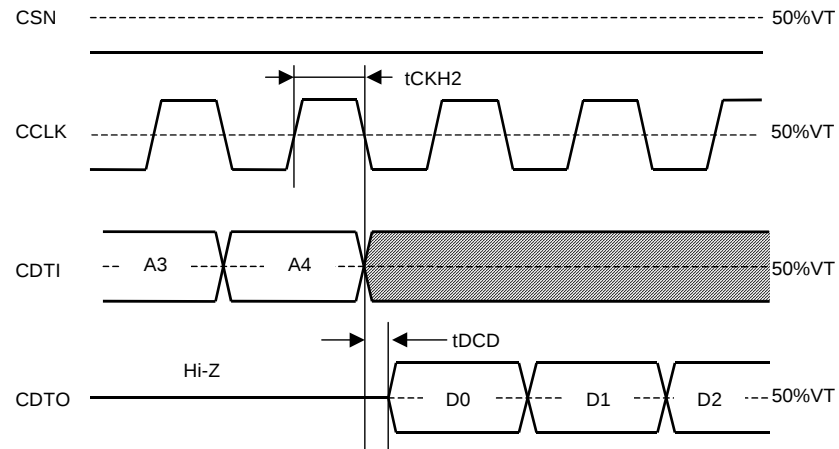


Figure 5. READ Data Output Timing 1

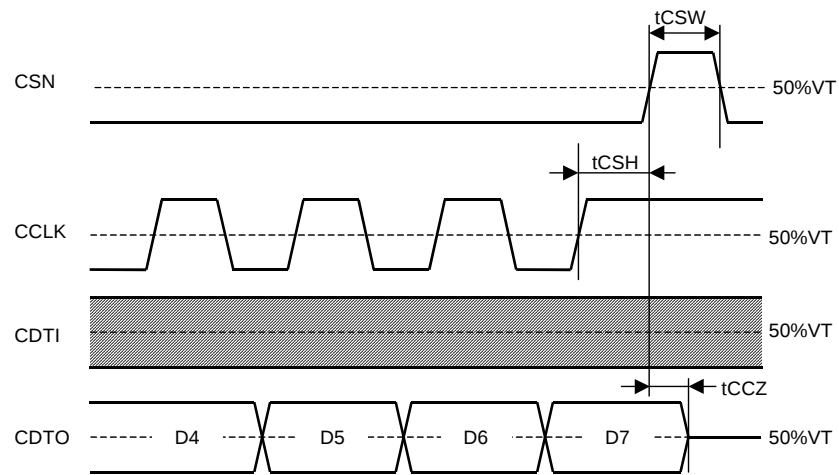


Figure 6. READ Data Input Timing 2

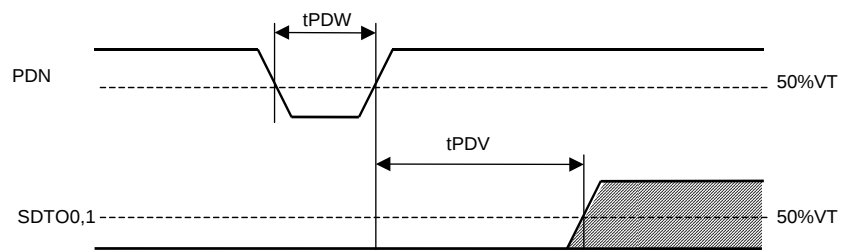


Figure 7. Reset Timing

|                           |
|---------------------------|
| <b>OPERATION OVERVIEW</b> |
|---------------------------|

**■ System Clock Input**

The clocks required to operate are MCLK (256fs/384fs), LRCK (fs) and BCLK (32fs~). The master clock (MCLK) should be synchronized with LRCK. The phase between these clocks does not matter. The frequency of MCLK can be input as 256fs or 384fs. When the 384fs is input, the internal master clock is divided into 2/3 automatically.

\*fs is sampling frequency.

All external clocks (MCLK, BCLK and LRCK) should always be present whenever the ADC or DAC is in operation. If these clocks are not provided, the AK4565 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the AK4565 should be placed in power-down mode.

**■ System Reset**

The AK4565 is placed in the power-down mode by bringing PDN “L”. This reset should always be done after power-up. After the system reset operation, the all internal registers are initial value.

Initialization cycle is  $4128/\text{fs}=86\text{ms}$  @  $\text{fs}=48\text{kHz}$ . During initializing cycle, the ADC digital data outputs of both channels are forced to a 2's complement “0”. Output data of ADC settles data equivalent for analog input signal after initializing cycle. This cycle is not for DAC.

**Writing to Addr = 01H must not be done during initialization cycle after exiting power-down mode by PDN pin. If the writing to 01H is done, a normal initialization cycle may not be done.**

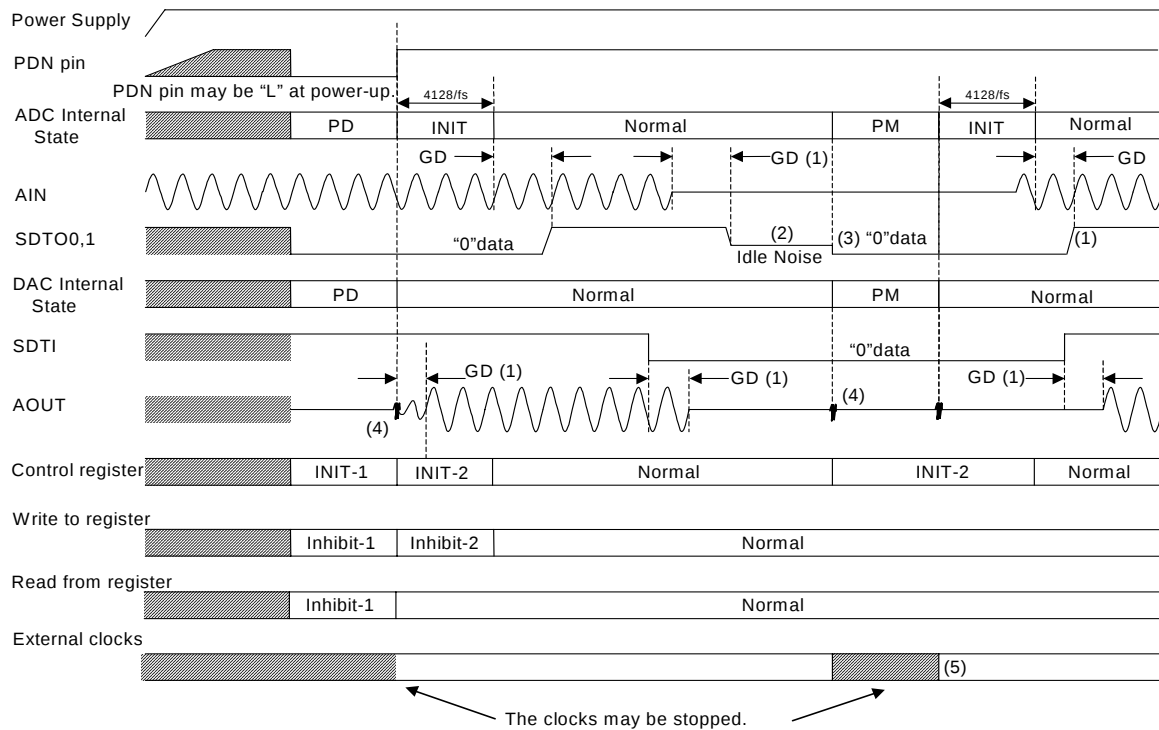


Figure 8. Power-up/Power-down Timing Example

- INIT: Initializing. At this time, STAT bit is "0". When this flag becomes "1", INIT process has completed. IPGA is MUTE state.
- PD: Power-down state. ADC is output "0", analog output of DAC goes floating.
- PM: Power-down state by operating Power Management bit
- INIT-1: Initializing all registers.
- INIT-2: Initializing read only registers in control registers.
- Inhibit-1: Inhibits writing and reading to all control registers.
- Inhibit-2: Inhibits writing to all control registers.

Note: Please refer to "explanation of register" about the condition of each register.

- (1) Digital output corresponding to the analog input and analog output corresponding to the digital input are delayed by the group delay (GD).
- (2) If the analog signal does not be input, the digital outputs have the op-amp of input and some noise in ADC.
- (3) ADC data is "0" data at power-down.
- (4) A few noise occurs at the "↓↑" of PDN signal. Please mute the analog output externally if the noise influences the system application.
- (5) When the external clocks are stopped, the AK4565 should be placed in the power-down state (PDN pin = "L" or PM3-0 bit = "0") .

## ■ Digital High Pass Filter (HPF)

The AK4565 has a Digital High Pass Filter (HPF) to cancel DC-offset in both the IPGA and ADC. The cut-off frequency of the HPF is 3.7Hz at  $f_s=48\text{kHz}$  and it is attenuated to  $-0.15\text{dB}$  at 20Hz. This cut-off frequency scales with the sampling frequency ( $f_s$ ).

## ■ Audio Serial Interface Format

The SDTI, SDTO0, SDTO1, BCLK and LRCK pins are connected to an external controller. The audio data format has four modes, MSB-first and 2's complement. The data format is set using the DIF1-0 bits. SDTI is latched by "↑" of BCLK. SDTO0 and SDTO1 are latched by "↓".

**Outputs data of SDTO0 are the same as SDTO1's. SDTO1 can be generated to "L" when DMUTE bit is "1".**

| No. | DIF1 bit | DIF0 bit | SDTO0/SDTO1(ADC)                  | SDTI (DAC)                        | BCLK         | Figure    |         |
|-----|----------|----------|-----------------------------------|-----------------------------------|--------------|-----------|---------|
| 0   | 0        | 0        | 20bit MSB justified               | 16bit LSB justified               | $\geq 32f_s$ | Figure 9  | Default |
| 1   | 0        | 1        | 20bit MSB justified               | 20bit LSB justified               | $\geq 40f_s$ | Figure 10 |         |
| 2   | 1        | 0        | 20bit MSB justified               | 20bit MSB justified               | $\geq 40f_s$ | Figure 11 |         |
| 3   | 1        | 1        | 16bit I <sup>2</sup> S compatible | 16bit I <sup>2</sup> S compatible | $= 32f_s$    | Figure 12 |         |
|     | 1        | 1        | 20bit I <sup>2</sup> S compatible | 20bit I <sup>2</sup> S compatible | $\geq 40f_s$ | Figure 12 |         |

Table 1. Audio Data Format

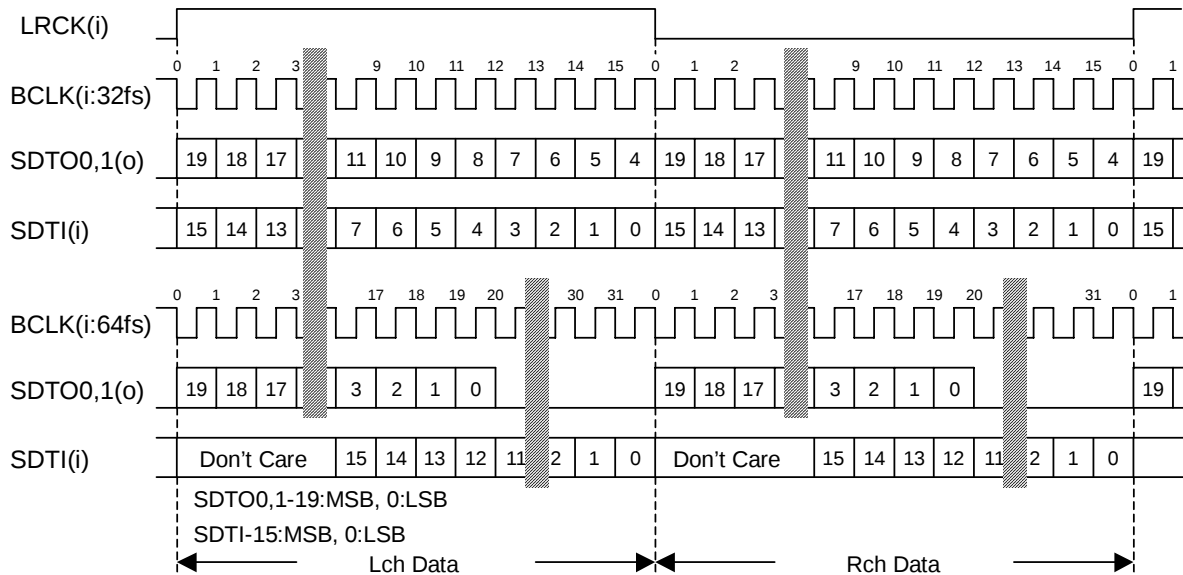


Figure 9. Audio Data Timing (No.0)

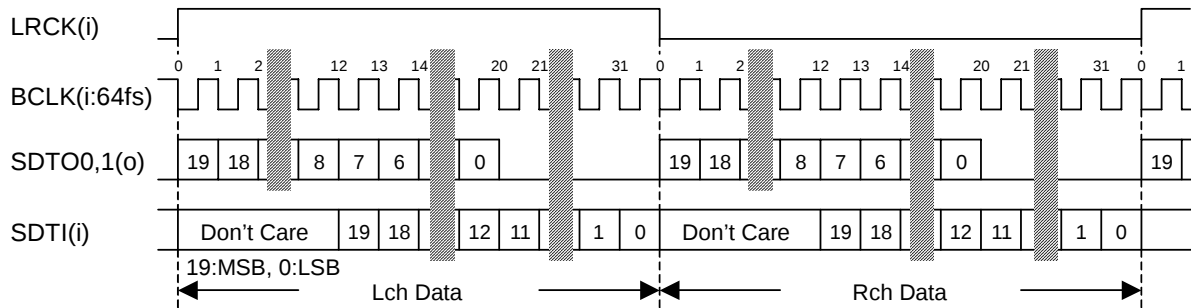


Figure 10. Audio Data Timing (No.1)

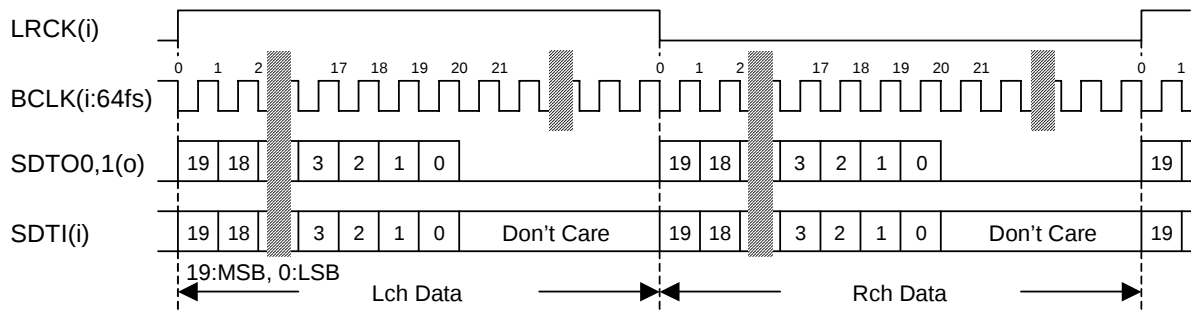


Figure 11. Audio Data Timing (No.2)

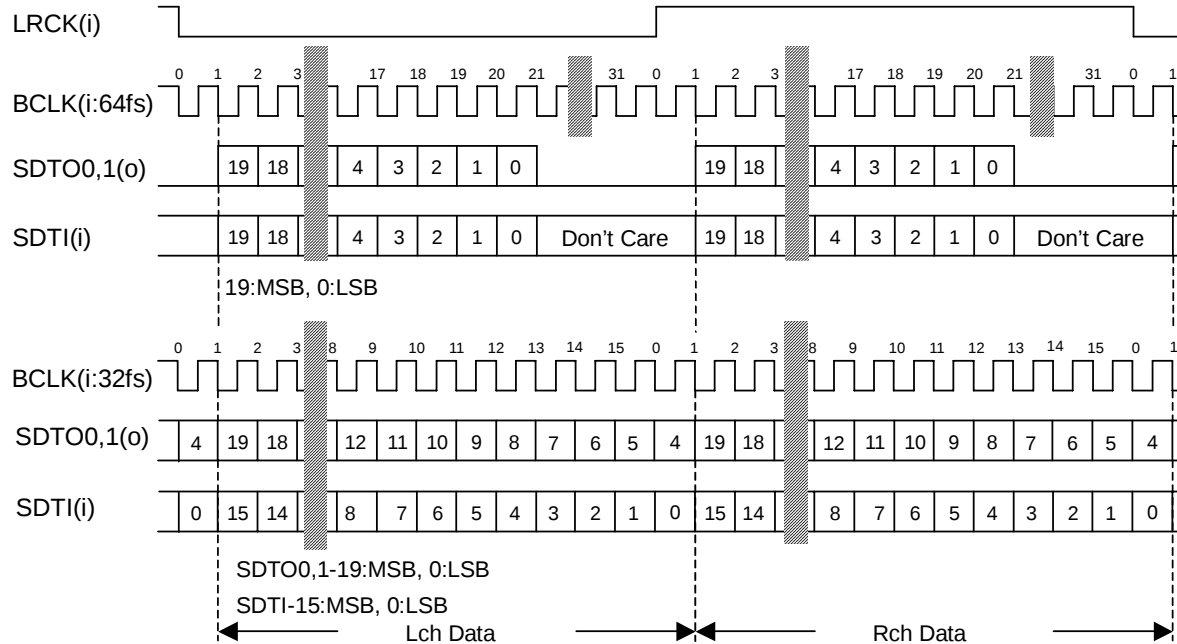


Figure 12. Audio Data Timing (No.3)

## ■ ALC Operation

### 1. ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceed ALC limiter detection level (LMTH), IPGA value is attenuated by ALC limiter ATT step (LMAT1-0) automatically. Then the IPGA value is changed commonly for L/R channels in IPGA.

When ZELMN = "1", timeout period is set by LTM1-0 bits. The operation for attenuation is done continuously until the input signal level becomes LMTH or less. After finishing the operation for attenuation, if ALC bit does not change into "0", the operation of attenuation repeats when the input signal level exceed LMTH.

When ZELMN = "0", the ALC1 limiter operation is attenuated by the set of ZTM1-0 bits. IPGA value is attenuated by zero crossing detection automatically.

When FR bit is "0", the ALC operation corresponds to the impulse noise. Then if the impulse noise is supplied at ZELMN = "0", the ALC recovery operation becomes the faster period than a set of ZTM1-0 bits. In case of ZELMN = "1", it becomes the same period as LTM1-0 bits.

When FR bit is "1", the ALC operation is done by normal period.

### 2. ALC Recovery Operation

The ALC recovery operation waits until a time of setting WTM1-0 bits after completing the ALC limiter. If the input signal does not exceed "ALC recovery waiting counter reset level (LMTH)", the ALC recovery operation is done. The IPGA value increases automatically by this operation up to the set reference level (REF6-0 bits). Then the IPGA value is set for L/R commonly. The ALC recovery operation is done at a period set by WTM1-0 bits.

When L/R channels in IPGA are detected by zero crossing operation during WTM1-0, the ALC recovery operation waits until WTM1-0 period and the next recovery operation is done.

During the ALC recovery operation or the recovery waiting, when either input signal level of L/R channels in IPGA exceed the ALC limiter detection level (LNTH), the ALC recovery operation changes into the ALC limiter operation immediately.

In case of "ALC recovery waiting counter reset level (LMTH) ≤ IPGA Output Signal < ALC limiter detection level (LMTH)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. Therefore, in case of "ALC recovery waiting counter reset level (LMTH) > IPGA Output Signal", the waiting timer of ALC recovery operation starts.

If the impulse noise is supplied at FR = "0", the ALC recovery operation becomes the faster period than a set of ZTM1-0 and WTM1-0 bits. When FR bit is "1", the ALC operation is done by normal period.

Other:

When a channel of one side enters the limiter operation during the waiting zero crossing, the present ALC recovery operation stops, according as the small value of IPGA (a channel of waiting zero crossing), the ALC limiter operation is done.

When both channels are waiting for the next ALC recovery operation, the ALC limiter operation is done from the IPGA value of a point in time.

ZTM1-0 bits set zero crossing timeout and WTM1-0 bits sets the ALC recovery operation period. When the ALC recovery waiting time (WTM1-0 bits) is shorter than zero crossing timeout period of ZTM1-0 bit, the ALC recovery is operated by the zero crossing timeout period of ZTM1-0 bit. Therefore, in this case the auto recovery operation period is not constant.

The following registers should be changed during the ALC operation.

- LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0, ZELMN

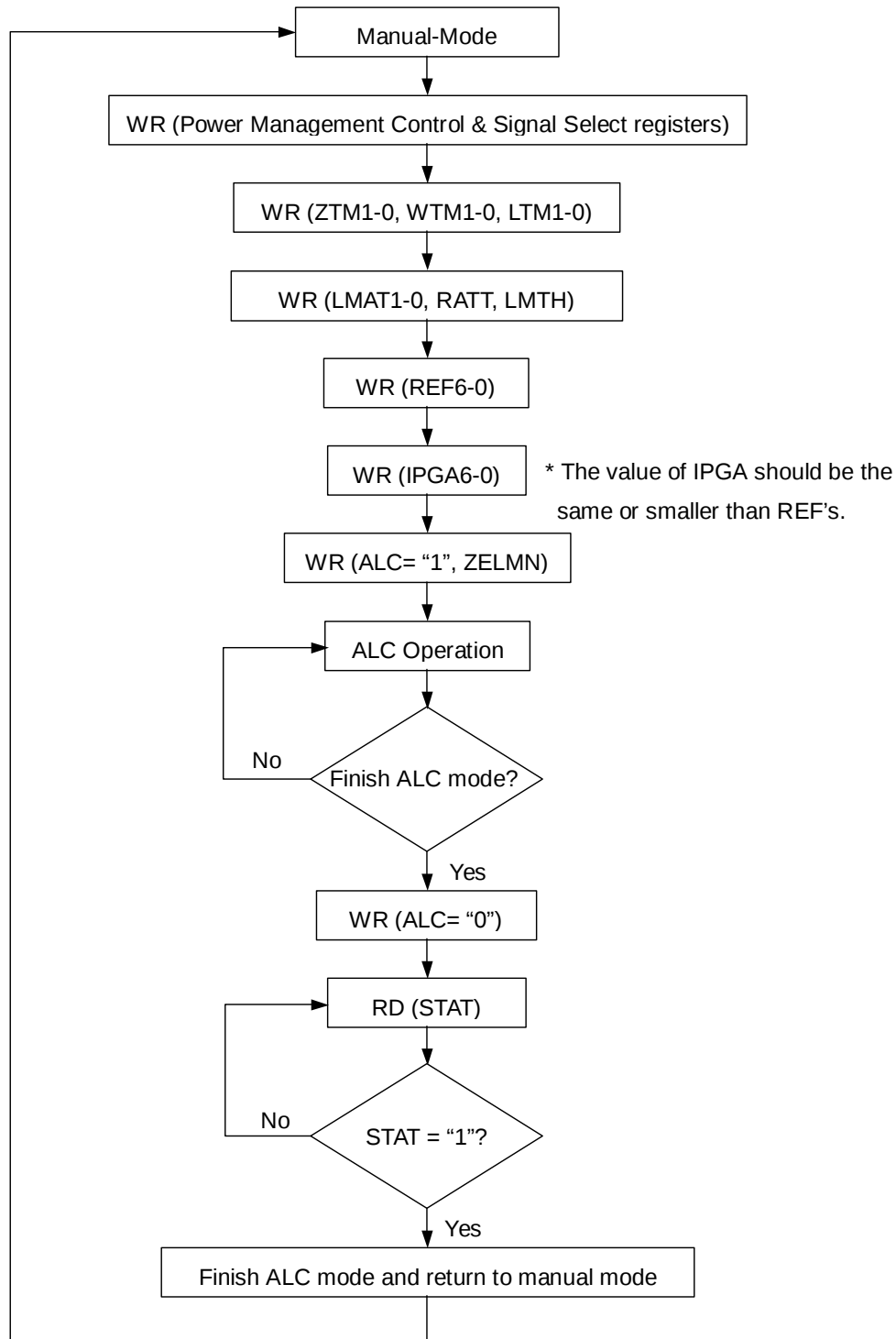


Figure 13. Registers set-up sequence at ALC operation

### ■ FADEIN Mode

In FADEIN Mode, the IPGA value increases gradually by the step set by FDATT bit when FDIN bit changes from “0” to “1”. The FADEIN period is set by FDTM1-0 bits. The FADEIN operation is done by the zero crossing detection. This operation stops when the IPGA value becomes the REF value or the limiter detection level (LMTH). If the limiter operation is done during FADAIN period, the FADEIN operation stops and the ALC operation starts.

NOTE: When FDIN and FDOUT bits are “1” at the same time, FADEOUT operation is prior to FADEIN operation.

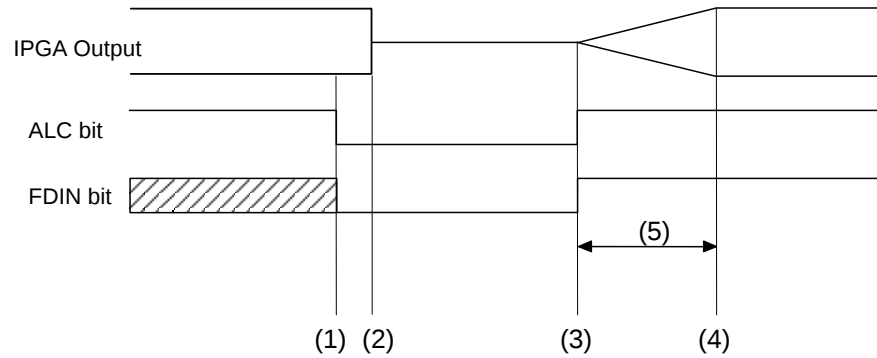


Figure 14. Example for controlling sequence in FADEIN operation

- (1) WR (ALC = FDIN = “0”): The ALC operation is disabled. To start the FADEIN operation, FDIN bit is written in “0”.
- (2) WR (IPGA = “MUTE”): The IPGA output is muted.
- (3) WR (ALC = FDIN = “1”): The FADEIN operation starts. The IPGA changes from the MUTE state to the FADEIN operation.
- (4) The FADEIN operation is done until the limiter detection level (LMTH) or the reference level (REF6-0). After completing the FADEIN operation, the AK4565 becomes the ALC operation.
- (5) FADEIN time is set by FDTM1-0 and FDATT bits  
 E.g. FDTM1-0 = 32ms, FDATT = 1step  

$$(96 \times \text{FDTM1-0}) / \text{FDATT} = 96 \times 32\text{ms} / 1 = 3.07\text{s}$$

## ■ FADEOUT Mode

In FADEOUT mode, the present IPGA value decreases gradually down to the MUTE state when FDOUT bit changes from “0” to “1”. This operation is done by the zero crossing detection. If the large signal is supplied to the ALC circuit during the FADEOUT operation, the ALC limiter operation starts. However, the total time of the FADEOUT operation is the same time, even if the limiter operation is done. The period of FADEOUT is set by FDTM1-0 bits, the number of step is set by FDATT bit. When FDOUT bit changes into “0” during the FADEOUT operation, the ALC operation start from the preset IPGA value. When FDOUT and ALC bits change into “0” at the same time, the FADEOUT operation stops and the IPGA kept the value at that time.

NOTE: When FDIN and FDOUT bits are set to “1” at the same time, FADEOUT operation is prior to FADEIN operation.

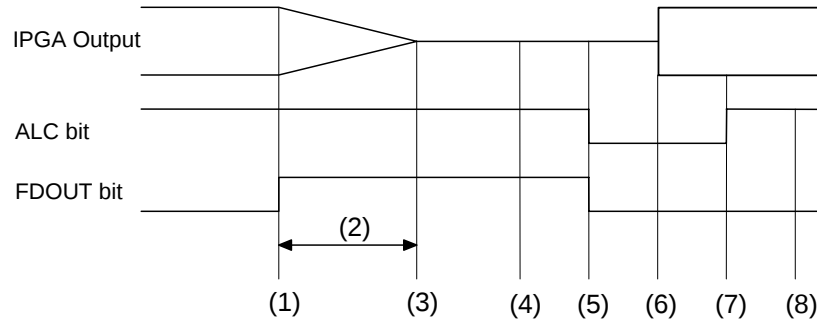


Figure 15. Example for controlling sequence in FADEOUT operation

- (1) WR (FDOUT = “1”): The FADEOUT operation starts. Then ALC bit should be always “1”.
- (2) FADEOUT time is set by FDTM1-0 and FDATT bits.  
During the FADEIN operation, the zero crossing timeout period is ignored and becomes the same as the FADEIN period.  
E.g.  $FDTM1-0 = 32\text{ms}$ ,  $FDATT = 1\text{step}$   
 $(96 \times FDTM1-0) / FDATT = 96 \times 32\text{ms} / 1 = 3.07\text{s}$
- (3) The FADEOUT operation is completed. The IPGA value is the MUTE state. If FDOUT bit keeps “1”, the IPGA value keeps the MUTE state.
- (4) Analog and digital outputs mutes externally. Then the IPGA value is the MUTE state.
- (5) WR (ALC = FDOUT = “0”): Exit the ALC and FADEOUT operations
- (6) WR (IPGA): The IPGA value changes the initial value (exiting MUTE state).
- (7) WR (ALC = “1”, FDOUT = “0”): The ALC operation restarts. But the ALC bit should be written until completing zero crossing detection operation of IPGA.
- (8) Release an external mute function for analog and digital outputs.

## ■ Operation of IPGA

[Writing operation at ALC Enable]

Writing to IPGA6-0 bit is ignored during ALC operation and FADEIN/OUT operation.

[Writing operation at ALC Disable]

**When writing to the control register continually, the control register should be written by an interval more than zero crossing timeout.** If not, there is a possibility that each IPGA of L/R channels has a different gain.

[IPGA Gain after completing ALC operation]

The IPGA gain changed by ALC operation. The actual gain of IPGA is changed during ALC operation but the IPGA register doesn't change. Therefore, when completing ALC operation (ALC bit; "1" → "0"), the IPGA register is different from the actual gain of IPGA. The value should be written to the IPGA register in order to set the actual gain of IPGA with a register value.

[Operation of IPGA at power-down by the control register]

IPGA gain is reset when PM0 bit is "0", and then IPGA operation starts from the default value when PM0 bit is changed to "1". When IPGA6-0 bits are read, the register values written by the last write operation are read out regardless the actual gain.

## ■ Control Register R/W Timing

The data on the 4 wires serial interface consists of op-code (3bit), address (LSB-first, 5bit) and control data (LSB-first, 8bit). The transmitting data is output to each bit by "↓" of CCLK, the receiving data is latched by "↑" of CCLK. Writing data becomes effective by "↑" of CSN. Reading data becomes Hi-z (Floating) by "↑" of CSN. CSN should be held to "H" at no access. In case of connecting between CDTI and CDTO, the I/F can be also controlled by 3-wires.

**CCLK always needs 16 edges of "↑" during CSN = "L". Reading/Writing of the address except 00H ~ 09H are inhibited. Reading/Writing of the control registers by except op0 = op1 = "1" are invalid.**

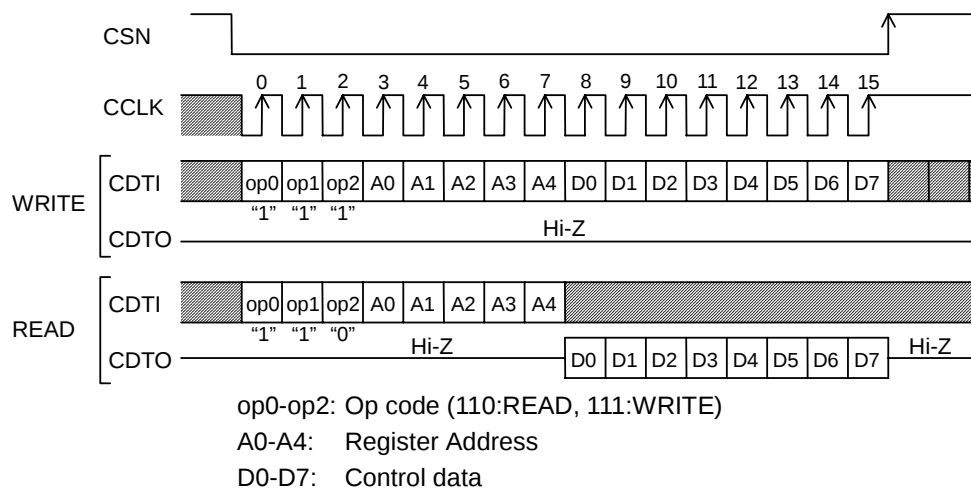


Figure 16. Control Data Timing

## ■ Register Map

| Addr | Register Name      | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|------|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 00H  | Input Select       | 0     | 0     | 0     | 0     | LINE  | EXT   | INT1  | INT0  |
| 01H  | Power Management   | 0     | 0     | PM3   | PM2   | 0     | PM1   | 0     | PM0   |
| 02H  | Mode Control       | 0     | 0     | DMUTE | FS    | DIF1  | DIF0  | DEM1  | DEM0  |
| 03H  | Timer Select       | FDTM1 | FDTM0 | ZTM1  | ZTM0  | WTM1  | WTM0  | LTM1  | LTM0  |
| 04H  | ALC Mode Control 1 | 0     | 0     | LMAT1 | LMAT0 | FDATT | RATT1 | RATT0 | LMTH  |
| 05H  | ALC Mode Control 2 | 0     | REF6  | REF5  | REF4  | REF3  | REF2  | REF1  | REF0  |
| 06H  | Operation Mode     | 0     | 0     | ZELMN | FR    | STAT  | FDIN  | FDOUT | ALC   |
| 07H  | Input PGA Control  | 0     | IPGA6 | IPGA5 | IPGA4 | IPGA3 | IPGA2 | IPGA1 | IPGA0 |
| 08H  | Test               | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 09H  | Test               | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

## ■ Register Definitions

All registers inhibit writing at PDN pin = “L”.

Writing to 08H and 09H is ignored and these addresses respond “0” at reading.

For addresses from 0AH to 1FH, data must not write.

| Addr    | Register Name | D7  | D6 | D5 | D4 | D3   | D2  | D1   | D0   |
|---------|---------------|-----|----|----|----|------|-----|------|------|
| 00H     | Input Select  | 0   | 0  | 0  | 0  | LINE | EXT | INT1 | INT0 |
| R/W     |               | R/W |    |    |    |      |     |      |      |
| Default |               | 0   | 0  | 0  | 0  | 0    | 0   | 0    | 1    |

INT0: Select ON/OFF of INTL0 and INTR0 (0: OFF, 1: ON)

INT1: Select ON/OFF of INTL1 and INTR1 (0: OFF, 1: ON)

EXT: Select ON/OFF of EXTL and EXTR (0: OFF, 1: ON)

LINE: Select ON/OFF of LIN and RIN (0:OFF, 1:ON)

**When LINE bit is “1”, INT0, INT1 and EXT bits are ignored. These inputs are always OFF.**

**When LINE bit is “1”, the gain table of IPGA switches LINE side.**

When LINE bit is “0”, if INT0, INT1 and EXT bits go to “1” at the same time, the input signals are mixed by 0dB gain.

| Addr    | Register Name    | D7  | D6 | D5  | D4  | D3 | D2  | D1 | D0  |
|---------|------------------|-----|----|-----|-----|----|-----|----|-----|
| 01H     | Power Management | 0   | 0  | PM3 | PM2 | 0  | PM1 | 0  | PM0 |
| R/W     |                  | R/W |    |     |     |    |     |    |     |
| Default |                  | 0   | 0  | 0   | 1   | 0  | 1   | 0  | 1   |

PM0: IPGA and ALC circuit power control.

0: Power OFF

1: Power ON (Default)

After exiting PM0 = "0", IPGA goes default value.

PM1: ADC power control.

0: Power OFF

1: Power ON (Default)

After exiting PM1 = "0", the initializing cycle (4128/fs) of ADC is started. Then output data of ADC becomes "0".

PM2: DAC power control.

0: Power OFF

1: Power ON (Default)

PM3: Used both as power control of analog loopback circuit and as selection of MUX. (0: DAC, 1: Analog loopback)

When PM3 goes "1", input for output-AMP is selected to analog loopback circuit from DAC output. Output MUX and AMP are powered-down when PDN = "L" or PM2 = PM3 = "0".

The loopback output and the MUX selecting DAC output is a MIXER with the switch in practice. Therefore, when both PM2 and PM3 select ON, the analog loopback signal and DAC output are mixed by Gain 1.

The AK4565 can be partially powered-down by ON/OFF ("1"/"0") of PM3-0 bits. When PDN pin goes "L", all the circuit in AK4565 can be powered-down regardless of PM3-0 bits.

When the AK4565 is powered-down by PM3-0 bits, contents of registers are kept. However IPGA gain is reset when PM0 bit is "0". (refer to "Operation of IPGA" description)

VCOM circuit is powered-down when PM bit is all "0".

MCLK, BCLK and LRCK should not stopped except the case of PM0 = PM1 = PM2 = PM3 = "0" or PDN = "L".

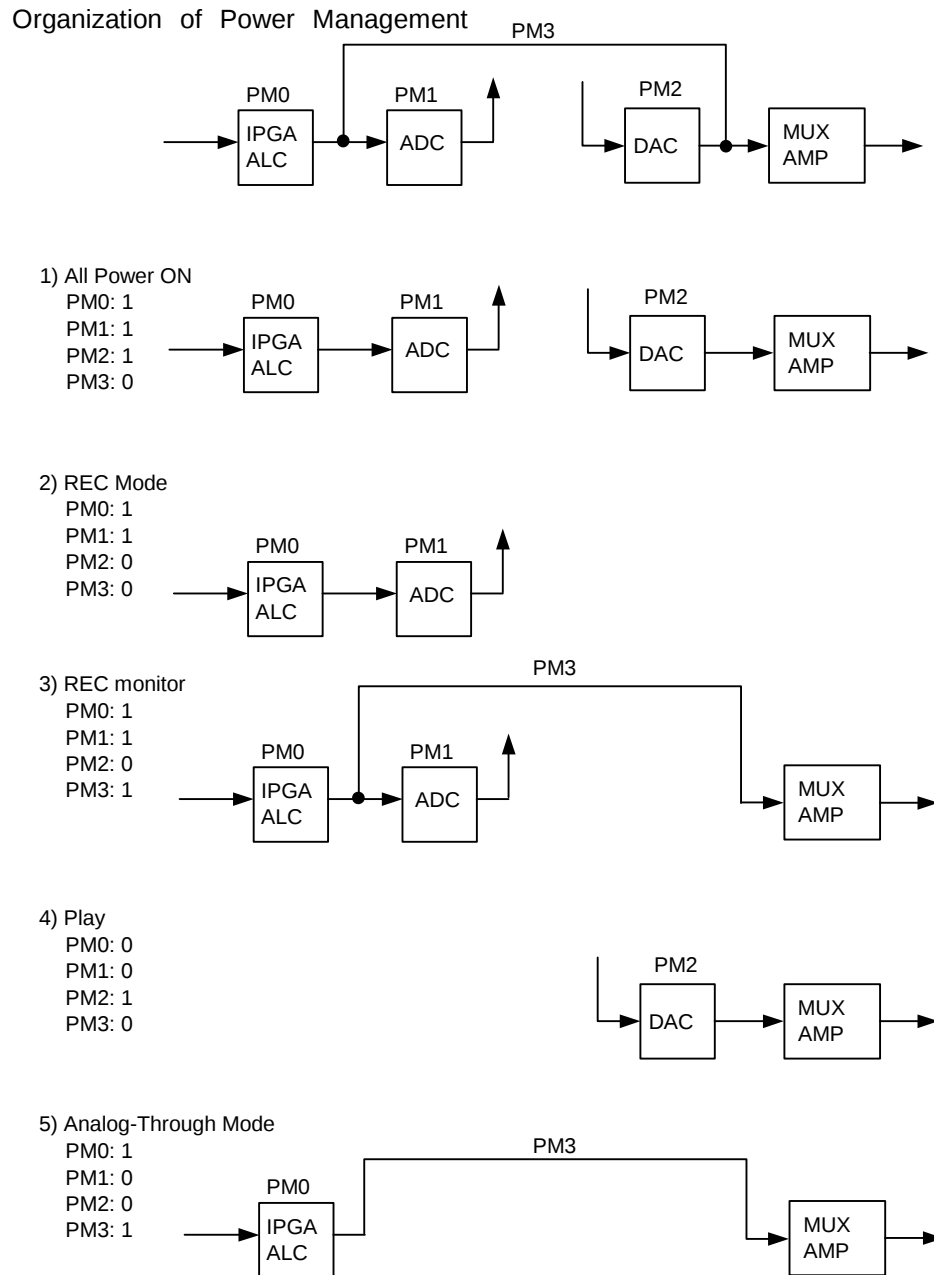


Figure 17. Power Management

| Addr    | Register Name | D7  | D6 | D5    | D4 | D3   | D2   | D1   | D0   |
|---------|---------------|-----|----|-------|----|------|------|------|------|
| 02H     | Mode Control  | 0   | 0  | DMUTE | FS | DIF1 | DIF0 | DEM1 | DEM0 |
| R/W     |               | R/W |    |       |    |      |      |      |      |
| Default |               | 0   | 0  | 0     | 1  | 0    | 0    | 0    | 1    |

#### DEM1-0: Select De-emphasis frequency

The AK4565 includes the digital de-emphasis filter ( $t_c = 50/15\mu s$ ) by IIR filter. The filter corresponds to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter selected by DEM0 and DEM1 bits are enabled for input audio data.

| DEM1 | DEM0 | Mode    |
|------|------|---------|
| 0    | 0    | 44.1kHz |
| 0    | 1    | OFF     |
| 1    | 0    | 48kHz   |
| 1    | 1    | 32kHz   |

Default

Table 2. Select De-emphasis frequency

#### DIF1-0: Select Audio Serial Interface Format

| No. | DIF1 bit | DIF0 bit | SDTO0/SDTO1(ADC)                  | SDTI (DAC)                        | BCLK        | Figure    |
|-----|----------|----------|-----------------------------------|-----------------------------------|-------------|-----------|
| 0   | 0        | 0        | 20bit MSB justified               | 16bit LSB justified               | $\geq 32fs$ | Figure 9  |
| 1   | 0        | 1        | 20bit MSB justified               | 20bit LSB justified               | $\geq 40fs$ | Figure 10 |
| 2   | 1        | 0        | 20bit MSB justified               | 20bit MSB justified               | $\geq 40fs$ | Figure 11 |
| 3   | 1        | 1        | 16bit I <sup>2</sup> S compatible | 16bit I <sup>2</sup> S compatible | = 32fs      | Figure 12 |
|     | 1        | 1        | 20bit I <sup>2</sup> S compatible | 20bit I <sup>2</sup> S compatible | $\geq 40fs$ | Figure 12 |

Default

Table 3. Select Audio Serial Interface Format

#### FS: Select Sampling Frequency

0:fs=32kHz

1:fs=48kHz (Default)

FS bit can set limiter period (LTM1-0 bit), recovery period (WTM1-0 bit), zero crossing timeout (ZTM1-0 bit) and FADEIN/FADEOUT period (FDTM1-0 bit) the same period at fs=32kHz and 48kHz.

#### DMUTE: Control of SDTO1 output data

0: SDTO1 output data is enabled.

1: SDTO1 output data is muted. (Default)

| Addr    | Register Name | D7    | D6    | D5   | D4   | D3   | D2   | D1   | D0   |
|---------|---------------|-------|-------|------|------|------|------|------|------|
| 03H     | Timer Select  | FDTM1 | FDTM0 | ZTM1 | ZTM0 | WTM1 | WTM0 | LTM1 | LTM0 |
| R/W     |               | R/W   |       |      |      |      |      |      |      |
| Default |               | 0     | 0     | 0    | 0    | 0    | 0    | 0    | 1    |

#### LTM1-0: ALC Limiter Period at ZELMN = "1"

The IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period specified by LTM1-0 bit.

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

| LTM1 | LTM0 | Period | Default |
|------|------|--------|---------|
| 0    | 0    | 63μs   |         |
| 0    | 1    | 125μs  |         |
| 1    | 0    | 250μs  |         |
| 1    | 1    | 500μs  |         |

Table 4. ALC Limiter Operation Period

#### WTM1-0: ALC Recovery Waiting Period

A period of recovery operation when any limiter operation does not occur during ALC operation.

Recovery operation is done at period set by WTM1-0 bits.

When the input signal level exceeds auto recovery waiting counter reset level set by LMTH bit, the auto recovery waiting counter is reset.

The waiting timer starts when the input signal level becomes below the auto recovery waiting counter reset level.

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

| WTM1 | WTM0 | Period | Default |
|------|------|--------|---------|
| 0    | 0    | 8ms    |         |
| 0    | 1    | 16ms   |         |
| 1    | 0    | 64ms   |         |
| 1    | 1    | 512ms  |         |

Table 5. ALC Recovery Operation Waiting Period

#### ZTM1-0: Zero crossing timeout at writing operation by μP, the ALC recovery operation and the ALC limiter operation at ZELMN = "0"

When IPGA of each L/R channels do zero crossing or timeout independently, the IPGA value is changed by μP WRITE operation, the ALC recovery operation or the ALC limiter operation at ZELMN = "0".

These periods are value at fs=32kHz (FS bit = "0") or fs=48kHz (FS bit = "1").

| ZTM1 | ZTM0 | Period | Default |
|------|------|--------|---------|
| 0    | 0    | 8ms    |         |
| 0    | 1    | 16ms   |         |
| 1    | 0    | 64ms   |         |
| 1    | 1    | 512ms  |         |

Table 6. Zero Crossing Timeout

**FDTM1-0: FADEIN/OUT Period Setting**

The FADEIN/OUT operation is done by a period set by FDTM1-0 bits when FDIN or FDOUT bits are set “1”. When IPGA of each L/R channel do zero crossing or timeout independently, the IPGA value is changed.

These period are value at fs=32kHz (FS bit = “0”) or fs=48kHz (FS bit = “1”).

| FDTM1 | FDTM0 | Period | Default |
|-------|-------|--------|---------|
| 0     | 0     | 24ms   |         |
| 0     | 1     | 32ms   |         |
| 1     | 0     | 48ms   |         |
| 1     | 1     | 64ms   |         |

Table 7. FADEIN/OUT Period

| Addr    | Register Name      | D7  | D6 | D5    | D4    | D3    | D2    | D1    | D0   |
|---------|--------------------|-----|----|-------|-------|-------|-------|-------|------|
| 04H     | ALC Mode Control 1 | 0   | 0  | LMAT1 | LMAT0 | FDATT | RATT1 | RATT0 | LMTH |
| R/W     |                    | R/W |    |       |       |       |       |       |      |
| Default |                    | 0   | 0  | 0     | 0     | 0     | 0     | 0     | 0    |

LMTH: Auto Limiter Detection Level / Auto Recovery Waiting Counter Reset Level

| LMTH | ALC Limiter Detection Level    | ALC Recovery Waiting Counter Reset Level              | Default |
|------|--------------------------------|-------------------------------------------------------|---------|
| 0    | ADC Input $\geq -4.0\text{dB}$ | $-4.0\text{dB} > \text{ADC Input} \geq -6.0\text{dB}$ |         |
| 1    | ADC Input $\geq -2.0\text{dB}$ | $-2.0\text{dB} > \text{ADC Input} \geq -4.0\text{dB}$ |         |

Table 8. Auto Limiter Detection Level / Auto Recovery Waiting Counter Reset Level

RATT1-0: ALC Recovery GAIN Step

During the ALC recovery operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is 30H, RATT1= “0” and RATT0= “1” are set, IPGA changes to 32H by the auto limiter operation, the input signal level is gained by 1dB (=0.5dB x 2).

When the IPGA value exceeds the reference level (REF6-0), the IPGA value does not increase.

| RATT1 | RATT0 | GAIN Step | Default |
|-------|-------|-----------|---------|
| 0     | 0     | 1         |         |
| 0     | 1     | 2         |         |
| 1     | 0     | 3         |         |
| 1     | 1     | 4         |         |

Table 9. ALC Recovery GAIN Step

FDATT: FADEIN/OUT ATT Step

During the FADEIN/OUT operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is 30H, FDATT = “1” are set, IPGA changes to 32H (FADEIN) or 2EH (FADEOUT) by the FADEIN/OUT operation, the input signal level is gained by 1dB(=0.5dB x 2). When the IPGA value exceeds the reference level (REF6-0) or 00H, the IPGA value does not increase.

| FDATT | ATT Step | Default |
|-------|----------|---------|
| 0     | 1        |         |
| 1     | 2        |         |

Table 10. FADEIN/OUT ATT Step

LMAT1-0: ALC Limiter ATT Step

During the ALC limiter operation, when input signal exceeds the ALC limiter detection level set by LMTH, the number of steps attenuated from current IPGA value is set. For example, when the current IPGA value is 60H in the state of LMAT1-0 = “11”, it becomes IPGA=5CH by the ALC limiter operation, the input signal level is attenuated by 2dB (=0.5dB x 4).

The ALC limiter period is set by LTM1-0 bits at ZELMN = “1” and ZTM1-0 bits at ZELMN = “0”.

When the attenuation value exceeds IPGA = “00H” (MUTE), it clips to “00”.

| LMAT1 | LMAT0 | ATT Step | Default |
|-------|-------|----------|---------|
| 0     | 0     | 1        |         |
| 0     | 1     | 2        |         |
| 1     | 0     | 3        |         |
| 1     | 1     | 4        |         |

Table 11. ALC Limiter ATT Step

| Addr    | Register Name      | D7  | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
|---------|--------------------|-----|------|------|------|------|------|------|------|
| 05H     | ALC Mode Control 2 | 0   | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| R/W     |                    | R/W |      |      |      |      |      |      |      |
| Default |                    | 0   | 28H  |      |      |      |      |      |      |

**REF6-0: Set the Reference value at ALC Recovery Operation**

During the ALC recovery operation, when IPGA value becomes the reference value set by REF6-0, the gain of the ALC recovery operation exceeds the reference value. The reference value is set commonly as for Lch and Rch of IPGA.

During the ALC recovery operation, if IPGA value exceeds the setting reference value by GAIN operation, IPGA does not become the larger than the reference value.

For example, when REF6-0 = 30H, RATT = 2 step and IPGA = 2FH, IPGA will become 2FH + 2 step = 31H by the ALC recovery operation, but IPGA value becomes 30H as REF value is 30H.

IPGA should be certainly set to the same value or smaller than REF value before entering ALC mode (including the FADEIN/OUT operation).

| DATA | GAIN(dB) |       | Step  | Level |
|------|----------|-------|-------|-------|
|      | MIC      | LINE  |       |       |
| 60H  | +28.0    | +6.0  | 0.5dB | 73    |
| 5FH  | +27.5    | +5.5  |       |       |
| 5EH  | +27.0    | +5.0  |       |       |
| •    | •        | •     |       |       |
| 28H  | +0.0     | -22.0 |       |       |
| 27H  | -0.5     | -22.5 |       |       |
| •    | •        | •     |       |       |
| 19H  | -7.5     | -29.5 |       |       |
| 18H  | -8.0     | -30.0 | 1dB   | 8     |
| 17H  | -9.0     | -31.0 |       |       |
| 16H  | -10.0    | -32.0 |       |       |
| •    | •        | •     |       |       |
| 11H  | -15.0    | -37.0 |       |       |
| 10H  | -16.0    | -38.0 | 2dB   | 12    |
| 0FH  | -18.0    | -40.0 |       |       |
| 0EH  | -20.0    | -42.0 |       |       |
| •    | •        | •     |       |       |
| 05H  | -38.0    | -60.0 |       |       |
| 04H  | -40.0    | -62.0 | 4dB   | 3     |
| 03H  | -44.0    | -66.0 |       |       |
| 02H  | -48.0    | -70.0 |       |       |
| 01H  | -52.0    | -74.0 |       |       |
| 00H  | MUTE     | MUTE  |       | 1     |

Table 12. Setting Reference Value at ALC Recovery Operation

| Addr    | Register Name  | D7  | D6 | D5        | D4 | D3   | D2   | D1    | D0  |
|---------|----------------|-----|----|-----------|----|------|------|-------|-----|
| 06H     | Operation Mode | 0   | 0  | ZELM<br>N | FR | STAT | FDIN | FDOUT | ALC |
| R/W     |                | R/W |    |           |    | RD   | R/W  |       |     |
| Default |                | 0   | 0  | 0         | 0  | 0    | 0    | 0     | 0   |

ALC: ALC Enable Flag

0: ALC Disable (Default)

1: ALC Enable

FDOUT: FADEOUT Enable Flag

0: FADEOUT Disable (Default)

1: FADEOUT Enable

FDIN: FADEIN Enable Flag

0: FADEIN Disable (Default)

1: FADEIN Enable

STAT: Status Flag

0: ALC (including FADEIN and FADEOUT) operation or initializing operation (Default)

1: Manual Mode

STAT bit is “0” during initializing operation after exiting power-down by PDN pin. After the finish of the initializing operation, STAT bit becomes “1”.

During the ALC operation, STAT bit becomes “1” after the max “1” ATT/GAIN operation is completed by internal state.

FR: Select ALC operation Mode

0: The ALC operation corresponds to impulse noise. (Default)

1: Normal operation

ZELMN: Enable zero crossing detection at ALC Limiter operation

0: Enable (Default)

1: Disable

In case of ZELMN = “0”, IPGA of each L/R channel do zero crossing or timeout independently, the IPGA value is changed by the ALC operation. Zero crossing timeout is the same as the ALC recovery operation. In case of ZELMN = “1”, the IPGA value is changed immediately.

| Addr    | Register Name     | D7  | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|---------|-------------------|-----|-------|-------|-------|-------|-------|-------|-------|
| 07H     | Input PGA Control | 0   | IPGA6 | IPGA5 | IPGA4 | IPGA3 | IPGA2 | IPGA1 | IPGA0 |
| R/W     |                   | R/W |       |       |       |       |       |       |       |
| Default |                   | 0   | 28H   |       |       |       |       |       |       |

IPGA6-0: Input Analog PGA; 97 levels; Commonly Lch and Rch of IPGA.

The IPGA value should be the same or smaller than REF value before the ALC operation including the FADEIN/FADEOUT operation.

When IPGA gain is changed, IPGA6-0 bits should be written while PM0 bit is “1” and ALC bit is “0”.  
(refer to “Operation of IPGA” description)

| DATA | GAIN(dB) |       | Step  | Level |
|------|----------|-------|-------|-------|
|      | MIC      | LINE  |       |       |
| 60H  | +28.0    | +6.0  | 0.5dB | 73    |
| 5FH  | +27.5    | +5.5  |       |       |
| 5EH  | +27.0    | +5.0  |       |       |
| •    | •        | •     |       |       |
| 28H  | +0.0     | -22.0 |       |       |
| 27H  | -0.5     | -22.5 |       |       |
| •    | •        | •     |       |       |
| 19H  | -7.5     | -29.5 |       |       |
| 18H  | -8.0     | -30.0 | 1dB   | 8     |
| 17H  | -9.0     | -31.0 |       |       |
| 16H  | -10.0    | -32.0 |       |       |
| •    | •        | •     |       |       |
| 11H  | -15.0    | -37.0 |       |       |
| 10H  | -16.0    | -38.0 | 2dB   | 12    |
| 0FH  | -18.0    | -40.0 |       |       |
| 0EH  | -20.0    | -42.0 |       |       |
| •    | •        | •     |       |       |
| 05H  | -38.0    | -60.0 |       |       |
| 04H  | -40.0    | -62.0 | 4dB   | 3     |
| 03H  | -44.0    | -66.0 |       |       |
| 02H  | -48.0    | -70.0 |       |       |
| 01H  | -52.0    | -74.0 |       | 1     |
| 00H  | MUTE     | MUTE  |       |       |

Table 13. Input Gain Setting

**IPGA value is reset at PM0 = “0”.**

## SYSTEM DESIGN

Figure 18 shows the system connection diagram. An evaluation board (AKD4565) is available which demonstrates the application circuit, the optimum layout, power supply arrangements and measurement results.

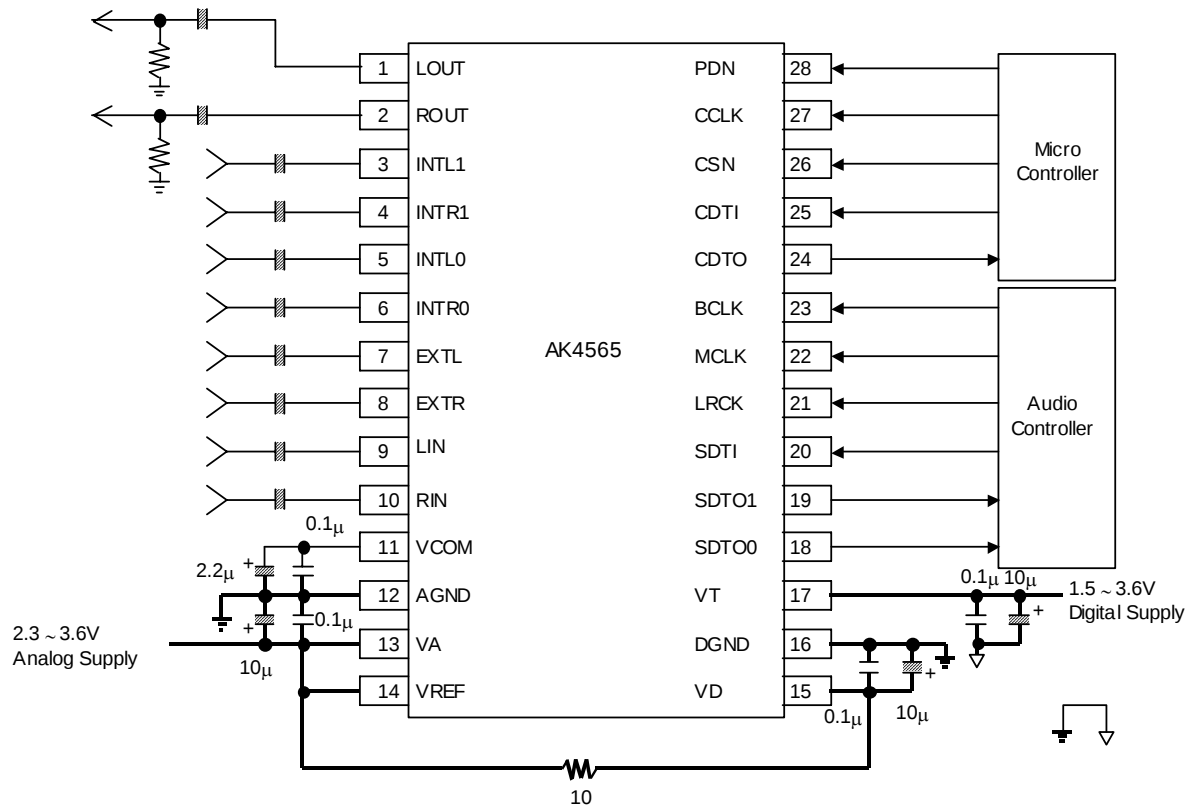


Figure 18. System Connection Diagram

**Note:**

- AGND and DGND of AK4565 should be distributed separately from the ground of external controller etc.
- When LOUT/ROUT drives some capacitive load, some resistor should be added in series between LOUT/ROUT and capacitive load.

## 1. Grounding and Power Supply Decoupling

The AK4565 requires careful attention to power supply and grounding arrangements. VA is usually supplied from analog supply in system and VD is supplied from analog supply in system via a resistor of 10 ohms. Alternatively if VA and VD are supplied separately, the power up sequence is not taken care. VT is a power supply pin to interface with the external ICs and is supplied from digital supply in the system. AGND and DGND of the AK4565 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4565 as possible, with the small value ceramic capacitor being the nearest.

## 2. Voltage Reference

The differential voltage between VREF and AGND sets the analog input/output range. VREF pin is normally connected to VA with a 0.1 $\mu$ F ceramic capacitor. VCOM is output to 0.45 x VA(typ.) and is a signal ground of this chip. An electrolytic capacitor 2.2 $\mu$ F parallel with a 0.1 $\mu$ F ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4565.

## 3. Analog Inputs

The analog inputs are single-ended and the input resistance is 10k $\Omega$  (typ) at MIC gain table and 125k $\Omega$  (typ) at LINE gain table. The input signal range scales with the VREF voltage and nominally 0.6 x VREF Vpp centered in the internal common voltage. Usually the input signal cuts DC with a capacitor. The cut-off frequency is  $f_c = (1/2\pi RC)$ . The AK4565 can accept input voltages to (VA-0.1) Vpp. The ADC output data format is 2's complement. The DC offset including ADC's own DC offset is removed by the internal HPF ( $f_c=3.7\text{Hz}@f_s=48\text{kHz}$ ).

The AK4565 samples the analog inputs at 64fs. The digital filter rejects noise above the stopband except for multiples of 64fs. The AK4565 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

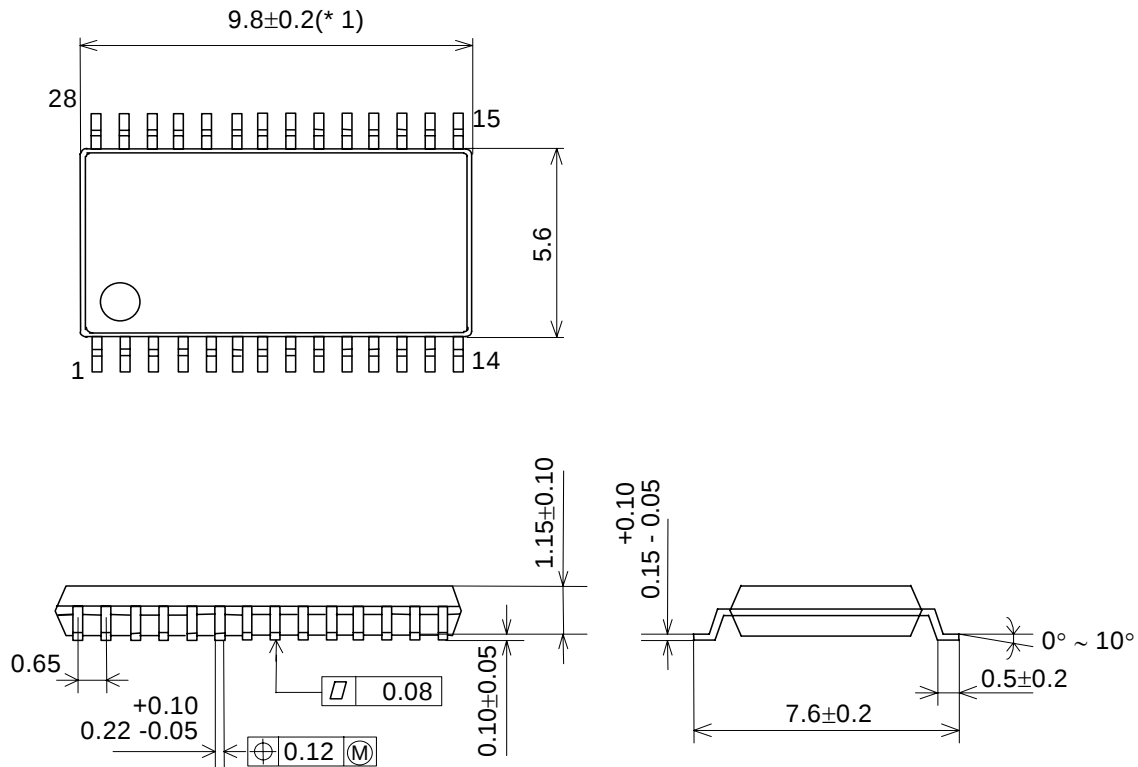
## 4. Analog Outputs

The analog outputs are single-ended and nominally 0.6 x VREF Vpp centered in the internal common voltage. The input data format is 2's complement. If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external circuit is required.

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of a few mV + VCOM voltage.

|         |
|---------|
| PACKAGE |
|---------|

28pin VSOP (Unit: mm)

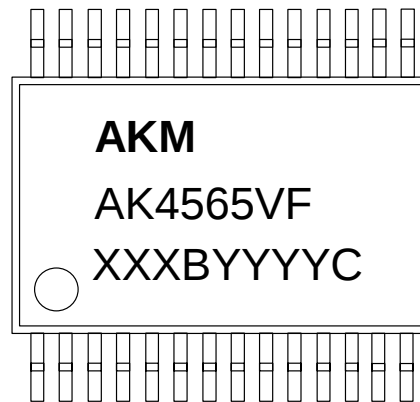


\*1: Dimension does not include mold flash.

#### ■ Material & Lead finish

|                               |                        |
|-------------------------------|------------------------|
| Package molding compound:     | Epoxy                  |
| Lead frame material:          | Cu                     |
| Lead frame surface treatment: | Solder (Pb free) plate |

|                |
|----------------|
| <b>MARKING</b> |
|----------------|



XXXBYYYYC     Date code identifier

XXXB : Lot number (X : Digit number, B : Alpha character)

YYYYC : Assembly date (Y : Digit number, C Alpha character)

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