

MC14532B

8-Bit Priority Encoder

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in} , V_{out}	-0.5 to $V_{DD} + 0.5$	V
Input or Output Current (DC or Transient) per Pin	I_{in} , I_{out}	± 10	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (8 Sec Soldering)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

TRUTH TABLE

Input									Output				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	0	1	0
1	0	0	0	0	0	0	1	X	1	0	0	0	1
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

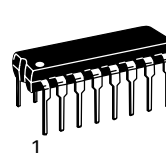
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



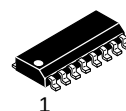
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MARKING DIAGRAMS



PDIP-16
P SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week
G = Pb-Free Package

PIN ASSIGNMENT

D4	1	16	V_{DD}
D5	2	15	E_{out}
D6	3	14	GS
D7	4	13	D3
E_{in}	5	12	D2
Q2	6	11	D1
Q1	7	10	D0
V_{SS}	8	9	Q0

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14532B

ORDERING INFORMATION

Device	Package	Shipping [†]
MC14532BCP	PDIP-16	25 Units / Rail
MC14532BCPG	PDIP-16 (Pb-Free)	
MC14532BD	SOIC-16	48 Units / Rail
MC14532BDG	SOIC-16 (Pb-Free)	
MC14532BDR2	SOIC-16	2500 / Tape & Reel
MC14532BDR2G	SOIC-16 (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
	V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
	V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I _{in}	15	–	± 0.1	–	± 0.00001	± 0.1	–	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I _{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (1.74 μA/kHz) f + I _{DD} I _T = (3.65 μA/kHz) f + I _{DD} I _T = (5.73 μA/kHz) f + I _{DD}							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

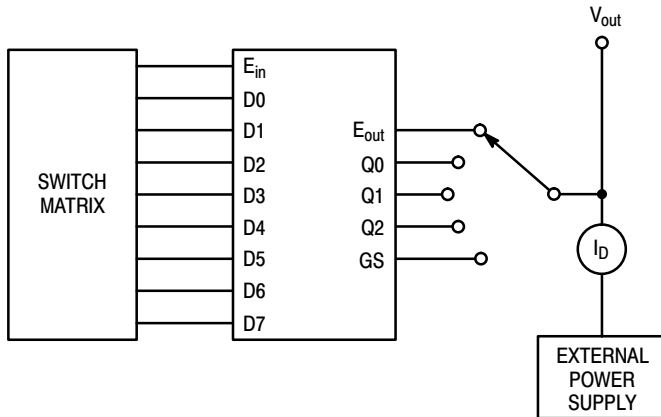
MC14532B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) (Note 5)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — E_{in} to E_{out} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 120 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	205 110 80	410 220 160	ns
Propagation Delay Time — E_{in} to GS $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	175 90 65	350 180 130	ns
Propagation Delay Time — E_{in} to Q_n $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PHL},$ t_{PLH}	5.0 10 15	— — —	280 140 100	560 280 200	ns
Propagation Delay Time — D_n to Q_n $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	300 170 110	600 340 220	ns
Propagation Delay Time — D_n to GS $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	— — —	280 140 100	560 280 200	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Output Under Test	$V_{GS} = V_{DD}$ $V_{DS} = V_{out}$ Sink Current		$V_{GS} = -V_{DD}$ $V_{DS} = V_{out} - V_{DD}$ Source Current		
	D0 thru D7	E_{in}	D0 thru D6	D7	E_{in}
E_{out}	X	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

Figure 1. Typical Sink and Source Current Characteristics

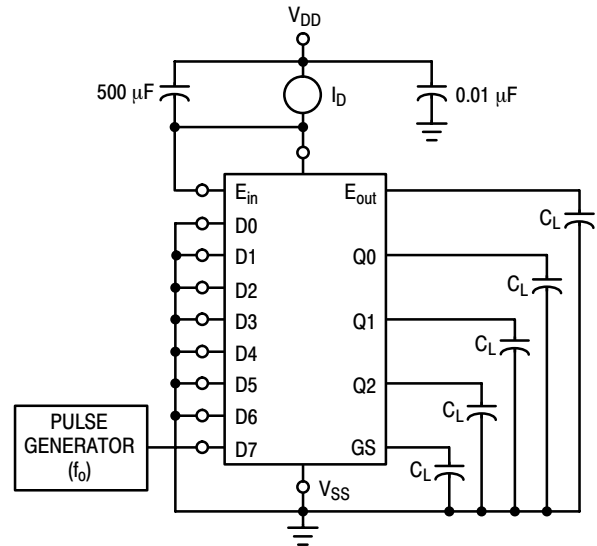


Figure 2. Typical Power Dissipation Test Circuit

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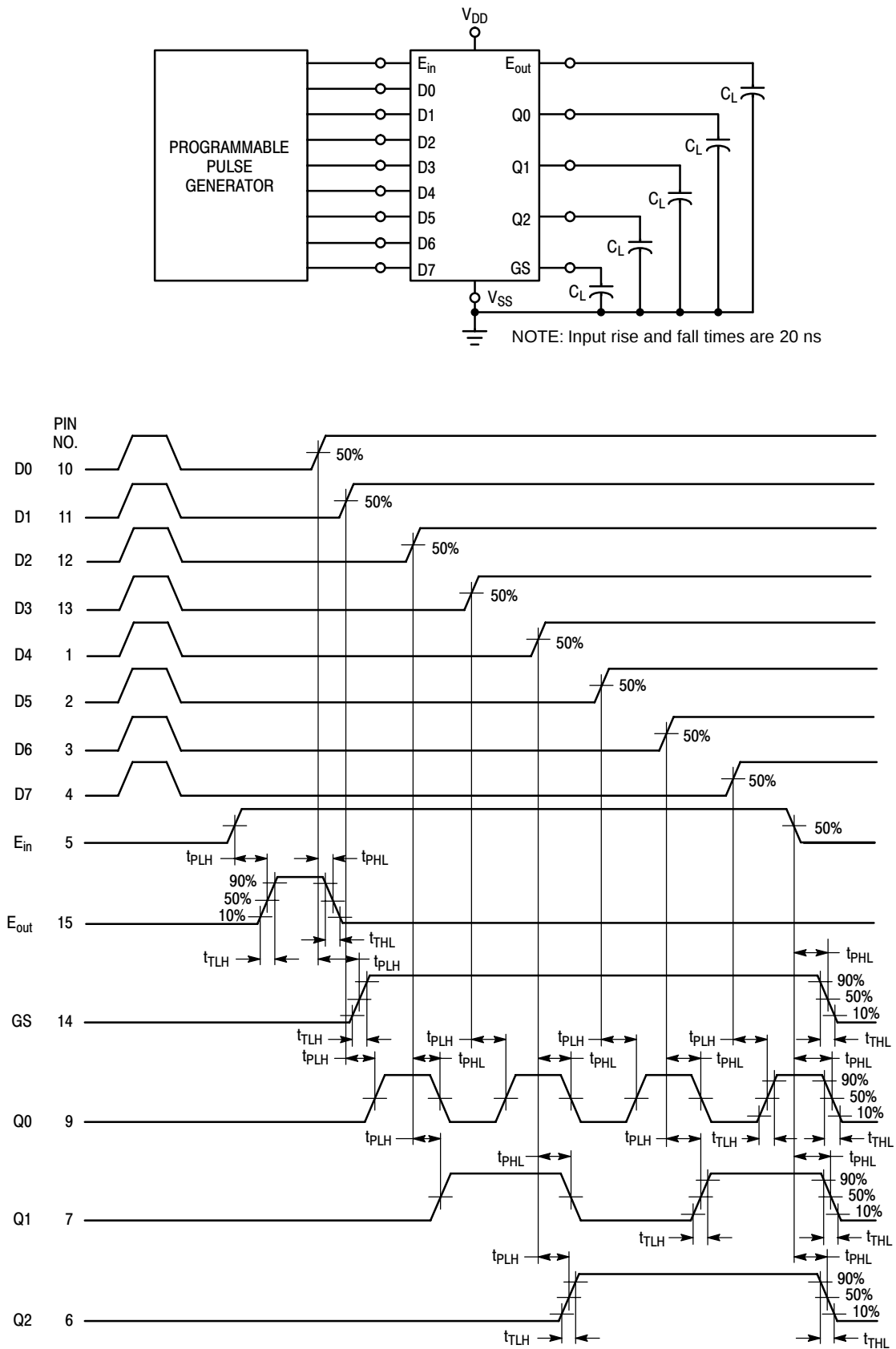


Figure 3. AC Test Circuit and Waveforms

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LOGIC EQUATIONS

$$E_{out} = E_{in} \cdot \bar{D}0 \cdot \bar{D}1 \cdot \bar{D}2 \cdot \bar{D}3 \cdot \bar{D}4 \cdot \bar{D}5 \cdot \bar{D}6 \cdot \bar{D}7$$

$$Q0 = E_{in} \cdot (D1 \cdot \bar{D}2 \cdot \bar{D}4 \cdot \bar{D}6 + D3 \cdot \bar{D}4 \cdot \bar{D}6 + D5 \cdot \bar{D}6 + D7)$$

$$Q1 = E_{in} \cdot (D2 \cdot \bar{D}4 \cdot \bar{D}5 + D3 \cdot \bar{D}4 \cdot \bar{D}5 + D6 + D7)$$

$$Q2 = E_{in} \cdot (D4 + D5 + D6 + D7)$$

$$GS = E_{in} \cdot (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$$

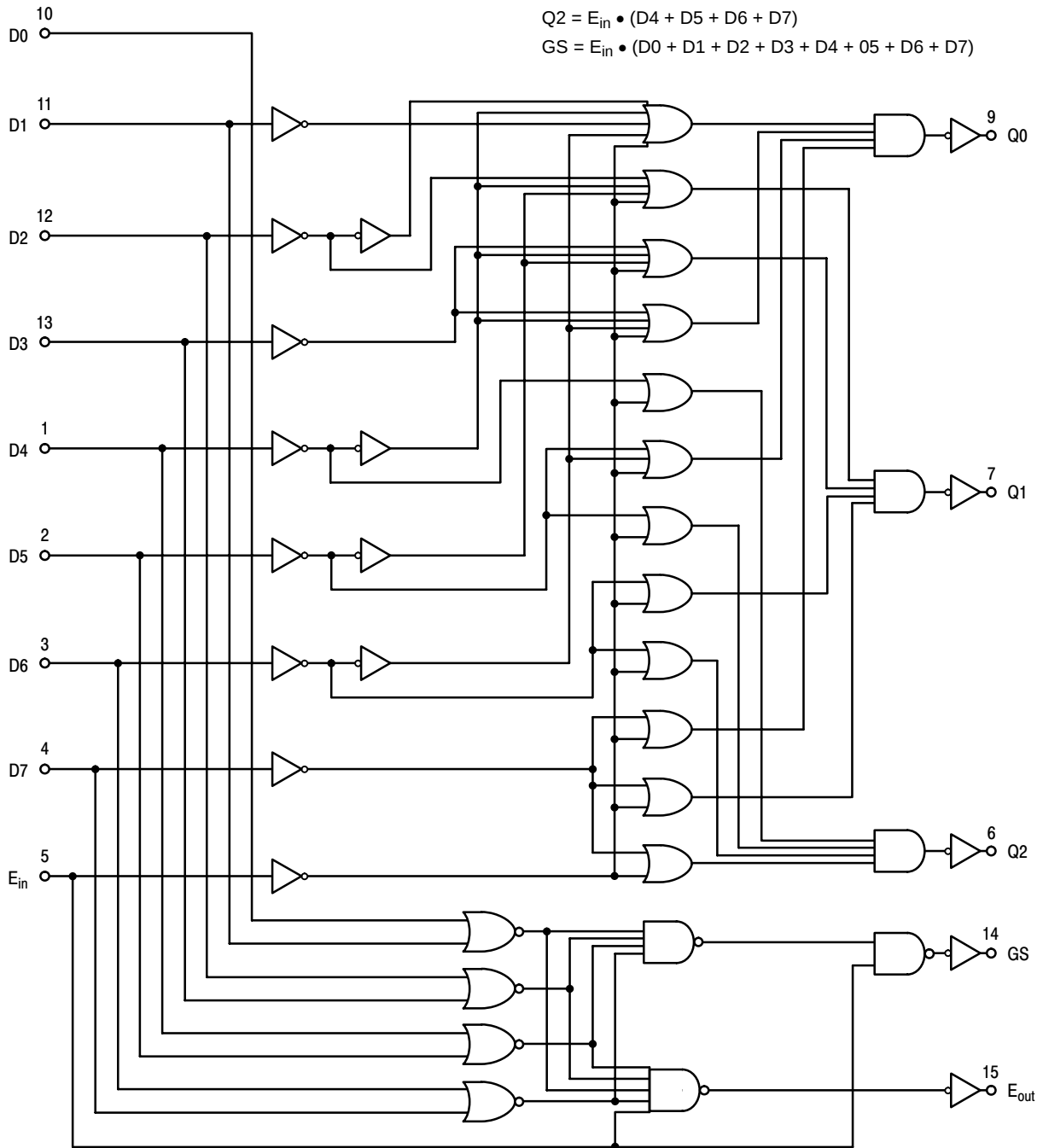


Figure 4. Logic Diagram
(Positive Logic)

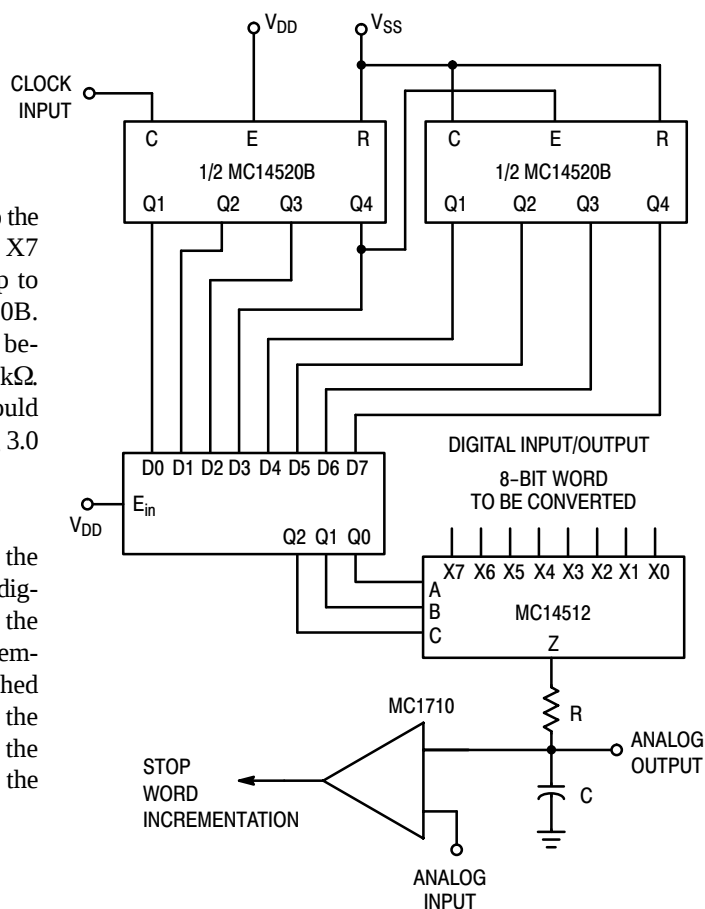
The diagram illustrates a 16-bit parallel adder circuit. It consists of two 8-bit 74181 ALUs and three 74148 BCD-to-7-segment decoders.

- 74181 ALU 1 (Left):** Its E_{in} is connected to V_{DD} . Its E_{out} is connected to the E_{in} of the second 74181 ALU. Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the first 74148 decoder.
- 74181 ALU 2 (Right):** Its E_{in} is connected to the E_{out} of the first 74181 ALU. Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the second 74148 decoder.
- 74148 Decoders:** Each decoder has a Q_3 output. The Q_3 output of the first decoder is connected to the Q_3 output of the second decoder. The Q_3 output of the second decoder is connected to the Q_3 output of the third decoder.
- 74148 Decoder 1:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the second 74148 decoder.
- 74148 Decoder 2:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the third 74148 decoder.
- 74148 Decoder 3:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the fourth 74148 decoder.
- 74148 Decoder 4:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the fifth 74148 decoder.
- 74148 Decoder 5:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the sixth 74148 decoder.
- 74148 Decoder 6:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the seventh 74148 decoder.
- 74148 Decoder 7:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the eighth 74148 decoder.
- 74148 Decoder 8:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the ninth 74148 decoder.
- 74148 Decoder 9:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the tenth 74148 decoder.
- 74148 Decoder 10:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the eleventh 74148 decoder.
- 74148 Decoder 11:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twelfth 74148 decoder.
- 74148 Decoder 12:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirteenth 74148 decoder.
- 74148 Decoder 13:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the fourteenth 74148 decoder.
- 74148 Decoder 14:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the fifteenth 74148 decoder.
- 74148 Decoder 15:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the sixteenth 74148 decoder.
- 74148 Decoder 16:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the seventeenth 74148 decoder.
- 74148 Decoder 17:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the eighteenth 74148 decoder.
- 74148 Decoder 18:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the nineteenth 74148 decoder.
- 74148 Decoder 19:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twentieth 74148 decoder.
- 74148 Decoder 20:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-first 74148 decoder.
- 74148 Decoder 21:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-second 74148 decoder.
- 74148 Decoder 22:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-third 74148 decoder.
- 74148 Decoder 23:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-fourth 74148 decoder.
- 74148 Decoder 24:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-fifth 74148 decoder.
- 74148 Decoder 25:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-sixth 74148 decoder.
- 74148 Decoder 26:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-seventh 74148 decoder.
- 74148 Decoder 27:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-eighth 74148 decoder.
- 74148 Decoder 28:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the twenty-ninth 74148 decoder.
- 74148 Decoder 29:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirtieth 74148 decoder.
- 74148 Decoder 30:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-first 74148 decoder.
- 74148 Decoder 31:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-second 74148 decoder.
- 74148 Decoder 32:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-third 74148 decoder.
- 74148 Decoder 33:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-fourth 74148 decoder.
- 74148 Decoder 34:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-fifth 74148 decoder.
- 74148 Decoder 35:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-sixth 74148 decoder.
- 74148 Decoder 36:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-seventh 74148 decoder.
- 74148 Decoder 37:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-eighth 74148 decoder.
- 74148 Decoder 38:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the Q_2 , Q_1 , and Q_0 inputs of the thirty-ninth 74148 decoder.
- 74148 Decoder 39:** Its Q_2 , Q_1 , and Q_0 outputs are connected to the <

DIGITAL TO ANALOG CONVERSION

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

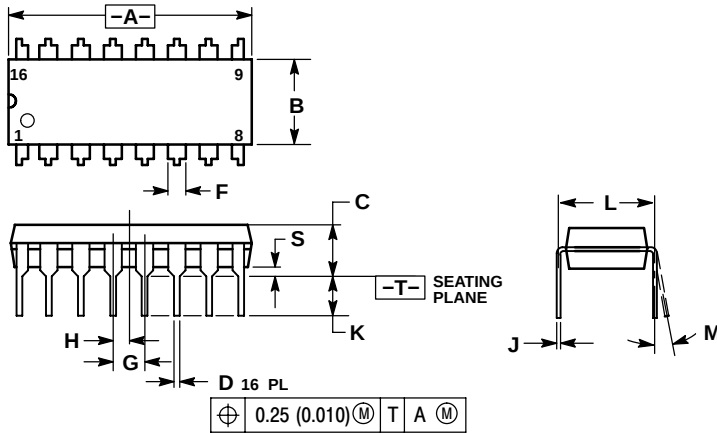


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MC14532B

PACKAGE DIMENSIONS

PDIP-16 CASE 648-08 ISSUE T

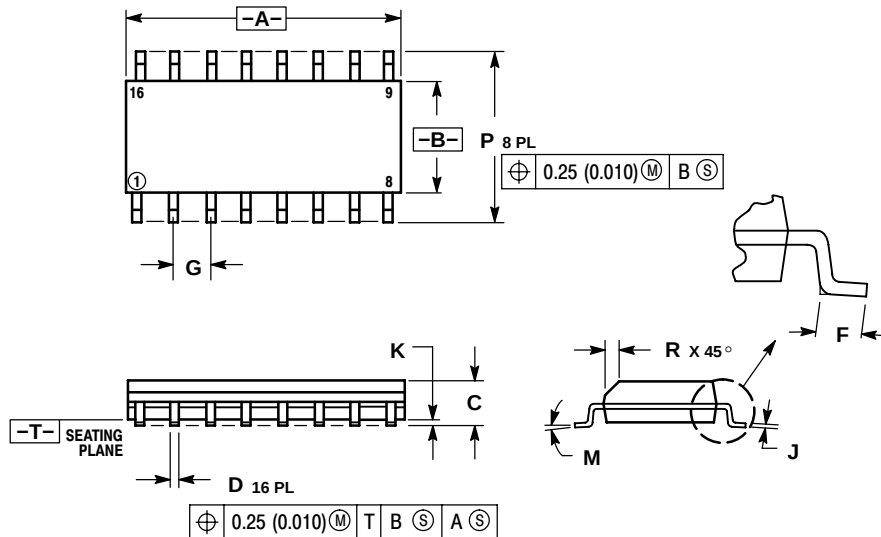


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16 CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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