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# **F<sup>2</sup>MC-16FX, CY96350 Series, 16-bit Proprietary Microcontroller**

CY96350 series is based on Cypress's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4 MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

## **Features**

- **Technology**
  - 0.18  $\mu$ m CMOS
- **CPU**
  - F<sup>2</sup>MC-16FX CPU
  - Up to 56 MHz internal, 17.8 ns instruction cycle time
  - Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
  - 8-byte instruction execution queue
  - Signed multiply (16-bit  $\times$  16-bit) and divide (32-bit/16-bit) instructions available
- **System clock**
  - On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)
  - 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).
  - Up to 56 MHz external clock
  - 32-100 kHz subsystem quartz clock
  - 100 kHz/2 MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
  - Clock source selectable from main- and subclock oscillator (part number suffix "W") and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.
  - Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)
  - Clock modulator
- **On-chip voltage regulator**
  - Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
- **Low voltage reset**
  - Reset is generated when supply voltage is below minimum.
- **Code Security**
  - Protects ROM content from unintended read-out
- **Memory Patch Function**
  - Replaces ROM content
  - Can also be used to implement embedded debug support
- **DMA**
  - Automatic transfer function independent of CPU, can be assigned freely to resources
- **Interrupts**
  - Fast Interrupt processing
  - 8 programmable priority levels
  - Non-Maskable Interrupt (NMI)
- **Timers**
  - Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
  - Watchdog Timer
- **CAN**
  - Supports CAN protocol version 2.0 part A and B
  - ISO16845 certified
  - Bit rates up to 1 Mbit/s
  - 32 message objects
  - Each message object has its own identifier mask
  - Programmable FIFO mode (concatenation of message objects)
  - Maskable interrupt
  - Disabled Automatic Retransmission mode for Time Triggered CAN applications
  - Programmable loop-back mode for self-test operation
- **USART**
  - Full duplex USARTs (SCI/LIN)
  - Wide range of baud rate settings using a dedicated reload timer
  - Special synchronous options for adapting to different synchronous serial protocols
  - LIN functionality working either as master or slave LIN device
- **I<sup>2</sup>C**
  - Up to 400 kbps
  - Master and Slave functionality, 7-bit and 10-bit addressing
- **A/D converter**
  - SAR-type
  - 10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

- **Reload Timers**
  - 16-bit wide
  - Prescaler with  $1/2^1$ ,  $1/2^2$ ,  $1/2^3$ ,  $1/2^4$ ,  $1/2^5$ ,  $1/2^6$  of peripheral clock frequency
  - Event count function
- **Free Running Timers**
  - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with  $1$ ,  $1/2^1$ ,  $1/2^2$ ,  $1/2^3$ ,  $1/2^4$ ,  $1/2^5$ ,  $1/2^6$ ,  $1/2^7$ ,  $1/2^8$  of peripheral clock frequency
- **Input Capture Units**
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, falling edge or rising & falling edge sensitive
- **Output Compare Units**
  - 16-bit wide
  - Signals an interrupt when a match with 16-bit I/O Timer occurs
  - A pair of compare registers can be used to generate an output signal.
- **Programmable Pulse Generator**
  - 16-bit down counter, cycle and duty setting registers
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows  $1$ ,  $1/4$ ,  $1/16$ ,  $1/64$  of peripheral clock as counter clock and Reload timer overflow as clock input
  - Can be triggered by software or reload timer
- **Real Time Clock**
  - Can be clocked either from sub oscillator (devices with part number suffix "W"), main oscillator or from the RC oscillator
  - Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1 s clock
- **External Interrupts**
  - Edge sensitive or level sensitive
  - Interrupt mask and pending bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- **Non Maskable Interrupt**
  - Disabled after reset
  - Once enabled, can not be disabled other than by reset.
  - Level high or level low sensitive
  - Pin shared with external interrupt 0.
- **External bus interface**
  - 8-bit or 16-bit bidirectional data
  - Up to 24-bit addresses
  - 6 chip select signals
  - Multiplexed address/data lines
  - Wait state request
  - External bus master possible
  - Timing programmable
- **I/O Ports**
  - Virtually all external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as I<sup>2</sup>C SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL
  - Bit-wise programmable pull-up resistor
  - Bit-wise programmable output driving strength for EMI optimization
- **Package**
  - 64-pin plastic LQFP
- **Flash Memory**
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the algorithm
  - Number of erase cycles: 10,000 times
  - Data retention time: 20 years
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erase

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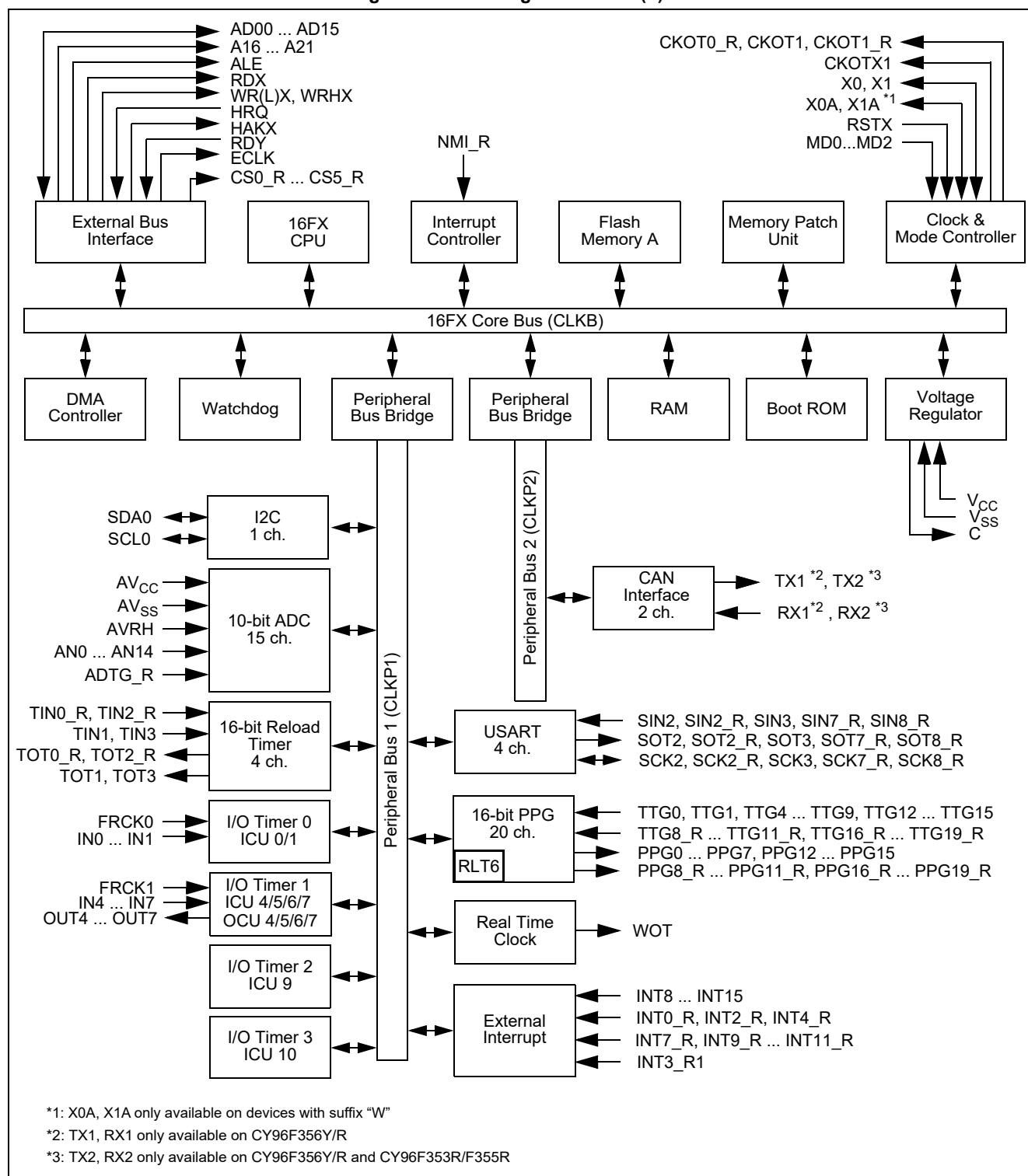
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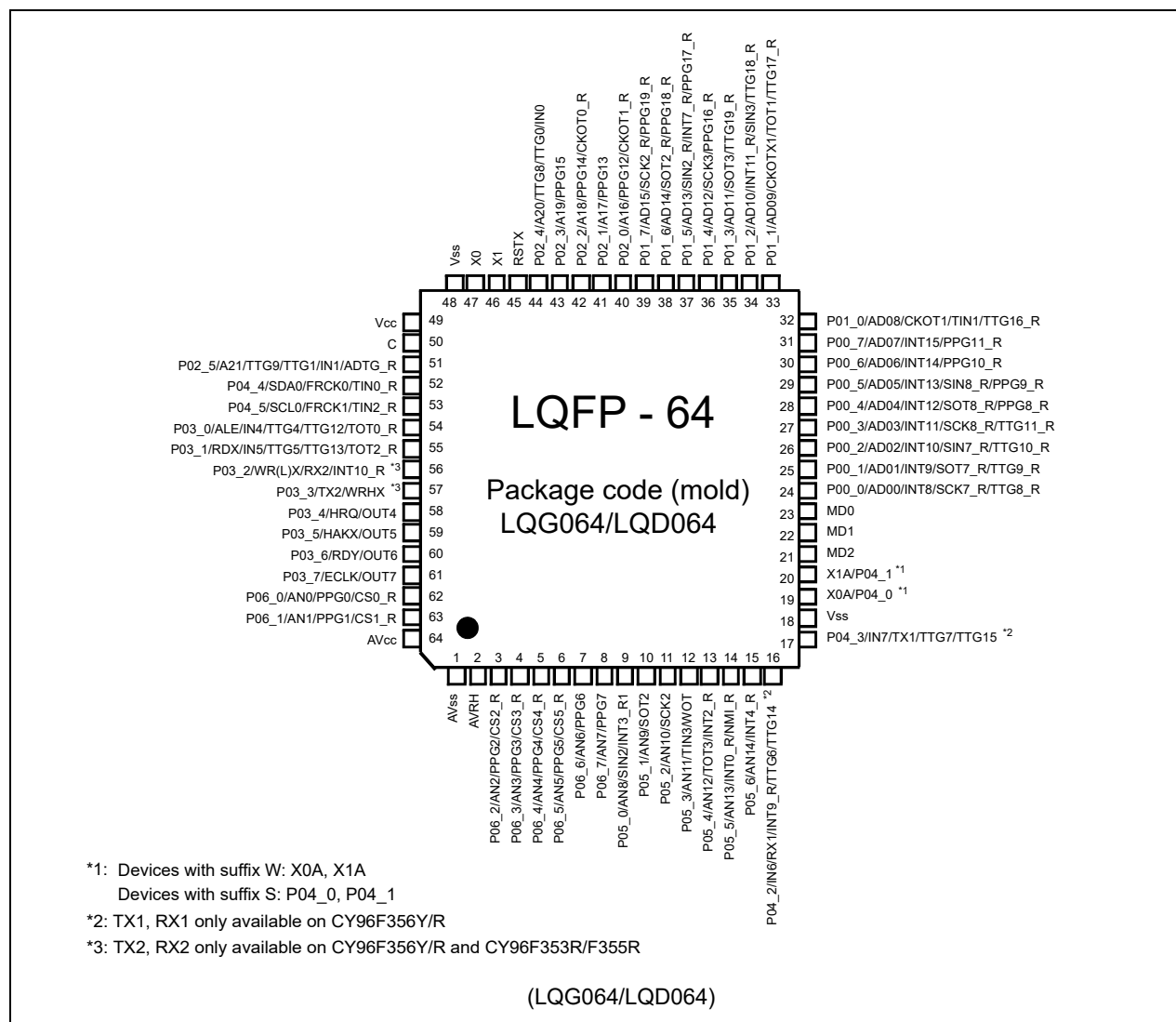
## Product Lineup

| Features                               |       | CY96V300C                                                      | CY96(F)35x                                                             |
|----------------------------------------|-------|----------------------------------------------------------------|------------------------------------------------------------------------|
| Product type                           |       | Evaluation sample                                              | Flash product: CY96F35x<br>Mask ROM product: CY9635x                   |
| Product options                        |       |                                                                |                                                                        |
| RS                                     |       | NA                                                             | Low voltage reset can be disabled / Single clock devices               |
| RW                                     |       |                                                                | Low voltage reset can be disabled / Dual clock devices                 |
| AS                                     |       |                                                                | No CAN / Low voltage reset can be disabled / Single clock devices      |
| AW                                     |       |                                                                | No CAN / Low voltage reset can be disabled / Dual clock devices        |
| Flash/ROM                              | RAM   |                                                                |                                                                        |
| 96 KB                                  | 8 KB  | ROM/Flash memory emulation by external RAM, 92 KB internal RAM | CY96F353RS/RW/AS/AW                                                    |
| 160 KB                                 | 8 KB  |                                                                | CY96F355RS/RW/AS/AW                                                    |
| 288 KB                                 | 12 KB |                                                                | CY96F356RS/RW/AS/AW                                                    |
| Package                                |       | BGA416                                                         | LQG064/LQD064                                                          |
| DMA                                    |       | 16 channels                                                    | 4 channels                                                             |
| USART                                  |       | 10 channels                                                    | 4 channels                                                             |
| I <sup>2</sup> C                       |       | 2 channels                                                     | 1 channel                                                              |
| A/D Converter                          |       | 40 channels                                                    | 15 channels                                                            |
| A/D Converter Reference Voltage switch |       | yes                                                            | No                                                                     |
| 16-bit Reload Timer                    |       | 6 channels + 1 channel (for PPG)                               | 4 channels + 1 channel (for PPG)                                       |
| 16-bit Free-Running Timer              |       | 4 channels                                                     | 4 channels (2 channels with external clock input pin)                  |
| 16-bit Output Compare                  |       | 12 channels                                                    | 4 channels                                                             |
| 16-bit Input Capture                   |       | 12 channels                                                    | 6 channels (plus 2 channels for LIN USART)                             |
| 16-bit Programmable Pulse Generator    |       | 20 channels                                                    | 20 channels                                                            |
| CAN Interface                          |       | 5 channels                                                     | CY96F35xA: no<br>CY96F353R/F355R: 1 channel<br>CY96F356R: 2 channels   |
| External Interrupts                    |       | 16 channels                                                    | 13 channels                                                            |
| Non-Maskable Interrupt                 |       | 1 channel                                                      |                                                                        |
| Real Time Clock                        |       | 1                                                              |                                                                        |
| I/O Ports                              |       | 136                                                            | 49 for part number with suffix "W", 51 for part number with suffix "S" |
| External bus interface                 |       | Yes                                                            |                                                                        |
| Chip select                            |       | 6 signals                                                      |                                                                        |
| Clock output function                  |       | 2 channels                                                     |                                                                        |
| Low voltage reset                      |       | Yes                                                            |                                                                        |
| On-chip RC-oscillator                  |       | Yes                                                            |                                                                        |

## Block Diagram

Figure 1. Block Diagram of CY96(F)35x





CY96(F)35x products are pin-compatible to F<sup>2</sup>MC-16LX family CY90350 series.

## Pin Function Description

**Table 1. Pin Function Description (1 / 2)**

| Pin Name         | Feature               | Description                                                                    |
|------------------|-----------------------|--------------------------------------------------------------------------------|
| ADn              | External bus          | External bus interface (multiplexed mode) address output and data input/output |
| ADTG_R           | ADC                   | Relocated A/D converter trigger input                                          |
| ALE              | External bus          | External bus Address Latch Enable output                                       |
| An               | External bus          | External bus address output                                                    |
| ANn              | ADC                   | A/D converter channel n input                                                  |
| AV <sub>CC</sub> | Supply                | Analog circuits power supply                                                   |
| AVRH             | ADC                   | A/D converter high reference voltage input                                     |
| AV <sub>SS</sub> | Supply                | Analog circuits power supply                                                   |
| C                | Voltage regulator     | Internally regulated power supply stabilization capacitor pin                  |
| CKOTn            | Clock output function | Clock Output function n output                                                 |
| CKOTn_R          | Clock output function | Relocated Clock Output function n output                                       |
| CKOTXn           | Clock output function | Clock Output function n inverted output                                        |
| ECLK             | External bus          | External bus clock output                                                      |
| CSn_R            | External bus          | Relocated External bus chip select n output                                    |
| FRCKn            | Free Running Timer    | Free Running Timer n input                                                     |
| HAKX             | External bus          | External bus Hold Acknowledge                                                  |
| HRQ              | External bus          | External bus Hold Request                                                      |
| INn              | ICU                   | Input Capture Unit n input                                                     |
| INTn             | External Interrupt    | External Interrupt n input                                                     |
| INTn_R           | External Interrupt    | Relocated External Interrupt n input                                           |
| MDn              | Core                  | Input pins for specifying the operating mode.                                  |
| NMI_R            | External Interrupt    | Relocated Non-Maskable Interrupt input                                         |
| OUTn             | OCU                   | Output Compare Unit n waveform output                                          |
| Pxx_n            | GPIO                  | General purpose IO                                                             |
| PPGn             | PPG                   | Programmable Pulse Generator n output                                          |
| PPGn_R           | PPG                   | Relocated Programmable Pulse Generator n output                                |
| RDX              | External bus          | External bus interface read strobe output                                      |
| RDY              | External bus          | External bus interface external wait state request input                       |
| RSTX             | Core                  | Reset input                                                                    |
| RXn              | CAN                   | CAN interface n RX input                                                       |
| SCKn             | USART                 | USART n serial clock input/output                                              |
| SCKn_R           | USART                 | Relocated USART n serial clock input/output                                    |
| SCLn             | I <sup>2</sup> C      | I <sup>2</sup> C interface n clock I/O input/output                            |
| SDAn             | I <sup>2</sup> C      | I <sup>2</sup> C interface n serial data I/O input/output                      |
| SINn             | USART                 | USART n serial data input                                                      |
| SINn_R           | USART                 | Relocated USART n serial data input                                            |
| SOTn             | USART                 | USART n serial data output                                                     |
| SOTn_R           | USART                 | Relocated USART n serial data output                                           |

**Table 1. Pin Function Description (2 / 2)**

| Pin Name        | Feature      | Description                                                   |
|-----------------|--------------|---------------------------------------------------------------|
| TINn            | Reload Timer | Reload Timer n event input                                    |
| TINn_R          | Reload Timer | Relocated Reload Timer n event input                          |
| TOTn            | Reload Timer | Reload Timer n output                                         |
| TOTn_R          | Reload Timer | Relocated Reload Timer n output                               |
| TTGn            | PPG          | Programmable Pulse Generator n trigger input                  |
| TTGn_R          | PPG          | Relocated Programmable Pulse Generator n trigger input        |
| TXn             | CAN          | CAN interface n TX output                                     |
| V <sub>CC</sub> | Supply       | Power supply                                                  |
| V <sub>SS</sub> | Supply       | Power supply                                                  |
| WOT             | RTC          | Real Timer clock output                                       |
| WRHX            | External bus | External bus High byte write strobe output                    |
| WRLX/WRX        | External bus | External bus Low byte / Word write strobe output              |
| X0              | Clock        | Oscillator input                                              |
| X0A             | Clock        | Subclock Oscillator input (only for devices with suffix "W")  |
| X1              | Clock        | Oscillator output                                             |
| X1A             | Clock        | Subclock Oscillator output (only for devices with suffix "W") |

## Pin Circuit Type

**Table 2. LQG064/LQD064**

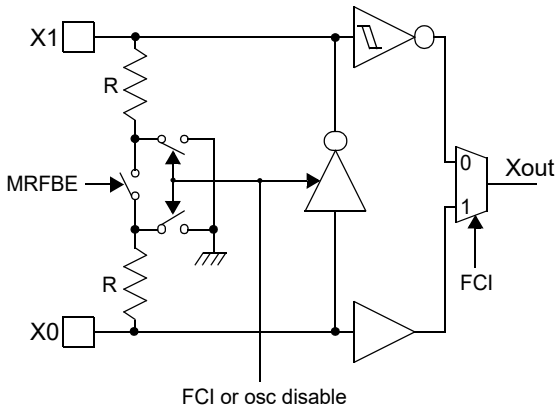
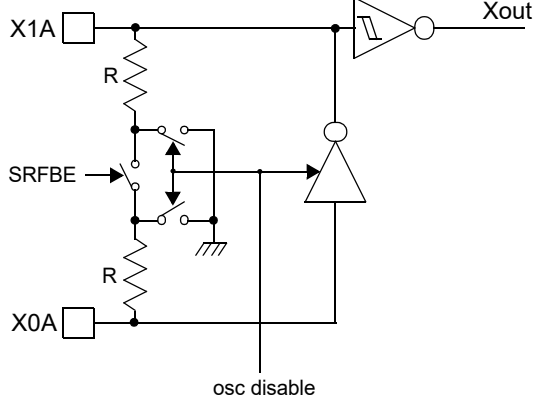
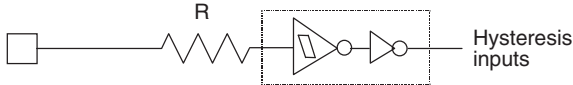
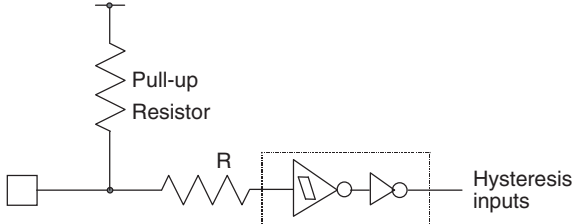
| Pin No.  | Circuit Type <sup>*1</sup> |
|----------|----------------------------|
| 1        | Supply                     |
| 2        | G                          |
| 3 to 15  | I                          |
| 16,17    | H                          |
| 18       | Supply                     |
| 19,20    | B <sup>*2</sup>            |
| 19,20    | H <sup>*3</sup>            |
| 21 to 23 | C                          |
| 24 to 44 | H                          |
| 45       | E                          |
| 46,47    | A                          |
| 48,49    | Supply                     |
| 50       | F                          |
| 51       | H                          |
| 52,53    | N                          |
| 54 to 61 | H                          |
| 62,63    | I                          |
| 64       | Supply                     |

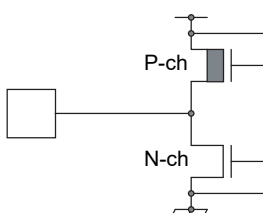
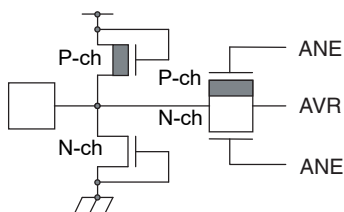
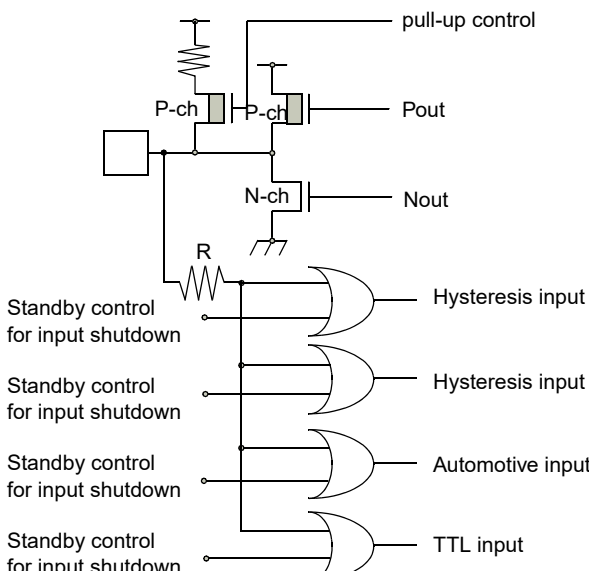
\*1: Please refer to I/O Circuit Type for details on the I/O circuit types

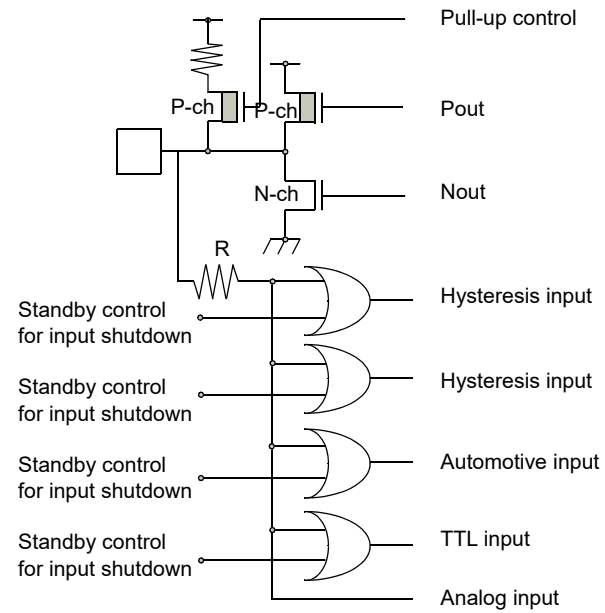
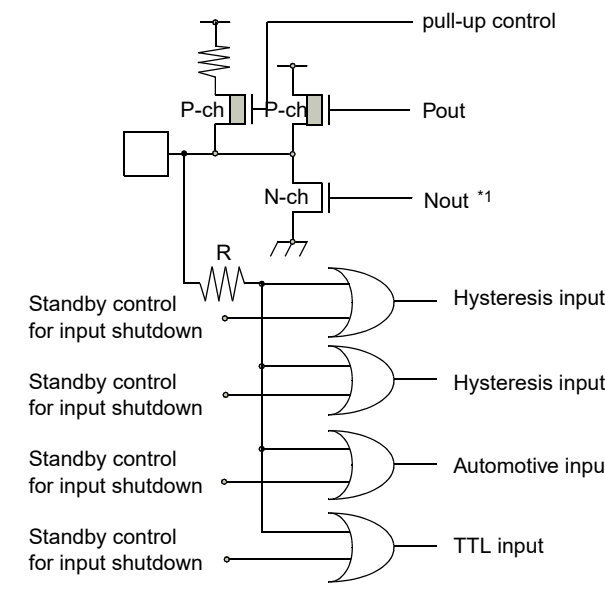
\*2: Devices with suffix "W"

\*3: Devices without suffix "W"

## I/O Circuit Type

| Type | Circuit                                                                             | Remarks                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|-------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A    |    | <p>High-speed oscillation circuit:</p> <ul style="list-style-type: none"> <li>■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)</li> <li>■ Programmable feedback resistor = approx. <math>2 \times 0.5 \text{ M}\Omega</math>. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode</li> </ul> |
| B    |   | <p>Low-speed oscillation circuit:</p> <ul style="list-style-type: none"> <li>■ Programmable feedback resistor = approx. <math>20 \text{ M}\Omega</math> ( X1A: <math>19.5 \text{ M}\Omega</math>, X0A: <math>0.5 \text{ M}\Omega</math> )<br/>Feedback resistor is grounded in the center when the oscillator is disabled</li> </ul>                                                                                                                             |
| C    |  | <ul style="list-style-type: none"> <li>■ Mask ROM and EVA device:<br/>CMOS Hysteresis input pin</li> <li>■ Flash device:<br/>CMOS input pin</li> </ul>                                                                                                                                                                                                                                                                                                           |
| E    |  | <ul style="list-style-type: none"> <li>■ CMOS Hysteresis input pin</li> <li>■ Pull-up resistor value: approx. <math>50 \text{ k}\Omega</math></li> </ul>                                                                                                                                                                                                                                                                                                         |

| Type | Circuit                                                                            | Remarks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F    |   | <ul style="list-style-type: none"> <li>Power supply input protection circuit</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| G    |   | <ul style="list-style-type: none"> <li>A/D converter ref+ (AVRH) power supply input pin with protection circuit</li> <li>Flash devices do not have a protection circuit against VCC for pin AVRH</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                        |
| H    |  | <ul style="list-style-type: none"> <li>CMOS level output (programmable <math>I_{OL} = 5\text{ mA}</math>, <math>I_{OH} = -5\text{ mA}</math> and <math>I_{OL} = 2\text{ mA}</math>, <math>I_{OH} = -2\text{ mA}</math>)</li> <li>2 different CMOS hysteresis inputs with input shutdown function</li> <li>Automotive input with input shutdown function</li> <li>TTL input with input shutdown function</li> <li>Programmable pull-up resistor: 50 k<math>\Omega</math> approx.</li> </ul> <p>Note: CY96F353/F355:<br/>Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported</p> |

| Type | Circuit                                                                             | Remarks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I    |    | <ul style="list-style-type: none"> <li>■ CMOS level output (programmable <math>I_{OL} = 5 \text{ mA}</math>, <math>I_{OH} = -5 \text{ mA}</math> and <math>I_{OL} = 2 \text{ mA}</math>, <math>I_{OH} = -2 \text{ mA}</math>)</li> <li>■ 2 different CMOS hysteresis inputs with input shutdown function</li> <li>■ Automotive input with input shutdown function</li> <li>■ TTL input with input shutdown function.</li> <li>■ Programmable pull-up resistor: 50 k<math>\Omega</math> approx.</li> <li>■ Analog input</li> </ul> <p>Note: CY96F353/F355:<br/>Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported</p> |
| N    |  | <ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 3 \text{ mA}</math>, <math>I_{OH} = -3 \text{ mA}</math>)</li> <li>■ 2 different CMOS hysteresis inputs with input shutdown function</li> <li>■ Automotive input with input shutdown function</li> <li>■ TTL input with input shutdown function</li> <li>■ Programmable pull-up resistor: 50 k<math>\Omega</math> approx.</li> </ul> <p>*1: N-channel transistor has slew rate control according to <math>I^2C</math> spec, irrespective of usage</p> <p>Note: CY96F353/F355:<br/>Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported</p>  |

## Memory Map

|                        | CY96V300C           |                                                | CY96(F)35x                            |                                          |
|------------------------|---------------------|------------------------------------------------|---------------------------------------|------------------------------------------|
| FF:FFF <sub>H</sub>    | Emulation ROM       |                                                | USER ROM / External Bus <sup>*4</sup> |                                          |
| DE:000 <sub>H</sub>    | External Bus        |                                                | External Bus                          |                                          |
| 10:000 <sub>H</sub>    | Boot-ROM            |                                                | Boot-ROM                              |                                          |
| 0F:E00 <sub>H</sub>    | Reserved            |                                                | Reserved                              |                                          |
| 0E:000 <sub>H</sub>    | External RAM        |                                                | Reserved                              |                                          |
| 02:000 <sub>H</sub>    | Internal RAM bank 1 | RAMEND <sup>*2</sup><br>RAMSTART <sup>*2</sup> | Reserved                              |                                          |
| 01:000 <sub>H</sub>    | ROM/RAM MIRROR      |                                                | Internal RAM bank 1                   | RAM availability depending on the device |
| 00:800 <sub>H</sub>    | Internal RAM bank 0 |                                                | Reserved                              |                                          |
|                        |                     |                                                | ROM/RAM MIRROR                        |                                          |
|                        |                     |                                                | Internal RAM bank 0                   |                                          |
|                        |                     |                                                | Reserved                              |                                          |
| RAMSTART <sup>*3</sup> | External Bus        |                                                | External Bus                          | External Bus end address <sup>*2</sup>   |
| 00:0C0 <sub>H</sub>    | Peripherals         |                                                | Peripherals                           |                                          |
| 00:038 <sub>H</sub>    | GPR <sup>*1</sup>   |                                                | GPR <sup>*1</sup>                     |                                          |
| 00:018 <sub>H</sub>    | DMA                 |                                                | DMA                                   |                                          |
| 00:010 <sub>H</sub>    | External Bus        |                                                | External Bus                          |                                          |
| 00:00F <sub>H</sub>    | Peripheral          |                                                | Peripheral                            |                                          |
| 00:000 <sub>H</sub>    |                     |                                                |                                       |                                          |

<sup>\*1</sup>: Unused GPR banks can be used as RAM area  
<sup>\*2</sup>: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.  
<sup>\*3</sup>: For EVA device, RAMSTART0 depends on the configuration of the emulated device.  
<sup>\*4</sup>: For details about USER ROM area, see the [User ROM Memory Map for Flash Devices](#) on the following pages.  
 The External Bus area and DMA area are only available if the device contains the corresponding resource.  
 The available RAM and ROM area depends on the device.

## RAMSTART/END and External Bus End Addresses

| Devices       | Bank 0<br>RAM Size | Bank 1<br>RAM Size | External Bus End<br>Address | RAMSTART0            | RAMSTART1 | RAMEND1 |
|---------------|--------------------|--------------------|-----------------------------|----------------------|-----------|---------|
| CY96F353/F355 | 8 KByte            | -                  | 00:51FF <sub>H</sub>        | 00:6240 <sub>H</sub> | -         | -       |
| CY96F356      | 12 KByte           | -                  | 00:51FF <sub>H</sub>        | 00:5240 <sub>H</sub> | -         | -       |

## User ROM Memory Map for Flash Devices

|                                 |                              | CY96F353               | CY96F355                | CY96F356                |         |
|---------------------------------|------------------------------|------------------------|-------------------------|-------------------------|---------|
| Alternative mode<br>CPU address | Flash memory<br>mode address | Flash size<br>96 kByte | Flash size<br>160 kByte | Flash size<br>288 kByte |         |
| FF:FFFF <sub>H</sub>            | 3F:FFFF <sub>H</sub>         | S39 - 64K              | S39 - 64K               | S39 - 64K               | Flash A |
| FE:FFFF <sub>H</sub>            | 3E:FFFF <sub>H</sub>         |                        | S38 - 64K               | S38 - 64K               |         |
| FD:FFFF <sub>H</sub>            | 3D:FFFF <sub>H</sub>         |                        |                         | S37 - 64K               |         |
| FC:FFFF <sub>H</sub>            | 3C:FFFF <sub>H</sub>         |                        |                         | S36 - 64K               |         |
| FB:FFFF <sub>H</sub>            | 3B:FFFF <sub>H</sub>         | External bus           | External bus            | External bus            |         |
| FA:FFFF <sub>H</sub>            | 3A:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F9:FFFF <sub>H</sub>            | 39:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F8:FFFF <sub>H</sub>            | 38:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F7:FFFF <sub>H</sub>            | 37:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F6:FFFF <sub>H</sub>            | 36:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F5:FFFF <sub>H</sub>            | 35:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F4:FFFF <sub>H</sub>            | 34:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F3:FFFF <sub>H</sub>            | 33:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F2:FFFF <sub>H</sub>            | 32:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F1:FFFF <sub>H</sub>            | 31:FFFF <sub>H</sub>         |                        |                         |                         |         |
| F0:FFFF <sub>H</sub>            | 30:FFFF <sub>H</sub>         |                        |                         |                         |         |
| E0:FFFF <sub>H</sub>            |                              |                        |                         |                         |         |
| E0:0000 <sub>H</sub>            |                              |                        |                         |                         |         |
| DF:FFFF <sub>H</sub>            |                              |                        |                         |                         |         |
| DF:8000 <sub>H</sub>            |                              |                        |                         |                         |         |
| DF:7FFF <sub>H</sub>            | 1F:7FFF <sub>H</sub>         | Reserved               | Reserved                | Reserved                | Flash A |
| DF:6000 <sub>H</sub>            | 1F:6000 <sub>H</sub>         | SA3 - 8K               | SA3 - 8K                | SA3 - 8K                |         |
| DF:5FFF <sub>H</sub>            | 1F:5FFF <sub>H</sub>         | SA2 - 8K               | SA2 - 8K                | SA2 - 8K                |         |
| DF:4000 <sub>H</sub>            | 1F:4000 <sub>H</sub>         | SA1 - 8K               | SA1 - 8K                | SA1 - 8K                |         |
| DF:3FFF <sub>H</sub>            | 1F:3FFF <sub>H</sub>         | SA0 - 8K <sup>*1</sup> | SA0 - 8K <sup>*1</sup>  | SA0 - 8K <sup>*1</sup>  |         |
| DF:0000 <sub>H</sub>            | 1F:0000 <sub>H</sub>         | Reserved               | Reserved                | Reserved                |         |
| DE:FFFF <sub>H</sub>            |                              |                        |                         |                         |         |
| DE:0000 <sub>H</sub>            |                              |                        |                         |                         |         |

<sup>\*1</sup>: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000<sub>H</sub> - DF:007F<sub>H</sub>

\*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000<sub>H</sub> - DF:007F<sub>H</sub>

## Serial Programming Communication Interface

**Table 3. USART pins for Flash serial programming (MD[2:0] = 010)**

| CY96F35x   |              |                 |
|------------|--------------|-----------------|
| Pin Number | USART Number | Normal Function |
| LQFP-64    |              |                 |
| 9          | USART2       | SIN2            |
| 10         |              | SOT2            |
| 11         |              | SCK2            |
| 34         | USART3       | SIN3            |
| 35         |              | SOT3            |
| 36         |              | SCK3            |
| 26         | USART7       | SIN7_R          |
| 25         |              | SOT7_R          |
| 24         |              | SCK7_R          |
| 29         | USART8       | SIN8_R          |
| 28         |              | SOT8_R          |
| 27         |              | SCK8_R          |

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00\_1 on pin 25.

If handshaking is used by the tool but P00\_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

## I/O Map

Table 4. I/O Map CY96(F)35x (1 / 21)

| Address                                  | Register                                                  | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|-----------------------------------------------------------|------------------------------|-------------------------------|--------|
| 000000 <sub>H</sub>                      | I/O Port P00 - Port Data Register                         | PDR00                        |                               | R/W    |
| 000001 <sub>H</sub>                      | I/O Port P01 - Port Data Register                         | PDR01                        |                               | R/W    |
| 000002 <sub>H</sub>                      | I/O Port P02 - Port Data Register                         | PDR02                        |                               | R/W    |
| 000003 <sub>H</sub>                      | I/O Port P03 - Port Data Register                         | PDR03                        |                               | R/W    |
| 000004 <sub>H</sub>                      | I/O Port P04 - Port Data Register                         | PDR04                        |                               | R/W    |
| 000005 <sub>H</sub>                      | I/O Port P05 - Port Data Register                         | PDR05                        |                               | R/W    |
| 000006 <sub>H</sub>                      | I/O Port P06 - Port Data Register                         | PDR06                        |                               | R/W    |
| 000007 <sub>H</sub> -000017 <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000018 <sub>H</sub>                      | ADC0 - Control Status register Low                        | ADCSL                        | ADCS                          | R/W    |
| 000019 <sub>H</sub>                      | ADC0 - Control Status register High                       | ADCSH                        |                               | R/W    |
| 00001A <sub>H</sub>                      | ADC0 - Data Register Low                                  | ADCRL                        | ADCR                          | R      |
| 00001B <sub>H</sub>                      | ADC0 - Data Register High                                 | ADCRH                        |                               | R      |
| 00001C <sub>H</sub>                      | ADC0 - Setting Register                                   |                              | ADSR                          | R/W    |
| 00001D <sub>H</sub>                      | ADC0 - Setting Register                                   |                              |                               | R/W    |
| 00001E <sub>H</sub>                      | ADC0 - Extended Configuration Register                    | ADECR                        |                               | R/W    |
| 00001F <sub>H</sub>                      | Reserved                                                  |                              |                               | -      |
| 000020 <sub>H</sub>                      | FRT0 - Data register of free-running timer                |                              | TCDT0                         | R/W    |
| 000021 <sub>H</sub>                      | FRT0 - Data register of free-running timer                |                              |                               | R/W    |
| 000022 <sub>H</sub>                      | FRT0 - Control status register of free-running timer Low  | TCCSL0                       | TCCS0                         | R/W    |
| 000023 <sub>H</sub>                      | FRT0 - Control status register of free-running timer High | TCCSH0                       |                               | R/W    |
| 000024 <sub>H</sub>                      | FRT1 - Data register of free-running timer                |                              | TCDT1                         | R/W    |
| 000025 <sub>H</sub>                      | FRT1 - Data register of free-running timer                |                              |                               | R/W    |
| 000026 <sub>H</sub>                      | FRT1 - Control status register of free-running timer Low  | TCCSL1                       | TCCS1                         | R/W    |
| 000027 <sub>H</sub>                      | FRT1 - Control status register of free-running timer High | TCCSH1                       |                               | R/W    |
| 000028 <sub>H</sub> -000033 <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000034 <sub>H</sub>                      | OCU4 - Output Compare Control Status                      | OCS4                         |                               | R/W    |
| 000035 <sub>H</sub>                      | OCU5 - Output Compare Control Status                      | OCS5                         |                               | R/W    |
| 000036 <sub>H</sub>                      | OCU4 - Compare Register                                   |                              | OCCP4                         | R/W    |
| 000037 <sub>H</sub>                      | OCU4 - Compare Register                                   |                              |                               | R/W    |
| 000038 <sub>H</sub>                      | OCU5 - Compare Register                                   |                              | OCCP5                         | R/W    |
| 000039 <sub>H</sub>                      | OCU5 - Compare Register                                   |                              |                               | R/W    |
| 00003A <sub>H</sub>                      | OCU6 - Output Compare Control Status                      | OCS6                         |                               | R/W    |
| 00003B <sub>H</sub>                      | OCU7 - Output Compare Control Status                      | OCS7                         |                               | R/W    |
| 00003C <sub>H</sub>                      | OCU6 - Compare Register                                   |                              | OCCP6                         | R/W    |
| 00003D <sub>H</sub>                      | OCU6 - Compare Register                                   |                              |                               | R/W    |
| 00003E <sub>H</sub>                      | OCU7 - Compare Register                                   |                              | OCCP7                         | R/W    |
| 00003F <sub>H</sub>                      | OCU7 - Compare Register                                   |                              |                               | R/W    |
| 000040 <sub>H</sub>                      | ICU0/ICU1 - Control Status Register                       | ICS01                        |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (2 / 21)**

| Address                                   | Register                                                | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|-------------------------------------------|---------------------------------------------------------|------------------------------|-------------------------------|--------|
| 000041 <sub>H</sub>                       | ICU0/ICU1 - Edge register                               | ICE01                        |                               | R/W    |
| 000042 <sub>H</sub>                       | ICU0 - Capture Register Low                             | IPCPL0                       | IPCP0                         | R      |
| 000043 <sub>H</sub>                       | ICU0 - Capture Register High                            | IPCPH0                       |                               | R      |
| 000044 <sub>H</sub>                       | ICU1 - Capture Register Low                             | IPCPL1                       | IPCP1                         | R      |
| 000045 <sub>H</sub>                       | ICU1 - Capture Register High                            | IPCPH1                       |                               | R      |
| 000046 <sub>H</sub> - 00004B <sub>H</sub> | Reserved                                                |                              |                               |        |
| 00004C <sub>H</sub>                       | ICU4/ICU5 - Control Status Register                     | ICS45                        |                               | R/W    |
| 00004D <sub>H</sub>                       | ICU4/ICU5 - Edge register                               | ICE45                        |                               | R/W    |
| 00004E <sub>H</sub>                       | ICU4 - Capture Register Low                             | IPCPL4                       | IPCP4                         | R      |
| 00004F <sub>H</sub>                       | ICU4 - Capture Register High                            | IPCPH4                       |                               | R      |
| 000050 <sub>H</sub>                       | ICU5 - Capture Register Low                             | IPCPL5                       | IPCP5                         | R      |
| 000051 <sub>H</sub>                       | ICU5 - Capture Register High                            | IPCPH5                       |                               | R      |
| 000052 <sub>H</sub>                       | ICU6/ICU7 - Control Status Register                     | ICS67                        |                               | R/W    |
| 000053 <sub>H</sub>                       | ICU6/ICU7 - Edge register                               | ICE67                        |                               | R/W    |
| 000054 <sub>H</sub>                       | ICU6 - Capture Register Low                             | IPCPL6                       | IPCP6                         | R      |
| 000055 <sub>H</sub>                       | ICU6 - Capture Register High                            | IPCPH6                       |                               | R      |
| 000056 <sub>H</sub>                       | ICU7 - Capture Register Low                             | IPCPL7                       | IPCP7                         | R      |
| 000057 <sub>H</sub>                       | ICU7 - Capture Register High                            | IPCPH7                       |                               | R      |
| 000058 <sub>H</sub>                       | EXTINT0 - External Interrupt Enable Register            | ENIR0                        |                               | R/W    |
| 000059 <sub>H</sub>                       | EXTINT0 - External Interrupt Interrupt request Register | EIRR0                        |                               | R/W    |
| 00005A <sub>H</sub>                       | EXTINT0 - External Interrupt Level Select Low           | ELVRL0                       | ELVR0                         | R/W    |
| 00005B <sub>H</sub>                       | EXTINT0 - External Interrupt Level Select High          | ELVRH0                       |                               | R/W    |
| 00005C <sub>H</sub>                       | EXTINT1 - External Interrupt Enable Register            | ENIR1                        |                               | R/W    |
| 00005D <sub>H</sub>                       | EXTINT1 - External Interrupt Interrupt request Register | EIRR1                        |                               | R/W    |
| 00005E <sub>H</sub>                       | EXTINT1 - External Interrupt Level Select Low           | ELVRL1                       | ELVR1                         | R/W    |
| 00005F <sub>H</sub>                       | EXTINT1 - External Interrupt Level Select High          | ELVRH1                       |                               | R/W    |
| 000060 <sub>H</sub>                       | RLT0 - Timer Control Status Register Low                | TMCSRL0                      | TMCSR0                        | R/W    |
| 000061 <sub>H</sub>                       | RLT0 - Timer Control Status Register High               | TMCSRH0                      |                               | R/W    |
| 000062 <sub>H</sub>                       | RLT0 - Reload Register - for writing                    |                              | TMRLR0                        | W      |
| 000062 <sub>H</sub>                       | RLT0 - Reload Register - for reading                    |                              | TMR0                          | R      |
| 000063 <sub>H</sub>                       | RLT0 - Reload Register - for writing                    |                              |                               | W      |
| 000063 <sub>H</sub>                       | RLT0 - Reload Register - for reading                    |                              |                               | R      |
| 000064 <sub>H</sub>                       | RLT1 - Timer Control Status Register Low                | TMCSRL1                      | TMCSR1                        | R/W    |
| 000065 <sub>H</sub>                       | RLT1 - Timer Control Status Register High               | TMCSRH1                      |                               | R/W    |
| 000066 <sub>H</sub>                       | RLT1 - Reload Register - for writing                    |                              | TMRLR1                        | W      |
| 000066 <sub>H</sub>                       | RLT1 - Reload Register - for reading                    |                              | TMR1                          | R      |
| 000067 <sub>H</sub>                       | RLT1 - Reload Register - for writing                    |                              |                               | W      |
| 000067 <sub>H</sub>                       | RLT1 - Reload Register - for reading                    |                              |                               | R      |
| 000068 <sub>H</sub>                       | RLT2 - Timer Control Status Register Low                | TMCSRL2                      | TMCSR2                        | R/W    |

**Table 4. I/O Map CY96(F)35x (3 / 21)**

| Address             | Register                                                       | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|---------------------|----------------------------------------------------------------|------------------------------|-------------------------------|--------|
| 000069 <sub>H</sub> | RLT2 - Timer Control Status Register High                      | TMCSRH2                      |                               | R/W    |
| 00006A <sub>H</sub> | RLT2 - Reload Register - for writing                           |                              | TMRLR2                        | W      |
| 00006A <sub>H</sub> | RLT2 - Reload Register - for reading                           |                              | TMR2                          | R      |
| 00006B <sub>H</sub> | RLT2 - Reload Register - for writing                           |                              |                               | W      |
| 00006B <sub>H</sub> | RLT2 - Reload Register - for reading                           |                              |                               | R      |
| 00006C <sub>H</sub> | RLT3 - Timer Control Status Register Low                       | TMCSRL3                      | TMCSR3                        | R/W    |
| 00006D <sub>H</sub> | RLT3 - Timer Control Status Register High                      | TMCSRH3                      |                               | R/W    |
| 00006E <sub>H</sub> | RLT3 - Reload Register - for writing                           |                              | TMRLR3                        | W      |
| 00006E <sub>H</sub> | RLT3 - Reload Register - for reading                           |                              | TMR3                          | R      |
| 00006F <sub>H</sub> | RLT3 - Reload Register - for writing                           |                              |                               | W      |
| 00006F <sub>H</sub> | RLT3 - Reload Register - for reading                           |                              |                               | R      |
| 000070 <sub>H</sub> | RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)  | TMCSRL6                      | TMCSR6                        | R/W    |
| 000071 <sub>H</sub> | RLT6 - Timer Control Status Register High (dedic. RLT for PPG) | TMCSRH6                      |                               | R/W    |
| 000072 <sub>H</sub> | RLT6 - Reload Register (dedic. RLT for PPG) - for writing      |                              | TMRLR6                        | W      |
| 000072 <sub>H</sub> | RLT6 - Reload Register (dedic. RLT for PPG) - for reading      |                              | TMR6                          | R      |
| 000073 <sub>H</sub> | RLT6 - Reload Register (dedic. RLT for PPG) - for writing      |                              |                               | W      |
| 000073 <sub>H</sub> | RLT6 - Reload Register (dedic. RLT for PPG) - for reading      |                              |                               | R      |
| 000074 <sub>H</sub> | PPG3-PPG0 - General Control register 1 Low                     | GCN1L0                       | GCN10                         | R/W    |
| 000075 <sub>H</sub> | PPG3-PPG0 - General Control register 1 High                    | GCN1H0                       |                               | R/W    |
| 000076 <sub>H</sub> | PPG3-PPG0 - General Control register 2 Low                     | GCN2L0                       | GCN20                         | R/W    |
| 000077 <sub>H</sub> | PPG3-PPG0 - General Control register 2 High                    | GCN2H0                       |                               | R/W    |
| 000078 <sub>H</sub> | PPG0 - Timer register                                          |                              | PTMR0                         | R      |
| 000079 <sub>H</sub> | PPG0 - Timer register                                          |                              |                               | R      |
| 00007A <sub>H</sub> | PPG0 - Period setting register                                 |                              | PCSR0                         | W      |
| 00007B <sub>H</sub> | PPG0 - Period setting register                                 |                              |                               | W      |
| 00007C <sub>H</sub> | PPG0 - Duty cycle register                                     |                              | PDUT0                         | W      |
| 00007D <sub>H</sub> | PPG0 - Duty cycle register                                     |                              |                               | W      |
| 00007E <sub>H</sub> | PPG0 - Control status register Low                             | PCNL0                        | PCN0                          | R/W    |
| 00007F <sub>H</sub> | PPG0 - Control status register High                            | PCNH0                        |                               | R/W    |
| 000080 <sub>H</sub> | PPG1 - Timer register                                          |                              | PTMR1                         | R      |
| 000081 <sub>H</sub> | PPG1 - Timer register                                          |                              |                               | R      |
| 000082 <sub>H</sub> | PPG1 - Period setting register                                 |                              | PCSR1                         | W      |
| 000083 <sub>H</sub> | PPG1 - Period setting register                                 |                              |                               | W      |
| 000084 <sub>H</sub> | PPG1 - Duty cycle register                                     |                              | PDUT1                         | W      |
| 000085 <sub>H</sub> | PPG1 - Duty cycle register                                     |                              |                               | W      |
| 000086 <sub>H</sub> | PPG1 - Control status register Low                             | PCNL1                        | PCN1                          | R/W    |
| 000087 <sub>H</sub> | PPG1 - Control status register High                            | PCNH1                        |                               | R/W    |
| 000088 <sub>H</sub> | PPG2 - Timer register                                          |                              | PTMR2                         | R      |

**Table 4. I/O Map CY96(F)35x (4 / 21)**

| Address             | Register                                    | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|---------------------|---------------------------------------------|------------------------------|-------------------------------|--------|
| 000089 <sub>H</sub> | PPG2 - Timer register                       |                              |                               | R      |
| 00008A <sub>H</sub> | PPG2 - Period setting register              |                              | PCSR2                         | W      |
| 00008B <sub>H</sub> | PPG2 - Period setting register              |                              |                               | W      |
| 00008C <sub>H</sub> | PPG2 - Duty cycle register                  |                              | PDUT2                         | W      |
| 00008D <sub>H</sub> | PPG2 - Duty cycle register                  |                              |                               | W      |
| 00008E <sub>H</sub> | PPG2 - Control status register Low          | PCNL2                        | PCN2                          | R/W    |
| 00008F <sub>H</sub> | PPG2 - Control status register High         | PCNH2                        |                               | R/W    |
| 000090 <sub>H</sub> | PPG3 - Timer register                       |                              | PTMR3                         | R      |
| 000091 <sub>H</sub> | PPG3 - Timer register                       |                              |                               | R      |
| 000092 <sub>H</sub> | PPG3 - Period setting register              |                              | PCSR3                         | W      |
| 000093 <sub>H</sub> | PPG3 - Period setting register              |                              |                               | W      |
| 000094 <sub>H</sub> | PPG3 - Duty cycle register                  |                              | PDUT3                         | W      |
| 000095 <sub>H</sub> | PPG3 - Duty cycle register                  |                              |                               | W      |
| 000096 <sub>H</sub> | PPG3 - Control status register Low          | PCNL3                        | PCN3                          | R/W    |
| 000097 <sub>H</sub> | PPG3 - Control status register High         | PCNH3                        |                               | R/W    |
| 000098 <sub>H</sub> | PPG7-PPG4 - General Control register 1 Low  | GCN1L1                       | GCN11                         | R/W    |
| 000099 <sub>H</sub> | PPG7-PPG4 - General Control register 1 High | GCN1H1                       |                               | R/W    |
| 00009A <sub>H</sub> | PPG7-PPG4 - General Control register 2 Low  | GCN2L1                       | GCN21                         | R/W    |
| 00009B <sub>H</sub> | PPG7-PPG4 - General Control register 2 High | GCN2H1                       |                               | R/W    |
| 00009C <sub>H</sub> | PPG4 - Timer register                       |                              | PTMR4                         | R      |
| 00009D <sub>H</sub> | PPG4 - Timer register                       |                              |                               | R      |
| 00009E <sub>H</sub> | PPG4 - Period setting register              |                              | PCSR4                         | W      |
| 00009F <sub>H</sub> | PPG4 - Period setting register              |                              |                               | W      |
| 0000A0 <sub>H</sub> | PPG4 - Duty cycle register                  |                              | PDUT4                         | W      |
| 0000A1 <sub>H</sub> | PPG4 - Duty cycle register                  |                              |                               | W      |
| 0000A2 <sub>H</sub> | PPG4 - Control status register Low          | PCNL4                        | PCN4                          | R/W    |
| 0000A3 <sub>H</sub> | PPG4 - Control status register High         | PCNH4                        |                               | R/W    |
| 0000A4 <sub>H</sub> | PPG5 - Timer register                       |                              | PTMR5                         | R      |
| 0000A5 <sub>H</sub> | PPG5 - Timer register                       |                              |                               | R      |
| 0000A6 <sub>H</sub> | PPG5 - Period setting register              |                              | PCSR5                         | W      |
| 0000A7 <sub>H</sub> | PPG5 - Period setting register              |                              |                               | W      |
| 0000A8 <sub>H</sub> | PPG5 - Duty cycle register                  |                              | PDUT5                         | W      |
| 0000A9 <sub>H</sub> | PPG5 - Duty cycle register                  |                              |                               | W      |
| 0000AA <sub>H</sub> | PPG5 - Control status register Low          | PCNL5                        | PCN5                          | R/W    |
| 0000AB <sub>H</sub> | PPG5 - Control status register High         | PCNH5                        |                               | R/W    |
| 0000AC <sub>H</sub> | I2C0 - Bus Status Register                  | IBSR0                        |                               | R      |
| 0000AD <sub>H</sub> | I2C0 - Bus Control Register                 | IBCR0                        |                               | R/W    |
| 0000AE <sub>H</sub> | I2C0 - Ten bit Slave address Register Low   | ITBAL0                       | ITBA0                         | R/W    |
| 0000AF <sub>H</sub> | I2C0 - Ten bit Slave address Register High  | ITBAH0                       |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (5 / 21)**

| Address                                  | Register                                      | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|-----------------------------------------------|------------------------------|-------------------------------|--------|
| 0000B0 <sub>H</sub>                      | I2C0 - Ten bit Address mask Register Low      | ITMKL0                       | ITMK0                         | R/W    |
| 0000B1 <sub>H</sub>                      | I2C0 - Ten bit Address mask Register High     | ITMKH0                       |                               | R/W    |
| 0000B2 <sub>H</sub>                      | I2C0 - Seven bit Slave address Register       | ISBA0                        |                               | R/W    |
| 0000B3 <sub>H</sub>                      | I2C0 - Seven bit Address mask Register        | ISMK0                        |                               | R/W    |
| 0000B4 <sub>H</sub>                      | I2C0 - Data Register                          | IDAR0                        |                               | R/W    |
| 0000B5 <sub>H</sub>                      | I2C0 - Clock Control Register                 | ICCR0                        |                               | R/W    |
| 0000B6 <sub>H</sub> -0000D3 <sub>H</sub> | Reserved                                      |                              |                               | -      |
| 0000D4 <sub>H</sub>                      | USART2 - Serial Mode Register                 | SMR2                         |                               | R/W    |
| 0000D5 <sub>H</sub>                      | USART2 - Serial Control Register              | SCR2                         |                               | R/W    |
| 0000D6 <sub>H</sub>                      | USART2 - TX Register                          | TDR2                         |                               | W      |
| 0000D6 <sub>H</sub>                      | USART2 - RX Register                          | RDR2                         |                               | R      |
| 0000D7 <sub>H</sub>                      | USART2 - Serial Status                        | SSR2                         |                               | R/W    |
| 0000D8 <sub>H</sub>                      | USART2 - Control/Com. Register                | ECCR2                        |                               | R/W    |
| 0000D9 <sub>H</sub>                      | USART2 - Ext. Status Register                 | ESCR2                        |                               | R/W    |
| 0000DA <sub>H</sub>                      | USART2 - Baud Rate Generator Register Low     | BGRL2                        | BGR2                          | R/W    |
| 0000DB <sub>H</sub>                      | USART2 - Baud Rate Generator Register High    | BGRH2                        |                               | R/W    |
| 0000DC <sub>H</sub>                      | USART2 - Extended Serial Interrupt Register   | ESIR2                        |                               | R/W    |
| 0000DD <sub>H</sub>                      | Reserved                                      |                              |                               | -      |
| 0000DE <sub>H</sub>                      | USART3 - Serial Mode Register                 | SMR3                         |                               | R/W    |
| 0000DF <sub>H</sub>                      | USART3 - Serial Control Register              | SCR3                         |                               | R/W    |
| 0000E0 <sub>H</sub>                      | USART3 - TX Register                          | TDR3                         |                               | W      |
| 0000E0 <sub>H</sub>                      | USART3 - RX Register                          | RDR3                         |                               | R      |
| 0000E1 <sub>H</sub>                      | USART3 - Serial Status                        | SSR3                         |                               | R/W    |
| 0000E2 <sub>H</sub>                      | USART3 - Control/Com. Register                | ECCR3                        |                               | R/W    |
| 0000E3 <sub>H</sub>                      | USART3 - Ext. Status Register                 | ESCR3                        |                               | R/W    |
| 0000E4 <sub>H</sub>                      | USART3 - Baud Rate Generator Register Low     | BGRL3                        | BGR3                          | R/W    |
| 0000E5 <sub>H</sub>                      | USART3 - Baud Rate Generator Register High    | BGRH3                        |                               | R/W    |
| 0000E6 <sub>H</sub>                      | USART3 - Extended Serial Interrupt Register   | ESIR3                        |                               | R/W    |
| 0000E7 <sub>H</sub> -0000EF <sub>H</sub> | Reserved                                      |                              |                               | -      |
| 0000F0 <sub>H</sub> -0000FF <sub>H</sub> | External Bus area                             | EXTBUS0                      |                               | R/W    |
| 000100 <sub>H</sub>                      | DMA0 - Buffer address pointer low byte        | BAPL0                        |                               | R/W    |
| 000101 <sub>H</sub>                      | DMA0 - Buffer address pointer middle byte     | BAPM0                        |                               | R/W    |
| 000102 <sub>H</sub>                      | DMA0 - Buffer address pointer high byte       | BAPH0                        |                               | R/W    |
| 000103 <sub>H</sub>                      | DMA0 - DMA control register                   | DMACS0                       |                               | R/W    |
| 000104 <sub>H</sub>                      | DMA0 - I/O register address pointer low byte  | IOAL0                        | IOA0                          | R/W    |
| 000105 <sub>H</sub>                      | DMA0 - I/O register address pointer high byte | IOAH0                        |                               | R/W    |
| 000106 <sub>H</sub>                      | DMA0 - Data counter low byte                  | DCTL0                        | DCT0                          | R/W    |
| 000107 <sub>H</sub>                      | DMA0 - Data counter high byte                 | DCTH0                        |                               | R/W    |
| 000108 <sub>H</sub>                      | DMA1 - Buffer address pointer low byte        | BAPL1                        |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (6 / 21)**

| Address                                  | Register                                      | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|-----------------------------------------------|------------------------------|-------------------------------|--------|
| 000109 <sub>H</sub>                      | DMA1 - Buffer address pointer middle byte     | BAPM1                        |                               | R/W    |
| 00010A <sub>H</sub>                      | DMA1 - Buffer address pointer high byte       | BAPH1                        |                               | R/W    |
| 00010B <sub>H</sub>                      | DMA1 - DMA control register                   | DMACS1                       |                               | R/W    |
| 00010C <sub>H</sub>                      | DMA1 - I/O register address pointer low byte  | IOAL1                        | IOA1                          | R/W    |
| 00010D <sub>H</sub>                      | DMA1 - I/O register address pointer high byte | IOAH1                        |                               | R/W    |
| 00010E <sub>H</sub>                      | DMA1 - Data counter low byte                  | DCTL1                        | DCT1                          | R/W    |
| 00010F <sub>H</sub>                      | DMA1 - Data counter high byte                 | DCTH1                        |                               | R/W    |
| 000110 <sub>H</sub>                      | DMA2 - Buffer address pointer low byte        | BAPL2                        |                               | R/W    |
| 000111 <sub>H</sub>                      | DMA2 - Buffer address pointer middle byte     | BAPM2                        |                               | R/W    |
| 000112 <sub>H</sub>                      | DMA2 - Buffer address pointer high byte       | BAPH2                        |                               | R/W    |
| 000113 <sub>H</sub>                      | DMA2 - DMA control register                   | DMACS2                       |                               | R/W    |
| 000114 <sub>H</sub>                      | DMA2 - I/O register address pointer low byte  | IOAL2                        | IOA2                          | R/W    |
| 000115 <sub>H</sub>                      | DMA2 - I/O register address pointer high byte | IOAH2                        |                               | R/W    |
| 000116 <sub>H</sub>                      | DMA2 - Data counter low byte                  | DCTL2                        | DCT2                          | R/W    |
| 000117 <sub>H</sub>                      | DMA2 - Data counter high byte                 | DCTH2                        |                               | R/W    |
| 000118 <sub>H</sub>                      | DMA3 - Buffer address pointer low byte        | BAPL3                        |                               | R/W    |
| 000119 <sub>H</sub>                      | DMA3 - Buffer address pointer middle byte     | BAPM3                        |                               | R/W    |
| 00011A <sub>H</sub>                      | DMA3 - Buffer address pointer high byte       | BAPH3                        |                               | R/W    |
| 00011B <sub>H</sub>                      | DMA3 - DMA control register                   | DMACS3                       |                               | R/W    |
| 00011C <sub>H</sub>                      | DMA3 - I/O register address pointer low byte  | IOAL3                        | IOA3                          | R/W    |
| 00011D <sub>H</sub>                      | DMA3 - I/O register address pointer high byte | IOAH3                        |                               | R/W    |
| 00011E <sub>H</sub>                      | DMA3 - Data counter low byte                  | DCTL3                        | DCT3                          | R/W    |
| 00011F <sub>H</sub>                      | DMA3 - Data counter high byte                 | DCTH3                        |                               | R/W    |
| 000120 <sub>H</sub> -00017F <sub>H</sub> | Reserved                                      |                              |                               | -      |
| 000180 <sub>H</sub> -00037F <sub>H</sub> | CPU - General Purpose registers (RAM access)  | GPR_RAM                      |                               | R/W    |
| 000380 <sub>H</sub>                      | DMA0 - Interrupt select                       | DISEL0                       |                               | R/W    |
| 000381 <sub>H</sub>                      | DMA1 - Interrupt select                       | DISEL1                       |                               | R/W    |
| 000382 <sub>H</sub>                      | DMA2 - Interrupt select                       | DISEL2                       |                               | R/W    |
| 000383 <sub>H</sub>                      | DMA3 - Interrupt select                       | DISEL3                       |                               | R/W    |
| 000384 <sub>H</sub> -00038F <sub>H</sub> | Reserved                                      |                              |                               | —      |
| 000390 <sub>H</sub>                      | DMA - Status register low byte                | DSRL                         | DSR                           | R/W    |
| 000391 <sub>H</sub>                      | DMA - Status register high byte               | DSRH                         |                               | R/W    |
| 000392 <sub>H</sub>                      | DMA - Stop status register low byte           | DSSRL                        | DSSR                          | R/W    |
| 000393 <sub>H</sub>                      | DMA - Stop status register high byte          | DSSRH                        |                               | R/W    |
| 000394 <sub>H</sub>                      | DMA - Enable register low byte                | DERL                         | DER                           | R/W    |
| 000395 <sub>H</sub>                      | DMA - Enable register high byte               | DERH                         |                               | R/W    |
| 000396 <sub>H</sub> -00039F <sub>H</sub> | Reserved                                      |                              |                               | -      |
| 0003A0 <sub>H</sub>                      | Interrupt level register                      | ILR                          | ICR                           | R/W    |
| 0003A1 <sub>H</sub>                      | Interrupt index register                      | IDX                          |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (7 / 21)**

| Address                                  | Register                                       | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|------------------------------------------------|------------------------------|-------------------------------|--------|
| 0003A2 <sub>H</sub>                      | Interrupt vector table base register Low       | TBRL                         | TBR                           | R/W    |
| 0003A3 <sub>H</sub>                      | Interrupt vector table base register High      | TBRH                         |                               | R/W    |
| 0003A4 <sub>H</sub>                      | Delayed Interrupt register                     | DIRR                         |                               | R/W    |
| 0003A5 <sub>H</sub>                      | Non Maskable Interrupt register                | NMI                          |                               | R/W    |
| 0003A6 <sub>H</sub> -0003AB <sub>H</sub> | Reserved                                       |                              |                               | -      |
| 0003AC <sub>H</sub>                      | EDSU communication interrupt selection Low     | EDSU2L                       | EDSU2                         | R/W    |
| 0003AD <sub>H</sub>                      | EDSU communication interrupt selection High    | EDSU2H                       |                               | R/W    |
| 0003AE <sub>H</sub>                      | ROM mirror control register                    | ROMM                         |                               | R/W    |
| 0003AF <sub>H</sub>                      | EDSU configuration register                    | EDSU                         |                               | R/W    |
| 0003B0 <sub>H</sub>                      | Memory patch control/status register ch 0/1    |                              | PFCS0                         | R/W    |
| 0003B1 <sub>H</sub>                      | Memory patch control/status register ch 0/1    |                              |                               | R/W    |
| 0003B2 <sub>H</sub>                      | Memory patch control/status register ch 2/3    |                              | PFCS1                         | R/W    |
| 0003B3 <sub>H</sub>                      | Memory patch control/status register ch 2/3    |                              |                               | R/W    |
| 0003B4 <sub>H</sub>                      | Memory patch control/status register ch 4/5    |                              | PFCS2                         | R/W    |
| 0003B5 <sub>H</sub>                      | Memory patch control/status register ch 4/5    |                              |                               | R/W    |
| 0003B6 <sub>H</sub>                      | Memory patch control/status register ch 6/7    |                              | PFCS3                         | R/W    |
| 0003B7 <sub>H</sub>                      | Memory patch control/status register ch 6/7    |                              |                               | R/W    |
| 0003B8 <sub>H</sub>                      | Memory Patch function - Patch address 0 low    | PFAL0                        |                               | R/W    |
| 0003B9 <sub>H</sub>                      | Memory Patch function - Patch address 0 middle | PFAM0                        |                               | R/W    |
| 0003BA <sub>H</sub>                      | Memory Patch function - Patch address 0 high   | PFAH0                        |                               | R/W    |
| 0003BB <sub>H</sub>                      | Memory Patch function - Patch address 1 low    | PFAL1                        |                               | R/W    |
| 0003BC <sub>H</sub>                      | Memory Patch function - Patch address 1 middle | PFAM1                        |                               | R/W    |
| 0003BD <sub>H</sub>                      | Memory Patch function - Patch address 1 high   | PFAH1                        |                               | R/W    |
| 0003BE <sub>H</sub>                      | Memory Patch function - Patch address 2 low    | PFAL2                        |                               | R/W    |
| 0003BF <sub>H</sub>                      | Memory Patch function - Patch address 2 middle | PFAM2                        |                               | R/W    |
| 0003C0 <sub>H</sub>                      | Memory Patch function - Patch address 2 high   | PFAH2                        |                               | R/W    |
| 0003C1 <sub>H</sub>                      | Memory Patch function - Patch address 3 low    | PFAL3                        |                               | R/W    |
| 0003C2 <sub>H</sub>                      | Memory Patch function - Patch address 3 middle | PFAM3                        |                               | R/W    |
| 0003C3 <sub>H</sub>                      | Memory Patch function - Patch address 3 high   | PFAH3                        |                               | R/W    |
| 0003C4 <sub>H</sub>                      | Memory Patch function - Patch address 4 low    | PFAL4                        |                               | R/W    |
| 0003C5 <sub>H</sub>                      | Memory Patch function - Patch address 4 middle | PFAM4                        |                               | R/W    |
| 0003C6 <sub>H</sub>                      | Memory Patch function - Patch address 4 high   | PFAH4                        |                               | R/W    |
| 0003C7 <sub>H</sub>                      | Memory Patch function - Patch address 5 low    | PFAL5                        |                               | R/W    |
| 0003C8 <sub>H</sub>                      | Memory Patch function - Patch address 5 middle | PFAM5                        |                               | R/W    |
| 0003C9 <sub>H</sub>                      | Memory Patch function - Patch address 5 high   | PFAH5                        |                               | R/W    |
| 0003CA <sub>H</sub>                      | Memory Patch function - Patch address 6 low    | PFAL6                        |                               | R/W    |
| 0003CB <sub>H</sub>                      | Memory Patch function - Patch address 6 middle | PFAM6                        |                               | R/W    |
| 0003CC <sub>H</sub>                      | Memory Patch function - Patch address 6 high   | PFAH6                        |                               | R/W    |
| 0003CD <sub>H</sub>                      | Memory Patch function - Patch address 7 low    | PFAL7                        |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (8 / 21)**

| Address                                  | Register                                       | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|------------------------------------------------|------------------------------|-------------------------------|--------|
| 0003CE <sub>H</sub>                      | Memory Patch function - Patch address 7 middle | PFAM7                        |                               | R/W    |
| 0003CF <sub>H</sub>                      | Memory Patch function - Patch address 7 high   | PFAH7                        |                               | R/W    |
| 0003D0 <sub>H</sub>                      | Memory Patch function - Patch data 0 Low       | PFDL0                        | PFD0                          | R/W    |
| 0003D1 <sub>H</sub>                      | Memory Patch function - Patch data 0 High      | PFDH0                        |                               | R/W    |
| 0003D2 <sub>H</sub>                      | Memory Patch function - Patch data 1 Low       | PFDL1                        | PFD1                          | R/W    |
| 0003D3 <sub>H</sub>                      | Memory Patch function - Patch data 1 High      | PFDH1                        |                               | R/W    |
| 0003D4 <sub>H</sub>                      | Memory Patch function - Patch data 2 Low       | PFDL2                        | PFD2                          | R/W    |
| 0003D5 <sub>H</sub>                      | Memory Patch function - Patch data 2 High      | PFDH2                        |                               | R/W    |
| 0003D6 <sub>H</sub>                      | Memory Patch function - Patch data 3 Low       | PFDL3                        | PFD3                          | R/W    |
| 0003D7 <sub>H</sub>                      | Memory Patch function - Patch data 3 High      | PFDH3                        |                               | R/W    |
| 0003D8 <sub>H</sub>                      | Memory Patch function - Patch data 4 Low       | PFDL4                        | PFD4                          | R/W    |
| 0003D9 <sub>H</sub>                      | Memory Patch function - Patch data 4 High      | PFDH4                        |                               | R/W    |
| 0003DA <sub>H</sub>                      | Memory Patch function - Patch data 5 Low       | PFDL5                        | PFD5                          | R/W    |
| 0003DB <sub>H</sub>                      | Memory Patch function - Patch data 5 High      | PFDH5                        |                               | R/W    |
| 0003DC <sub>H</sub>                      | Memory Patch function - Patch data 6 Low       | PFDL6                        | PFD6                          | R/W    |
| 0003DD <sub>H</sub>                      | Memory Patch function - Patch data 6 High      | PFDH6                        |                               | R/W    |
| 0003DE <sub>H</sub>                      | Memory Patch function - Patch data 7 Low       | PFDL7                        | PFD7                          | R/W    |
| 0003DF <sub>H</sub>                      | Memory Patch function - Patch data 7 High      | PFDH7                        |                               | R/W    |
| 0003E0 <sub>H</sub> -0003F0 <sub>H</sub> | Reserved                                       |                              |                               | -      |
| 0003F1 <sub>H</sub>                      | Memory Control Status Register A               | MCSRA                        |                               | R/W    |
| 0003F2 <sub>H</sub>                      | Memory Timing Configuration Register A Low     | MTCRAL                       | MTCRA                         | R/W    |
| 0003F3 <sub>H</sub>                      | Memory Timing Configuration Register A High    | MTCRAH                       |                               | R/W    |
| 0003F4 <sub>H</sub> -0003F8 <sub>H</sub> | Reserved                                       |                              |                               | -      |
| 0003F9 <sub>H</sub>                      | Flash Memory Write Control register 1          | FMWC1                        |                               | R/W    |
| 0003FA <sub>H</sub>                      | Flash Memory Write Control register 2          | FMWC2                        |                               | R/W    |
| 0003FB <sub>H</sub>                      | Flash Memory Write Control register 3          | FMWC3                        |                               | R/W    |
| 0003FC <sub>H</sub>                      | Flash Memory Write Control register 4          | FMWC4                        |                               | R/W    |
| 0003FD <sub>H</sub>                      | Flash Memory Write Control register 5          | FMWC5                        |                               | R/W    |
| 0003FE <sub>H</sub> -0003FF <sub>H</sub> | Reserved                                       |                              |                               | -      |
| 000400 <sub>H</sub>                      | Standby Mode control register                  | SMCR                         |                               | R/W    |
| 000401 <sub>H</sub>                      | Clock select register                          | CKSR                         |                               | R/W    |
| 000402 <sub>H</sub>                      | Clock Stabilization select register            | CKSSR                        |                               | R/W    |
| 000403 <sub>H</sub>                      | Clock monitor register                         | CKMR                         |                               | R      |
| 000404 <sub>H</sub>                      | Clock Frequency control register Low           | CKFCRL                       | CKFCR                         | R/W    |
| 000405 <sub>H</sub>                      | Clock Frequency control register High          | CKFCRH                       |                               | R/W    |
| 000406 <sub>H</sub>                      | PLL Control register Low                       | PLLCRL                       | PLLCR                         | R/W    |
| 000407 <sub>H</sub>                      | PLL Control register High                      | PLLCRH                       |                               | R/W    |
| 000408 <sub>H</sub>                      | RC clock timer control register                | RCTCR                        |                               | R/W    |
| 000409 <sub>H</sub>                      | Main clock timer control register              | MCTCR                        |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (9 / 21)**

| Address                                  | Register                                                  | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|-----------------------------------------------------------|------------------------------|-------------------------------|--------|
| 00040A <sub>H</sub>                      | Sub clock timer control register                          | SCTCR                        |                               | R/W    |
| 00040B <sub>H</sub>                      | Reset cause and clock status register with clear function | RCCSRC                       |                               | R      |
| 00040C <sub>H</sub>                      | Reset configuration register                              | RCR                          |                               | R/W    |
| 00040D <sub>H</sub>                      | Reset cause and clock status register                     | RCCSR                        |                               | R      |
| 00040E <sub>H</sub>                      | Watch dog timer configuration register                    | WDTC                         |                               | R/W    |
| 00040F <sub>H</sub>                      | Watch dog timer clear pattern register                    | WDTCP                        |                               | W      |
| 000410 <sub>H</sub> -000414 <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000415 <sub>H</sub>                      | Clock output activation register                          | COAR                         |                               | R/W    |
| 000416 <sub>H</sub>                      | Clock output configuration register 0                     | COCR0                        |                               | R/W    |
| 000417 <sub>H</sub>                      | Clock output configuration register 1                     | COCR1                        |                               | R/W    |
| 000418 <sub>H</sub>                      | Clock Modulator control register                          | CMCR                         |                               | R/W    |
| 000419 <sub>H</sub>                      | Reserved                                                  |                              |                               | -      |
| 00041A <sub>H</sub>                      | Clock Modulator Parameter register Low                    | CMPL                         | CMPL                          | R/W    |
| 00041B <sub>H</sub>                      | Clock Modulator Parameter register High                   | CMPLH                        |                               | R/W    |
| 00041C <sub>H</sub> -00042B <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 00042C <sub>H</sub>                      | Voltage Regulator Control register                        | VRCR                         |                               | R/W    |
| 00042D <sub>H</sub>                      | Clock Input and LVD Control Register                      | CILCR                        |                               | R/W    |
| 00042E <sub>H</sub> -00042F <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000430 <sub>H</sub>                      | I/O Port P00 - Data Direction Register                    | DDR00                        |                               | R/W    |
| 000431 <sub>H</sub>                      | I/O Port P01 - Data Direction Register                    | DDR01                        |                               | R/W    |
| 000432 <sub>H</sub>                      | I/O Port P02 - Data Direction Register                    | DDR02                        |                               | R/W    |
| 000433 <sub>H</sub>                      | I/O Port P03 - Data Direction Register                    | DDR03                        |                               | R/W    |
| 000434 <sub>H</sub>                      | I/O Port P04 - Data Direction Register                    | DDR04                        |                               | R/W    |
| 000435 <sub>H</sub>                      | I/O Port P05 - Data Direction Register                    | DDR05                        |                               | R/W    |
| 000436 <sub>H</sub>                      | I/O Port P06 - Data Direction Register                    | DDR06                        |                               | R/W    |
| 000437 <sub>H</sub> -000443 <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000444 <sub>H</sub>                      | I/O Port P00 - Port Input Enable Register                 | PIER00                       |                               | R/W    |
| 000445 <sub>H</sub>                      | I/O Port P01 - Port Input Enable Register                 | PIER01                       |                               | R/W    |
| 000446 <sub>H</sub>                      | I/O Port P02 - Port Input Enable Register                 | PIER02                       |                               | R/W    |
| 000447 <sub>H</sub>                      | I/O Port P03 - Port Input Enable Register                 | PIER03                       |                               | R/W    |
| 000448 <sub>H</sub>                      | I/O Port P04 - Port Input Enable Register                 | PIER04                       |                               | R/W    |
| 000449 <sub>H</sub>                      | I/O Port P05 - Port Input Enable Register                 | PIER05                       |                               | R/W    |
| 00044A <sub>H</sub>                      | I/O Port P06 - Port Input Enable Register                 | PIER06                       |                               | R/W    |
| 00044B <sub>H</sub> -000457 <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000458 <sub>H</sub>                      | I/O Port P00 - Port Input Level Register                  | PILR00                       |                               | R/W    |
| 000459 <sub>H</sub>                      | I/O Port P01 - Port Input Level Register                  | PILR01                       |                               | R/W    |
| 00045A <sub>H</sub>                      | I/O Port P02 - Port Input Level Register                  | PILR02                       |                               | R/W    |
| 00045B <sub>H</sub>                      | I/O Port P03 - Port Input Level Register                  | PILR03                       |                               | R/W    |
| 00045C <sub>H</sub>                      | I/O Port P04 - Port Input Level Register                  | PILR04                       |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (10 / 21)**

| Address                                  | Register                                          | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|---------------------------------------------------|------------------------------|-------------------------------|--------|
| 00045D <sub>H</sub>                      | I/O Port P05 - Port Input Level Register          | PILR05                       |                               | R/W    |
| 00045E <sub>H</sub>                      | I/O Port P06 - Port Input Level Register          | PILR06                       |                               | R/W    |
| 00045F <sub>H</sub> -00046B <sub>H</sub> | Reserved                                          |                              |                               | -      |
| 00046C <sub>H</sub>                      | I/O Port P00 - Extended Port Input Level Register | EPILR00                      |                               | R/W    |
| 00046D <sub>H</sub>                      | I/O Port P01 - Extended Port Input Level Register | EPILR01                      |                               | R/W    |
| 00046E <sub>H</sub>                      | I/O Port P02 - Extended Port Input Level Register | EPILR02                      |                               | R/W    |
| 00046F <sub>H</sub>                      | I/O Port P03 - Extended Port Input Level Register | EPILR03                      |                               | R/W    |
| 000470 <sub>H</sub>                      | I/O Port P04 - Extended Port Input Level Register | EPILR04                      |                               | R/W    |
| 000471 <sub>H</sub>                      | I/O Port P05 - Extended Port Input Level Register | EPILR05                      |                               | R/W    |
| 000472 <sub>H</sub>                      | I/O Port P06 - Extended Port Input Level Register | EPILR06                      |                               | R/W    |
| 000473 <sub>H</sub> -00047F <sub>H</sub> | Reserved                                          |                              |                               | -      |
| 000480 <sub>H</sub>                      | I/O Port P00 - Port Output Drive Register         | PODR00                       |                               | R/W    |
| 000481 <sub>H</sub>                      | I/O Port P01 - Port Output Drive Register         | PODR01                       |                               | R/W    |
| 000482 <sub>H</sub>                      | I/O Port P02 - Port Output Drive Register         | PODR02                       |                               | R/W    |
| 000483 <sub>H</sub>                      | I/O Port P03 - Port Output Drive Register         | PODR03                       |                               | R/W    |
| 000484 <sub>H</sub>                      | I/O Port P04 - Port Output Drive Register         | PODR04                       |                               | R/W    |
| 000485 <sub>H</sub>                      | I/O Port P05 - Port Output Drive Register         | PODR05                       |                               | R/W    |
| 000486 <sub>H</sub>                      | I/O Port P06 - Port Output Drive Register         | PODR06                       |                               | R/W    |
| 000487 <sub>H</sub> -0004A7 <sub>H</sub> | Reserved                                          |                              |                               | -      |
| 0004A8 <sub>H</sub>                      | I/O Port P00 - Pull-Up resistor Control Register  | PUCR00                       |                               | R/W    |
| 0004A9 <sub>H</sub>                      | I/O Port P01 - Pull-Up resistor Control Register  | PUCR01                       |                               | R/W    |
| 0004AA <sub>H</sub>                      | I/O Port P02 - Pull-Up resistor Control Register  | PUCR02                       |                               | R/W    |
| 0004AB <sub>H</sub>                      | I/O Port P03 - Pull-Up resistor Control Register  | PUCR03                       |                               | R/W    |
| 0004AC <sub>H</sub>                      | I/O Port P04 - Pull-Up resistor Control Register  | PUCR04                       |                               | R/W    |
| 0004AD <sub>H</sub>                      | I/O Port P05 - Pull-Up resistor Control Register  | PUCR05                       |                               | R/W    |
| 0004AE <sub>H</sub>                      | I/O Port P06 - Pull-Up resistor Control Register  | PUCR06                       |                               | R/W    |
| 0004AF <sub>H</sub> -0004BB <sub>H</sub> | Reserved                                          |                              |                               | -      |
| 0004BC <sub>H</sub>                      | I/O Port P00 - External Pin State Register        | EPSR00                       |                               | R      |
| 0004BD <sub>H</sub>                      | I/O Port P01 - External Pin State Register        | EPSR01                       |                               | R      |
| 0004BE <sub>H</sub>                      | I/O Port P02 - External Pin State Register        | EPSR02                       |                               | R      |
| 0004BF <sub>H</sub>                      | I/O Port P03 - External Pin State Register        | EPSR03                       |                               | R      |
| 0004C0 <sub>H</sub>                      | I/O Port P04 - External Pin State Register        | EPSR04                       |                               | R      |
| 0004C1 <sub>H</sub>                      | I/O Port P05 - External Pin State Register        | EPSR05                       |                               | R      |
| 0004C2 <sub>H</sub>                      | I/O Port P06 - External Pin State Register        | EPSR06                       |                               | R      |
| 0004C3 <sub>H</sub> -0004CF <sub>H</sub> | Reserved                                          |                              |                               | -      |
| 0004D0 <sub>H</sub>                      | ADC analog input enable register 0                | ADER0                        |                               | R/W    |
| 0004D1 <sub>H</sub>                      | ADC analog input enable register 1                | ADER1                        |                               | R/W    |
| 0004D2 <sub>H</sub>                      | ADC analog input enable register 2                | ADER2                        |                               | R/W    |
| 0004D3 <sub>H</sub>                      | ADC analog input enable register 3                | ADER3                        |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (11 / 21)**

| Address                                  | Register                                                  | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|-----------------------------------------------------------|------------------------------|-------------------------------|--------|
| 0004D4 <sub>H</sub>                      | ADC analog input enable register 4                        | ADER4                        |                               | R/W    |
| 0004D5 <sub>H</sub>                      | Reserved                                                  |                              |                               | -      |
| 0004D6 <sub>H</sub>                      | Peripheral Resource Relocation Register 0                 | PRRR0                        |                               | R/W    |
| 0004D7 <sub>H</sub>                      | Peripheral Resource Relocation Register 1                 | PRRR1                        |                               | R/W    |
| 0004D8 <sub>H</sub>                      | Peripheral Resource Relocation Register 2                 | PRRR2                        |                               | R/W    |
| 0004D9 <sub>H</sub>                      | Peripheral Resource Relocation Register 3                 | PRRR3                        |                               | R/W    |
| 0004DA <sub>H</sub>                      | Peripheral Resource Relocation Register 4                 | PRRR4                        |                               | R/W    |
| 0004DB <sub>H</sub>                      | Peripheral Resource Relocation Register 5                 | PRRR5                        |                               | R/W    |
| 0004DC <sub>H</sub>                      | Peripheral Resource Relocation Register 6                 | PRRR6                        |                               | R/W    |
| 0004DD <sub>H</sub>                      | Peripheral Resource Relocation Register 7                 | PRRR7                        |                               | R/W    |
| 0004DE <sub>H</sub>                      | Peripheral Resource Relocation Register 8                 | PRRR8                        |                               | R/W    |
| 0004DF <sub>H</sub>                      | Peripheral Resource Relocation Register 9                 | PRRR9                        |                               | R/W    |
| 0004E0 <sub>H</sub>                      | RTC - Sub Second Register L                               | WTBRL0                       | WTBR0                         | R/W    |
| 0004E1 <sub>H</sub>                      | RTC - Sub Second Register M                               | WTBRH0                       |                               | R/W    |
| 0004E2 <sub>H</sub>                      | RTC - Sub-Second Register H                               | WTBR1                        |                               | R/W    |
| 0004E3 <sub>H</sub>                      | RTC - Second Register                                     | WTSR                         |                               | R/W    |
| 0004E4 <sub>H</sub>                      | RTC - Minutes                                             | WTMR                         |                               | R/W    |
| 0004E5 <sub>H</sub>                      | RTC - Hour                                                | WTHR                         |                               | R/W    |
| 0004E6 <sub>H</sub>                      | RTC - Timer Control Extended Register                     | WTCEER                       |                               | R/W    |
| 0004E7 <sub>H</sub>                      | RTC - Clock select register                               | WTCKSR                       |                               | R/W    |
| 0004E8 <sub>H</sub>                      | RTC - Timer Control Register Low                          | WTCRL                        | WTCR                          | R/W    |
| 0004E9 <sub>H</sub>                      | RTC - Timer Control Register High                         | WTCRH                        |                               | R/W    |
| 0004EA <sub>H</sub>                      | CAL - Calibration unit Control register                   | CUCR                         |                               | R/W    |
| 0004EB <sub>H</sub>                      | Reserved                                                  |                              |                               | -      |
| 0004EC <sub>H</sub>                      | CAL - Duration Timer Data Register Low                    | CUTDL                        | CUTD                          | R/W    |
| 0004ED <sub>H</sub>                      | CAL - Duration Timer Data Register High                   | CUTDH                        |                               | R/W    |
| 0004EE <sub>H</sub>                      | CAL - Calibration Timer Register 2 Low                    | CUTR2L                       | CUTR2                         | R      |
| 0004EF <sub>H</sub>                      | CAL - Calibration Timer Register 2 High                   | CUTR2H                       |                               | R      |
| 0004F0 <sub>H</sub>                      | CAL - Calibration Timer Register 1 Low                    | CUTR1L                       | CUTR1                         | R      |
| 0004F1 <sub>H</sub>                      | CAL - Calibration Timer Register 1 High                   | CUTR1H                       |                               | R      |
| 0004F2 <sub>H</sub> -0004F9 <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 0004FA <sub>H</sub>                      | RLT - Timer input select (for Cascading)                  | TMISR                        |                               | R/W    |
| 0004FB <sub>H</sub> -0004FF <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000500 <sub>H</sub>                      | FRT2 - Data register of free-running timer                |                              | TCDT2                         | R/W    |
| 000501 <sub>H</sub>                      | FRT2 - Data register of free-running timer                |                              |                               | R/W    |
| 000502 <sub>H</sub>                      | FRT2 - Control status register of free-running timer Low  | TCCSL2                       | TCCS2                         | R/W    |
| 000503 <sub>H</sub>                      | FRT2 - Control status register of free-running timer High | TCCSH2                       |                               | R/W    |
| 000504 <sub>H</sub>                      | FRT3 - Data register of free-running timer                |                              | TCDT3                         | R/W    |
| 000505 <sub>H</sub>                      | FRT3 - Data register of free-running timer                |                              |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (12 / 21)**

| Address                                  | Register                                                  | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|-----------------------------------------------------------|------------------------------|-------------------------------|--------|
| 000506 <sub>H</sub>                      | FRT3 - Control status register of free-running timer Low  | TCCSL3                       | TCCS3                         | R/W    |
| 000507 <sub>H</sub>                      | FRT3 - Control status register of free-running timer High | TCCSH3                       |                               | R/W    |
| 000508 <sub>H</sub> -000513 <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000514 <sub>H</sub>                      | ICU8/ICU9 - Control Status Register                       | ICS89                        |                               | R/W    |
| 000515 <sub>H</sub>                      | ICU8/ICU9 - Edge Register                                 | ICE89                        |                               | R/W    |
| 000516 <sub>H</sub>                      | ICU8 - Capture Register Low                               | IPCPL8                       | IPCP8                         | R      |
| 000517 <sub>H</sub>                      | ICU8 - Capture Register High                              | ICPH8                        |                               | R      |
| 000518 <sub>H</sub>                      | ICU9 - Capture Register Low                               | IPCPL9                       | IPCP9                         | R      |
| 000519 <sub>H</sub>                      | ICU9 - Capture Register High                              | ICPH9                        |                               | R      |
| 00051A <sub>H</sub>                      | ICU10/ICU11 - Control Status Register                     | ICS1011                      |                               | R/W    |
| 00051B <sub>H</sub>                      | ICU10/ICU11 - Edge Register                               | ICE1011                      |                               | R/W    |
| 00051C <sub>H</sub>                      | ICU10 - Capture Register Low                              | IPCPL10                      | IPCP10                        | R      |
| 00051D <sub>H</sub>                      | ICU10 - Capture Register High                             | ICPH10                       |                               | R      |
| 00051E <sub>H</sub>                      | ICU11 - Capture Register Low                              | IPCPL11                      | IPCP11                        | R      |
| 00051F <sub>H</sub>                      | ICU11 - Capture Register High                             | ICPH11                       |                               | R      |
| 000520 <sub>H</sub> -00053D <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 00053E <sub>H</sub>                      | USART7 - Serial Mode Register                             | SMR7                         |                               | R/W    |
| 00053F <sub>H</sub>                      | USART7 - Serial Control Register                          | SCR7                         |                               | R/W    |
| 000540 <sub>H</sub>                      | USART7 - Serial TX Register                               | TDR7                         |                               | W      |
| 000540 <sub>H</sub>                      | USART7 - Serial RX Register                               | RDR7                         |                               | R      |
| 000541 <sub>H</sub>                      | USART7 - Serial Status Register                           | SSR7                         |                               | R/W    |
| 000542 <sub>H</sub>                      | USART7 - Ext. Control/Com. Register                       | ECCR7                        |                               | R/W    |
| 000543 <sub>H</sub>                      | USART7 - Ext. Status Com. Register                        | ESCR7                        |                               | R/W    |
| 000544 <sub>H</sub>                      | USART7 - Baud Rate Generator Register Low                 | BGRL7                        | BGR7                          | R/W    |
| 000545 <sub>H</sub>                      | USART7 - Baud Rate Generator Register High                | BGRH7                        |                               | R/W    |
| 000546 <sub>H</sub>                      | USART7 - Extended Serial Interrupt Register               | ESIR7                        |                               | R/W    |
| 000547 <sub>H</sub>                      | Reserved                                                  |                              |                               | -      |
| 000548 <sub>H</sub>                      | USART8 - Serial Mode Register                             | SMR8                         |                               | R/W    |
| 000549 <sub>H</sub>                      | USART8 - Serial Control Register                          | SCR8                         |                               | R/W    |
| 00054A <sub>H</sub>                      | USART8 - Serial TX Register                               | TDR8                         |                               | W      |
| 00054A <sub>H</sub>                      | USART8 - Serial RX Register                               | RDR8                         |                               | R      |
| 00054B <sub>H</sub>                      | USART8 - Serial Status Register                           | SSR8                         |                               | R/W    |
| 00054C <sub>H</sub>                      | USART8 - Ext. Control/Com. Register                       | ECCR8                        |                               | R/W    |
| 00054D <sub>H</sub>                      | USART8 - Ext. Status Com. Register                        | ESCR8                        |                               | R/W    |
| 00054E <sub>H</sub>                      | USART8 - Baud Rate Generator Register Low                 | BGRL8                        | BGR8                          | R/W    |
| 00054F <sub>H</sub>                      | USART8 - Baud Rate Generator Register High                | BGRH8                        |                               | R/W    |
| 000550 <sub>H</sub>                      | USART8 - Extended Serial Interrupt Register               | ESIR8                        |                               | R/W    |
| 000551 <sub>H</sub> -000563 <sub>H</sub> | Reserved                                                  |                              |                               | -      |
| 000564 <sub>H</sub>                      | PPG6 - Timer register                                     |                              | PTMR6                         | R      |

**Table 4. I/O Map CY96(F)35x (13 / 21)**

| Address             | Register                                     | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|---------------------|----------------------------------------------|------------------------------|-------------------------------|--------|
| 000565 <sub>H</sub> | PPG6 - Timer register                        |                              |                               | R      |
| 000566 <sub>H</sub> | PPG6 - Period setting register               |                              | PCSR6                         | W      |
| 000567 <sub>H</sub> | PPG6 - Period setting register               |                              |                               | W      |
| 000568 <sub>H</sub> | PPG6 - Duty cycle register                   |                              | PDUT6                         | W      |
| 000569 <sub>H</sub> | PPG6 - Duty cycle register                   |                              |                               | W      |
| 00056A <sub>H</sub> | PPG6 - Control status register Low           | PCNL6                        | PCN6                          | R/W    |
| 00056B <sub>H</sub> | PPG6 - Control status register High          | PCNH6                        |                               | R/W    |
| 00056C <sub>H</sub> | PPG7 - Timer register                        |                              | PTMR7                         | R      |
| 00056D <sub>H</sub> | PPG7 - Timer register                        |                              |                               | R      |
| 00056E <sub>H</sub> | PPG7 - Period setting register               |                              | PCSR7                         | W      |
| 00056F <sub>H</sub> | PPG7 - Period setting register               |                              |                               | W      |
| 000570 <sub>H</sub> | PPG7 - Duty cycle register                   |                              | PDUT7                         | W      |
| 000571 <sub>H</sub> | PPG7 - Duty cycle register                   |                              |                               | W      |
| 000572 <sub>H</sub> | PPG7 - Control status register Low           | PCNL7                        | PCN7                          | R/W    |
| 000573 <sub>H</sub> | PPG7 - Control status register High          | PCNH7                        |                               | R/W    |
| 000574 <sub>H</sub> | PPG11-PPG8 - General Control register 1 Low  | GCN1L2                       | GCN12                         | R/W    |
| 000575 <sub>H</sub> | PPG11-PPG8 - General Control register 1 High | GCN1H2                       |                               | R/W    |
| 000576 <sub>H</sub> | PPG11-PPG8 - General Control register 2 Low  | GCN2L2                       | GCN22                         | R/W    |
| 000577 <sub>H</sub> | PPG11-PPG8 - General Control register 2 High | GCN2H2                       |                               | R/W    |
| 000578 <sub>H</sub> | PPG8 - Timer register                        |                              | PTMR8                         | R      |
| 000579 <sub>H</sub> | PPG8 - Timer register                        |                              |                               | R      |
| 00057A <sub>H</sub> | PPG8 - Period setting register               |                              | PCSR8                         | W      |
| 00057B <sub>H</sub> | PPG8 - Period setting register               |                              |                               | W      |
| 00057C <sub>H</sub> | PPG8 - Duty cycle register                   |                              | PDUT8                         | W      |
| 00057D <sub>H</sub> | PPG8 - Duty cycle register                   |                              |                               | W      |
| 00057E <sub>H</sub> | PPG8 - Control status register Low           | PCNL8                        | PCN8                          | R/W    |
| 00057F <sub>H</sub> | PPG8 - Control status register High          | PCNH8                        |                               | R/W    |
| 000580 <sub>H</sub> | PPG9 - Timer register                        |                              | PTMR9                         | R      |
| 000581 <sub>H</sub> | PPG9 - Timer register                        |                              |                               | R      |
| 000582 <sub>H</sub> | PPG9 - Period setting register               |                              | PCSR9                         | W      |
| 000583 <sub>H</sub> | PPG9 - Period setting register               |                              |                               | W      |
| 000584 <sub>H</sub> | PPG9 - Duty cycle register                   |                              | PDUT9                         | W      |
| 000585 <sub>H</sub> | PPG9 - Duty cycle register                   |                              |                               | W      |
| 000586 <sub>H</sub> | PPG9 - Control status register Low           | PCNL9                        | PCN9                          | R/W    |
| 000587 <sub>H</sub> | PPG9 - Control status register High          | PCNH9                        |                               | R/W    |
| 000588 <sub>H</sub> | PPG10 - Timer register                       |                              | PTMR10                        | R      |
| 000589 <sub>H</sub> | PPG10 - Timer register                       |                              |                               | R      |
| 00058A <sub>H</sub> | PPG10 - Period setting register              |                              | PCSR10                        | W      |
| 00058B <sub>H</sub> | PPG10 - Period setting register              |                              |                               | W      |

**Table 4. I/O Map CY96(F)35x (14 / 21)**

| Address             | Register                                      | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|---------------------|-----------------------------------------------|------------------------------|-------------------------------|--------|
| 00058C <sub>H</sub> | PPG10 - Duty cycle register                   |                              | PDUT10                        | W      |
| 00058D <sub>H</sub> | PPG10 - Duty cycle register                   |                              |                               | W      |
| 00058E <sub>H</sub> | PPG10 - Control status register Low           | PCNL10                       | PCN10                         | R/W    |
| 00058F <sub>H</sub> | PPG10 - Control status register High          | PCNH10                       |                               | R/W    |
| 000590 <sub>H</sub> | PPG11 - Timer register                        |                              | PTMR11                        | R      |
| 000591 <sub>H</sub> | PPG11 - Timer register                        |                              |                               | R      |
| 000592 <sub>H</sub> | PPG11 - Period setting register               |                              | PCSR11                        | W      |
| 000593 <sub>H</sub> | PPG11 - Period setting register               |                              |                               | W      |
| 000594 <sub>H</sub> | PPG11 - Duty cycle register                   |                              | PDUT11                        | W      |
| 000595 <sub>H</sub> | PPG11 - Duty cycle register                   |                              |                               | W      |
| 000596 <sub>H</sub> | PPG11 - Control status register Low           | PCNL11                       | PCN11                         | R/W    |
| 000597 <sub>H</sub> | PPG11 - Control status register High          | PCNH11                       |                               | R/W    |
| 000598 <sub>H</sub> | PPG15-PPG12 - General Control register 1 Low  | GCN1L3                       | GCN13                         | R/W    |
| 000599 <sub>H</sub> | PPG15-PPG12 - General Control register 1 High | GCN1H3                       |                               | R/W    |
| 00059A <sub>H</sub> | PPG15-PPG12 - General Control register 2 Low  | GCN2L3                       | GCN23                         | R/W    |
| 00059B <sub>H</sub> | PPG15-PPG12 - General Control register 2 High | GCN2H3                       |                               | R/W    |
| 00059C <sub>H</sub> | PPG12 - Timer register                        |                              | PTMR12                        | R      |
| 00059D <sub>H</sub> | PPG12 - Timer register                        |                              |                               | R      |
| 00059E <sub>H</sub> | PPG12 - Period setting register               |                              | PCSR12                        | W      |
| 00059F <sub>H</sub> | PPG12 - Period setting register               |                              |                               | W      |
| 0005A0 <sub>H</sub> | PPG12 - Duty cycle register                   |                              | PDUT12                        | W      |
| 0005A1 <sub>H</sub> | PPG12 - Duty cycle register                   |                              |                               | W      |
| 0005A2 <sub>H</sub> | PPG12 - Control status register Low           | PCNL12                       | PCN12                         | R/W    |
| 0005A3 <sub>H</sub> | PPG12 - Control status register High          | PCNH12                       |                               | R/W    |
| 0005A4 <sub>H</sub> | PPG13 - Timer register                        |                              | PTMR13                        | R      |
| 0005A5 <sub>H</sub> | PPG13 - Timer register                        |                              |                               | R      |
| 0005A6 <sub>H</sub> | PPG13 - Period setting register               |                              | PCSR13                        | W      |
| 0005A7 <sub>H</sub> | PPG13 - Period setting register               |                              |                               | W      |
| 0005A8 <sub>H</sub> | PPG13 - Duty cycle register                   |                              | PDUT13                        | W      |
| 0005A9 <sub>H</sub> | PPG13 - Duty cycle register                   |                              |                               | W      |
| 0005AA <sub>H</sub> | PPG13 - Control status register Low           | PCNL13                       | PCN13                         | R/W    |
| 0005AB <sub>H</sub> | PPG13 - Control status register High          | PCNH13                       |                               | R/W    |
| 0005AC <sub>H</sub> | PPG14 - Timer register                        |                              | PTMR14                        | R      |
| 0005AD <sub>H</sub> | PPG14 - Timer register                        |                              |                               | R      |
| 0005AE <sub>H</sub> | PPG14 - Period setting register               |                              | PCSR14                        | W      |
| 0005AF <sub>H</sub> | PPG14 - Period setting register               |                              |                               | W      |
| 0005B0 <sub>H</sub> | PPG14 - Duty cycle register                   |                              | PDUT14                        | W      |
| 0005B1 <sub>H</sub> | PPG14 - Duty cycle register                   |                              |                               | W      |
| 0005B2 <sub>H</sub> | PPG14 - Control status register Low           | PCNL14                       | PCN14                         | R/W    |

**Table 4. I/O Map CY96(F)35x (15 / 21)**

| Address             | Register                                      | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|---------------------|-----------------------------------------------|------------------------------|-------------------------------|--------|
| 0005B3 <sub>H</sub> | PPG14 - Control status register High          | PCNH14                       |                               | R/W    |
| 0005B4 <sub>H</sub> | PPG15 - Timer register                        |                              | PTMR15                        | R      |
| 0005B5 <sub>H</sub> | PPG15 - Timer register                        |                              |                               | R      |
| 0005B6 <sub>H</sub> | PPG15 - Period setting register               |                              | PCSR15                        | W      |
| 0005B7 <sub>H</sub> | PPG15 - Period setting register               |                              |                               | W      |
| 0005B8 <sub>H</sub> | PPG15 - Duty cycle register                   |                              | PDUT15                        | W      |
| 0005B9 <sub>H</sub> | PPG15 - Duty cycle register                   |                              |                               | W      |
| 0005BA <sub>H</sub> | PPG15 - Control status register Low           | PCNL15                       | PCN15                         | R/W    |
| 0005BB <sub>H</sub> | PPG15 - Control status register High          | PCNH15                       |                               | R/W    |
| 0005BC <sub>H</sub> | PPG19-PPG16 - General Control register 1 Low  | GCN1L4                       | GCN14                         | R/W    |
| 0005BD <sub>H</sub> | PPG19-PPG16 - General Control register 1 High | GCN1H4                       |                               | R/W    |
| 0005BE <sub>H</sub> | PPG19-PPG16 - General Control register 2 Low  | GCN2L4                       | GCN24                         | R/W    |
| 0005BF <sub>H</sub> | PPG19-PPG16 - General Control register 2 High | GCN2H4                       |                               | R/W    |
| 0005C0 <sub>H</sub> | PPG16 - Timer register                        |                              | PTMR16                        | R      |
| 0005C1 <sub>H</sub> | PPG16 - Timer register                        |                              |                               | R      |
| 0005C2 <sub>H</sub> | PPG16 - Period setting register               |                              | PCSR16                        | W      |
| 0005C3 <sub>H</sub> | PPG16 - Period setting register               |                              |                               | W      |
| 0005C4 <sub>H</sub> | PPG16 - Duty cycle register                   |                              | PDUT16                        | W      |
| 0005C5 <sub>H</sub> | PPG16 - Duty cycle register                   |                              |                               | W      |
| 0005C6 <sub>H</sub> | PPG16 - Control status register Low           | PCNL16                       | PCN16                         | R/W    |
| 0005C7 <sub>H</sub> | PPG16 - Control status register High          | PCNH16                       |                               | R/W    |
| 0005C8 <sub>H</sub> | PPG17 - Timer register                        |                              | PTMR17                        | R      |
| 0005C9 <sub>H</sub> | PPG17 - Timer register                        |                              |                               | R      |
| 0005CA <sub>H</sub> | PPG17 - Period setting register               |                              | PCSR17                        | W      |
| 0005CB <sub>H</sub> | PPG17 - Period setting register               |                              |                               | W      |
| 0005CC <sub>H</sub> | PPG17 - Duty cycle register                   |                              | PDUT17                        | W      |
| 0005CD <sub>H</sub> | PPG17 - Duty cycle register                   |                              |                               | W      |
| 0005CE <sub>H</sub> | PPG17 - Control status register Low           | PCNL17                       | PCN17                         | R/W    |
| 0005CF <sub>H</sub> | PPG17 - Control status register High          | PCNH17                       |                               | R/W    |
| 0005D0 <sub>H</sub> | PPG18 - Timer register                        |                              | PTMR18                        | R      |
| 0005D1 <sub>H</sub> | PPG18 - Timer register                        |                              |                               | R      |
| 0005D2 <sub>H</sub> | PPG18 - Period setting register               |                              | PCSR18                        | W      |
| 0005D3 <sub>H</sub> | PPG18 - Period setting register               |                              |                               | W      |
| 0005D4 <sub>H</sub> | PPG18 - Duty cycle register                   |                              | PDUT18                        | W      |
| 0005D5 <sub>H</sub> | PPG18 - Duty cycle register                   |                              |                               | W      |
| 0005D6 <sub>H</sub> | PPG18 - Control status register Low           | PCNL18                       | PCN18                         | R/W    |
| 0005D7 <sub>H</sub> | PPG18 - Control status register High          | PCNH18                       |                               | R/W    |
| 0005D8 <sub>H</sub> | PPG19 - Timer register                        |                              | PTMR19                        | R      |
| 0005D9 <sub>H</sub> | PPG19 - Timer register                        |                              |                               | R      |

**Table 4. I/O Map CY96(F)35x (16 / 21)**

| Address                                  | Register                                          | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|---------------------------------------------------|------------------------------|-------------------------------|--------|
| 0005DA <sub>H</sub>                      | PPG19 - Period setting register                   |                              | PCSR19                        | W      |
| 0005DB <sub>H</sub>                      | PPG19 - Period setting register                   |                              |                               | W      |
| 0005DC <sub>H</sub>                      | PPG19 - Duty cycle register                       |                              | PDUT19                        | W      |
| 0005DD <sub>H</sub>                      | PPG19 - Duty cycle register                       |                              |                               | W      |
| 0005DE <sub>H</sub>                      | PPG19 - Control status register Low               | PCNL19                       | PCN19                         | R/W    |
| 0005DF <sub>H</sub>                      | PPG19 - Control status register High              | PCNH19                       |                               | R/W    |
| 0005E0 <sub>H</sub> -00065F <sub>H</sub> | Reserved                                          |                              |                               | -      |
| 000660 <sub>H</sub>                      | Peripheral Resource Relocation Register 10        | PRRR10                       |                               | R/W    |
| 000661 <sub>H</sub>                      | Peripheral Resource Relocation Register 11        | PRRR11                       |                               | R/W    |
| 000662 <sub>H</sub>                      | Peripheral Resource Relocation Register 12        | PRRR12                       |                               | R/W    |
| 000663 <sub>H</sub>                      | Peripheral Resource Relocation Register 13        | PRRR13                       |                               | W      |
| 000664 <sub>H</sub> -0006DF <sub>H</sub> | Reserved                                          |                              |                               | -      |
| 0006E0 <sub>H</sub>                      | External Bus - Area configuration register 0 Low  | EACL0                        | EAC0                          | R/W    |
| 0006E1 <sub>H</sub>                      | External Bus - Area configuration register 0 High | EACH0                        |                               | R/W    |
| 0006E2 <sub>H</sub>                      | External Bus - Area configuration register 1 Low  | EACL1                        | EAC1                          | R/W    |
| 0006E3 <sub>H</sub>                      | External Bus - Area configuration register 1 High | EACH1                        |                               | R/W    |
| 0006E4 <sub>H</sub>                      | External Bus - Area configuration register 2 Low  | EACL2                        | EAC2                          | R/W    |
| 0006E5 <sub>H</sub>                      | External Bus - Area configuration register 2 High | EACH2                        |                               | R/W    |
| 0006E6 <sub>H</sub>                      | External Bus - Area configuration register 3 Low  | EACL3                        | EAC3                          | R/W    |
| 0006E7 <sub>H</sub>                      | External Bus - Area configuration register 3 High | EACH3                        |                               | R/W    |
| 0006E8 <sub>H</sub>                      | External Bus - Area configuration register 4 Low  | EACL4                        | EAC4                          | R/W    |
| 0006E9 <sub>H</sub>                      | External Bus - Area configuration register 4 High | EACH4                        |                               | R/W    |
| 0006EA <sub>H</sub>                      | External Bus - Area configuration register 5 Low  | EACL5                        | EAC5                          | R/W    |
| 0006EB <sub>H</sub>                      | External Bus - Area configuration register 5 High | EACH5                        |                               | R/W    |
| 0006EC <sub>H</sub>                      | External Bus - Area select register 2             | EAS2                         |                               | R/W    |
| 0006ED <sub>H</sub>                      | External Bus - Area select register 3             | EAS3                         |                               | R/W    |
| 0006EE <sub>H</sub>                      | External Bus - Area select register 4             | EAS4                         |                               | R/W    |
| 0006EF <sub>H</sub>                      | External Bus - Area select register 5             | EAS5                         |                               | R/W    |
| 0006F0 <sub>H</sub>                      | External Bus - Mode register                      | EBM                          |                               | R/W    |
| 0006F1 <sub>H</sub>                      | External Bus - Clock and Function register        | EBCF                         |                               | R/W    |
| 0006F2 <sub>H</sub>                      | External Bus - Address output enable register 0   | EBAE0                        |                               | R/W    |
| 0006F3 <sub>H</sub>                      | External Bus - Address output enable register 1   | EBAE1                        |                               | R/W    |
| 0006F4 <sub>H</sub>                      | External Bus - Address output enable register 2   | EBAE2                        |                               | R/W    |
| 0006F5 <sub>H</sub>                      | External Bus - Control signal register            | EBCS                         |                               | R/W    |
| 0006F6 <sub>H</sub> -0007FF <sub>H</sub> | Reserved                                          |                              |                               | -      |
| 000800 <sub>H</sub>                      | CAN1 - Control register Low                       | CTRLRL1                      | CTRLR1                        | R/W    |
| 000801 <sub>H</sub>                      | CAN1 - Control register High (reserved)           | CTRLRH1                      |                               | R      |
| 000802 <sub>H</sub>                      | CAN1 - Status register Low                        | STATRL1                      | STATR1                        | R/W    |
| 000803 <sub>H</sub>                      | CAN1 - Status register High (reserved)            | STATRH1                      |                               | R      |

**Table 4. I/O Map CY96(F)35x (17 / 21)**

| Address                                  | Register                                         | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|--------------------------------------------------|------------------------------|-------------------------------|--------|
| 000804 <sub>H</sub>                      | CAN1 - Error Counter Low (Transmit)              | ERRCNTL1                     | ERRCNT1                       | R      |
| 000805 <sub>H</sub>                      | CAN1 - Error Counter High (Receive)              | ERRCNTH1                     |                               | R      |
| 000806 <sub>H</sub>                      | CAN1 - Bit Timing Register Low                   | BTRL1                        | BTR1                          | R/W    |
| 000807 <sub>H</sub>                      | CAN1 - Bit Timing Register High                  | BTRH1                        |                               | R/W    |
| 000808 <sub>H</sub>                      | CAN1 - Interrupt Register Low                    | INTRL1                       | INTR1                         | R      |
| 000809 <sub>H</sub>                      | CAN1 - Interrupt Register High                   | INTRH1                       |                               | R      |
| 00080A <sub>H</sub>                      | CAN1 - Test Register Low                         | TESTRL1                      | TESTR1                        | R/W    |
| 00080B <sub>H</sub>                      | CAN1 - Test Register High (reserved)             | TESTRH1                      |                               | R      |
| 00080C <sub>H</sub>                      | CAN1 - BRP Extension register Low                | BRPERL1                      | BRPER1                        | R/W    |
| 00080D <sub>H</sub>                      | CAN1 - BRP Extension register High (reserved)    | BRPERH1                      |                               | R      |
| 00080E <sub>H</sub> -00080F <sub>H</sub> | Reserved                                         |                              |                               | -      |
| 000810 <sub>H</sub>                      | CAN1 - IF1 Command request register Low          | IF1CREQL1                    | IF1CREQ1                      | R/W    |
| 000811 <sub>H</sub>                      | CAN1 - IF1 Command request register High         | IF1CREQH1                    |                               | R/W    |
| 000812 <sub>H</sub>                      | CAN1 - IF1 Command Mask register Low             | IF1CMSKL1                    | IF1CMSK1                      | R/W    |
| 000813 <sub>H</sub>                      | CAN1 - IF1 Command Mask register High (reserved) | IF1CMSKH1                    |                               | R      |
| 000814 <sub>H</sub>                      | CAN1 - IF1 Mask 1 Register Low                   | IF1MSK1L1                    | IF1MSK11                      | R/W    |
| 000815 <sub>H</sub>                      | CAN1 - IF1 Mask 1 Register High                  | IF1MSK1H1                    |                               | R/W    |
| 000816 <sub>H</sub>                      | CAN1 - IF1 Mask 2 Register Low                   | IF1MSK2L1                    | IF1MSK21                      | R/W    |
| 000817 <sub>H</sub>                      | CAN1 - IF1 Mask 2 Register High                  | IF1MSK2H1                    |                               | R/W    |
| 000818 <sub>H</sub>                      | CAN1 - IF1 Arbitration 1 Register Low            | IF1ARB1L1                    | IF1ARB11                      | R/W    |
| 000819 <sub>H</sub>                      | CAN1 - IF1 Arbitration 1 Register High           | IF1ARB1H1                    |                               | R/W    |
| 00081A <sub>H</sub>                      | CAN1 - IF1 Arbitration 2 Register Low            | IF1ARB2L1                    | IF1ARB21                      | R/W    |
| 00081B <sub>H</sub>                      | CAN1 - IF1 Arbitration 2 Register High           | IF1ARB2H1                    |                               | R/W    |
| 00081C <sub>H</sub>                      | CAN1 - IF1 Message Control Register Low          | IF1MCTRL1                    | IF1MCTR1                      | R/W    |
| 00081D <sub>H</sub>                      | CAN1 - IF1 Message Control Register High         | IF1MCTRH1                    |                               | R/W    |
| 00081E <sub>H</sub>                      | CAN1 - IF1 Data A1 Low                           | IF1DTA1L1                    | IF1DTA11                      | R/W    |
| 00081F <sub>H</sub>                      | CAN1 - IF1 Data A1 High                          | IF1DTA1H1                    |                               | R/W    |
| 000820 <sub>H</sub>                      | CAN1 - IF1 Data A2 Low                           | IF1DTA2L1                    | IF1DTA21                      | R/W    |
| 000821 <sub>H</sub>                      | CAN1 - IF1 Data A2 High                          | IF1DTA2H1                    |                               | R/W    |
| 000822 <sub>H</sub>                      | CAN1 - IF1 Data B1 Low                           | IF1DTB1L1                    | IF1DTB11                      | R/W    |
| 000823 <sub>H</sub>                      | CAN1 - IF1 Data B1 High                          | IF1DTB1H1                    |                               | R/W    |
| 000824 <sub>H</sub>                      | CAN1 - IF1 Data B2 Low                           | IF1DTB2L1                    | IF1DTB21                      | R/W    |
| 000825 <sub>H</sub>                      | CAN1 - IF1 Data B2 High                          | IF1DTB2H1                    |                               | R/W    |
| 000826 <sub>H</sub> -00083F <sub>H</sub> | Reserved                                         |                              |                               | -      |
| 000840 <sub>H</sub>                      | CAN1 - IF2 Command request register Low          | IF2CREQL1                    | IF2CREQ1                      | R/W    |
| 000841 <sub>H</sub>                      | CAN1 - IF2 Command request register High         | IF2CREQH1                    |                               | R/W    |
| 000842 <sub>H</sub>                      | CAN1 - IF2 Command Mask register Low             | IF2CMSKL1                    | IF2CMSK1                      | R/W    |
| 000843 <sub>H</sub>                      | CAN1 - IF2 Command Mask register High (reserved) | IF2CMSKH1                    |                               | R      |
| 000844 <sub>H</sub>                      | CAN1 - IF2 Mask 1 Register Low                   | IF2MSK1L1                    | IF2MSK11                      | R/W    |

**Table 4. I/O Map CY96(F)35x (18 / 21)**

| Address                                  | Register                                    | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|---------------------------------------------|------------------------------|-------------------------------|--------|
| 000845 <sub>H</sub>                      | CAN1 - IF2 Mask 1 Register High             | IF2MSK1H1                    |                               | R/W    |
| 000846 <sub>H</sub>                      | CAN1 - IF2 Mask 2 Register Low              | IF2MSK2L1                    | IF2MSK21                      | R/W    |
| 000847 <sub>H</sub>                      | CAN1 - IF2 Mask 2 Register High             | IF2MSK2H1                    |                               | R/W    |
| 000848 <sub>H</sub>                      | CAN1 - IF2 Arbitration 1 Register Low       | IF2ARB1L1                    | IF2ARB11                      | R/W    |
| 000849 <sub>H</sub>                      | CAN1 - IF2 Arbitration 1 Register High      | IF2ARB1H1                    |                               | R/W    |
| 00084A <sub>H</sub>                      | CAN1 - IF2 Arbitration 2 Register Low       | IF2ARB2L1                    | IF2ARB21                      | R/W    |
| 00084B <sub>H</sub>                      | CAN1 - IF2 Arbitration 2 Register High      | IF2ARB2H1                    |                               | R/W    |
| 00084C <sub>H</sub>                      | CAN1 - IF2 Message Control Register Low     | IF2MCTRL1                    | IF2MCTR1                      | R/W    |
| 00084D <sub>H</sub>                      | CAN1 - IF2 Message Control Register High    | IF2MCTRH1                    |                               | R/W    |
| 00084E <sub>H</sub>                      | CAN1 - IF2 Data A1 Low                      | IF2DTA1L1                    | IF2DTA11                      | R/W    |
| 00084F <sub>H</sub>                      | CAN1 - IF2 Data A1 High                     | IF2DTA1H1                    |                               | R/W    |
| 000850 <sub>H</sub>                      | CAN1 - IF2 Data A2 Low                      | IF2DTA2L1                    | IF2DTA21                      | R/W    |
| 000851 <sub>H</sub>                      | CAN1 - IF2 Data A2 High                     | IF2DTA2H1                    |                               | R/W    |
| 000852 <sub>H</sub>                      | CAN1 - IF2 Data B1 Low                      | IF2DTB1L1                    | IF2DTB11                      | R/W    |
| 000853 <sub>H</sub>                      | CAN1 - IF2 Data B1 High                     | IF2DTB1H1                    |                               | R/W    |
| 000854 <sub>H</sub>                      | CAN1 - IF2 Data B2 Low                      | IF2DTB2L1                    | IF2DTB21                      | R/W    |
| 000855 <sub>H</sub>                      | CAN1 - IF2 Data B2 High                     | IF2DTB2H1                    |                               | R/W    |
| 000856 <sub>H</sub> -00087F <sub>H</sub> | Reserved                                    |                              |                               | -      |
| 000880 <sub>H</sub>                      | CAN1 - Transmission Request 1 Register Low  | TREQR1L1                     | TREQR11                       | R      |
| 000881 <sub>H</sub>                      | CAN1 - Transmission Request 1 Register High | TREQR1H1                     |                               | R      |
| 000882 <sub>H</sub>                      | CAN1 - Transmission Request 2 Register Low  | TREQR2L1                     | TREQR21                       | R      |
| 000883 <sub>H</sub>                      | CAN1 - Transmission Request 2 Register High | TREQR2H1                     |                               | R      |
| 000884 <sub>H</sub> -00088F <sub>H</sub> | Reserved                                    |                              |                               | -      |
| 000890 <sub>H</sub>                      | CAN1 - New Data 1 Register Low              | NEWDT1L1                     | NEWDT11                       | R      |
| 000891 <sub>H</sub>                      | CAN1 - New Data 1 Register High             | NEWDT1H1                     |                               | R      |
| 000892 <sub>H</sub>                      | CAN1 - New Data 2 Register Low              | NEWDT2L1                     | NEWDT21                       | R      |
| 000893 <sub>H</sub>                      | CAN1 - New Data 2 Register High             | NEWDT2H1                     |                               | R      |
| 000894 <sub>H</sub> -00089F <sub>H</sub> | Reserved                                    |                              |                               | -      |
| 0008A0 <sub>H</sub>                      | CAN1 - Interrupt Pending 1 Register Low     | INTPND1L1                    | INTPND11                      | R      |
| 0008A1 <sub>H</sub>                      | CAN1 - Interrupt Pending 1 Register High    | INTPND1H1                    |                               | R      |
| 0008A2 <sub>H</sub>                      | CAN1 - Interrupt Pending 2 Register Low     | INTPND2L1                    | INTPND21                      | R      |
| 0008A3 <sub>H</sub>                      | CAN1 - Interrupt Pending 2 Register High    | INTPND2H1                    |                               | R      |
| 0008A4 <sub>H</sub> -0008AF <sub>H</sub> | Reserved                                    |                              |                               | -      |
| 0008B0 <sub>H</sub>                      | CAN1 - Message Valid 1 Register Low         | MSGVAL1L1                    | MSGVAL11                      | R      |
| 0008B1 <sub>H</sub>                      | CAN1 - Message Valid 1 Register High        | MSGVAL1H1                    |                               | R      |
| 0008B2 <sub>H</sub>                      | CAN1 - Message Valid 2 Register Low         | MSGVAL2L1                    | MSGVAL21                      | R      |
| 0008B3 <sub>H</sub>                      | CAN1 - Message Valid 2 Register High        | MSGVAL2H1                    |                               | R      |
| 0008B4 <sub>H</sub> -0008CD <sub>H</sub> | Reserved                                    |                              |                               | -      |
| 0008CE <sub>H</sub>                      | CAN1 - Output enable register               | COER1                        |                               | R/W    |

**Table 4. I/O Map CY96(F)35x (19 / 21)**

| Address                                  | Register                                         | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|--------------------------------------------------|------------------------------|-------------------------------|--------|
| 0008CF <sub>H</sub> -0008FF <sub>H</sub> | Reserved                                         |                              |                               | -      |
| 000900 <sub>H</sub>                      | CAN2 - Control register Low                      | CTRLRL2                      | CTRLR2                        | R/W    |
| 000901 <sub>H</sub>                      | CAN2 - Control register High (reserved)          | CTRLRH2                      |                               | R      |
| 000902 <sub>H</sub>                      | CAN2 - Status register Low                       | STATRL2                      | STATR2                        | R/W    |
| 000903 <sub>H</sub>                      | CAN2 - Status register High (reserved)           | STATRH2                      |                               | R      |
| 000904 <sub>H</sub>                      | CAN2 - Error Counter Low (Transmit)              | ERRCNTL2                     | ERRCNT2                       | R      |
| 000905 <sub>H</sub>                      | CAN2 - Error Counter High (Receive)              | ERRCNTH2                     |                               | R      |
| 000906 <sub>H</sub>                      | CAN2 - Bit Timing Register Low                   | BTRL2                        | BTR2                          | R/W    |
| 000907 <sub>H</sub>                      | CAN2 - Bit Timing Register High                  | BTRH2                        |                               | R/W    |
| 000908 <sub>H</sub>                      | CAN2 - Interrupt Register Low                    | INTRL2                       | INTR2                         | R      |
| 000909 <sub>H</sub>                      | CAN2 - Interrupt Register High                   | INTRH2                       |                               | R      |
| 00090A <sub>H</sub>                      | CAN2 - Test Register Low                         | TESTRL2                      | TESTR2                        | R/W    |
| 00090B <sub>H</sub>                      | CAN2 - Test Register High (reserved)             | TESTRH2                      |                               | R      |
| 00090C <sub>H</sub>                      | CAN2 - BRP Extension register Low                | BRPERL2                      | BRPER2                        | R/W    |
| 00090D <sub>H</sub>                      | CAN2 - BRP Extension register High (reserved)    | BRPERH2                      |                               | R      |
| 00090E <sub>H</sub> -00090F <sub>H</sub> | Reserved                                         |                              |                               | -      |
| 000910 <sub>H</sub>                      | CAN2 - IF1 Command request register Low          | IF1CREQL2                    | IF1CREQ2                      | R/W    |
| 000911 <sub>H</sub>                      | CAN2 - IF1 Command request register High         | IF1CREQH2                    |                               | R/W    |
| 000912 <sub>H</sub>                      | CAN2 - IF1 Command Mask register Low             | IF1CMSKL2                    | IF1CMSK2                      | R/W    |
| 000913 <sub>H</sub>                      | CAN2 - IF1 Command Mask register High (reserved) | IF1CMSKH2                    |                               | R      |
| 000914 <sub>H</sub>                      | CAN2 - IF1 Mask 1 Register Low                   | IF1MSK1L2                    | IF1MSK12                      | R/W    |
| 000915 <sub>H</sub>                      | CAN2 - IF1 Mask 1 Register High                  | IF1MSK1H2                    |                               | R/W    |
| 000916 <sub>H</sub>                      | CAN2 - IF1 Mask 2 Register Low                   | IF1MSK2L2                    | IF1MSK22                      | R/W    |
| 000917 <sub>H</sub>                      | CAN2 - IF1 Mask 2 Register High                  | IF1MSK2H2                    |                               | R/W    |
| 000918 <sub>H</sub>                      | CAN2 - IF1 Arbitration 1 Register Low            | IF1ARB1L2                    | IF1ARB12                      | R/W    |
| 000919 <sub>H</sub>                      | CAN2 - IF1 Arbitration 1 Register High           | IF1ARB1H2                    |                               | R/W    |
| 00091A <sub>H</sub>                      | CAN2 - IF1 Arbitration 2 Register Low            | IF1ARB2L2                    | IF1ARB22                      | R/W    |
| 00091B <sub>H</sub>                      | CAN2 - IF1 Arbitration 2 Register High           | IF1ARB2H2                    |                               | R/W    |
| 00091C <sub>H</sub>                      | CAN2 - IF1 Message Control Register Low          | IF1MCTRL2                    | IF1MCTR2                      | R/W    |
| 00091D <sub>H</sub>                      | CAN2 - IF1 Message Control Register High         | IF1MCTRH2                    |                               | R/W    |
| 00091E <sub>H</sub>                      | CAN2 - IF1 Data A1 Low                           | IF1DTA1L2                    | IF1DTA12                      | R/W    |
| 00091F <sub>H</sub>                      | CAN2 - IF1 Data A1 High                          | IF1DTA1H2                    |                               | R/W    |
| 000920 <sub>H</sub>                      | CAN2 - IF1 Data A2 Low                           | IF1DTA2L2                    | IF1DTA22                      | R/W    |
| 000921 <sub>H</sub>                      | CAN2 - IF1 Data A2 High                          | IF1DTA2H2                    |                               | R/W    |
| 000922 <sub>H</sub>                      | CAN2 - IF1 Data B1 Low                           | IF1DTB1L2                    | IF1DTB12                      | R/W    |
| 000923 <sub>H</sub>                      | CAN2 - IF1 Data B1 High                          | IF1DTB1H2                    |                               | R/W    |
| 000924 <sub>H</sub>                      | CAN2 - IF1 Data B2 Low                           | IF1DTB2L2                    | IF1DTB22                      | R/W    |
| 000925 <sub>H</sub>                      | CAN2 - IF1 Data B2 High                          | IF1DTB2H2                    |                               | R/W    |
| 000926 <sub>H</sub> -00093F <sub>H</sub> | Reserved                                         |                              |                               | -      |

**Table 4. I/O Map CY96(F)35x (20 / 21)**

| Address                                  | Register                                         | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|--------------------------------------------------|------------------------------|-------------------------------|--------|
| 000940 <sub>H</sub>                      | CAN2 - IF2 Command request register Low          | IF2CREQL2                    | IF2CREQ2                      | R/W    |
| 000941 <sub>H</sub>                      | CAN2 - IF2 Command request register High         | IF2CREQH2                    |                               | R/W    |
| 000942 <sub>H</sub>                      | CAN2 - IF2 Command Mask register Low             | IF2CMSKL2                    | IF2CMSK2                      | R/W    |
| 000943 <sub>H</sub>                      | CAN2 - IF2 Command Mask register High (reserved) | IF2CMSKH2                    |                               | R      |
| 000944 <sub>H</sub>                      | CAN2 - IF2 Mask 1 Register Low                   | IF2MSK1L2                    | IF2MSK12                      | R/W    |
| 000945 <sub>H</sub>                      | CAN2 - IF2 Mask 1 Register High                  | IF2MSK1H2                    |                               | R/W    |
| 000946 <sub>H</sub>                      | CAN2 - IF2 Mask 2 Register Low                   | IF2MSK2L2                    | IF2MSK22                      | R/W    |
| 000947 <sub>H</sub>                      | CAN2 - IF2 Mask 2 Register High                  | IF2MSK2H2                    |                               | R/W    |
| 000948 <sub>H</sub>                      | CAN2 - IF2 Arbitration 1 Register Low            | IF2ARB1L2                    | IF2ARB12                      | R/W    |
| 000949 <sub>H</sub>                      | CAN2 - IF2 Arbitration 1 Register High           | IF2ARB1H2                    |                               | R/W    |
| 00094A <sub>H</sub>                      | CAN2 - IF2 Arbitration 2 Register Low            | IF2ARB2L2                    | IF2ARB22                      | R/W    |
| 00094B <sub>H</sub>                      | CAN2 - IF2 Arbitration 2 Register High           | IF2ARB2H2                    |                               | R/W    |
| 00094C <sub>H</sub>                      | CAN2 - IF2 Message Control Register Low          | IF2MCTRL2                    | IF2MCTR2                      | R/W    |
| 00094D <sub>H</sub>                      | CAN2 - IF2 Message Control Register High         | IF2MCTRH2                    |                               | R/W    |
| 00094E <sub>H</sub>                      | CAN2 - IF2 Data A1 Low                           | IF2DTA1L2                    | IF2DTA12                      | R/W    |
| 00094F <sub>H</sub>                      | CAN2 - IF2 Data A1 High                          | IF2DTA1H2                    |                               | R/W    |
| 000950 <sub>H</sub>                      | CAN2 - IF2 Data A2 Low                           | IF2DTA2L2                    | IF2DTA22                      | R/W    |
| 000951 <sub>H</sub>                      | CAN2 - IF2 Data A2 High                          | IF2DTA2H2                    |                               | R/W    |
| 000952 <sub>H</sub>                      | CAN2 - IF2 Data B1 Low                           | IF2DTB1L2                    | IF2DTB12                      | R/W    |
| 000953 <sub>H</sub>                      | CAN2 - IF2 Data B1 High                          | IF2DTB1H2                    |                               | R/W    |
| 000954 <sub>H</sub>                      | CAN2 - IF2 Data B2 Low                           | IF2DTB2L2                    | IF2DTB22                      | R/W    |
| 000955 <sub>H</sub>                      | CAN2 - IF2 Data B2 High                          | IF2DTB2H2                    |                               | R/W    |
| 000956 <sub>H</sub> -00097F <sub>H</sub> | Reserved                                         |                              |                               | -      |
| 000980 <sub>H</sub>                      | CAN2 - Transmission Request 1 Register Low       | TREQR1L2                     | TREQR12                       | R      |
| 000981 <sub>H</sub>                      | CAN2 - Transmission Request 1 Register High      | TREQR1H2                     |                               | R      |
| 000982 <sub>H</sub>                      | CAN2 - Transmission Request 2 Register Low       | TREQR2L2                     | TREQR22                       | R      |
| 000983 <sub>H</sub>                      | CAN2 - Transmission Request 2 Register High      | TREQR2H2                     |                               | R      |
| 000984 <sub>H</sub> -00098F <sub>H</sub> | Reserved                                         |                              |                               | -      |
| 000990 <sub>H</sub>                      | CAN2 - New Data 1 Register Low                   | NEWDT1L2                     | NEWDT12                       | R      |
| 000991 <sub>H</sub>                      | CAN2 - New Data 1 Register High                  | NEWDT1H2                     |                               | R      |
| 000992 <sub>H</sub>                      | CAN2 - New Data 2 Register Low                   | NEWDT2L2                     | NEWDT22                       | R      |
| 000993 <sub>H</sub>                      | CAN2 - New Data 2 Register High                  | NEWDT2H2                     |                               | R      |
| 000994 <sub>H</sub> -00099F <sub>H</sub> | Reserved                                         |                              |                               | -      |
| 0009A0 <sub>H</sub>                      | CAN2 - Interrupt Pending 1 Register Low          | INTPND1L2                    | INTPND12                      | R      |
| 0009A1 <sub>H</sub>                      | CAN2 - Interrupt Pending 1 Register High         | INTPND1H2                    |                               | R      |
| 0009A2 <sub>H</sub>                      | CAN2 - Interrupt Pending 2 Register Low          | INTPND2L2                    | INTPND22                      | R      |
| 0009A3 <sub>H</sub>                      | CAN2 - Interrupt Pending 2 Register High         | INTPND2H2                    |                               | R      |
| 0009A4 <sub>H</sub> -0009AF <sub>H</sub> | Reserved                                         |                              |                               | -      |
| 0009B0 <sub>H</sub>                      | CAN2 - Message Valid 1 Register Low              | MSGVAL1L2                    | MSGVAL12                      | R      |

**Table 4. I/O Map CY96(F)35x (21 / 21)**

| Address                                  | Register                             | Abbreviation<br>8-bit Access | Abbreviation<br>16-bit Access | Access |
|------------------------------------------|--------------------------------------|------------------------------|-------------------------------|--------|
| 0009B1 <sub>H</sub>                      | CAN2 - Message Valid 1 Register High | MSGVAL1H2                    |                               | R      |
| 0009B2 <sub>H</sub>                      | CAN2 - Message Valid 2 Register Low  | MSGVAL2L2                    | MSGVAL22                      | R      |
| 0009B3 <sub>H</sub>                      | CAN2 - Message Valid 2 Register High | MSGVAL2H2                    |                               | R      |
| 0009B4 <sub>H</sub> -0009CD <sub>H</sub> | Reserved                             |                              |                               | -      |
| 0009CE <sub>H</sub>                      | CAN2 - Output enable register        | COER2                        |                               | R/W    |
| 0009CF <sub>H</sub> -000BFF <sub>H</sub> | Reserved                             |                              |                               | -      |

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading 'X'.  
 Registers of resources which are described in this table, but which are not supported by the device, should also be handled as "Reserved".

## Interrupt Vector Table

Table 5. Interrupt Vector Table CY96(F)35x (1 / 3)

| Vector Number | Offset in Vector Table | Vector Name | Cleared by DMA | Index in ICR to Program | Description                                             |
|---------------|------------------------|-------------|----------------|-------------------------|---------------------------------------------------------|
| 0             | 3FC <sub>H</sub>       | CALLV0      | No             | -                       |                                                         |
| 1             | 3F8 <sub>H</sub>       | CALLV1      | No             | -                       |                                                         |
| 2             | 3F4 <sub>H</sub>       | CALLV2      | No             | -                       |                                                         |
| 3             | 3F0 <sub>H</sub>       | CALLV3      | No             | -                       |                                                         |
| 4             | 3EC <sub>H</sub>       | CALLV4      | No             | -                       |                                                         |
| 5             | 3E8 <sub>H</sub>       | CALLV5      | No             | -                       |                                                         |
| 6             | 3E4 <sub>H</sub>       | CALLV6      | No             | -                       |                                                         |
| 7             | 3E0 <sub>H</sub>       | CALLV7      | No             | -                       |                                                         |
| 8             | 3DC <sub>H</sub>       | RESET       | No             | -                       |                                                         |
| 9             | 3D8 <sub>H</sub>       | INT9        | No             | -                       |                                                         |
| 10            | 3D4 <sub>H</sub>       | EXCEPTION   | No             | -                       |                                                         |
| 11            | 3D0 <sub>H</sub>       | NMI         | No             | -                       | Non-Maskable Interrupt                                  |
| 12            | 3CC <sub>H</sub>       | DLY         | No             | 12                      | Delayed Interrupt                                       |
| 13            | 3C8 <sub>H</sub>       | RC_TIMER    | No             | 13                      | RC Timer                                                |
| 14            | 3C4 <sub>H</sub>       | MC_TIMER    | No             | 14                      | Main Clock Timer                                        |
| 15            | 3C0 <sub>H</sub>       | SC_TIMER    | No             | 15                      | Sub Clock Timer                                         |
| 16            | 3BC <sub>H</sub>       | PLL_UNLOCK  | No             | 16                      | Reserved                                                |
| 17            | 3B8 <sub>H</sub>       | EXTINT0     | Yes            | 17                      | External Interrupt 0                                    |
| 18            | 3B4 <sub>H</sub>       |             |                |                         | Reserved                                                |
| 19            | 3B0 <sub>H</sub>       | EXTINT2     | Yes            | 19                      | External Interrupt 2                                    |
| 20            | 3AC <sub>H</sub>       | EXTINT3     | Yes            | 20                      | External Interrupt 3                                    |
| 21            | 3A8 <sub>H</sub>       | EXTINT4     | Yes            | 21                      | External Interrupt 4                                    |
| 22            | 3A4 <sub>H</sub>       |             |                |                         | Reserved                                                |
| 23            | 3A0 <sub>H</sub>       | EXTINT7     | Yes            | 23                      | External Interrupt 7                                    |
| 24            | 39C <sub>H</sub>       | EXTINT8     | Yes            | 24                      | External Interrupt 8                                    |
| 25            | 398 <sub>H</sub>       | EXTINT9     | Yes            | 25                      | External Interrupt 9                                    |
| 26            | 394 <sub>H</sub>       | EXTINT10    | Yes            | 26                      | External Interrupt 10                                   |
| 27            | 390 <sub>H</sub>       | EXTINT11    | Yes            | 27                      | External Interrupt 11                                   |
| 28            | 38C <sub>H</sub>       | EXTINT12    | Yes            | 28                      | External Interrupt 12                                   |
| 29            | 388 <sub>H</sub>       | EXTINT13    | Yes            | 29                      | External Interrupt 13                                   |
| 30            | 384 <sub>H</sub>       | EXTINT14    | Yes            | 30                      | External Interrupt 14                                   |
| 31            | 380 <sub>H</sub>       | EXTINT15    | Yes            | 31                      | External Interrupt 15                                   |
| 32            | 37C <sub>H</sub>       | CAN1        | No             | 32                      | CAN Controller 1 (only CY96F356Y/R)                     |
| 33            | 378 <sub>H</sub>       | CAN2        | No             | 33                      | CAN Controller 2 (only CY96F356Y/R and CY96F353R/F355R) |
| 34            | 374 <sub>H</sub>       | PPG0        | Yes            | 34                      | Programmable Pulse Generator 0                          |
| 35            | 370 <sub>H</sub>       | PPG1        | Yes            | 35                      | Programmable Pulse Generator 1                          |

**Table 5. Interrupt Vector Table CY96(F)35x (2 / 3)**

| Vector Number | Offset in Vector Table | Vector Name | Cleared by DMA | Index in ICR to Program | Description                        |
|---------------|------------------------|-------------|----------------|-------------------------|------------------------------------|
| 36            | 36C <sub>H</sub>       | PPG2        | Yes            | 36                      | Programmable Pulse Generator 2     |
| 37            | 368 <sub>H</sub>       | PPG3        | Yes            | 37                      | Programmable Pulse Generator 3     |
| 38            | 364 <sub>H</sub>       | PPG4        | Yes            | 38                      | Programmable Pulse Generator 4     |
| 39            | 360                    | PPG5        | Yes            | 39                      | Programmable Pulse Generator 5     |
| 40            | 35C <sub>H</sub>       | PPG6        | Yes            | 40                      | Programmable Pulse Generator 6     |
| 41            | 358 <sub>H</sub>       | PPG7        | Yes            | 41                      | Programmable Pulse Generator 7     |
| 42            | 354 <sub>H</sub>       | PPG8        | Yes            | 42                      | Programmable Pulse Generator 8     |
| 43            | 350 <sub>H</sub>       | PPG9        | Yes            | 43                      | Programmable Pulse Generator 9     |
| 44            | 34C <sub>H</sub>       | PPG10       | Yes            | 44                      | Programmable Pulse Generator 10    |
| 45            | 348 <sub>H</sub>       | PPG11       | Yes            | 45                      | Programmable Pulse Generator 11    |
| 46            | 344 <sub>H</sub>       | PPG12       | Yes            | 46                      | Programmable Pulse Generator 12    |
| 47            | 340 <sub>H</sub>       | PPG13       | Yes            | 47                      | Programmable Pulse Generator 13    |
| 48            | 33C <sub>H</sub>       | PPG14       | Yes            | 48                      | Programmable Pulse Generator 14    |
| 49            | 338 <sub>H</sub>       | PPG15       | Yes            | 49                      | Programmable Pulse Generator 15    |
| 50            | 334 <sub>H</sub>       | PPG16       | Yes            | 50                      | Programmable Pulse Generator 16    |
| 51            | 330 <sub>H</sub>       | PPG17       | Yes            | 51                      | Programmable Pulse Generator 17    |
| 52            | 32C <sub>H</sub>       | PPG18       | Yes            | 52                      | Programmable Pulse Generator 18    |
| 53            | 328 <sub>H</sub>       | PPG19       | Yes            | 53                      | Programmable Pulse Generator 19    |
| 54            | 324 <sub>H</sub>       | RLT0        | Yes            | 54                      | Reload Timer 0                     |
| 55            | 320 <sub>H</sub>       | RLT1        | Yes            | 55                      | Reload Timer 1                     |
| 56            | 31C <sub>H</sub>       | RLT2        | Yes            | 56                      | Reload Timer 2                     |
| 57            | 318 <sub>H</sub>       | RLT3        | Yes            | 57                      | Reload Timer 3                     |
| 58            | 314 <sub>H</sub>       | PPGRLT      | Yes            | 58                      | Reload Timer 6 - dedicated for PPG |
| 59            | 310 <sub>H</sub>       | ICU0        | Yes            | 59                      | Input Capture Unit 0               |
| 60            | 30C <sub>H</sub>       | ICU1        | Yes            | 60                      | Input Capture Unit 1               |
| 61            | 308 <sub>H</sub>       |             |                |                         | Reserved                           |
| 62            | 304 <sub>H</sub>       |             |                |                         | Reserved                           |
| 63            | 300 <sub>H</sub>       | ICU4        | Yes            | 63                      | Input Capture Unit 4               |
| 64            | 2FC <sub>H</sub>       | ICU5        | Yes            | 64                      | Input Capture Unit 5               |
| 65            | 2F8 <sub>H</sub>       | ICU6        | Yes            | 65                      | Input Capture Unit 6               |
| 66            | 2F4 <sub>H</sub>       | ICU7        | Yes            | 66                      | Input Capture Unit 7               |
| 67            | 2F0 <sub>H</sub>       |             |                |                         | Reserved                           |
| 68            | 2EC <sub>H</sub>       | ICU9        | Yes            | 68                      | Input Capture Unit 9               |
| 69            | 2E8 <sub>H</sub>       | ICU10       | Yes            | 69                      | Input Capture Unit 10              |
| 70            | 2E4 <sub>H</sub>       |             |                |                         | Reserved                           |
| 71            | 2E0 <sub>H</sub>       | OCU4        | Yes            | 71                      | Output Compare Unit 4              |
| 72            | 2DC <sub>H</sub>       | OCU5        | Yes            | 72                      | Output Compare Unit 5              |
| 73            | 2D8 <sub>H</sub>       | OCU6        | Yes            | 73                      | Output Compare Unit 6              |

**Table 5. Interrupt Vector Table CY96(F)35x (3 / 3)**

| Vector Number | Offset in Vector Table | Vector Name | Cleared by DMA | Index in ICR to Program | Description                         |
|---------------|------------------------|-------------|----------------|-------------------------|-------------------------------------|
| 74            | 2D4 <sub>H</sub>       | OCU7        | Yes            | 74                      | Output Compare Unit 7               |
| 75            | 2D0 <sub>H</sub>       |             |                |                         | Reserved                            |
| 76            | 2CC <sub>H</sub>       |             |                |                         | Reserved                            |
| 77            | 2C8 <sub>H</sub>       | FRT0        | Yes            | 77                      | Free Running Timer 0                |
| 78            | 2C4 <sub>H</sub>       | FRT1        | Yes            | 78                      | Free Running Timer 1                |
| 79            | 2C0 <sub>H</sub>       | FRT2        | Yes            | 79                      | Free Running Timer 2                |
| 80            | 2BC <sub>H</sub>       | FRT3        | Yes            | 80                      | Free Running Timer 3                |
| 81            | 2B8 <sub>H</sub>       | RTC0        | No             | 81                      | Real Timer Clock                    |
| 82            | 2B4 <sub>H</sub>       | CAL0        | No             | 82                      | Clock Calibration Unit              |
| 83            | 2B0 <sub>H</sub>       | IIC0        | Yes            | 83                      | I2C interface                       |
| 84            | 2AC <sub>H</sub>       | ADC0        | Yes            | 84                      | A/D Converter                       |
| 85            | 2A8 <sub>H</sub>       | LINR2       | Yes            | 85                      | LIN USART 2 RX                      |
| 86            | 2A4 <sub>H</sub>       | LINT2       | Yes            | 86                      | LIN USART 2 TX                      |
| 87            | 2A0 <sub>H</sub>       | LINR3       | Yes            | 87                      | LIN USART 3 RX                      |
| 88            | 29C <sub>H</sub>       | LINT3       | Yes            | 88                      | LIN USART 3 TX                      |
| 89            | 298 <sub>H</sub>       | LINR7       | Yes            | 89                      | LIN USART 7 RX                      |
| 90            | 294 <sub>H</sub>       | LINT7       | Yes            | 90                      | LIN USART 7 TX                      |
| 91            | 290 <sub>H</sub>       | LINR8       | Yes            | 91                      | LIN USART 8 RX                      |
| 92            | 28C <sub>H</sub>       | LINT8       | Yes            | 92                      | LIN USART 8 TX                      |
| 93            | 288 <sub>H</sub>       | FLASH_A     | No             | 93                      | Flash memory A (only Flash devices) |

## Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins ( $V_{CC}/V_{SS}$ )
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Clock modulator

### 1. Latch-up Prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  pins and  $V_{SS}$  pins.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

### 2. Unused Pins Handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 k $\Omega$ .

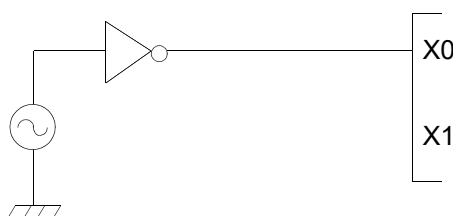
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

### 3. External Clock Usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

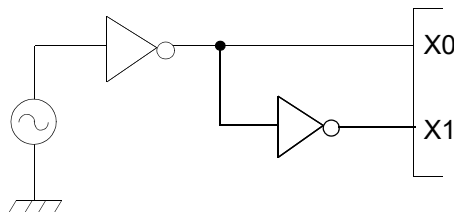
#### 1. Single phase external clock

- When using a single phase external clock, X0 (X0A) pin must be driven and X1 (X1A) pin left open.



## 2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



## 4. Unused Sub Clock Signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

## 5. Notes on PLL Clock Mode Operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

## 6. Power Supply Pins ( $V_{CC}/V_{SS}$ )

It is required that all  $V_{CC}$ -level as well as all  $V_{SS}$ -level power supply pins are at the same potential. If there is more than one  $V_{CC}$  or  $V_{SS}$  level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

$V_{CC}$  and  $V_{SS}$  must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1  $\mu\text{F}$  between  $V_{CC}$  and  $V_{SS}$  as close as possible to  $V_{CC}$  and  $V_{SS}$  pins.

Please add the bypass capacitor of the power supply in order to not exceed 0.1V/ $\mu\text{s}$ .

## 7. Crystal Oscillator and Ceramic Resonator Circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

## 8. Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

It is required to turn the A/D converter power supply ( $AV_{CC}$ ,  $AV_{RH}$ ,  $AV_{RL}$ ) and analog inputs ( $AN_n$ ) on after turning the digital power supply ( $V_{CC}$ ) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed  $AV_{RH}$  or  $AV_{CC}$  (turning the analog and digital power supplies simultaneously on or off is acceptable).

## 9. Pin Handling when Not Using the A/D Converter

It is required to connect the unused pins of the A/D converter as  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AV_{RH} = AV_{RL} = V_{SS}$ .

## 10. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50  $\mu\text{s}$  from 0.2 V to 2.7 V.

## 11. Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the  $V_{CC}$  power supply voltage, a malfunction may occur. The  $V_{CC}$  power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that  $V_{CC}$  ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10 % of the standard  $V_{CC}$  power supply voltage and the transient fluctuation rate becomes 0.1 V/ $\mu\text{s}$  or less in instantaneous fluctuation for power supply switching.

## **12. Serial Communication**

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

## **13. Clock modulator**

Please contact Cypress before using this function.

## Electrical Characteristics

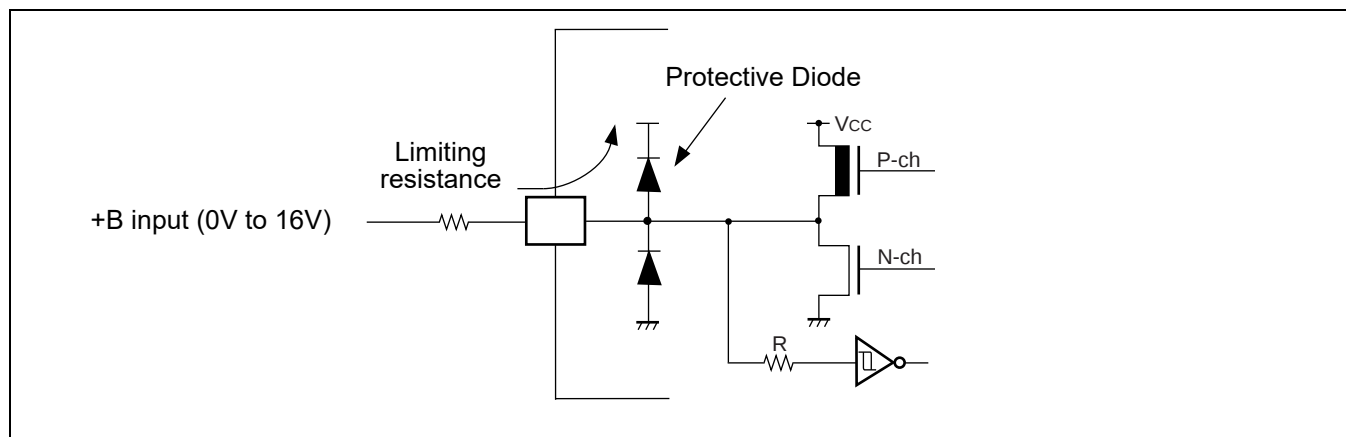
### Absolute Maximum Ratings

| Parameter                                                 | Symbol             | Rating         |                   | Unit       | Remarks                                                                               |
|-----------------------------------------------------------|--------------------|----------------|-------------------|------------|---------------------------------------------------------------------------------------|
|                                                           |                    | Min            | Max               |            |                                                                                       |
| Power supply voltage                                      | $V_{CC}$           | $V_{SS} - 0.3$ | $V_{SS} + 6.0$    | V          |                                                                                       |
|                                                           | $AV_{CC}$          | $V_{SS} - 0.3$ | $V_{SS} + 6.0$    | V          | $V_{CC} = AV_{CC}^{*1}$                                                               |
| AD Converter voltage references                           | $AV_{RH}, AV_{RL}$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$    | V          | $AV_{CC} \geq AV_{RH}, AV_{CC} \geq AV_{RL}, AV_{RH} > AV_{RL}, AV_{RL} \geq AV_{SS}$ |
| Input voltage                                             | $V_I$              | $V_{SS} - 0.3$ | $V_{SS} + 6.0$    | V          | $V_I \leq V_{CC} + 0.3 V^{*2}$                                                        |
| Output voltage                                            | $V_O$              | $V_{SS} - 0.3$ | $V_{SS} + 6.0$    | V          | $V_O \leq V_{CC} + 0.3 V^{*2}$                                                        |
| Maximum Clamp Current                                     | $I_{CLAMP}$        | -4.0           | +4.0              | mA         | Applicable to general purpose I/O pins <sup>*3</sup>                                  |
| Total Maximum Clamp Current                               | $\sum  I_{CLAMP} $ | -              | 40                | mA         | Applicable to general purpose I/O pins <sup>*3</sup>                                  |
| "L" level maximum output current                          | $I_{OL1}$          | -              | 15                | mA         | Outputs with driving strength set to 2 mA / 3 mA / 5 mA                               |
| "L" level average output current                          | $I_{OLAV2}$        | -              | 2                 | mA         | Outputs with driving strength set to 2mA                                              |
|                                                           | $I_{OLAV3}$        | -              | 3                 | mA         | Outputs of I/O circuit type "N"                                                       |
|                                                           | $I_{OLAV5}$        | -              | 5                 | mA         | Outputs with driving strength set to 5mA                                              |
| "L" level maximum overall output current                  | $\sum I_{OL1}$     | -              | 100               | mA         | Normal outputs                                                                        |
| "L" level average overall output current                  | $\sum I_{OLAV1}$   | -              | 50                | mA         | Normal outputs                                                                        |
| "H" level maximum output current                          | $I_{OH1}$          | -              | -15               | mA         | Outputs with driving strength set to 2 mA / 3 mA / 5 mA                               |
| "H" level average output current                          | $I_{OHAV2}$        | -              | -2                | mA         | Outputs with driving strength set to 2 mA                                             |
|                                                           | $I_{OHAV3}$        | -              | -3                | mA         | Outputs of I/O circuit type "N"                                                       |
|                                                           | $I_{OHAV5}$        | -              | -5                | mA         | Outputs with driving strength set to 5 mA                                             |
| "H" level maximum overall output current                  | $\sum I_{OH1}$     | -              | -100              | mA         | Normal outputs                                                                        |
| "H" level average overall output current                  | $\sum I_{OHAV1}$   | -              | -50               | mA         | Normal outputs                                                                        |
| Permitted Power dissipation (Flash devices) <sup>*4</sup> | $P_D$              | -              | 320 <sup>*5</sup> | mW         | $T_A = 105^\circ C$                                                                   |
|                                                           |                    | -              | 640 <sup>*5</sup> | mW         | $T_A = 85^\circ C$                                                                    |
|                                                           |                    | -              | 800 <sup>*5</sup> | mW         | $T_A = 75^\circ C$                                                                    |
|                                                           |                    | -              | 400 <sup>*5</sup> | mW         | $T_A = 125^\circ C$ , no Flash program/erase                                          |
|                                                           |                    | -              | 560 <sup>*5</sup> | mW         | $T_A = 115^\circ C$ , no Flash program/erase                                          |
| Operating ambient temperature                             | $T_A$              | 0              | +70               | $^\circ C$ | CY96V300C                                                                             |
|                                                           |                    | -40            | +105              |            |                                                                                       |
|                                                           |                    | -40            | +125              |            | <sup>*6</sup>                                                                         |
| Storage temperature                                       | $T_{STG}$          | -55            | +150              | $^\circ C$ |                                                                                       |

\*1:  $AV_{CC}$  and  $V_{CC}$  must be set to the same voltage. It is required that  $AV_{CC}$  does not exceed  $V_{CC}$  and that the voltage at the analog inputs does not exceed  $AV_{CC}$  neither when the power is switched on.

\*2:  $V_I$  and  $V_O$  should not exceed  $V_{CC} + 0.3$  V.  $V_I$  should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_I$  rating. Input/output voltages of standard ports depend on  $V_{CC}$ .

- \*3:
- Applicable to all general-purpose I/O pins (Pnn\_m).
  - Use within recommended operating conditions.
  - Use at DC voltage (current)
  - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
  - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).
  - Sample recommended circuits:



\*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$$P_{IO} = S (V_{OL} * I_{OL} + V_{OH} * I_{OH}) \text{ (IO load power dissipation, sum is performed on all IO ports)}$$

$$P_{INT} = V_{CC} * (I_{CC} + I_A) \text{ (internal power dissipation)}$$

$I_{CC}$  is the total core current consumption into  $V_{CC}$  as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.

$I_A$  is the analog current consumption into  $AV_{CC}$ .

\*5: Worst case value for a package mounted on single layer PCB at specified  $T_A$  without air flow.

\*6: Please contact Cypress for reliability limitations when using under these conditions.

#### WARNING:

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

**Recommended Operating Conditions**

| Parameter                    | Symbol          | Value |     |     | Unit | Remarks                                                                                |
|------------------------------|-----------------|-------|-----|-----|------|----------------------------------------------------------------------------------------|
|                              |                 | Min   | Typ | Max |      |                                                                                        |
| Power supply voltage         | V <sub>CC</sub> | 3.0   | -   | 5.5 | V    |                                                                                        |
| Smoothing capacitor at C pin | C <sub>S</sub>  | 3.5   | 4.7 | 15  | μF   | Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics. |

**WARNING:**

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions. Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

**DC Characteristics**
 $(T_A = -40\text{ }^{\circ}\text{C to } 125\text{ }^{\circ}\text{C}, V_{CC} = AV_{CC} = 3.0\text{ V to } 5.5\text{ V}, V_{SS} = AV_{SS} = 0\text{ V})$ 

| Parameter       | Symbol     | Pin                  | Condition                                       | Value            |     |                  | Unit | Remarks                    |
|-----------------|------------|----------------------|-------------------------------------------------|------------------|-----|------------------|------|----------------------------|
|                 |            |                      |                                                 | Min              | Typ | Max              |      |                            |
| Input H voltage | $V_{IH}$   | Port inputs<br>Pnn_m | CMOS Hysteresis<br>0.8/0.2 input<br>selected    | $0.8 V_{CC}$     | -   | $V_{CC} + 0.3$   | V    |                            |
|                 |            |                      | CMOS Hysteresis<br>0.7/0.3 input<br>selected    | $0.7 V_{CC}$     | -   | $V_{CC} + 0.3$   | V    | $V_{CC} \geq 4.5\text{ V}$ |
|                 |            |                      |                                                 | 0.74<br>$V_{CC}$ | -   | $V_{CC} + 0.3$   | V    | $V_{CC} < 4.5\text{ V}$    |
|                 |            |                      | AUTOMOTIVE<br>Hysteresis input<br>selected      | $0.8 V_{CC}$     | -   | $V_{CC} + 0.3$   | V    |                            |
|                 |            |                      | TTL input selected                              | 2.0              | -   | $V_{CC} + 0.3$   | V    |                            |
|                 | $V_{IH0F}$ | X0                   | External clock in<br>"Fast Clock Input<br>mode" | $0.8 V_{CC}$     | -   | $V_{CC} + 0.3$   | V    |                            |
|                 | $V_{IH0S}$ | X0,X1,<br>X0A,X1A    | External clock in<br>"oscillation mode"         | 2.5              | -   | $V_{CC} + 0.3$   | V    |                            |
|                 | $V_{IHR}$  | RSTX                 | -                                               | $0.8 V_{CC}$     | -   | $V_{CC} + 0.3$   | V    | CMOS Hysteresis input      |
|                 | $V_{IHM}$  | MD2-MD0              | -                                               | $V_{CC} - 0.3$   | -   | $V_{CC} + 0.3$   | V    |                            |
| Input L voltage | $V_{IL}$   | Port inputs<br>Pnn_m | CMOS Hysteresis<br>0.8/0.2 input<br>selected    | $V_{SS} - 0.3$   | -   | $0.2 V_{CC}$     | V    |                            |
|                 |            |                      | CMOS Hysteresis<br>0.7/0.3 input<br>selected    | $V_{SS} - 0.3$   | -   | $0.3 V_{CC}$     | V    |                            |
|                 |            |                      |                                                 | $V_{SS} - 0.3$   | -   | $0.5 V_{CC}$     | V    | $V_{CC} \geq 4.5\text{ V}$ |
|                 |            |                      | AUTOMOTIVE<br>Hysteresis input<br>selected      | $V_{SS} - 0.3$   | -   | 0.46<br>$V_{CC}$ |      | $V_{CC} < 4.5\text{ V}$    |
|                 |            |                      |                                                 | $V_{SS} - 0.3$   | -   | 0.8              | V    |                            |
|                 | $V_{IL0F}$ | X0                   | External clock in<br>"Fast Clock Input<br>mode" | $V_{SS} - 0.3$   | -   | $0.2 V_{CC}$     | V    |                            |
|                 | $V_{IL0S}$ | X0,X1,<br>X0A,X1A    | External clock in<br>"oscillation mode"         | $V_{SS} - 0.3$   | -   | 0.4              | V    |                            |
|                 | $V_{ILR}$  | RSTX                 | -                                               | $V_{SS} - 0.3$   | -   | $0.2 V_{CC}$     | V    | CMOS Hysteresis input      |
|                 | $V_{ILM}$  | MD2-MD0              | -                                               | $V_{SS} - 0.3$   | -   | $V_{SS} + 0.3$   | V    |                            |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter          | Symbol    | Pin            | Condition                                                               | Value          |     |     | Unit             | Remarks                                  |
|--------------------|-----------|----------------|-------------------------------------------------------------------------|----------------|-----|-----|------------------|------------------------------------------|
|                    |           |                |                                                                         | Min            | Typ | Max |                  |                                          |
| Output H voltage   | $V_{OH2}$ | Normal outputs | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$<br>$I_{OH} = -2\text{ mA}$ | $V_{CC} - 0.5$ | -   | -   | V                | Driving strength set to 2 mA (PODR:OD=1) |
|                    |           |                | $3.0\text{ V} \leq V_{CC} < 4.5\text{ V}$<br>$I_{OH} = -1.6\text{ mA}$  |                |     |     |                  |                                          |
|                    | $V_{OH5}$ | Normal outputs | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$<br>$I_{OH} = -5\text{ mA}$ | $V_{CC} - 0.5$ | -   | -   | V                | Driving strength set to 5 mA (PODR:OD=0) |
|                    |           |                | $3.0\text{ V} \leq V_{CC} < 4.5\text{ V}$<br>$I_{OH} = -3\text{ mA}$    |                |     |     |                  |                                          |
|                    | $V_{OH3}$ | 3 mA outputs   | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$<br>$I_{OH} = -3\text{ mA}$ | $V_{CC} - 0.5$ | -   | -   | V                | I/O circuit type "N"                     |
|                    |           |                | $3.0\text{ V} \leq V_{CC} < 4.5\text{ V}$<br>$I_{OH} = -2\text{ mA}$    |                |     |     |                  |                                          |
| Output L voltage   | $V_{OL2}$ | Normal outputs | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$<br>$I_{OL} = +2\text{ mA}$ | -              | -   | 0.4 | V                | Driving strength set to 2 mA             |
|                    |           |                | $3.0\text{ V} \leq V_{CC} < 4.5\text{ V}$<br>$I_{OL} = +1.6\text{ mA}$  |                |     |     |                  |                                          |
|                    | $V_{OL5}$ | Normal outputs | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$<br>$I_{OL} = +5\text{ mA}$ | -              | -   | 0.4 | V                | Driving strength set to 5 mA             |
|                    |           |                | $3.0\text{ V} \leq V_{CC} < 4.5\text{ V}$<br>$I_{OL} = +3\text{ mA}$    |                |     |     |                  |                                          |
|                    | $V_{OL3}$ | 3 mA outputs   | $3.0\text{ V} \leq V_{CC} \leq 5.5\text{ V}$<br>$I_{OL} = +3\text{ mA}$ | -              | -   | 0.4 | V                | I/O circuit type "N"                     |
|                    |           |                |                                                                         |                |     |     |                  |                                          |
| Input leak current | $I_{IL}$  | Pnn_m          | $V_{SS} < V_I < V_{CC}$<br>$AV_{SS}, AV_{RL} < V_I < AV_{CC}, AV_{RH}$  | -1             | -   | +1  | $\mu\text{A}$    | Single port pin                          |
| Pull-up resistance | $R_{UP}$  | Pnn_m, RSTX    | $V_{CC} = 3.3\text{ V} \pm 10\%$                                        | 40             | 100 | 160 | $\text{k}\Omega$ |                                          |
|                    |           |                | $V_{CC} = 5.0\text{ V} \pm 10\%$                                        | 25             | 50  | 100 | $\text{k}\Omega$ |                                          |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                                       | Symbol              | Condition (at T <sub>A</sub> )                                                                                                                  | Value   |      |      | Remarks |               |
|-------------------------------------------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|---------|------|------|---------|---------------|
|                                                 |                     |                                                                                                                                                 | Typ     | Max  | Unit |         |               |
| Power supply current in Run modes <sup>*1</sup> | I <sub>CCPLL</sub>  | PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 16MHz, CLKP2 = 8MHz<br>1 Flash/ROM wait state (CLKRC and CLKSC stopped)                              | +25 °C  | 14.5 | 19.5 | mA      | CY96F353/F355 |
|                                                 |                     |                                                                                                                                                 | +125 °C | 16   | 23   |         |               |
|                                                 |                     |                                                                                                                                                 | +25 °C  | 15   | 20   | mA      | CY96F356      |
|                                                 |                     |                                                                                                                                                 | +125 °C | 16.5 | 23.5 |         |               |
|                                                 |                     | PLL Run mode with CLKS1/2 = CLKB = CLKP1= 32MHz, CLKP2 = 16MHz<br>2 Flash/ROM wait states (CLKRC and CLKSC stopped)                             | +25 °C  | 23   | 29   | mA      | CY96F353/F355 |
|                                                 |                     |                                                                                                                                                 | +125 °C | 25   | 33   |         |               |
|                                                 |                     |                                                                                                                                                 | +25 °C  | 24   | 30   | mA      | CY96F356      |
|                                                 |                     |                                                                                                                                                 | +125 °C | 26   | 34   |         |               |
|                                                 |                     | PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz<br>0 Flash/ROM wait states (CLKRC and CLKSC stopped)                                  | +25 °C  | 26   | 38   | mA      | CY96F353/F355 |
|                                                 |                     |                                                                                                                                                 | +125 °C | 28   | 42   |         |               |
|                                                 |                     |                                                                                                                                                 | +25 °C  | 28   | 40   | mA      | CY96F356      |
|                                                 |                     |                                                                                                                                                 | +125 °C | 30   | 44   |         |               |
|                                                 |                     | PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz, CLKP2 = 28MHz<br>2 Flash/ROM wait states (CLKRC and CLKSC stopped. Core voltage at 1.9V)       | +25 °C  | 40   | 51   | mA      | CY96F353/F355 |
|                                                 |                     |                                                                                                                                                 | +125 °C | 42   | 55   |         |               |
|                                                 |                     |                                                                                                                                                 | +25 °C  | 41   | 52   | mA      | CY96F356      |
|                                                 |                     |                                                                                                                                                 | +125 °C | 43   | 56   |         |               |
|                                                 |                     | PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz<br>1 Flash/ROM wait state (CLKRC and CLKSC stopped. Core voltage at 1.9V) | +25 °C  | 43   | 56   | mA      | CY96F353/F355 |
|                                                 |                     |                                                                                                                                                 | +125 °C | 45   | 60   |         |               |
|                                                 |                     |                                                                                                                                                 | +25 °C  | 44   | 58   | mA      | CY96F356      |
|                                                 |                     |                                                                                                                                                 | +125 °C | 46   | 62   |         |               |
|                                                 | I <sub>CCMAIN</sub> | Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4 MHz<br>1 Flash/ROM wait state (CLKPLL, CLKSC and CLKRC stopped)                                 | +25 °C  | 4    | 5    | mA      | CY96F353/F355 |
|                                                 |                     |                                                                                                                                                 | +125 °C | 4.7  | 8    |         |               |
|                                                 |                     |                                                                                                                                                 | +25 °C  | 4.2  | 5.2  | mA      | CY96F356      |
|                                                 |                     |                                                                                                                                                 | +125 °C | 4.9  | 8.2  |         |               |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                                       | Symbol             | Condition (at T <sub>A</sub> )                                                                                                                                                                            | Value              |                                                                                                                                                       |         | Remarks |                   |    |                   |
|-------------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------|-------------------|----|-------------------|
|                                                 |                    |                                                                                                                                                                                                           | Typ                | Max                                                                                                                                                   | Unit    |         |                   |    |                   |
| Power supply current in Run modes <sup>*1</sup> | I <sub>CCRCH</sub> | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2 MHz<br>1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped)                                                                                             | +25 °C             | 2.5                                                                                                                                                   | 3.5     | mA      | CY96F353/F355     |    |                   |
|                                                 |                    |                                                                                                                                                                                                           | +125 °C            | 3.2                                                                                                                                                   | 6.5     |         |                   |    |                   |
|                                                 |                    |                                                                                                                                                                                                           | +25 °C             | 2.7                                                                                                                                                   | 3.7     | mA      | CY96F356          |    |                   |
|                                                 |                    |                                                                                                                                                                                                           | +125 °C            | 3.4                                                                                                                                                   | 6.7     |         |                   |    |                   |
|                                                 | I <sub>CCRCL</sub> | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100 kHz, SMCR:LPMS = 0<br>1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)                                      | +25 °C             | 0.18                                                                                                                                                  | 0.3     | mA      | CY96F353/F355     |    |                   |
|                                                 |                    |                                                                                                                                                                                                           | +125 °C            | 0.73                                                                                                                                                  | 3.1     |         |                   |    |                   |
|                                                 |                    |                                                                                                                                                                                                           | +25 °C             | 0.4                                                                                                                                                   | 0.6     | mA      | CY96F356          |    |                   |
|                                                 |                    |                                                                                                                                                                                                           | +125 °C            | 0.95                                                                                                                                                  | 3.4     |         |                   |    |                   |
|                                                 |                    | RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100 kHz, SMCR:LPMS = 1<br>1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed) | +25 °C             | 0.15                                                                                                                                                  | 0.25    | mA      | CY96F353/F355/356 |    |                   |
|                                                 |                    |                                                                                                                                                                                                           | +125 °C            | 0.7                                                                                                                                                   | 3.05    |         |                   |    |                   |
|                                                 |                    |                                                                                                                                                                                                           | I <sub>CCSUB</sub> | Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32 kHz<br>1 Flash/ROM wait state (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed) | +25 °C  | 0.1     | 0.2               | mA | CY96F353/F355/356 |
|                                                 |                    |                                                                                                                                                                                                           |                    |                                                                                                                                                       | +125 °C | 0.65    | 3                 |    |                   |

$(T_A = -40\text{ }^{\circ}\text{C to } 125\text{ }^{\circ}\text{C}, V_{CC} = AV_{CC} = 3.0\text{ V to } 5.5\text{ V}, V_{SS} = AV_{SS} = 0\text{ V})$ 

| Parameter                              | Symbol              | Condition (at T <sub>A</sub> )                                                                                                     |                                                                                           | Value   |      |      | Remarks            |               |
|----------------------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|---------|------|------|--------------------|---------------|
|                                        |                     |                                                                                                                                    |                                                                                           | Typ     | Max  | Unit |                    |               |
| Power supply current in Sleep modes *1 | I <sub>CCSPLL</sub> | PLL Sleep mode with<br>CLKS1/2 = CLKP1 =<br>16MHz, CLKP2 = 8MHz<br>(CLKRC and CLKSC<br>stopped)                                    | +25 °C                                                                                    | 4       | 6    | mA   | CY96F353/F355/F356 |               |
|                                        |                     |                                                                                                                                    | +125 °C                                                                                   | 4.7     | 9    |      |                    |               |
|                                        |                     | PLL Sleep mode with<br>CLKS1/2 = CLKP1= 32MHz,<br>CLKP2 = 16MHz<br>(CLKRC and CLKSC<br>stopped)                                    | +25 °C                                                                                    | 7       | 9.5  | mA   | CY96F353/F355/F356 |               |
|                                        |                     |                                                                                                                                    | +125 °C                                                                                   | 8       | 12.5 |      |                    |               |
|                                        |                     | PLL Sleep mode with<br>CLKS1/2 = 48MHz,<br>CLKP1/2 = 24MHz<br>(CLKRC and CLKSC<br>stopped)                                         | +25 °C                                                                                    | 7       | 9    | mA   | CY96F353/F355/F356 |               |
|                                        |                     |                                                                                                                                    | +125 °C                                                                                   | 8       | 12   |      |                    |               |
|                                        |                     | PLL Sleep mode with<br>CLKS1/2 = CLKP1=<br>56MHz, CLKP2 = 28MHz<br>(CLKRC and CLKSC<br>stopped. Core voltage at<br>1.9V)           | +25 °C                                                                                    | 11      | 14.5 | mA   | CY96F353/F355/F356 |               |
|                                        |                     |                                                                                                                                    | +125 °C                                                                                   | 12      | 17.5 |      |                    |               |
|                                        |                     | PLL Sleep mode with<br>CLKS1/2 = 96MHz,<br>CLKP1= 48MHz,<br>CLKP2 = 24MHz<br>(CLKRC and CLKSC<br>stopped. Core voltage at<br>1.9V) | +25 °C                                                                                    | 12      | 15   | mA   | CY96F353/F355/F356 |               |
|                                        |                     |                                                                                                                                    | +125 °C                                                                                   | 13      | 18   |      |                    |               |
|                                        |                     | I <sub>CCSMAIN</sub>                                                                                                               | Main Sleep mode with<br>CLKS1/2 = CLKP1/2 = 4 MHz<br>(CLKPLL, CLKSC and CLKRC<br>stopped) | +25 °C  | 1    | 1.3  | mA                 | CY96F353/F355 |
|                                        |                     |                                                                                                                                    |                                                                                           | +125 °C | 1.6  | 4.1  |                    |               |
|                                        | +25 °C              |                                                                                                                                    |                                                                                           | 1.3     | 1.8  | mA   | CY96F356           |               |
|                                        | +125 °C             |                                                                                                                                    |                                                                                           | 1.9     | 4.6  |      |                    |               |
|                                        | I <sub>CCSRCH</sub> | RC Sleep mode with CLKS1/2<br>= CLKP1/2 = 2 MHz<br>(CLKMC, CLKPLL and CLKSC<br>stopped)                                            | +25 °C                                                                                    | 0.55    | 1.1  | mA   | CY96F353/F355      |               |
|                                        |                     |                                                                                                                                    | +125 °C                                                                                   | 1.15    | 3.9  |      |                    |               |
|                                        |                     |                                                                                                                                    | +25 °C                                                                                    | 0.8     | 1.4  | mA   | CY96F356           |               |
|                                        |                     |                                                                                                                                    | +125 °C                                                                                   | 1.4     | 4.2  |      |                    |               |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                                         | Symbol              | Condition (at T <sub>A</sub> )                                                                                                         | Value   |      |      | Remarks |                    |
|---------------------------------------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------|---------|------|------|---------|--------------------|
|                                                   |                     |                                                                                                                                        | Typ     | Max  | Unit |         |                    |
| Power supply current in Sleep modes <sup>*1</sup> | I <sub>CCSRCL</sub> | RC Sleep mode with CLKS1/2 = CLKP1/2 = 100 kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode) | +25 °C  | 0.08 | 0.2  | mA      | CY96F353/F355      |
|                                                   |                     |                                                                                                                                        | +125 °C | 0.59 | 2.95 |         |                    |
|                                                   |                     |                                                                                                                                        | +25 °C  | 0.3  | 0.5  | mA      | CY96F356           |
|                                                   |                     |                                                                                                                                        | +125 °C | 0.8  | 3.3  |         |                    |
|                                                   |                     | RC Sleep mode with CLKS1/2 = CLKP1/2 = 100 kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)  | +25 °C  | 0.05 | 0.15 | mA      | CY96F353/F355/F356 |
|                                                   |                     |                                                                                                                                        | +125 °C | 0.56 | 2.9  |         |                    |
|                                                   | I <sub>CCSSUB</sub> | Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32 kHz (CLKMC, CLKPLL and CLKRC stopped)                                                       | +25 °C  | 0.04 | 0.12 | mA      | CY96F353/F355/F356 |
|                                                   |                     |                                                                                                                                        | +125 °C | 0.53 | 2.9  |         |                    |
| Power supply current in Timer modes <sup>*1</sup> | I <sub>CCTPLL</sub> | PLL Timer mode with CLKMC = 4 MHz, CLKPLL = 48 MHz (CLKRC and CLKSC stopped.)                                                          | +25 °C  | 1.3  | 1.8  | mA      | CY96F353/F355      |
|                                                   |                     |                                                                                                                                        | +125 °C | 1.9  | 4.8  |         |                    |
|                                                   |                     |                                                                                                                                        | +25 °C  | 1.5  | 2    | mA      | CY96F356           |
|                                                   |                     |                                                                                                                                        | +125 °C | 2.1  | 5    |         |                    |

$(T_A = -40\text{ }^{\circ}\text{C to } 125\text{ }^{\circ}\text{C}, V_{CC} = AV_{CC} = 3.0\text{ V to } 5.5\text{ V}, V_{SS} = AV_{SS} = 0\text{ V})$ 

| Parameter                           | Symbol                                                                                                                  | Condition (at T <sub>A</sub> )                                                                                             | Value                                                                                                                      |         |       | Remarks |                    |                    |
|-------------------------------------|-------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|---------|-------|---------|--------------------|--------------------|
|                                     |                                                                                                                         |                                                                                                                            | Typ                                                                                                                        | Max     | Unit  |         |                    |                    |
| Power supply current in Timer modes | I <sub>CCTMAIN</sub>                                                                                                    | Main Timer mode with CLKMC = 4 MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode) | +25 °C                                                                                                                     | 0.11    | 0.2   | mA      | CY96F353/F355      |                    |
|                                     |                                                                                                                         |                                                                                                                            | +125 °C                                                                                                                    | 0.63    | 3     |         |                    |                    |
|                                     |                                                                                                                         |                                                                                                                            | +25 °C                                                                                                                     | 0.35    | 0.5   | mA      | CY96F356           |                    |
|                                     |                                                                                                                         |                                                                                                                            | +125 °C                                                                                                                    | 0.85    | 3.3   |         |                    |                    |
|                                     |                                                                                                                         | Main Timer mode with CLKMC = 4 MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)  | +25 °C                                                                                                                     | 0.08    | 0.15  | mA      | CY96F353/F355/F356 |                    |
|                                     |                                                                                                                         |                                                                                                                            | +125 °C                                                                                                                    | 0.6     | 2.9   |         |                    |                    |
|                                     |                                                                                                                         | I <sub>CCTRCH</sub>                                                                                                        | RC Timer mode with CLKRC = 2 MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)   | +25 °C  | 0.1   | 0.2     | mA                 | CY96F353/F355      |
|                                     |                                                                                                                         |                                                                                                                            |                                                                                                                            | +125 °C | 0.63  | 3       |                    |                    |
|                                     | +25 °C                                                                                                                  |                                                                                                                            |                                                                                                                            | 0.35    | 0.5   | mA      | CY96F356           |                    |
|                                     | +125 °C                                                                                                                 |                                                                                                                            |                                                                                                                            | 0.85    | 3.3   |         |                    |                    |
|                                     | RC Timer mode with CLKRC = 2 MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode) |                                                                                                                            | +25 °C                                                                                                                     | 0.07    | 0.15  | mA      | CY96F353/F355/F356 |                    |
|                                     |                                                                                                                         |                                                                                                                            | +125 °C                                                                                                                    | 0.6     | 2.9   |         |                    |                    |
|                                     | I <sub>CCTRCL</sub>                                                                                                     |                                                                                                                            | RC Timer mode with CLKRC = 100 kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode) | +25 °C  | 0.06  | 0.15    | mA                 | CY96F353/F355      |
|                                     |                                                                                                                         |                                                                                                                            |                                                                                                                            | +125 °C | 0.56  | 2.95    |                    |                    |
|                                     |                                                                                                                         | +25 °C                                                                                                                     |                                                                                                                            | 0.3     | 0.45  | mA      | CY96F356           |                    |
|                                     |                                                                                                                         | +125 °C                                                                                                                    |                                                                                                                            | 0.8     | 3.2   |         |                    |                    |
|                                     |                                                                                                                         | RC Timer mode with CLKRC = 100 kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)  | +25 °C                                                                                                                     | 0.03    | 0.1   | mA      | CY96F353/F355/F356 |                    |
|                                     |                                                                                                                         |                                                                                                                            | +125 °C                                                                                                                    | 0.53    | 2.85  |         |                    |                    |
|                                     |                                                                                                                         | I <sub>CCTSUB</sub>                                                                                                        | Sub Timer mode with CLKSC = 32 kHz (CLKMC, CLKPLL and CLKRC stopped)                                                       | +25 °C  | 0.035 | 0.1     | mA                 | CY96F353/F355/F356 |
|                                     |                                                                                                                         |                                                                                                                            |                                                                                                                            | +125 °C | 0.53  | 2.85    |                    |                    |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                                            | Symbol        | Condition (at $T_A$ )                                        | Value   |       |      | Remarks                                                                                    |
|------------------------------------------------------|---------------|--------------------------------------------------------------|---------|-------|------|--------------------------------------------------------------------------------------------|
|                                                      |               |                                                              | Typ     | Max   | Unit |                                                                                            |
| Power supply current in Stop Mode                    | $I_{CCH}$     | VRCR:LPMB[2:0] = 110 <sub>B</sub><br>(Core voltage at 1.8 V) | +25 °C  | 0.02  | 0.08 | mA<br>CY96F353/F355/F356                                                                   |
|                                                      |               |                                                              | +125 °C | 0.52  | 2.8  |                                                                                            |
|                                                      |               | VRCR:LPMB[2:0] = 000 <sub>B</sub><br>(Core voltage at 1.2 V) | +25 °C  | 0.015 | 0.06 | mA<br>CY96F353/F355/F356                                                                   |
|                                                      |               |                                                              | +125 °C | 0.4   | 2.3  |                                                                                            |
| Power supply current for active Low Voltage detector | $I_{CCLVD}$   | Low voltage detector enabled<br>(RCR:LVDE = 1)               | +25 °C  | 5     | 10   | $\mu\text{A}$<br>CY96F353/F355<br>Must be added to all current above                       |
|                                                      |               |                                                              | +125 °C | 7     | 20   |                                                                                            |
|                                                      |               |                                                              | +25 °C  | 90    | 140  | $\mu\text{A}$<br>CY96F356<br>Must be added to all current above                            |
|                                                      |               |                                                              | +125 °C | 100   | 150  |                                                                                            |
| Power supply current for active Clock modulator      | $I_{CCLOMO}$  | Clock modulator enabled<br>(CMCR:PDX = 1)                    | -       | 3     | 4.5  | $\text{mA}$<br>Must be added to all current above                                          |
| Flash Write/Erase current                            | $I_{CCFLASH}$ | Current for one Flash module                                 | -       | 15    | 40   | $\text{mA}$<br>Must be added to all current above                                          |
| Input capacitance                                    | $C_{IN}$      | -                                                            | -       | 5     | 15   | $\text{pF}$<br>Other than C, $AV_{CC}$ , $AV_{SS}$ , $AVRH$ , $AVRL$ , $V_{CC}$ , $V_{SS}$ |

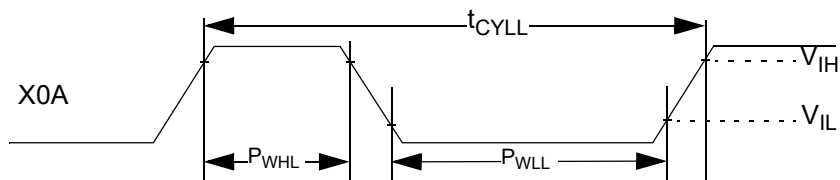
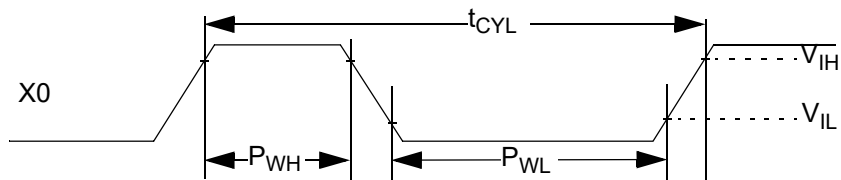
\*: The power supply current is measured with a 4 MHz external clock connected to the Main oscillator and a 32 kHz external clock connected to the Sub oscillator. See chapter "Standby mode and voltage regulator control circuit" of the Hardware Manual for further details about voltage regulator control.

## AC Characteristics

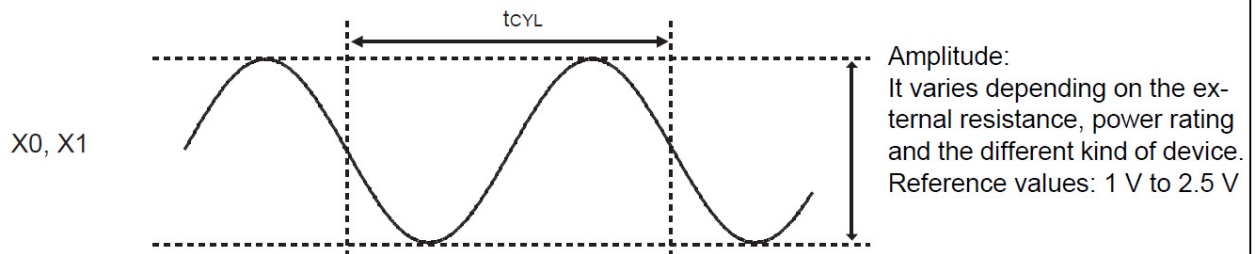
### Source Clock Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

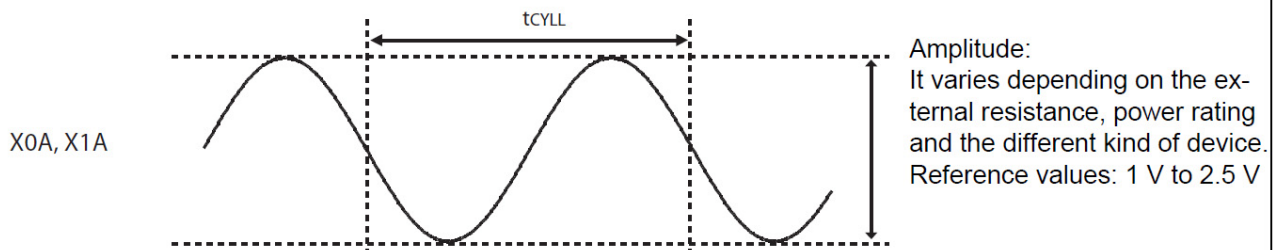
| Parameter                   | Symbol             | Pin      | Value                     |        |         | Unit          | Remarks                                                                                                                        |
|-----------------------------|--------------------|----------|---------------------------|--------|---------|---------------|--------------------------------------------------------------------------------------------------------------------------------|
|                             |                    |          | Min                       | Typ    | Max     |               |                                                                                                                                |
| Clock frequency             | $f_C$              | X0, X1   | 3                         | -      | 16      | MHz           | When using a crystal oscillator, PLL off                                                                                       |
|                             |                    |          | 0                         | -      | 16      | MHz           | When using an opposite phase external clock, PLL off                                                                           |
|                             |                    |          | 3.5                       | -      | 16      | MHz           | When using a crystal oscillator or opposite phase external clock, PLL on                                                       |
| Clock frequency             | $f_{FCI}$          | X0       | 0                         | -      | 56      | MHz           | When using a single phase external clock in "Fast Clock Input mode", PLL off                                                   |
|                             |                    |          | 3.5                       | -      | 56      | MHz           | When using a single phase external clock in "Fast Clock Input mode", PLL on                                                    |
| Clock frequency             | $f_{CL}$           | X0A, X1A | 32                        | 32.768 | 100     | kHz           | When using an oscillation circuit                                                                                              |
|                             |                    |          | 0                         | -      | 100     | kHz           | When using an opposite phase external clock                                                                                    |
|                             |                    | X0A      | 0                         | -      | 50      | kHz           | When using a single phase external clock                                                                                       |
| Clock frequency             | $f_{CR}$           | -        | 50                        | 100    | 200     | kHz           | When using slow frequency of RC oscillator                                                                                     |
|                             |                    |          | 1                         | 2      | 4       | MHz           | When using fast frequency of RC oscillator                                                                                     |
| RC clock stabilization time | $t_{RCSTAB}$       | -        | 64 or 256 RC clock cycles |        |         |               | Applied after any reset and when activating the RC oscillator.<br>CY96F356: 64 cycles<br>others: 256 cycles                    |
| PLL Clock frequency         | $f_{CLKVCO}$       | -        | 64                        | -      | 200     | MHz           | Permitted VCO output frequency of PLL (CLKVCO)                                                                                 |
| PLL Phase Jitter            | $T_{PSKEW}$        | -        | -                         | -      | $\pm 5$ | ns            | For CLKMC (PLL input clock) $\geq 4\text{ MHz}$ , jitter coming from external oscillator, crystal or resonator is not covered. |
| Input clock pulse width     | $P_{WH}, P_{WL}$   | X0, X1   | 8                         | -      | -       | ns            | Duty ratio is about 30 % to 70 %                                                                                               |
| Input clock pulse width     | $P_{WHL}, P_{WLL}$ | X0A, X1A | 5                         | -      | -       | $\mu\text{s}$ |                                                                                                                                |



#### When using an oscillation circuit



#### When using an oscillation circuit



### Internal Clock Timing

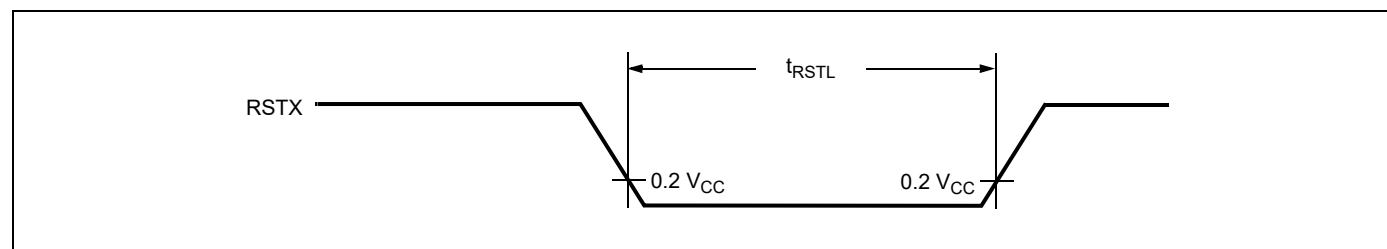
( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                                                                        | Symbol                                  | Core Voltage Settings |     |       |     | Unit | Remarks           |
|----------------------------------------------------------------------------------|-----------------------------------------|-----------------------|-----|-------|-----|------|-------------------|
|                                                                                  |                                         | 1.8 V                 |     | 1.9 V |     |      |                   |
|                                                                                  |                                         | Min                   | Max | Min   | Max |      |                   |
| Internal System clock frequency (CLKS1 and CLKS2)                                | f <sub>CLKS1</sub> , f <sub>CLKS2</sub> | 0                     | 92  | 0     | 96  | MHz  | Others than below |
|                                                                                  |                                         | 0                     | 88  | 0     | 96  | MHz  | CY96F356          |
| Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1) | f <sub>CLKB</sub> , f <sub>CLKP1</sub>  | 0                     | 52  | 0     | 56  | MHz  |                   |
| Internal peripheral clock frequency (CLKP2)                                      | f <sub>CLKP2</sub>                      | 0                     | 28  | 0     | 32  | MHz  |                   |

### External Reset Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

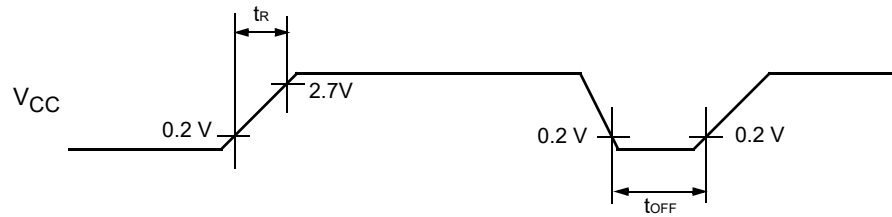
| Parameter        | Symbol     | Pin  | Value |     |     | Unit | Remarks |
|------------------|------------|------|-------|-----|-----|------|---------|
|                  |            |      | Min   | Typ | Max |      |         |
| Reset input time | $t_{RSTL}$ | RSTX | 500   | -   | -   | ns   |         |



### Power On Reset Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter          | Symbol    | Pin             | Value |     |     | Unit | Remarks |
|--------------------|-----------|-----------------|-------|-----|-----|------|---------|
|                    |           |                 | Min   | Typ | Max |      |         |
| Power on rise time | $t_R$     | V <sub>CC</sub> | 0.05  | -   | 30  | ms   |         |
| Power off time     | $t_{OFF}$ | V <sub>CC</sub> | 1     | -   | -   | ms   |         |



If the power supply is changed too rapidly, a power-on reset may occur.  
 We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

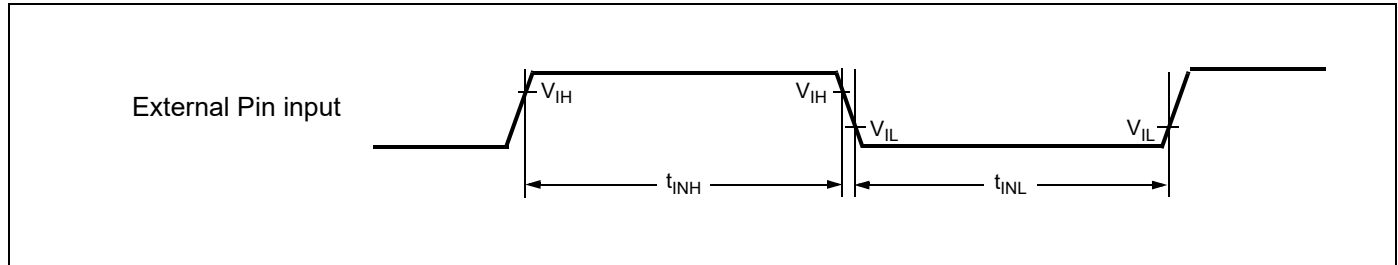


### External Input Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter         | Symbol                 | Pin       | Condition | Value                                                      |     | Unit | Used Pin Input Function           |
|-------------------|------------------------|-----------|-----------|------------------------------------------------------------|-----|------|-----------------------------------|
|                   |                        |           |           | Min                                                        | Max |      |                                   |
| Input pulse width | $t_{INH}$<br>$t_{INL}$ | INTn(_R)  | -         | 200                                                        | -   | ns   | External Interrupt                |
|                   |                        | NMI(_R)   |           |                                                            |     |      | NMI                               |
|                   |                        | Pnn_m     |           | $2 \cdot t_{CLKP1} + 200$<br>( $t_{CLKP1} = 1/f_{CLKP1}$ ) | -   | ns   | General Purpose IO                |
|                   |                        | TINn(_R)  |           |                                                            |     |      | Reload Timer                      |
|                   |                        | TTGn(_R)  |           |                                                            |     |      | PPG Trigger input                 |
|                   |                        | ADTG(_R)  |           |                                                            |     |      | AD Converter Trigger              |
|                   |                        | FRCKn(_R) |           |                                                            |     |      | Free Running Timer external clock |
|                   |                        | INn(_R)   |           |                                                            |     |      | Input Capture                     |
|                   |                        |           |           |                                                            |     |      |                                   |

Note : Relocated Resource Inputs have same characteristics



### External Bus Timing

Note: The values given below are for an I/O driving strength  $IO_{drive} = 5$  mA. If  $IO_{drive}$  is 2 mA, all the maximum output timing described in the different tables must then be increased by 10 ns.

### Basic Timing

( $T_A = -40$  °C to  $+125$  °C,  $V_{CC} = 5.0$  V  $\pm$  10 %,  $V_{SS} = 0.0$  V,  $IO_{drive} = 5$  mA,  $C_L = 50$  pF)

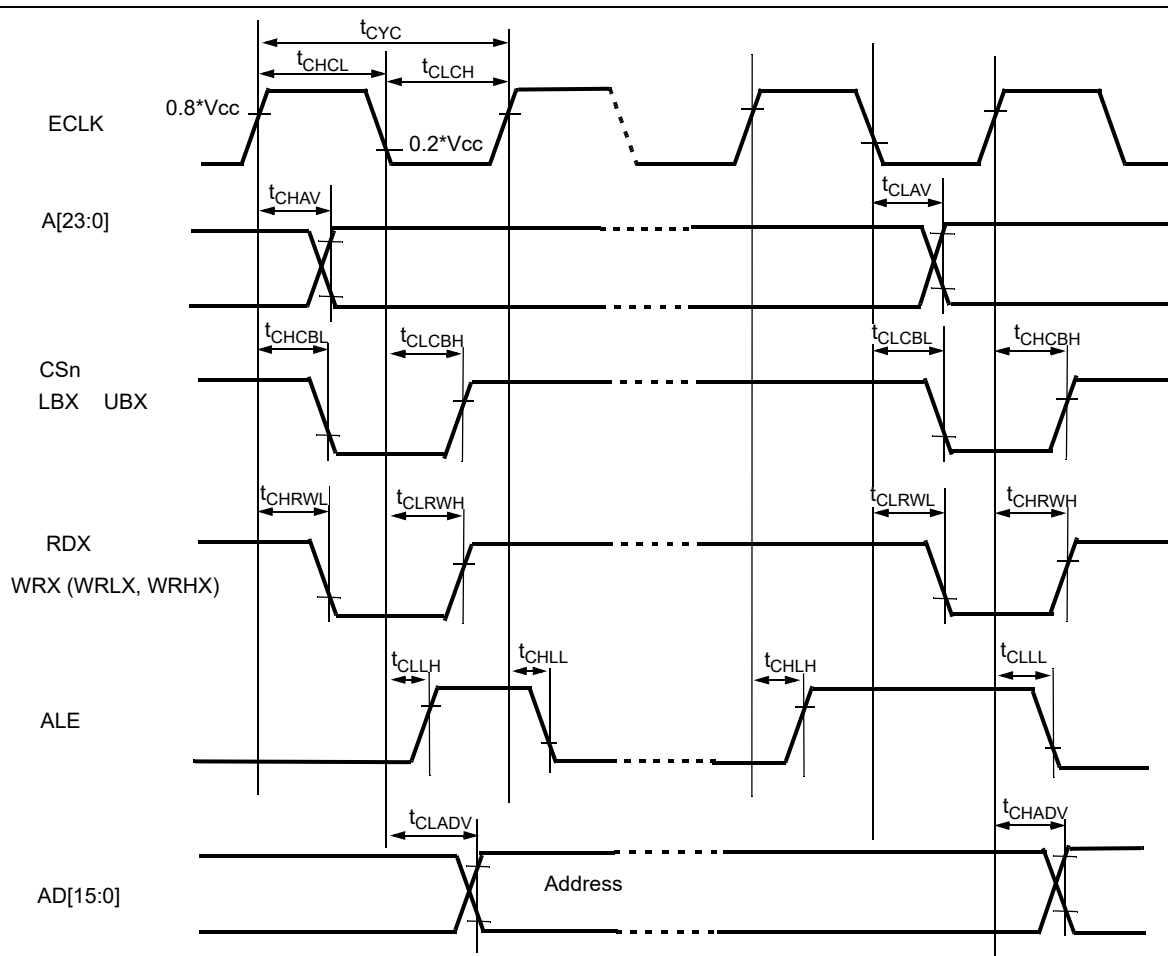
| Parameter                     | Symbol       | Pin                              | Condition | Value         |               | Unit | Remarks |
|-------------------------------|--------------|----------------------------------|-----------|---------------|---------------|------|---------|
|                               |              |                                  |           | Min           | Max           |      |         |
| ECLK                          | $t_{CYC}$    | ECLK                             | -         | 25            | -             | ns   |         |
|                               | $t_{CHCL}$   |                                  |           | $t_{CYC}/2-5$ | $t_{CYC}/2+5$ |      |         |
|                               | $t_{CLCH}$   |                                  |           | $t_{CYC}/2-5$ | $t_{CYC}/2+5$ |      |         |
| ECLK →<br>UBX/ LBX / CSn time | $t_{CHCBH}$  | CSn, UBX, LBX,<br>ECLK           | -         | -20           | +20           | ns   |         |
|                               | $t_{CHCBL}$  |                                  |           | -20           | +20           |      |         |
|                               | $t_{CLCBH}$  |                                  |           | -20           | +20           |      |         |
|                               | $t_{CLCBL}$  |                                  |           | -20           | +20           |      |         |
| ECLK → ALE time               | $t_{CHLH}$   | ALE, ECLK                        | -         | -10           | +10           | ns   |         |
|                               | $t_{CHLL}$   |                                  |           | -10           | +10           |      |         |
|                               | $t_{CLLH}$   |                                  |           | -10           | +10           |      |         |
|                               | $t_{CLLL}$   |                                  |           | -10           | +10           |      |         |
| ECLK → address valid time     | $t_{CHAV}$   | A[23:16], ECLK                   |           | -15           | +15           | ns   |         |
|                               | $t_{CLAV}$   |                                  |           | -15           | +15           |      |         |
|                               | $t_{CLADV}$  | AD[15:0], ECLK                   |           | -15           | +15           | ns   |         |
|                               | $t_{CHADV}$  |                                  |           | -15           | +15           |      |         |
| ECLK → RDX /WRX time          | $t_{CHRWLH}$ | RDX, WRX,<br>WRLX, WRHX,<br>ECLK | -         | -10           | +10           | ns   |         |
|                               | $t_{CHRWL}$  |                                  |           | -10           | +10           |      |         |
|                               | $t_{CLRWH}$  |                                  |           | -10           | +10           |      |         |
|                               | $t_{CLRWL}$  |                                  |           | -10           | +10           |      |         |

( $T_A = -40$  °C to  $+125$  °C,  $V_{CC} = 3.0$  to  $4.5$  V,  $V_{SS} = 0.0$  V,  $IO_{drive} = 5$  mA,  $C_L = 50$  pF)

| Parameter                     | Symbol      | Pin                    | Condition | Value         |               | Unit | Remarks |
|-------------------------------|-------------|------------------------|-----------|---------------|---------------|------|---------|
|                               |             |                        |           | Min           | Max           |      |         |
| ECLK                          | $t_{CYC}$   | ECLK                   | -         | 30            | -             | ns   |         |
|                               | $t_{CHCL}$  |                        |           | $t_{CYC}/2-8$ | $t_{CYC}/2+8$ |      |         |
|                               | $t_{CLCH}$  |                        |           | $t_{CYC}/2-8$ | $t_{CYC}/2+8$ |      |         |
| ECLK →<br>UBX/ LBX / CSn time | $t_{CHCBH}$ | CSn, UBX, LBX,<br>ECLK | -         | -25           | +25           | ns   |         |
|                               | $t_{CHCBL}$ |                        |           | -25           | +25           |      |         |
|                               | $t_{CLCBH}$ |                        |           | -25           | +25           |      |         |
|                               | $t_{CLCBL}$ |                        |           | -25           | +25           |      |         |
| ECLK → ALE time               | $t_{CHLH}$  | ALE, ECLK              | -         | -15           | +15           | ns   |         |
|                               | $t_{CHLL}$  |                        |           | -15           | +15           |      |         |
|                               | $t_{CLLH}$  |                        |           | -15           | +15           |      |         |
|                               | $t_{CLLL}$  |                        |           | -15           | +15           |      |         |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 3.0$  to  $4.5\text{V}$ ,  $V_{SS} = 0.0\text{V}$ ,  $I_{Odrive} = 5\text{mA}$ ,  $C_L = 50\text{pF}$ )

| Parameter                 | Symbol      | Pin                              | Condition | Value |     | Unit | Remarks |
|---------------------------|-------------|----------------------------------|-----------|-------|-----|------|---------|
|                           |             |                                  |           | Min   | Max |      |         |
| ECLK → address valid time | $t_{CHAV}$  | A[23:16], ECLK                   |           | -20   | +20 | ns   |         |
|                           | $t_{CLAV}$  |                                  |           | -20   | +20 |      |         |
|                           | $t_{CLADV}$ | AD[15:0], ECLK                   |           | -20   | +20 | ns   |         |
|                           | $t_{CHADV}$ |                                  |           | -20   | +20 |      |         |
| ECLK → RDX /WRX time      | $t_{CHRWL}$ | RDX, WRX,<br>WRLX, WRHX,<br>ECLK | -         | -15   | +15 | ns   |         |
|                           | $t_{CHRWL}$ |                                  |           | -15   | +15 |      |         |
|                           | $t_{CLRWH}$ |                                  |           | -15   | +15 |      |         |
|                           | $t_{CLRWL}$ |                                  |           | -15   | +15 |      |         |



Refer to the Hardware Manual for detailed Timing Charts

**Bus Timing (Read)**
 $(T_A = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{ mA}, C_L = 50\text{ pF})$ 

| Parameter                           | Symbol              | Pin                | Conditions                      | Value                   |                          | Unit | Remarks             |
|-------------------------------------|---------------------|--------------------|---------------------------------|-------------------------|--------------------------|------|---------------------|
|                                     |                     |                    |                                 | Min                     | Max                      |      |                     |
| ALE pulse width                     | t <sub>LHLL</sub>   | ALE                | EACL:STS=0 and EACL:ACE=0       | t <sub>CYC</sub> /2-5   | -                        | ns   |                     |
|                                     |                     |                    | EACL:STS=1                      | t <sub>CYC</sub> -5     | -                        |      |                     |
|                                     |                     |                    | EACL:STS=0 and EACL:ACE=1       | 3t <sub>CYC</sub> /2-5  | -                        |      |                     |
| Valid address<br>⇒ ALE ↓ time       | t <sub>AVLL</sub>   | ALE, A[23:16],     | EACL:STS=0 and EACL:ACE=0       | t <sub>CYC</sub> -15    | -                        | ns   |                     |
|                                     |                     |                    | EACL:STS=1 and EACL:ACE=0       | 3t <sub>CYC</sub> /2-15 | -                        |      |                     |
|                                     |                     |                    | EACL:STS=0 and EACL:ACE=1       | 2t <sub>CYC</sub> -15   | -                        |      |                     |
|                                     |                     |                    | EACL:STS=1 and EACL:ACE=1       | 5t <sub>CYC</sub> /2-15 | -                        |      |                     |
|                                     | t <sub>ADVLL</sub>  | ALE,AD[15:0]       | EACL:STS=0 and EACL:ACE=0       | t <sub>CYC</sub> /2-15  | -                        | ns   |                     |
|                                     |                     |                    | EACL:STS=1 and EACL:ACE=0       | t <sub>CYC</sub> -15    | -                        |      |                     |
|                                     |                     |                    | EACL:STS=0 and EACL:ACE=1       | 3t <sub>CYC</sub> /2-15 | -                        |      |                     |
|                                     |                     |                    | EACL:STS=1 and EACL:ACE=1       | 2t <sub>CYC</sub> -15   | -                        |      |                     |
| ALE ↓<br>⇒ Address valid time       | t <sub>LLAX</sub>   | ALE, AD[15:0]      | EACL:STS=0                      | t <sub>CYC</sub> /2-15  | -                        | ns   |                     |
|                                     |                     |                    | EACL:STS=1                      | -15                     | -                        |      |                     |
| Valid address<br>⇒ RDX ↓ time       | t <sub>AVRL</sub>   | RDX, A[23:16]      | EACL:ACE=0                      | 3t <sub>CYC</sub> /2-15 | -                        | ns   |                     |
|                                     |                     |                    | EACL:ACE=1                      | 5t <sub>CYC</sub> /2-15 | -                        |      |                     |
|                                     | t <sub>ADVRL</sub>  | RDX, AD[15:0]      | EACL:ACE=0                      | t <sub>CYC</sub> -15    | -                        | ns   |                     |
|                                     |                     |                    | EACL:ACE=1                      | 2t <sub>CYC</sub> -15   | -                        |      |                     |
| Valid address<br>⇒ Valid data input | t <sub>AVDV</sub>   | A[23:16], AD[15:0] | EACL:ACE=0                      | -                       | 3t <sub>CYC</sub> -55    | ns   | w/o cycle extension |
|                                     |                     |                    | EACL:ACE=1                      | -                       | 4t <sub>CYC</sub> -55    |      |                     |
|                                     | t <sub>ADV DV</sub> | AD[15:0]           | EACL:ACE=0                      | -                       | 5t <sub>CYC</sub> /2-55  | ns   | w/o cycle extension |
|                                     |                     |                    | EACL:ACE=1                      | -                       | 7t <sub>CYC</sub> /2-55  |      |                     |
| RDX pulse width                     | t <sub>RLRH</sub>   | RDX                | -                               | 3 t <sub>CYC</sub> /2-5 | -                        | ns   | w/o cycle extension |
| RDX ↓ ⇒ Valid data input            | t <sub>RLDV</sub>   | RDX, AD[15:0]      | -                               | -                       | 3 t <sub>CYC</sub> /2-50 | ns   | w/o cycle extension |
| RDX ↑ ⇒ Data hold time              | t <sub>RHDX</sub>   | RDX, AD[15:0]      | -                               | 0                       | -                        | ns   |                     |
| Address valid ⇒ Data hold time      | t <sub>AXDX</sub>   | A[23:16], AD[15:0] | -                               | 0                       | -                        | ns   |                     |
| RDX ↑ ⇒ ALE ↑ time                  | t <sub>RHLH</sub>   | RDX, ALE           | EACL:STS=1 and EACL:ACE=1       | 3t <sub>CYC</sub> /2-10 | -                        | ns   |                     |
|                                     |                     |                    | other ECL:STS, EACL:ACE setting | t <sub>CYC</sub> /2-10  | -                        |      |                     |

$(T_A = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{ mA}, C_L = 50\text{ pF})$ 

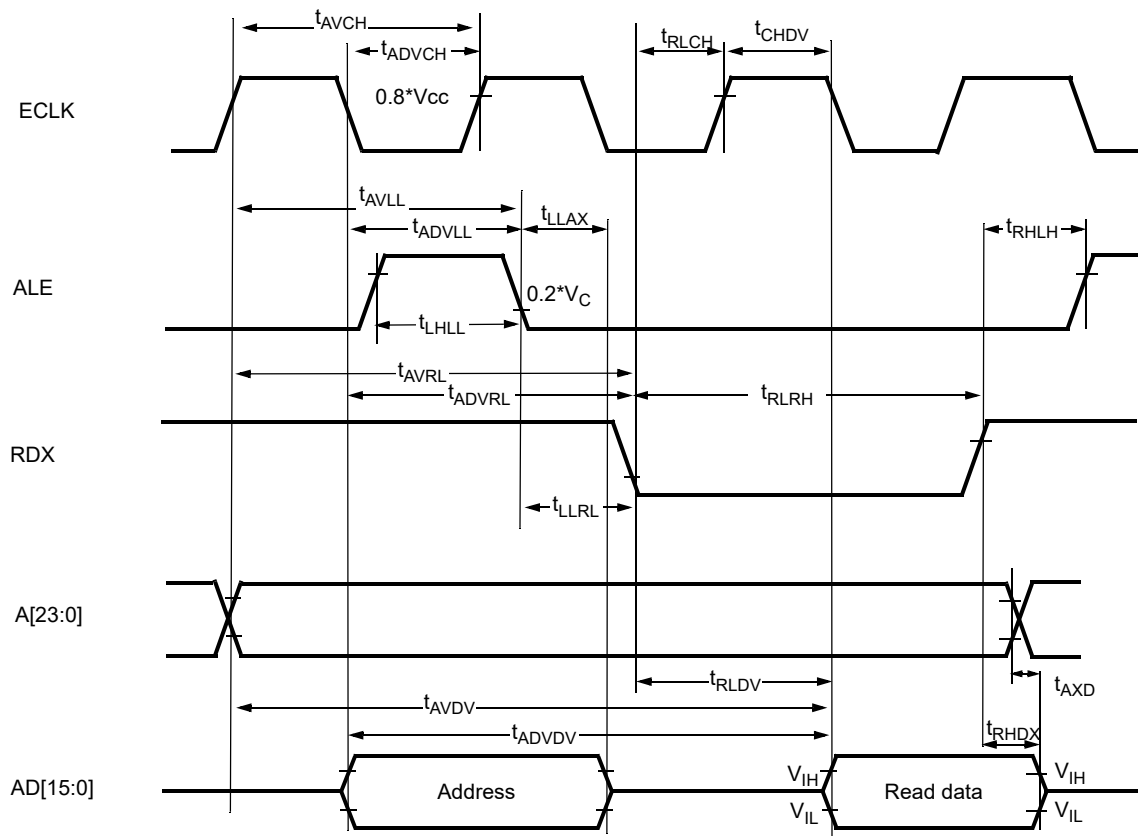
| Parameter                      | Symbol             | Pin            | Conditions | Value                  |                       | Unit | Remarks |
|--------------------------------|--------------------|----------------|------------|------------------------|-----------------------|------|---------|
|                                |                    |                |            | Min                    | Max                   |      |         |
| Valid address<br>⇒ ECLK ↑ time | t <sub>AVCH</sub>  | A[23:16], ECLK | -          | t <sub>CYC</sub> -15   | -                     | ns   |         |
|                                | t <sub>ADVCH</sub> | AD[15:0], ECLK | -          | t <sub>CYC</sub> /2-15 | -                     |      |         |
| RDX ↓ ⇒ ECLK ↑ time            | t <sub>RLCH</sub>  | RDX, ECLK      | -          | t <sub>CYC</sub> /2-10 | -                     | ns   |         |
| ALE ↓ ⇒ RDX ↓ time             | t <sub>LLRL</sub>  | ALE, RDX       | EACL:STS=0 | t <sub>CYC</sub> /2-10 | -                     | ns   |         |
|                                |                    |                | EACL:STS=1 | -10                    | -                     |      |         |
| ECLK ↑ ⇒ Valid data input      | t <sub>CHDV</sub>  | AD[15:0], ECLK | -          | -                      | t <sub>CYC</sub> - 50 | ns   |         |

 $(T_A = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}, V_{CC} = 3.0\text{ to } 4.5\text{ V}, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{ mA}, C_L = 50\text{ pF})$ 

| Parameter                           | Sym-<br>bol         | Pin                | Conditions                | Value                   |                         | Unit | Remarks             |
|-------------------------------------|---------------------|--------------------|---------------------------|-------------------------|-------------------------|------|---------------------|
|                                     |                     |                    |                           | Min                     | Max                     |      |                     |
| ALE pulse width                     | t <sub>LHLL</sub>   | ALE                | EACL:STS=0 and EACL:ACE=0 | t <sub>CYC</sub> /2-8   | -                       | ns   | EBM:NMS = 0         |
|                                     |                     |                    | EACL:STS=1                | t <sub>CYC</sub> -8     | -                       |      |                     |
|                                     |                     |                    | EACL:STS=0 and EACL:ACE=1 | 3t <sub>CYC</sub> /2-8  | -                       |      |                     |
| Valid address<br>⇒ ALE ↓ time       | t <sub>AVLL</sub>   | ALE, A[23:16],     | EACL:STS=0 and EACL:ACE=0 | t <sub>CYC</sub> -20    | -                       | ns   |                     |
|                                     |                     |                    | EACL:STS=1 and EACL:ACE=0 | 3t <sub>CYC</sub> /2-20 | -                       |      |                     |
|                                     |                     |                    | EACL:STS=0 and EACL:ACE=1 | 2t <sub>CYC</sub> -20   | -                       |      |                     |
|                                     |                     |                    | EACL:STS=1 and EACL:ACE=1 | 5t <sub>CYC</sub> /2-20 | -                       |      |                     |
|                                     | t <sub>ADVLL</sub>  | ALE, AD[15:0]      | EACL:STS=0 and EACL:ACE=0 | t <sub>CYC</sub> /2-20  | -                       | ns   |                     |
|                                     |                     |                    | EACL:STS=1 and EACL:ACE=0 | t <sub>CYC</sub> -20    | -                       |      |                     |
|                                     |                     |                    | EACL:STS=0 and EACL:ACE=1 | 3t <sub>CYC</sub> /2-20 | -                       |      |                     |
|                                     |                     |                    | EACL:STS=1 and EACL:ACE=1 | 2t <sub>CYC</sub> -20   | -                       |      |                     |
| ALE ↓<br>⇒ Address valid time       | t <sub>LLAX</sub>   | ALE, AD[15:0]      | EACL:STS=0                | t <sub>CYC</sub> /2-20  | -                       | ns   |                     |
|                                     |                     |                    | EACL:STS=1                | -20                     | -                       |      |                     |
| Valid address<br>⇒ RDX ↓ time       | t <sub>AVRL</sub>   | RDX, A[23:16]      | EACL:ACE=0                | 3t <sub>CYC</sub> /2-20 | -                       | ns   |                     |
|                                     |                     |                    | EACL:ACE=1                | 5t <sub>CYC</sub> /2-20 | -                       |      |                     |
|                                     | t <sub>ADVRL</sub>  | RDX, AD[15:0]      | EACL:ACE=0                | t <sub>CYC</sub> -20    | -                       | ns   |                     |
|                                     |                     |                    | EACL:ACE=1                | 2t <sub>CYC</sub> -20   | -                       |      |                     |
| Valid address<br>⇒ Valid data input | t <sub>AVDV</sub>   | A[23:16], AD[15:0] | EACL:ACE=0                | -                       | 3t <sub>CYC</sub> -60   | ns   | w/o cycle extension |
|                                     |                     |                    | EACL:ACE=1                | -                       | 4t <sub>CYC</sub> -60   |      |                     |
|                                     | t <sub>ADV DV</sub> | AD[15:0]           | EACL:ACE=0                | -                       | 5t <sub>CYC</sub> /2-60 | ns   | w/o cycle extension |
|                                     |                     |                    | EACL:ACE=1                | -                       | 7t <sub>CYC</sub> /2-60 |      |                     |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 3.0$  to  $4.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $I_{O_{drive}} = 5\text{ mA}$ ,  $C_L = 50\text{ pF}$ )

| Parameter                                          | Symbol      | Pin            | Conditions                      | Value           |                 | Unit | Remarks             |
|----------------------------------------------------|-------------|----------------|---------------------------------|-----------------|-----------------|------|---------------------|
|                                                    |             |                |                                 | Min             | Max             |      |                     |
| RDX pulse width                                    | $t_{RLRH}$  | RDX            | -                               | $3t_{CYC}/2-8$  | -               | ns   | w/o cycle extension |
| RDX $\downarrow \Rightarrow$ Valid data input      | $t_{RLDV}$  | RDX, AD[15:0]  | -                               | -               | $3t_{CYC}/2-55$ | ns   | w/o cycle extension |
| RDX $\uparrow \Rightarrow$ Data hold time          | $t_{RHDX}$  | RDX, AD[15:0]  | -                               | 0               | -               | ns   |                     |
| Address valid $\Rightarrow$ Data hold time         | $t_{AXDX}$  | A[23:0]        | -                               | 0               | -               | ns   |                     |
| RDX $\uparrow \Rightarrow$ ALE $\uparrow$ time     | $t_{RHLH}$  | RDX, ALE       | EACL:STS=1 and EACL:ACE=1       | $3t_{CYC}/2-15$ | -               | ns   |                     |
|                                                    |             |                | other ECL:STS, EACL:ACE setting | $t_{CYC}/2-15$  | -               |      |                     |
| Valid address $\Rightarrow$ ECLK $\uparrow$ time   | $t_{AVCH}$  | A[23:0], ECLK  | -                               | $t_{CYC}-20$    | -               | ns   |                     |
|                                                    | $t_{ADVCH}$ | AD[15:0], ECLK |                                 | $t_{CYC}/2-20$  | -               |      |                     |
| RDX $\downarrow \Rightarrow$ ECLK $\uparrow$ time  | $t_{RLCH}$  | RDX, ECLK      | -                               | $t_{CYC}/2-15$  | -               | ns   |                     |
| ALE $\downarrow \Rightarrow$ RDX $\downarrow$ time | $t_{LLRL}$  | ALE, RDX       | EACL:STS=0                      | $t_{CYC}/2-15$  | -               | ns   |                     |
|                                                    |             |                | EACL:STS=1                      | -15             | -               |      |                     |
| ECLK $\uparrow \Rightarrow$ Valid data input       | $t_{CHDV}$  | AD[15:0], ECLK | -                               | -               | $t_{CYC}-55$    | ns   |                     |



Refer to the Hardware Manual for detailed Timing Charts

**Bus Timing (Write)**
 $(T_A = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{ mA}, C_L = 50\text{ pF})$ 

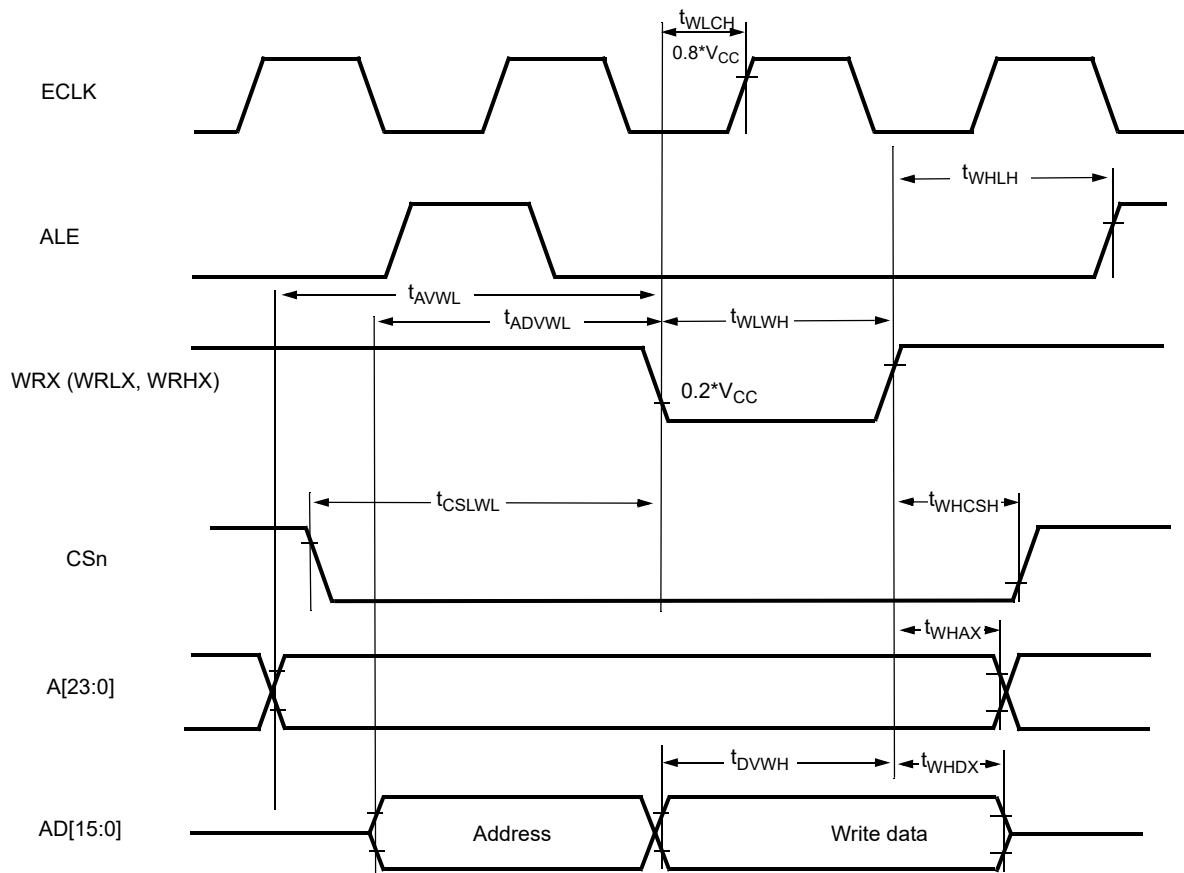
| Parameter                         | Symbol      | Pin                          | Condition                                | Value           |                 | Unit | Remarks             |
|-----------------------------------|-------------|------------------------------|------------------------------------------|-----------------|-----------------|------|---------------------|
|                                   |             |                              |                                          | Min             | Max             |      |                     |
| Valid address<br>⇒ WRX ↓ time     | $t_{AVWL}$  | WRX, WRLX,<br>WRHX, A[23:16] | EACL:ACE=0                               | $3t_{CYC}/2-15$ | -               | ns   |                     |
|                                   |             |                              | EACL:ACE=1                               | $5t_{CYC}/2-15$ | -               |      |                     |
|                                   | $t_{ADVWL}$ | WRX, WRLX,<br>WRHX, AD[15:0] | EACL:ACE=0                               | $t_{CYC}-15$    | -               | ns   |                     |
|                                   |             |                              | EACL:ACE=1                               | $2t_{CYC}-15$   | -               |      |                     |
| WRX pulse width                   | $t_{WLWH}$  | WRX, WRLX,<br>WRHX           | -                                        | $t_{CYC}-5$     | -               | ns   | w/o cycle extension |
| Valid data output<br>⇒ WRX ↑ time | $t_{DVWH}$  | WRX, WRLX,<br>WRHX, AD[15:0] | -                                        | $t_{CYC}-20$    | -               | ns   | w/o cycle extension |
| WRX ↑<br>⇒ Data hold time         | $t_{WHDX}$  | WRX, WRLX,<br>WRHX, AD[15:0] | -                                        | $t_{CYC}/2-15$  | -               | ns   |                     |
| WRX ↑<br>⇒ Address valid time     | $t_{WHAX}$  | WRX, WRLX,<br>WRHX, A[23:16] | EBM:NMS=0                                | $t_{CYC}/2-15$  | -               | ns   |                     |
| WRX ↑ ⇒ ALE ↑ time                | $t_{WHLH}$  | WRX, WRLX,<br>WRHX, ALE      | EBM:ACE=1 and<br>EACL:STS=1              | $2t_{CYC}-10$   | -               | ns   |                     |
|                                   |             |                              | other EBM:ACE<br>and<br>EACL:STS setting | $t_{CYC}-10$    | -               |      |                     |
| WRX ↓ ⇒ ECLK ↑ time               | $t_{WLCH}$  | WRX, WRLX,<br>WRHX, ECLK     | -                                        | $t_{CYC}/2-10$  | -               | ns   |                     |
| CSn ⇒ WRX time                    | $t_{CSLWL}$ | WRX, WRLX,<br>WRHX, CSn      | EACL:ACE=0<br>EBM:NMS=0                  | -               | $3t_{CYC}/2-15$ | ns   |                     |
|                                   |             |                              | EACL:ACE=1<br>EBM:NMS=0                  | -               | $5t_{CYC}/2-15$ |      |                     |
| WRX ⇒ CSn time                    | $t_{WHCSH}$ | WRX, WRLX,<br>WRHX, CSn      | EBM:NMS=0                                | $t_{CYC}/2-15$  | -               | ns   |                     |

 $(T_A = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}, V_{CC} = 3.0\text{ to } 4.5\text{ V}, V_{SS} = 0.0\text{ V}, I_{Odrive} = 5\text{ mA}, C_L = 50\text{ pF})$ 

| Parameter                     | Symbol      | Pin                          | Condition  | Value           |     | Unit | Remarks |
|-------------------------------|-------------|------------------------------|------------|-----------------|-----|------|---------|
|                               |             |                              |            | Min             | Max |      |         |
| Valid address<br>⇒ WRX ↓ time | $t_{AVWL}$  | WRX, WRLX,<br>WRHX, A[23:16] | EACL:ACE=0 | $3t_{CYC}/2-20$ | -   | ns   |         |
|                               |             |                              | EACL:ACE=1 | $5t_{CYC}/2-20$ | -   |      |         |
|                               | $t_{ADVWL}$ | WRX, WRLX,<br>WRHX, AD[15:0] | EACL:ACE=0 | $t_{CYC}-20$    | -   | ns   |         |
|                               |             |                              | EACL:ACE=1 | $2t_{CYC}-20$   | -   |      |         |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 3.0$  to  $4.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $I_{Odrive} = 5\text{ mA}$ ,  $C_L = 50\text{ pF}$ )

| Parameter                         | Symbol      | Pin                       | Condition                          | Value          |                 | Unit | Remarks             |
|-----------------------------------|-------------|---------------------------|------------------------------------|----------------|-----------------|------|---------------------|
|                                   |             |                           |                                    | Min            | Max             |      |                     |
| WRX pulse width                   | $t_{WLWH}$  | WRX, WRXL, WRHX           | -                                  | $t_{CYC}-8$    | -               | ns   | w/o cycle extension |
| Valid data output<br>⇒ WRX ↑ time | $t_{DVWH}$  | WRX, WRLX, WRHX, AD[15:0] | -                                  | $t_{CYC}-25$   | -               | ns   | w/o cycle extension |
| WRX ↑<br>⇒ Data hold time         | $t_{WHDX}$  | WRX, WRLX, WRHX, AD[15:0] | -                                  | $t_{CYC}/2-20$ | -               | ns   |                     |
| WRX ↑<br>⇒ Address valid time     | $t_{WHAX}$  | WRX, WRLX, WRHX, A[23:16] | -                                  | $t_{CYC}/2-20$ | -               | ns   |                     |
| WRX ↑ ⇒ ALE ↑ time                | $t_{WHLH}$  | WRX, WRLX, WRHX, ALE      | EBM:ACE=1 and EACL:STS=1           | $2t_{CYC}-15$  | -               | ns   |                     |
|                                   |             |                           | other EBM:ACE and EACL:STS setting | $t_{CYC}-15$   | -               |      |                     |
| WRX ↓ ⇒ ECLK ↑ time               | $t_{WLCH}$  | WRX, WRLX, WRHX, ECLK     | -                                  | $t_{CYC}/2-15$ | -               | ns   |                     |
| CSn ⇒ WRX time                    | $t_{CSLWL}$ | WRX, WRLX, WRHX, CSn      | EACL:ACE=0                         | -              | $3t_{CYC}/2-20$ | ns   |                     |
|                                   |             |                           | EACL:ACE=1                         | -              | $5t_{CYC}/2-20$ |      |                     |
| WRX ⇒ CSn time                    | $t_{WHCSH}$ | WRX, WRLX, WRHX, CSn      | -                                  | $t_{CYC}/2-20$ | -               | ns   |                     |



Refer to the Hardware Manual for detailed Timing Charts

### Ready Input Timing

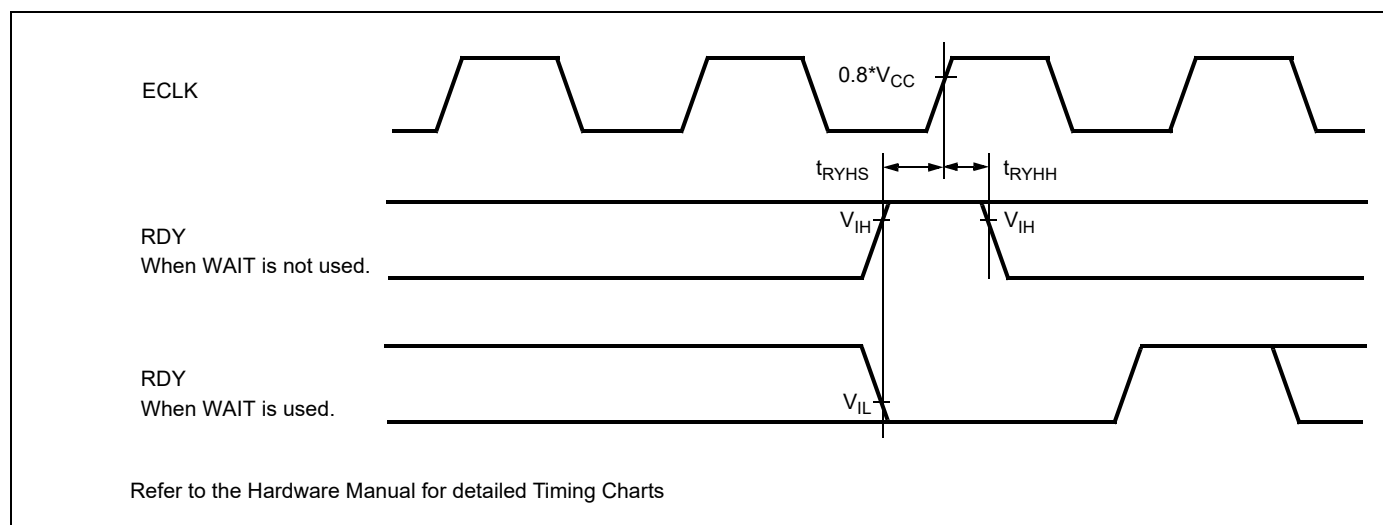
( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $I_{Odrive} = 5\text{ mA}$ ,  $C_L = 50\text{ pF}$ )

| Parameter      | Symbol     | Pin | Test Condition | Rated Value |     | Units | Remarks |
|----------------|------------|-----|----------------|-------------|-----|-------|---------|
|                |            |     |                | Min         | Max |       |         |
| RDY setup time | $t_{RYHS}$ | RDY | -              | 35          | -   | ns    |         |
| RDY hold time  | $t_{RYHH}$ | RDY |                | 0           | -   | ns    |         |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 3.0$  to  $4.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $I_{Odrive} = 5\text{ mA}$ ,  $C_L = 50\text{ pF}$ )

| Parameter      | Symbol     | Pin | Test Condition | Rated Value |     | Units | Remarks |
|----------------|------------|-----|----------------|-------------|-----|-------|---------|
|                |            |     |                | Min         | Max |       |         |
| RDY setup time | $t_{RYHS}$ | RDY | -              | 45          | -   | ns    |         |
| RDY hold time  | $t_{RYHH}$ | RDY |                | 0           | -   | ns    |         |

Note : If the RDY setup time is insufficient, use the auto-ready function.



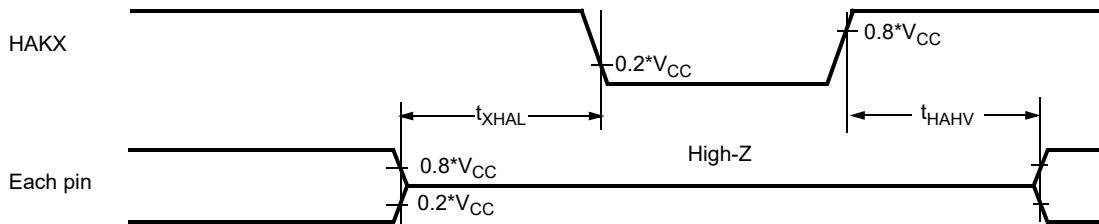
### Hold Timing

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $I_{Odrive} = 5\text{ mA}$ ,  $C_L = 50\text{ pF}$ )

| Parameter                                         | Symbol     | Pin  | Condition | Value        |                | Units | Remarks |
|---------------------------------------------------|------------|------|-----------|--------------|----------------|-------|---------|
|                                                   |            |      |           | Min          | Max            |       |         |
| Pin floating $\Rightarrow$ HAKX $\downarrow$ time | $t_{XHAL}$ | HAKX | -         | $t_{CYC}-20$ | $t_{CYC} + 20$ | ns    |         |
| HAKX $\uparrow$ time $\Rightarrow$ Pin valid time | $t_{HAHV}$ | HAKX |           | $t_{CYC}-20$ | $t_{CYC} + 20$ | ns    |         |

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $V_{CC} = 3.0$  to  $4.5\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $I_{Odrive} = 5\text{ mA}$ ,  $C_L = 50\text{ pF}$ )

| Parameter                                         | Symbol     | Pin  | Condition | Value        |                | Units | Remarks |
|---------------------------------------------------|------------|------|-----------|--------------|----------------|-------|---------|
|                                                   |            |      |           | Min          | Max            |       |         |
| Pin floating $\Rightarrow$ HAKX $\downarrow$ time | $t_{XHAL}$ | HAKX | -         | $t_{CYC}-25$ | $t_{CYC} + 25$ | ns    |         |
| HAKX $\uparrow$ time $\Rightarrow$ Pin valid time | $t_{HAHV}$ | HAKX |           | $t_{CYC}-25$ | $t_{CYC} + 25$ | ns    |         |



Refer to the Hardware Manual for detailed Timing Charts

### USART Timing

Note: The values given below are for an I/O driving strength  $IO_{drive} = 5$  mA. If  $IO_{drive}$  is 2 mA, all the maximum output timing described in the different tables must then be increased by 10 ns.

( $T_A = -40$  °C to 125 °C,  $V_{CC} = 3.0$  V to 5.5 V,  $V_{SS} = AV_{SS} = 0$  V,  $IO_{drive} = 5$  mA,  $C_L = 50$  pF)

| Parameter                    | Symbol      | Pin        | Condition                 | $V_{CC} = AV_{CC} = 4.5$ V to 5.5 V |                    | $V_{CC} = AV_{CC} = 3.0$ V to 4.5 V |                    | Unit |
|------------------------------|-------------|------------|---------------------------|-------------------------------------|--------------------|-------------------------------------|--------------------|------|
|                              |             |            |                           | Min                                 | Max                | Min                                 | Max                |      |
| Serial clock cycle time      | $t_{SCYCI}$ | SCKn       | Internal Shift Clock Mode | $4 t_{CLKP1}$                       | -                  | $4 t_{CLKP1}$                       | -                  | ns   |
| SCK ↓ → SOT delay time       | $t_{SLOVI}$ | SCKn, SOTn |                           | -20                                 | +20                | -30                                 | +30                | ns   |
| SOT → SCK ↑ delay time       | $t_{OVSHI}$ | SCKn, SOTn |                           | $N * t_{CLKP1} - 20$                | -                  | $N * t_{CLKP1} - 30$                | -                  | ns   |
| Valid SIN → SCK ↑            | $t_{IVSHI}$ | SCKn, SINn |                           | $t_{CLKP1} + 45$                    | -                  | $t_{CLKP1} + 55$                    | -                  | ns   |
| SCK ↑ → Valid SIN hold time  | $t_{SHIXI}$ | SCKn, SINn |                           | 0                                   | -                  | 0                                   | -                  | ns   |
| Serial clock "L" pulse width | $t_{LSHE}$  | SCKn       | External Shift Clock Mode | $t_{CLKP1} + 10$                    | -                  | $t_{CLKP1} + 10$                    | -                  | ns   |
| Serial clock "H" pulse width | $t_{HSLE}$  | SCKn       |                           | $t_{CLKP1} + 10$                    | -                  | $t_{CLKP1} + 10$                    | -                  | ns   |
| SCK ↓ → SOT delay time       | $t_{SLOVE}$ | SCKn, SOTn |                           | -                                   | $2 t_{CLKP1} + 45$ | -                                   | $2 t_{CLKP1} + 55$ | ns   |
| Valid SIN → SCK ↑            | $t_{IVSHE}$ | SCKn, SINn |                           | $t_{CLKP1}/2 + 10$                  | -                  | $t_{CLKP1}/2 + 10$                  | -                  | ns   |
| SCK ↑ → Valid SIN hold time  | $t_{SHIXE}$ | SCKn, SINn |                           | $t_{CLKP1} + 10$                    | -                  | $t_{CLKP1} + 10$                    | -                  | ns   |
| SCK fall time                | $t_{FE}$    | SCKn       |                           | -                                   | 20                 | -                                   | 20                 | ns   |
| SCK rise time                | $t_{RE}$    | SCKn       |                           | -                                   | 20                 | -                                   | 20                 | ns   |

#### Notes:

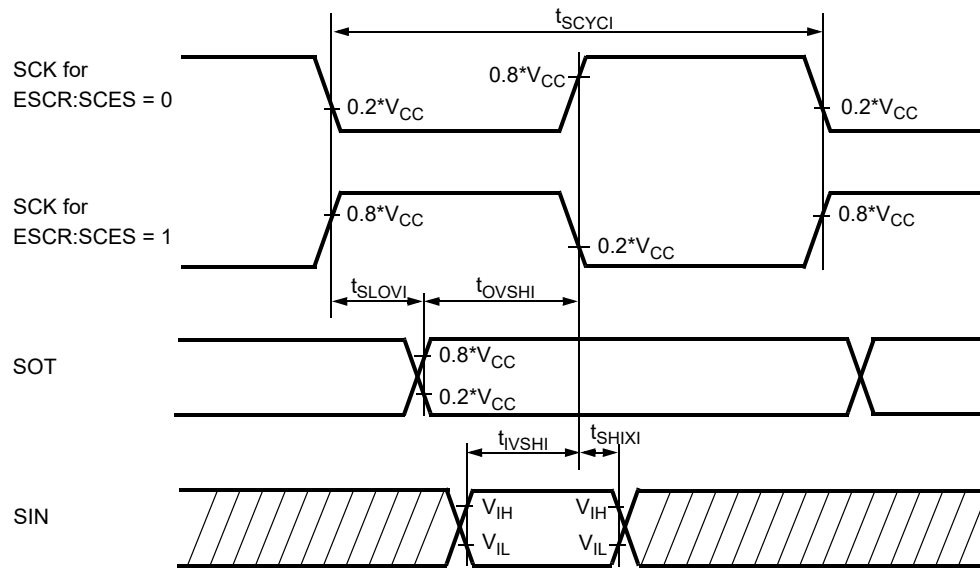
- AC characteristic in CLK synchronized mode.
- $C_L$  is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "CY96300 Super series Hardware Manual"
- $t_{CLKP1}$  is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

\*1: Parameter N depends on  $t_{SCYCI}$  and can be calculated as follows:

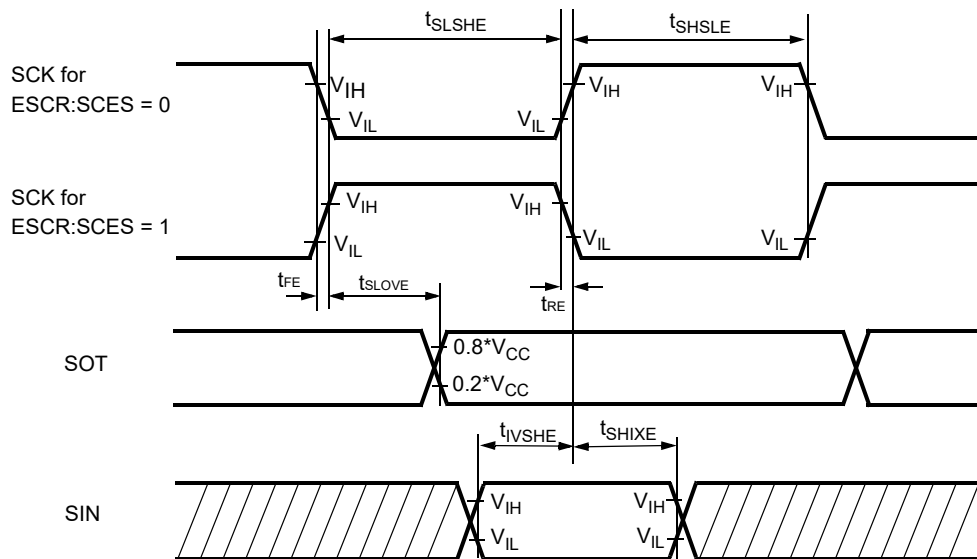
- if  $t_{SCYCI} = 2 * k * t_{CLKP1}$ , then  $N = k$ , where k is an integer > 2
- if  $t_{SCYCI} = (2 * k + 1) * t_{CLKP1}$ , then  $N = k + 1$ , where k is an integer > 1

Examples:

| $t_{SCYCI}$                    | N   |
|--------------------------------|-----|
| $4 * t_{CLKP1}$                | 2   |
| $5 * t_{CLKP1}, 6 * t_{CLKP1}$ | 3   |
| $7 * t_{CLKP1}, 8 * t_{CLKP1}$ | 4   |
| ...                            | ... |



**Internal Shift Clock Mode**



**External Shift Clock Mode**

## I<sup>2</sup>C Timing

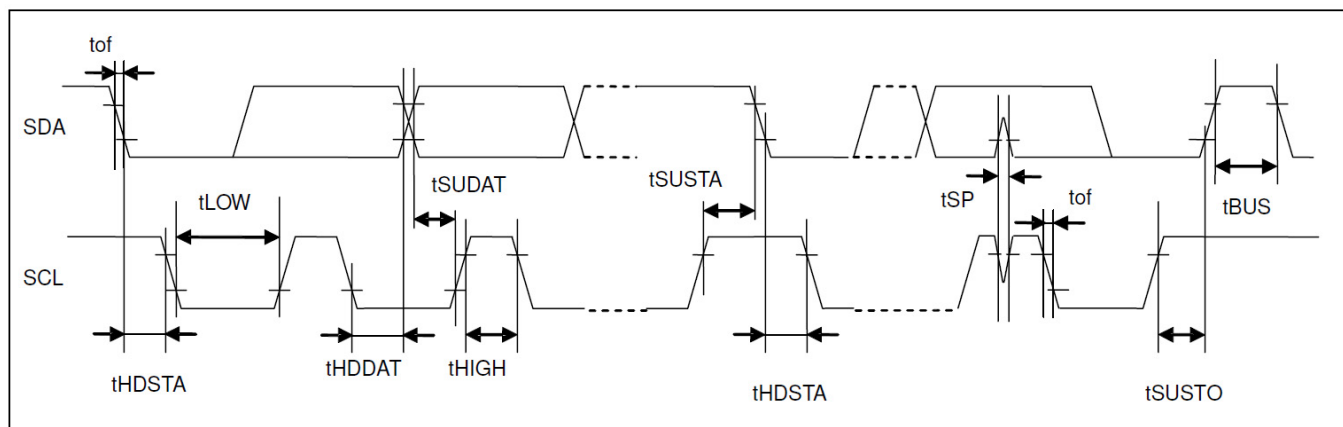
(T<sub>A</sub> = -40 °C to 125 °C, V<sub>CC</sub> = AV<sub>CC</sub> = 3.0 V to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

| Parameter                                                                                                    | Symbol             | Standard-mode                         |      | Fast-mode <sup>*1</sup>               |                                    | Unit |
|--------------------------------------------------------------------------------------------------------------|--------------------|---------------------------------------|------|---------------------------------------|------------------------------------|------|
|                                                                                                              |                    | Min                                   | Max  | Min                                   | Max                                |      |
| SCL clock frequency                                                                                          | f <sub>SCL</sub>   | 0                                     | 100  | 0                                     | 400                                | kHz  |
| Hold time (repeated) START condition<br>SDA↓→SCL↓                                                            | t <sub>HDSTA</sub> | 4.0                                   | -    | 0.6                                   | -                                  | μs   |
| "L" width of the SCL clock                                                                                   | t <sub>LOW</sub>   | 4.7                                   | -    | 1.3                                   | -                                  | μs   |
| "H" width of the SCL clock                                                                                   | t <sub>HIGH</sub>  | 4.0                                   | -    | 0.6                                   | -                                  | μs   |
| Set-up time for a repeated START condition<br>SCL↑→SDA↓                                                      | t <sub>SUSTA</sub> | 4.7                                   | -    | 0.6                                   | -                                  | μs   |
| Data hold time<br>SCL↓→SDA↓↑                                                                                 | t <sub>HDDAT</sub> | 0                                     | 3.45 | 0                                     | 0.9                                | μs   |
| Data set-up time<br>SDA↓↑→SCL↑                                                                               | t <sub>SUDAT</sub> | 250                                   | -    | 100                                   | -                                  | ns   |
| Set-up time for STOP condition<br>SCL↑→SDA↑                                                                  | t <sub>SUSTO</sub> | 4.0                                   | -    | 0.6                                   | -                                  | μs   |
| Bus free time between a STOP and START condition                                                             | t <sub>BUS</sub>   | 4.7                                   | -    | 1.3                                   | -                                  | μs   |
| Output fall time from 0.7*V <sub>CC</sub> to 0.3*V <sub>CC</sub> with a bus capacitance from 10 pF to 400 pF | t <sub>of</sub>    | 20 + 0.1*C <sub>b</sub> <sup>*2</sup> | 300  | 20 + 0.1*C <sub>b</sub> <sup>*2</sup> | 300                                | ns   |
| Capacitive load for each bus line                                                                            | C <sub>b</sub>     | -                                     | 400  | -                                     | 400                                | pF   |
| Pulse width of spikes which will be suppressed by input noise filter                                         | t <sub>SP</sub>    | N/A                                   | N/A  | 0                                     | 1*t <sub>CLKP1</sub> <sup>*3</sup> | ns   |

\*1: For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.

\*2: C<sub>b</sub> = capacitance of one bus line in pF.

\*3: t<sub>CLKP1</sub> is the cycle time of the peripheral clock CLKP1.



- V<sub>OH</sub> = 0.7 \* V<sub>CC</sub>
- V<sub>OL</sub> = 0.3 \* V<sub>CC</sub>
- CMOS Hysteresis 0.7/0.3 input selected

## Analog Digital Converter

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ,  $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$ ,  $V_{CC} = \text{AV}_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = \text{AV}_{SS} = 0\text{ V}$ )

| Parameter                                        | Symbol    | Pin              | Value                  |              |                        | Unit          | Remarks                                                                                                                                           |
|--------------------------------------------------|-----------|------------------|------------------------|--------------|------------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                  |           |                  | Min                    | Typ          | Max                    |               |                                                                                                                                                   |
| Resolution                                       | -         | -                | -                      | -            | 10                     | bit           |                                                                                                                                                   |
| Total error                                      | -         | -                | -                      | -            | $\pm 3$                | LSB           |                                                                                                                                                   |
| Nonlinearity error                               | -         | -                | -                      | -            | $\pm 2.5$              | LSB           |                                                                                                                                                   |
| Differential nonlinearity error                  | -         | -                | -                      | -            | $\pm 1.9$              | LSB           |                                                                                                                                                   |
| Zero reading voltage                             | $V_{OT}$  | ANn              | AVRL-1.5 LSB           | AVRL+0.5 LSB | AVRL+2.5 LSB           | V             |                                                                                                                                                   |
| Full scale reading voltage                       | $V_{FST}$ | ANn              | AVRH-3.5 LSB           | AVRH-1.5 LSB | AVRH+0.5 LSB           | V             |                                                                                                                                                   |
| Compare time                                     | -         | -                | 1.0                    | -            | 16,500                 | $\mu\text{s}$ | $4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$                                                                                              |
|                                                  |           |                  | 2.0                    | -            | -                      | $\mu\text{s}$ | $3.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$                                                                                                 |
| Sampling time                                    | -         | -                | 0.5                    | -            | -                      | $\mu\text{s}$ | $4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$                                                                                              |
|                                                  |           |                  | 1.2                    | -            | -                      | $\mu\text{s}$ | $3.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$                                                                                                 |
| Analog input leakage current (during conversion) | $I_{AIN}$ | ANn              | -1                     | -            | +1                     | $\mu\text{A}$ | $T_A \leq 105\text{ }^{\circ}\text{C}$ ,<br>$\text{AV}_{SS}$ , $\text{AVRL} < V_I < \text{AV}_{CC}$ , $\text{AVRH}$                               |
|                                                  |           |                  | -1.2                   | -            | +1.2                   | $\mu\text{A}$ | $105\text{ }^{\circ}\text{C} < T_A \leq 125\text{ }^{\circ}\text{C}$ ,<br>$\text{AV}_{SS}$ , $\text{AVRL} < V_I < \text{AV}_{CC}$ , $\text{AVRH}$ |
| Analog input voltage range                       | $V_{AIN}$ | ANn              | AVRL                   | -            | AVRH                   | V             |                                                                                                                                                   |
| Reference voltage range                          | AVRH      | AVRH             | $0.75 \text{ AV}_{CC}$ | -            | $\text{AV}_{CC}$       | V             |                                                                                                                                                   |
|                                                  | AVRL      | AVRL             | $\text{AV}_{SS}$       | -            | $0.25 \text{ AV}_{CC}$ | V             |                                                                                                                                                   |
| Power supply current                             | $I_A$     | $\text{AV}_{CC}$ | -                      | 2.5          | 5                      | mA            | A/D Converter active                                                                                                                              |
|                                                  | $I_{AH}$  | $\text{AV}_{CC}$ | -                      | -            | 5                      | $\mu\text{A}$ | A/D Converter not operated                                                                                                                        |
| Reference voltage current                        | $I_R$     | AVRH/AVRL        | -                      | 0.7          | 1                      | mA            | A/D Converter active                                                                                                                              |
|                                                  | $I_{RH}$  | AVRH/AVRL        | -                      | -            | 5                      | $\mu\text{A}$ | A/D Converter not operated                                                                                                                        |
| Offset between input channels                    | -         | ANn              | -                      | -            | 4                      | LSB           |                                                                                                                                                   |

Note: The accuracy gets worse as  $|\text{AVRH} - \text{AVRL}|$  becomes smaller.

### Definition of A/D Converter Terms

**Resolution:** Analog variation that is recognized by an A/D converter.

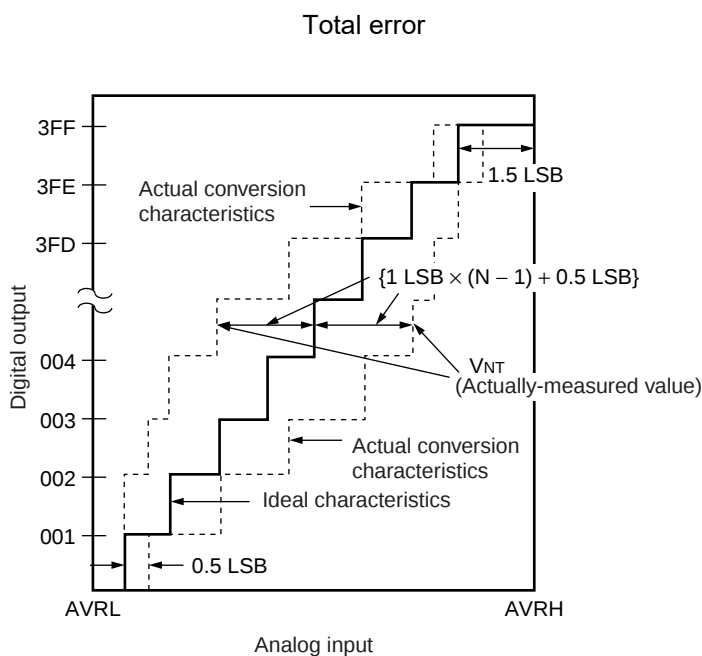
**Total error:** Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

**Nonlinearity error:** Deviation between a line across zero-transition line ("00 0000 0000" <--> "00 0000 0001") and full-scale transition line ("11 1111 1110" <--> "11 1111 1111") and actual conversion characteristics.

**Differential nonlinearity error:** Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

**Zero reading voltage:** Input voltage which results in the minimum conversion value.

**Full scale reading voltage:** Input voltage which results in the maximum conversion value.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} [\text{LSB}]$$

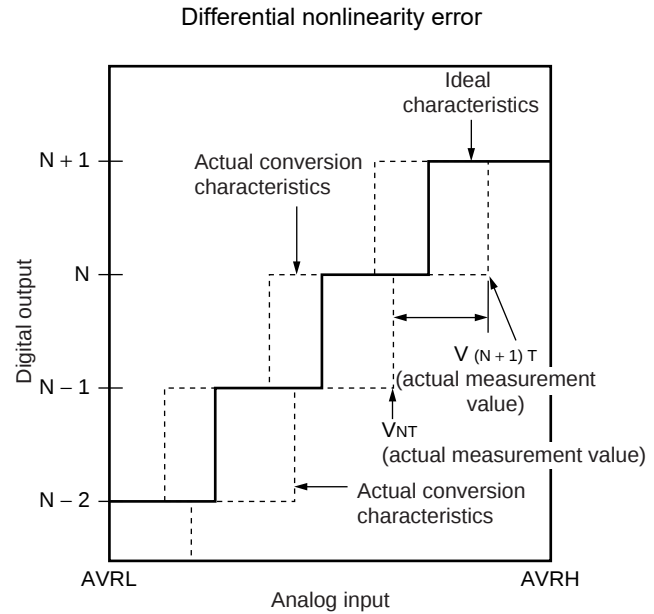
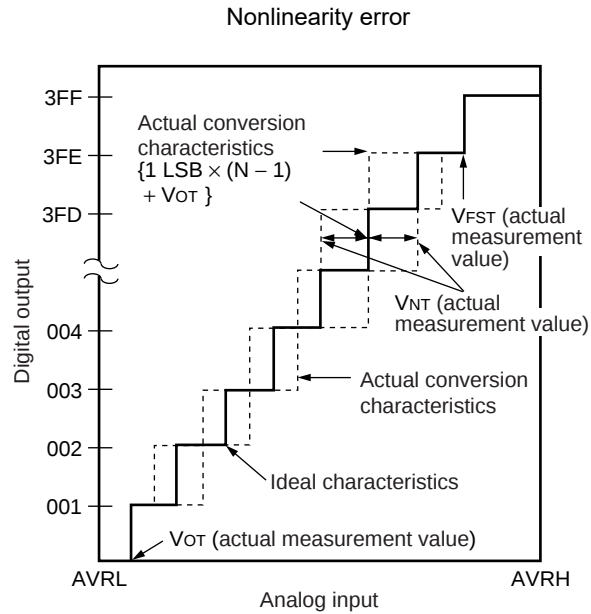
$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVRH - AVRL}{1024} [\text{V}]$$

N: A/D converter digital output value

$$V_{OT} (\text{Ideal value}) = AVRL + 0.5 \text{ LSB} [\text{V}]$$

$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB} [\text{V}]$$

V<sub>NT</sub>: A voltage at which digital output transitions from (N - 1) to N.



$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N: A/D converter digital output value

$V_{OT}$ : Voltage at which digital output transits from "000<sub>H</sub>" to "001<sub>H</sub>."

$V_{FST}$ : Voltage at which digital output transits from "3FE<sub>H</sub>" to "3FF<sub>H</sub>."



The sampling time should be set to minimum “7τ”. The following approximation formula for the replacement model above can be used:

$$T_{\text{sam}} [\text{min}] = 7 \times (R_{\text{ext}} \times (C_{\text{ext}} + C_{\text{IN}}) + (R_{\text{ext}} + R_{\text{ADC}}) \times C_{\text{ADC}})$$

- Do not select a sampling time below the absolute minimum permitted value  
(0.5μs for 4.5V ≤ AVCC ≤ 5.5V; 1.2 μs for 3.0V ≤ AVCC < 4.5V).
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin. In this case the internal sampling capacitance C<sub>ADC</sub> will be charged out of this external capacitance.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I<sub>IL</sub> (static current before the sampling switch) or the analog input leakage current I<sub>AIN</sub> (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I<sub>IL</sub> cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

### Low Voltage Detector Characteristics

(T<sub>A</sub> = -40 °C to +125 °C, V<sub>CC</sub> = AV<sub>CC</sub> = 3.0 V - 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

| Parameter          | Symbol               | Value *1 |      | Value *2 |      | Unit | Remarks                                     |
|--------------------|----------------------|----------|------|----------|------|------|---------------------------------------------|
|                    |                      | Min      | Max  | Min      | Max  |      |                                             |
| Stabilization time | T <sub>LVDSTAB</sub> | -        | 75   | -        | 110  | μs   | After power-up or change of detection level |
| Level 0            | V <sub>DL0</sub>     | 2.7      | 2.9  | 2.5      | 2.9  | V    | CILCR:LVL[3:0]="0000"                       |
| Level 1            | V <sub>DL1</sub>     | 2.9      | 3.1  | 2.8      | 3.2  | V    | CILCR:LVL[3:0]="0001"                       |
| Level 2            | V <sub>DL2</sub>     | 3.1      | 3.3  | 3        | 3.4  | V    | CILCR:LVL[3:0]="0010"                       |
| Level 3            | V <sub>DL3</sub>     | 3.5      | 3.75 | 3.35     | 3.8  | V    | CILCR:LVL[3:0]="0011"                       |
| Level 4            | V <sub>DL4</sub>     | 3.6      | 3.85 | 3.5      | 3.95 | V    | CILCR:LVL[3:0]="0100"                       |
| Level 5            | V <sub>DL5</sub>     | 3.7      | 3.95 | 3.6      | 4.1  | V    | CILCR:LVL[3:0]="0101"                       |
| Level 6            | V <sub>DL6</sub>     | 3.8      | 4.05 | 3.7      | 4.2  | V    | CILCR:LVL[3:0]="0110"                       |
| Level 7            | V <sub>DL7</sub>     | 3.9      | 4.15 | 3.8      | 4.3  | V    | CILCR:LVL[3:0]="0111"                       |
| Level 8            | V <sub>DL8</sub>     | 4.0      | 4.25 | 3.9      | 4.4  | V    | CILCR:LVL[3:0]="1000"                       |
| Level 9            | V <sub>DL9</sub>     | 4.1      | 4.35 | 3.95     | 4.5  | V    | CILCR:LVL[3:0]="1001"                       |
| Level 10           | V <sub>DL10</sub>    | not used |      | not used |      | -    |                                             |
| Level 11           | V <sub>DL11</sub>    | not used |      | not used |      | -    |                                             |
| Level 12           | V <sub>DL12</sub>    | not used |      | 2.6      | 3    | V    | CILCR:LVL[3:0]="1100"                       |
| Level 13           | V <sub>DL13</sub>    | not used |      | not used |      | -    |                                             |
| Level 14           | V <sub>DL14</sub>    | not used |      | not used |      | -    |                                             |
| Level 15           | V <sub>DL15</sub>    | not used |      | not used |      | -    |                                             |

\*1: Valid for all devices except devices listed under “\*2”

\*2: Valid for: CY96F353/F355

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

For correct detection, the slope of the voltage level must satisfy  $\left| \frac{dV}{dt} \right| \leq 0.004 \frac{V}{\mu s}$ .

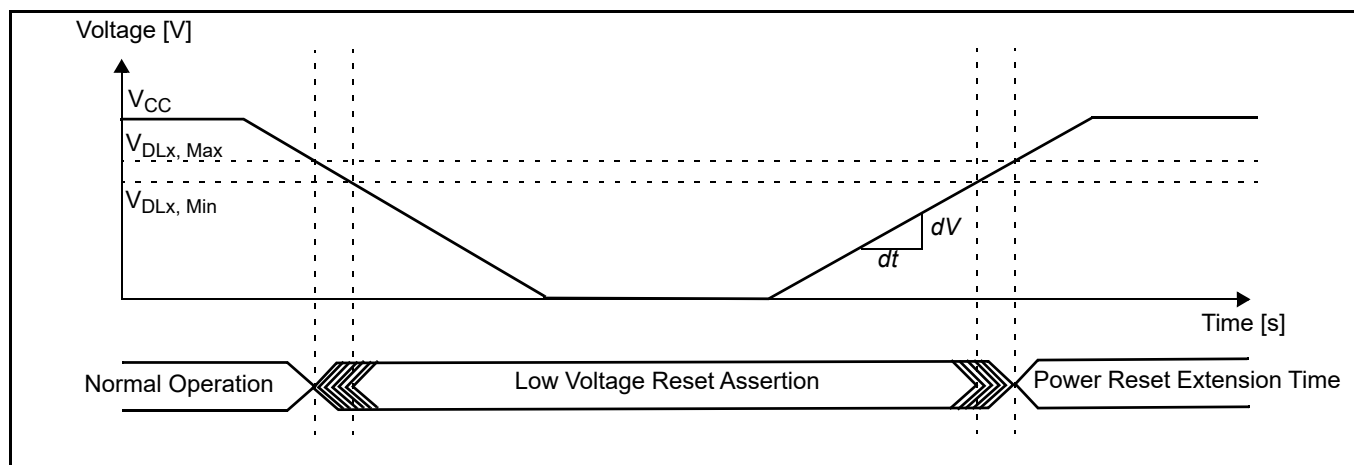
Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of V<sub>CC</sub> = 2.7 V. The electrical characteristics however are only valid in the specified range (usually down to 3.0 V).

Please use the inclination of the power-supply voltage with 0.1V/μs or less.

### Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



### Flash Memory Program/Erase Characteristics

( $T_A = -40\text{ }^{\circ}\text{C}$  to  $105\text{ }^{\circ}\text{C}$ ,  $V_{CC} = AV_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

| Parameter                            | Value  |               |               | Unit  | Remarks                                                                              |
|--------------------------------------|--------|---------------|---------------|-------|--------------------------------------------------------------------------------------|
|                                      | Min    | Typ           | Max           |       |                                                                                      |
| Sector erase time                    | -      | 0.9           | 3.6           | s     | Without erasure pre-programming time                                                 |
| Chip erase time                      | -      | $n \cdot 0.9$ | $n \cdot 3.6$ | s     | Without erasure pre-programming time (n is the number of Flash sector of the device) |
| Word (16-bit width) programming time | -      | 23            | 370           | us    | Without overhead time for submitting write command                                   |
| Program/Erase cycle                  | 10 000 | -             | -             | cycle |                                                                                      |
| Flash data retention time            | 20     | -             | -             | year  | <sup>*1</sup>                                                                        |

\*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at  $85\text{ }^{\circ}\text{C}$ )

## Example Characteristics

### Temperature dependency of power supply currents

The following diagrams show the current consumption of samples with typical wafer process parameters in different operation modes.

Common condition for all operation modes:

- VCC = AVCC = 5.0 V
- Main clock = 4 MHz external clock
- Sub clock = 32 kHz external clock

#### Operation Mode Details

| Mode name  | Details                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PLL Run 56 | PLL Run mode current $I_{CCPLL}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = 56\text{MHz}</math></li> <li>■ <math>f_{CLKP2} = 28\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.9V (VRCCR:HPM[1:0] = 11<sub>B</sub>)</li> <li>■ 2 Flash/ROM wait states (MTCRA=233A<sub>H</sub>)</li> <li>■ RC oscillator and Sub oscillator stopped</li> </ul>                                      |
| PLL Run 48 | PLL Run mode current $I_{CCPLL}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 96\text{MHz}</math></li> <li>■ <math>f_{CLKB} = f_{CLKP1} = 48\text{MHz}</math></li> <li>■ <math>f_{CLKP2} = 24\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.9V (VRCCR:HPM[1:0] = 11<sub>B</sub>)</li> <li>■ 1 Flash/ROM wait states (MTCRA=6B09<sub>H</sub>)</li> <li>■ RC oscillator and Sub oscillator stopped</li> </ul> |
| PLL Run 24 | PLL Run mode current $I_{CCPLL}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 48\text{MHz}</math></li> <li>■ <math>f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 24\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.8V (VRCCR:HPM[1:0] = 10<sub>B</sub>)</li> <li>■ 0 Flash/ROM wait states (MTCRA=2208<sub>H</sub>)</li> <li>■ RC oscillator and Sub oscillator stopped</li> </ul>                                      |
| Main Run   | Main Run mode current $I_{CCMAIN}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 4\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.8V (VRCCR:HPM[1:0] = 10<sub>B</sub>)</li> <li>■ 1 Flash/ROM wait states (MTCRA=0239<sub>H</sub>)</li> <li>■ PLL, RC oscillator and Sub oscillator stopped</li> </ul>                                                                     |

## Operation Mode Details

| Mode name    | Details                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RC Run 2M    | RC Run mode current $I_{CCRCH}$ with the following settings: <ul style="list-style-type: none"> <li>■ RC oscillator set to 2MHz (CKFCR:RCFS = 1)</li> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 2\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.8V (VR CR:HPM[1:0] = 10<sub>B</sub>)</li> <li>■ 1 Flash/ROM wait states (MTCRA=0239<sub>H</sub>)</li> <li>■ PLL, Main oscillator and Sub oscillator stopped</li> </ul>                        |
| RC Run 100k  | RC Run mode current $I_{CCRCL}$ with the following settings: <ul style="list-style-type: none"> <li>■ RC oscillator set to 100kHz (CKFCR:RCFS = 0)</li> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 100\text{kHz}</math></li> <li>■ Regulator in Low Power Mode A (SMCR:LPMS = 1)</li> <li>■ Core voltage at 1.8V (VR CR:LPMA[2:0] = 110<sub>B</sub>)</li> <li>■ 1 Flash/ROM wait states (MTCRA=0239<sub>H</sub>)</li> <li>■ PLL, Main oscillator and Sub oscillator stopped</li> </ul> |
| Sub Run      | Sub Run mode current $I_{CCSUB}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 32\text{kHz}</math></li> <li>■ Regulator in Low Power Mode A (by hardware)</li> <li>■ Core voltage at 1.8V (VR CR:LPMA[2:0] = 110<sub>B</sub>)</li> <li>■ 1 Flash/ROM wait states (MTCRA=0239<sub>H</sub>)</li> <li>■ PLL, RC oscillator and Main oscillator stopped</li> </ul>                                                            |
| PLL Sleep 56 | PLL Sleep mode current $I_{CCSPLL}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = 56\text{MHz}</math></li> <li>■ <math>f_{CLKP2} = 28\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.9V (VR CR:HPM[1:0] = 11<sub>B</sub>)</li> <li>■ RC oscillator and Sub oscillator stopped</li> </ul>                                                                                                                  |
| PLL Sleep 48 | PLL Sleep mode current $I_{CCSPLL}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 96\text{MHz}</math></li> <li>■ <math>f_{CLKP1} = 48\text{MHz}</math></li> <li>■ <math>f_{CLKP2} = 24\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.9V (VR CR:HPM[1:0] = 11<sub>B</sub>)</li> <li>■ RC oscillator and Sub oscillator stopped</li> </ul>                                                                             |

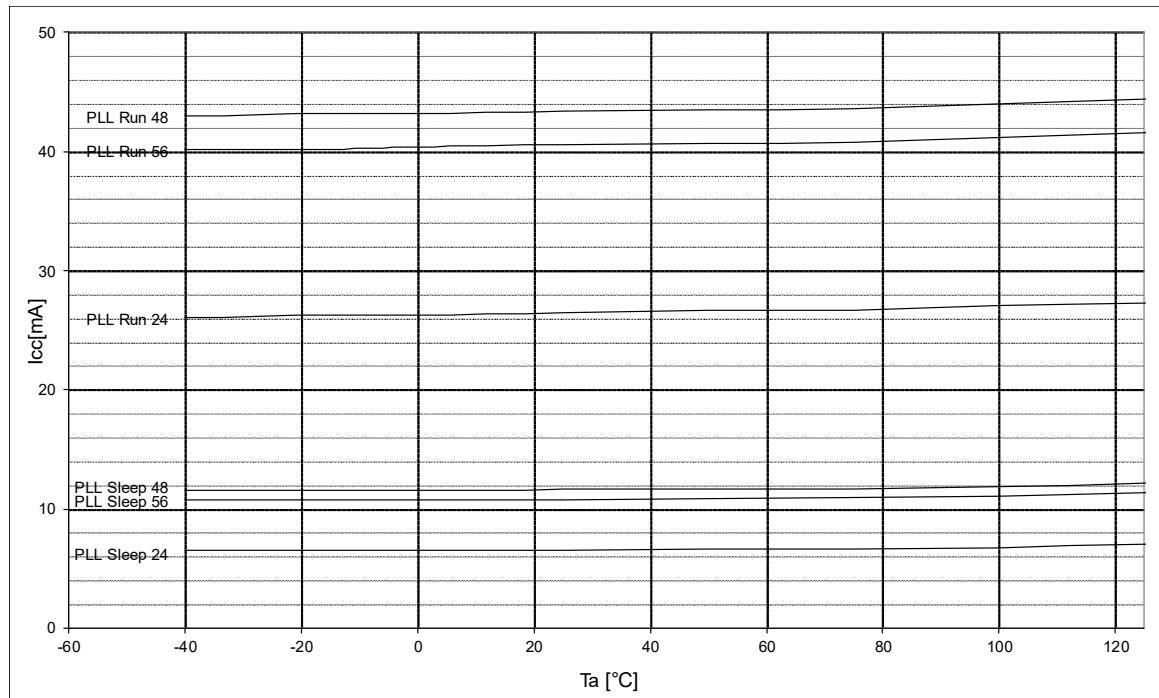
## Operation Mode Details

| Mode name     | Details                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PLL Sleep 24  | PLL Sleep mode current $I_{CCSPLL}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 48\text{MHz}</math></li> <li>■ <math>f_{CLKP1} = f_{CLKP2} = 24\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.8V (VRCCR:HPM[1:0] = 10<sub>B</sub>)</li> <li>■ RC oscillator and Sub oscillator stopped</li> </ul>                                               |
| Main Sleep    | Main Sleep mode current $I_{CCSMAIN}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 4\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.8V (VRCCR:HPM[1:0] = 10<sub>B</sub>)</li> <li>■ PLL, RC oscillator and Sub oscillator stopped</li> </ul>                                                                              |
| RC Sleep 2M   | RC Sleep mode current $I_{CCSRCH}$ with the following settings: <ul style="list-style-type: none"> <li>■ RC oscillator set to 2MHz (CKFCR:RCFS = 1)</li> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 2\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.8V (VRCCR:HPM[1:0] = 10<sub>B</sub>)</li> <li>■ PLL, Main oscillator and Sub oscillator stopped</li> </ul>                         |
| RC Sleep 100k | RC Sleep mode current $I_{CCSRCL}$ with the following settings: <ul style="list-style-type: none"> <li>■ RC oscillator set to 100kHz (CKFCR:RCFS = 0)</li> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 100\text{kHz}</math></li> <li>■ Regulator in Low Power Mode A (SMCR:LPMSS = 1)</li> <li>■ Core voltage at 1.8V (VRCCR:LPMA[2:0] = 110<sub>B</sub>)</li> <li>■ PLL, Main oscillator and Sub oscillator stopped</li> </ul> |
| Sub Sleep     | Sub Sleep mode current $I_{CCSSUB}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2} = 32\text{kHz}</math></li> <li>■ Regulator in Low Power Mode A (by hardware)</li> <li>■ Core voltage at 1.8V (VRCCR:LPMA[2:0] = 110<sub>B</sub>)</li> <li>■ PLL, RC oscillator and Main oscillator stopped</li> </ul>                                                             |
| PLL Timer 48  | PLL Timer mode current $I_{CCTPLL}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 48\text{MHz}</math></li> <li>■ Regulator in High Power Mode</li> <li>■ Core voltage at 1.8V (VRCCR:HPM[1:0] = 10<sub>B</sub>)</li> <li>■ RC oscillator and Sub oscillator stopped</li> </ul>                                                                                                            |

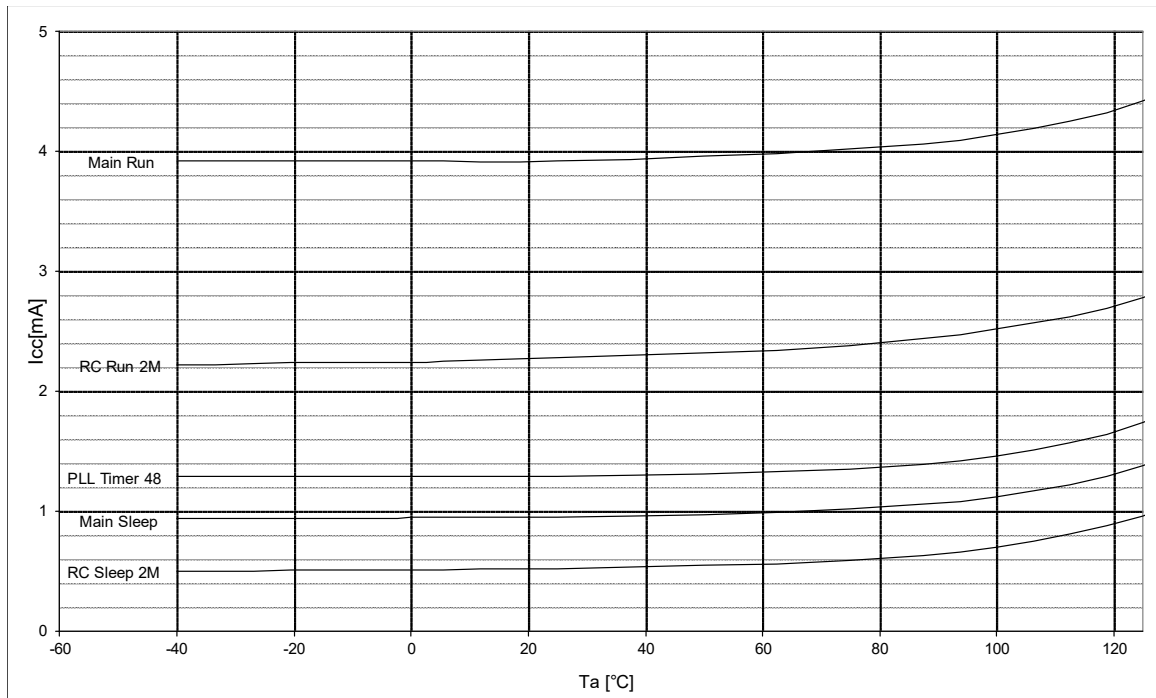
## Operation Mode Details

| Mode name     | Details                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Main Timer    | Main Timer mode current $I_{CCTMAIN}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 4\text{MHz}</math></li> <li>■ Regulator in Low Power Mode A (SMCR:LPMS = 1)</li> <li>■ Core voltage at 1.8V (VR CR:LPMA[2:0] = 110<sub>B</sub>)</li> <li>■ PLL, RC oscillator and Sub oscillator stopped</li> </ul>                                                          |
| RC Timer 2M   | RC Timer mode current $I_{CCTRCH}$ with the following settings: <ul style="list-style-type: none"> <li>■ RC oscillator set to 2MHz (CKFCR:RCFS = 1)</li> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 2\text{MHz}</math></li> <li>■ Regulator in Low Power Mode A (SMCR:LPMS = 1)</li> <li>■ Core voltage at 1.8V (VR CR:LPMA[2:0] = 110<sub>B</sub>)</li> <li>■ PLL, Main oscillator and Sub oscillator stopped</li> </ul>     |
| RC Timer 100k | RC Timer mode current $I_{CCTRCL}$ with the following settings: <ul style="list-style-type: none"> <li>■ RC oscillator set to 100kHz (CKFCR:RCFS = 0)</li> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 100\text{kHz}</math></li> <li>■ Regulator in Low Power Mode A (SMCR:LPMS = 1)</li> <li>■ Core voltage at 1.8V (VR CR:LPMA[2:0] = 110<sub>B</sub>)</li> <li>■ PLL, Main oscillator and Sub oscillator stopped</li> </ul> |
| Sub Timer     | Sub Timer mode current $I_{CCTSUB}$ with the following settings: <ul style="list-style-type: none"> <li>■ <math>f_{CLKS1} = f_{CLKS2} = 32\text{kHz}</math></li> <li>■ Regulator in Low Power Mode A (by hardware)</li> <li>■ Core voltage at 1.8V (VR CR:LPMA[2:0] = 110<sub>B</sub>)</li> <li>■ PLL, RC oscillator and Main oscillator stopped</li> </ul>                                                            |
| Stop 1.8V     | Stop mode current $I_{CCH}$ with the following settings: <ul style="list-style-type: none"> <li>■ Regulator in Low Power Mode B (by hardware)</li> <li>■ Core voltage at 1.8V (VR CR:LPMB[2:0] = 110<sub>B</sub>)</li> </ul>                                                                                                                                                                                           |
| Stop 1.2V     | Stop mode current $I_{CCH}$ with the following settings: <ul style="list-style-type: none"> <li>■ Regulator in Low Power Mode B (by hardware)</li> <li>■ Core voltage at 1.2V (VR CR:LPMB[2:0] = 000<sub>B</sub>)</li> </ul>                                                                                                                                                                                           |

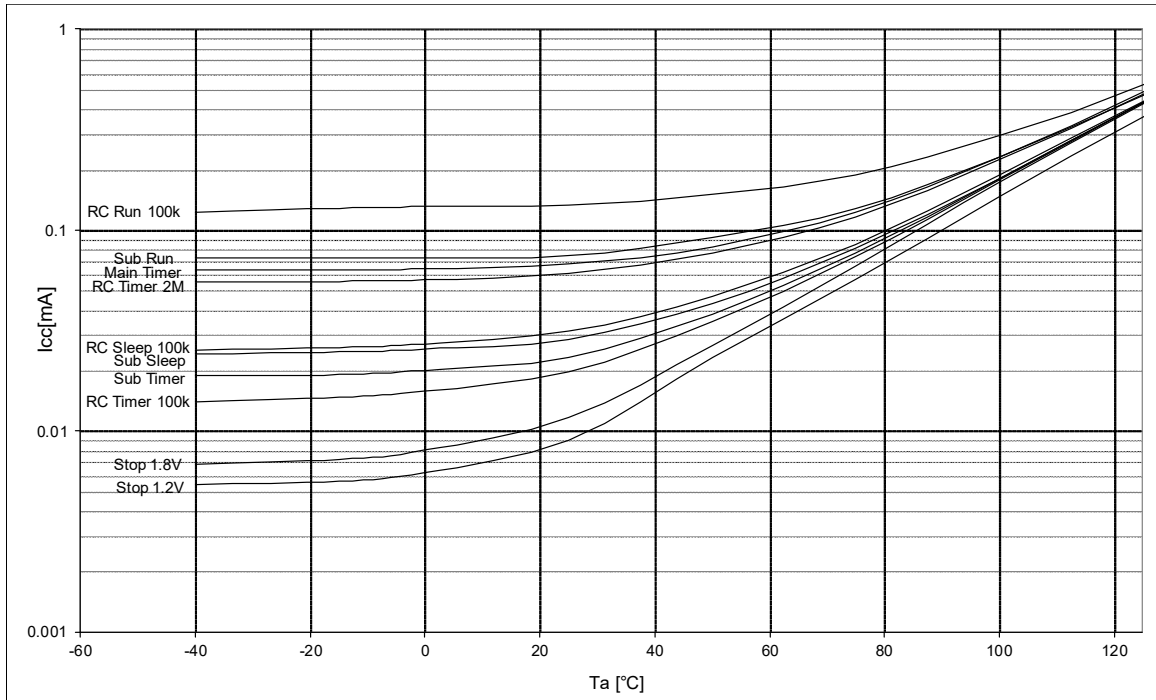
**Figure 3. CY96F353/F355 PLL Run and Sleep Mode Currents**



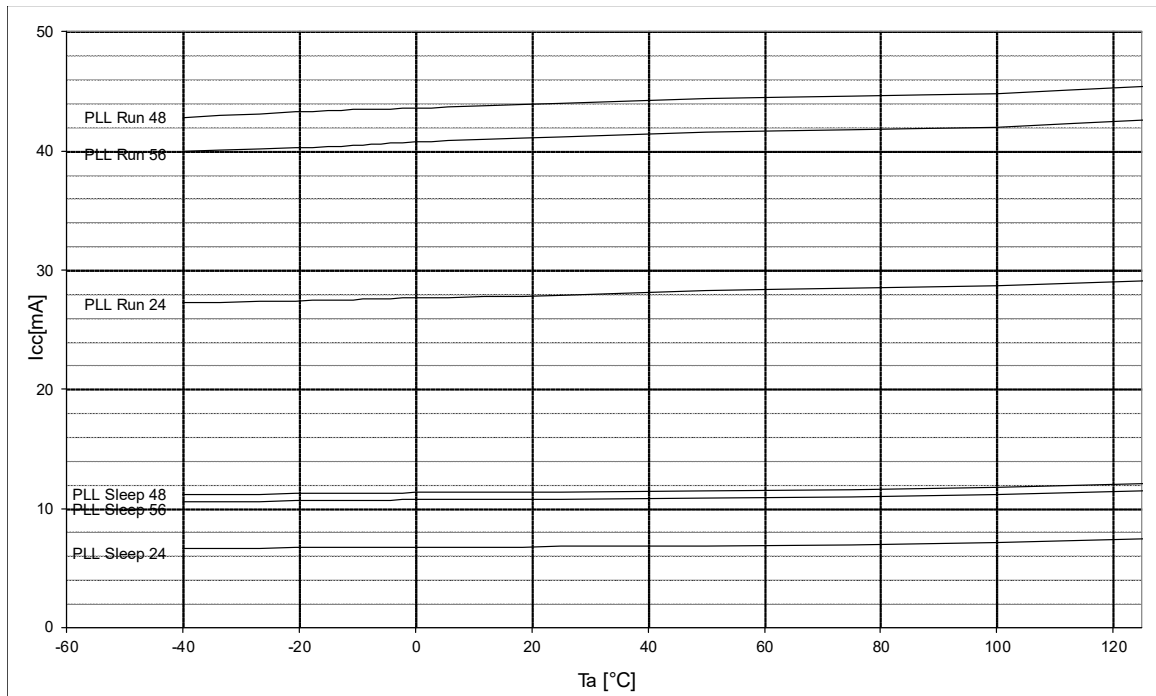
**Figure 4. CY96F353/F355 Operation Modes with Medium Currents**



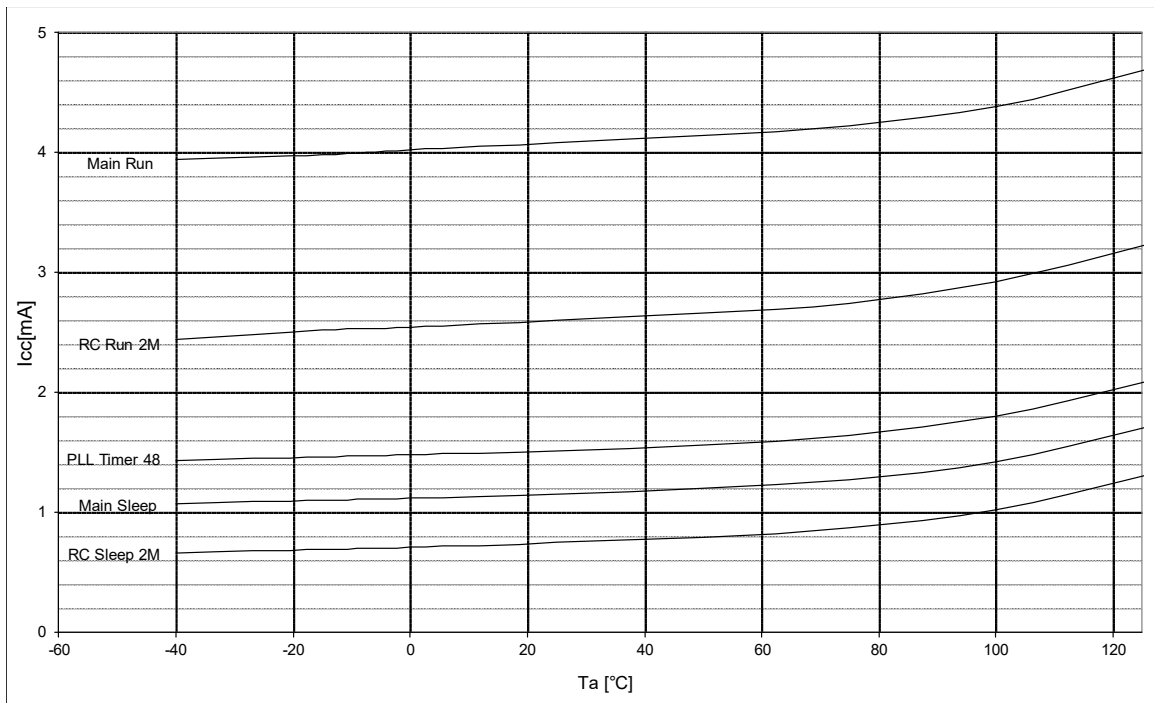
**Figure 5. CY96F353/F355 Low Power Mode Currents**



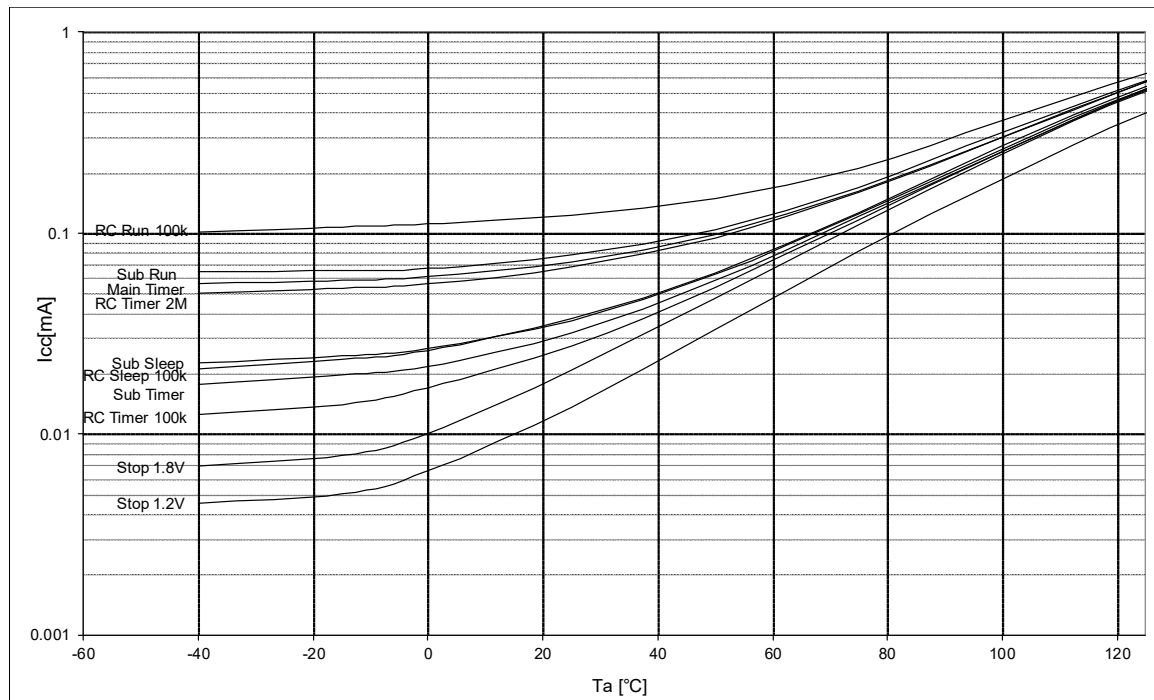
**Figure 6. CY96F356 PLL Run and Sleep Mode Currents**



**Figure 7. CY96F356 Operation Modes with Medium Currents**



**Figure 8. CY96F356 Low Power Mode Currents**



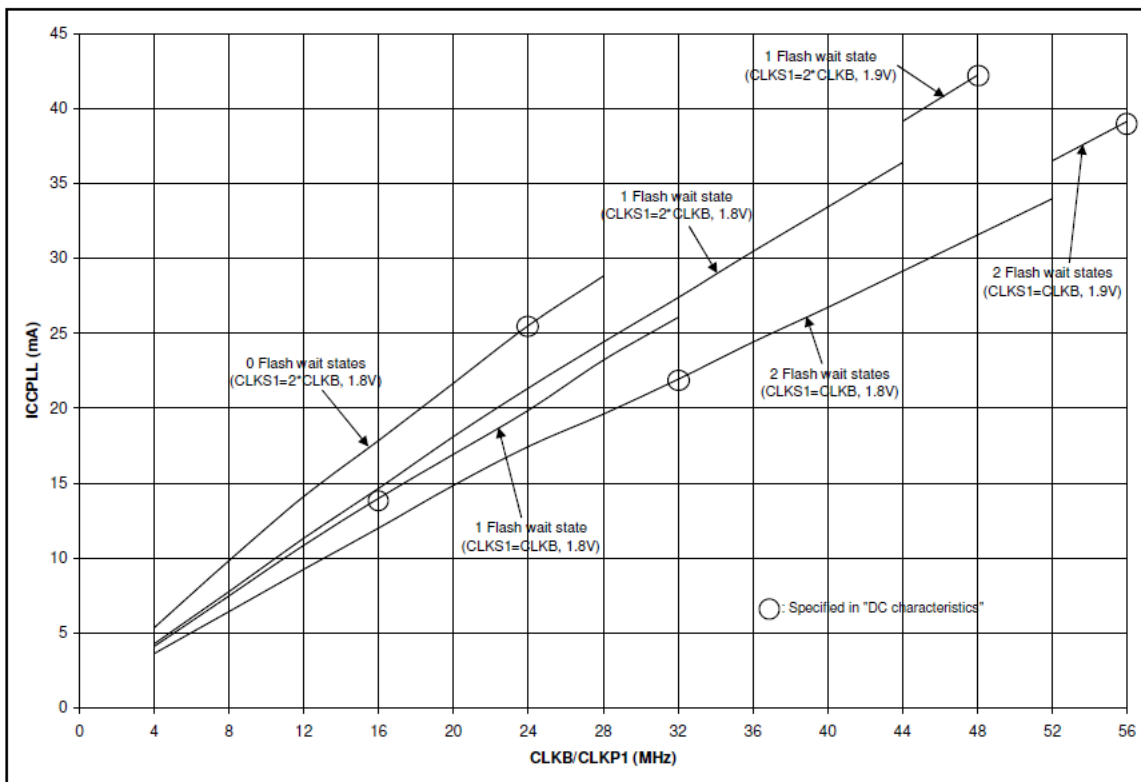
## Frequency dependency of power supply currents in PLL Run mode

The following diagrams show the current consumption of samples with typical wafer process parameters in PLL Run mode at different frequencies and Flash timing settings.

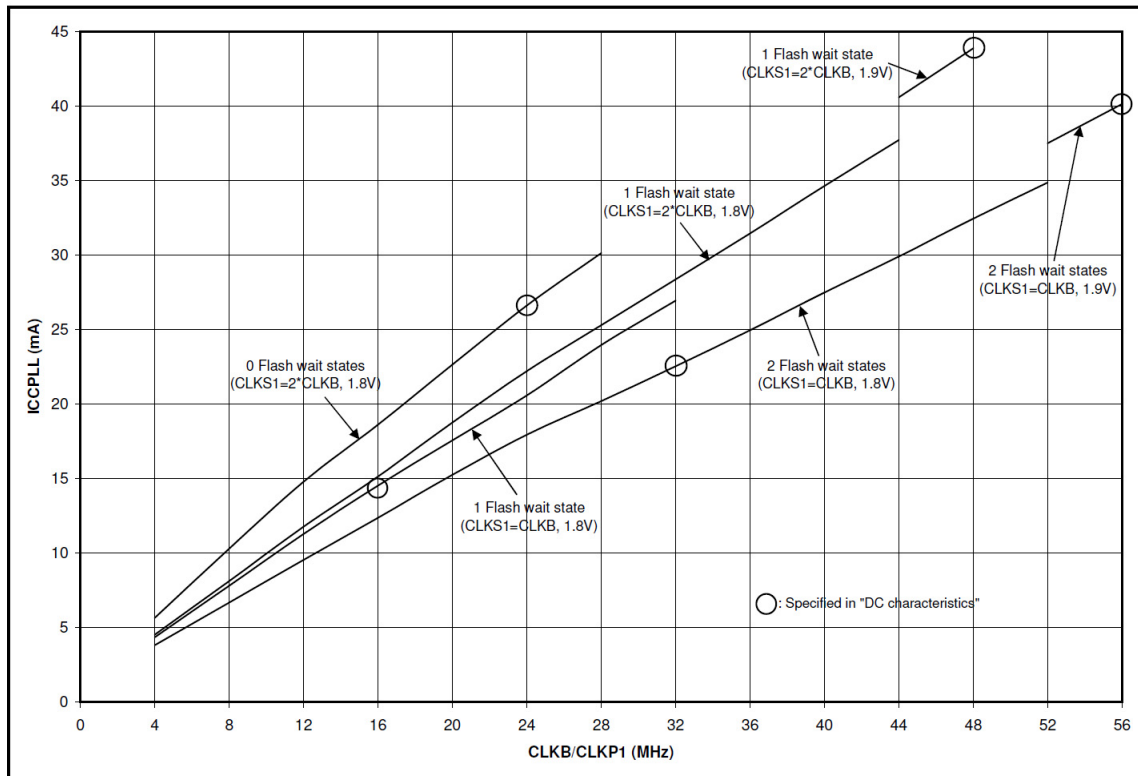
Measurement conditions:

- VCC = AVCC = 5.0V
- Ta = 25°C
- f<sub>CLKS1</sub> = f<sub>CLKB</sub> or f<sub>CLKS1</sub> = 2\*f<sub>CLKB</sub> as described in diagram
- f<sub>CLKS2</sub> = f<sub>CLKS1</sub>
- f<sub>CLKP1</sub> = f<sub>CLKB</sub>
- f<sub>CLKP2</sub> = f<sub>CLKB</sub>/2
- Core voltage at 1.8V (VRCCR:HPM[1:0] = 10B) or 1.9V (VRCCR:HPM[1:0] = 11B) as described in diagram
- Main clock = 4MHz external clock
- Flash memory timing settings:
  - MTCRA=2128H/2208H (0 Flash wait states, f<sub>CLKS1</sub> = 2\*f<sub>CLKB</sub>)
  - MTCRA=0239H/2129H (1 Flash wait state, f<sub>CLKS1</sub> = f<sub>CLKB</sub>)
  - MTCRA=4C09H/6B09H (1 Flash wait state, f<sub>CLKS1</sub> = 2\*f<sub>CLKB</sub>)
  - MTCRA=233AH (2 Flash wait states, f<sub>CLKS1</sub> = f<sub>CLKB</sub>)
- Average Flash access rate (number of read accesses to the Flash per CLKB clock cycle, no buffer hit):
  - 0 Flash wait states: 0.5
  - 1 Flash wait states: 0.33
  - 2 Flash wait states: 0.25

**Figure 9. CY96F353/F355 PLL Run Mode Currents**

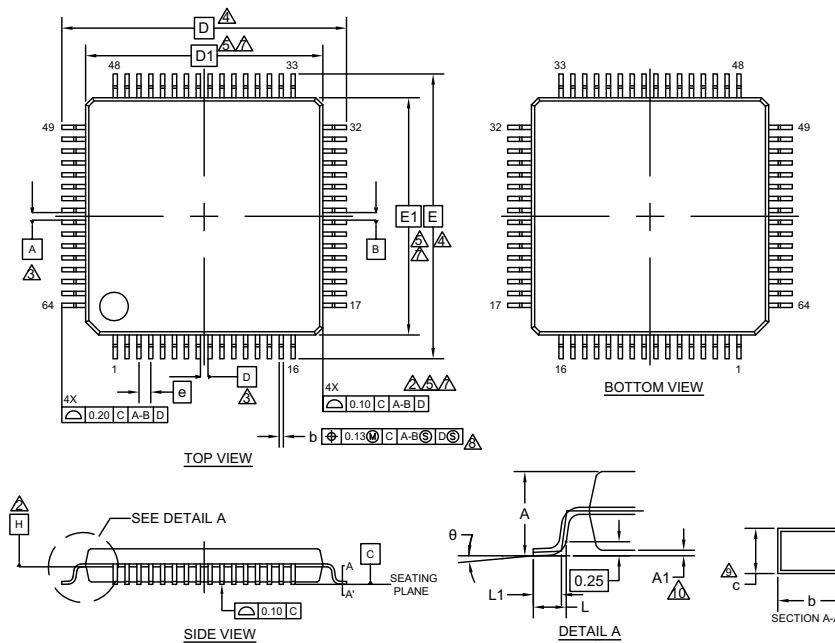


**Figure 10. CY96F356 PLL Run Mode Currents**



## Package Dimension

### CY96(F)35x LQFP 64 - LQG064



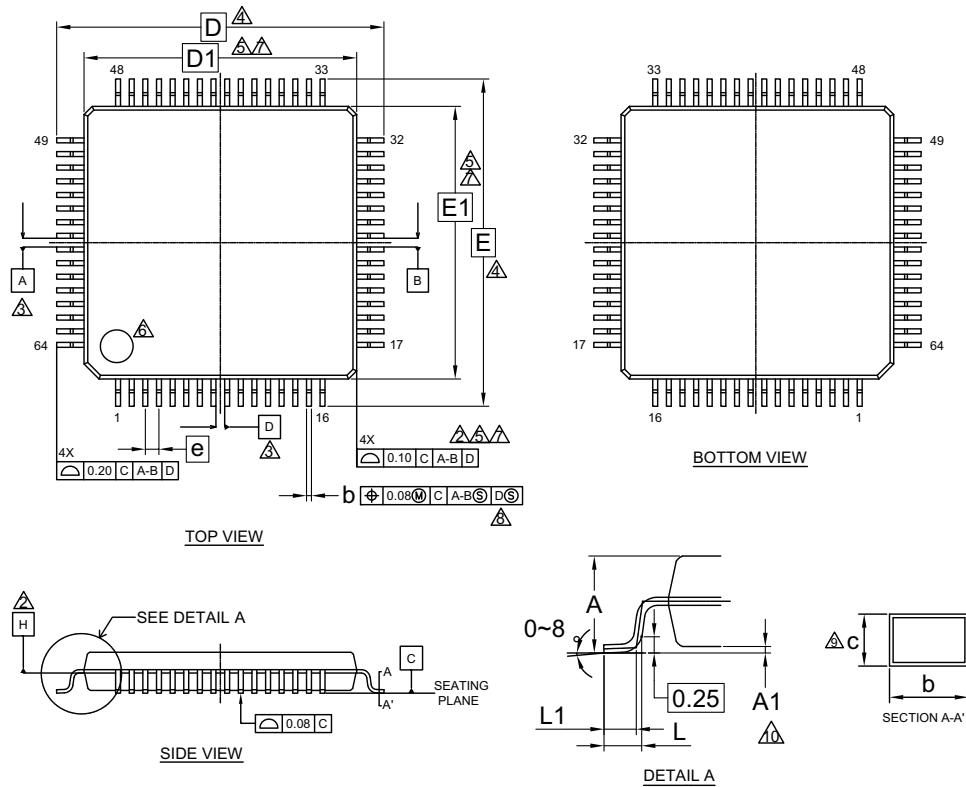
| SYMBOL   | DIMENSION |      |      |
|----------|-----------|------|------|
|          | MIN.      | NOM. | MAX. |
| A        | —         | —    | 1.70 |
| A1       | 0.00      | —    | 0.20 |
| b        | 0.27      | 0.32 | 0.37 |
| c        | 0.09      | —    | 0.20 |
| D        | 14.00 BSC |      |      |
| D1       | 12.00 BSC |      |      |
| e        | 0.65 BSC  |      |      |
| E        | 14.00 BSC |      |      |
| E1       | 12.00 BSC |      |      |
| L        | 0.45      | 0.60 | 0.75 |
| L1       | 0.30      | 0.50 | 0.70 |
| $\theta$ | 0°        | —    | 8°   |

## NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 \*\*

PACKAGE OUTLINE, 64 LEAD LQFP  
 12.0X12.0X1.7 MM LQG064 REV\*\*

**CY96(F)35x LQFP 64 - LQD064**


| SYMBOL | DIMENSIONS |      |      |
|--------|------------|------|------|
|        | MIN.       | NOM. | MAX. |
| A      | —          | —    | 1.70 |
| A1     | 0.00       | —    | 0.20 |
| b      | 0.15       | —    | 0.27 |
| c      | 0.09       | —    | 0.20 |
| D      | 12.00 BSC. |      |      |
| D1     | 10.00 BSC. |      |      |
| e      | 0.50 BSC.  |      |      |
| E      | 12.00 BSC. |      |      |
| E1     | 10.00 BSC. |      |      |
| L      | 0.45       | 0.60 | 0.75 |
| L1     | 0.30       | 0.50 | 0.70 |

**NOTES**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 \*\*

 PACKAGE OUTLINE, 64 LEAD LQFP  
 10.0X10.0X1.7 MM LQD064 Rev\*\*

## Ordering Information

### MCU with CAN Controller

| Part number              | Flash/ROM        | Subclock | Package                       |
|--------------------------|------------------|----------|-------------------------------|
| CY96F355RSBPMC-GS-UJE2   | Flash A (160 KB) | No       | 64 pins Plastic LQFP (LQG064) |
| CY96F355RSBPMC1-GS-UJE2  |                  |          | 64 pins Plastic LQFP (LQD064) |
| CY96F355RSBPMC1-GSUJERE2 |                  |          | 64 pins Plastic LQFP (LQD064) |
| CY96F356RSBPMC1-GS-UJE1  | Flash A (288 KB) | No       | 64 pins Plastic LQFP (LQD064) |
| CY96F356RSBPMC1-GS-UJE2  |                  |          | 64 pins Plastic LQFP (LQG064) |
| CY96F356RSBPMC-GS-UJE2   |                  |          |                               |
| CY96F356RSBPMC-GS-UJERE2 |                  |          | 64 pins Plastic LQFP (LQG064) |
| CY96F356RWBPMC1-GS-UJE2  |                  | Yes      | 64 pins Plastic LQFP (LQD064) |
| CY96F356RWBPMC-GS-UJE2   |                  |          | 64 pins Plastic LQFP (LQG064) |

### MCU without CAN Controller

| Part number             | Flash/ROM        | Subclock | Package                       |
|-------------------------|------------------|----------|-------------------------------|
| CY96F353ASBPMC1-GS-UJE2 | Flash A (96 KB)  | No       | 64 pins Plastic LQFP (LQD064) |
| CY96F356ASBPMC-GS-UJE2  | Flash A (288 KB) | No       | 64 pins Plastic LQFP (LQG064) |

**This datasheet is also valid for the following outdated devices:**

CY96F356YSA, CY96F356RSA, CY96F356YWA, CY96F356RWA, CY96F356ASA, CY96F356AWA, CY96F353RSA, CY96F353RWA, CY96F355RSA, CY96F355RWA, CY96F353ASA, CY96F353AWA, CY96F355ASA, CY96F355AWA.

## Major Changes

| Page          | Section                                                                                    | Change Result                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|---------------|--------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev *A        |                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| -             | Marketing Part Numbers changed from an MB prefix to a CY prefix.                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1             | -                                                                                          | Deleted the following comment.<br>Note: F2MC is the abbreviation of Fujitsu Flexible Microcontroller                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 6<br>87<br>89 | Pin Assignment<br>Package Dimension CY96(F)35x<br>LQFP 64 - LQG064<br>Ordering Information | Package description modified to JEDEC description.<br>(before) FPT-64P-M23<br>(after) LQG064                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 6<br>88<br>89 | Pin Assignment<br>Package Dimension CY96(F)35x<br>LQFP 64 - LQD064<br>Ordering Information | Package description modified to JEDEC description.<br>(before) FPT-64P-M24<br>(after) LQD064                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 15            | Serial Programming Communication Interface                                                 | Corporate name changed from Fujitsu to Cypress.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 89            | Ordering Information                                                                       | <p>Deleted the following part number.<br/>           MB96F353RSB PMC-GSE2, MB96F353RWB PMC-GSE2,<br/>           MB96F353RSB PMC1-GSE2, MB96F353RWB PMC1-GSE2,<br/>           MB96F355RWB PMC-GSE2, MB96F355RWB PMC1-GSE2, MB96F356RSB<br/>           PMC-GSE2, MB96F356RWB PMC-GSE2,<br/>           MB96F356RSB PMC1-GSE2, MB96F356RWB PMC1-GSE2,<br/>           MB96V300CRB-ES (for evaluation), MB96F353ASB PMC-GSE2,<br/>           MB96F353AWB PMC-GSE2, MB96F353AWB PMC1-GSE2, MB96F355ASB<br/>           PMC-GSE2, MB96F355AWB PMC-GSE2,<br/>           MB96F355ASB PMC1-GSE2, MB96F355AWB PMC1-GSE2, MB96F356ASB<br/>           PMC-GSE2, MB96F356AWB PMC-GSE2,<br/>           MB96F356ASB PMC1-GSE2, MB96F356AWB PMC1-GSE2</p> <p>Revised the following parts number.<br/>           (before)<br/>           - MB96F355RSB PMC-GSE2<br/>           - MB96F355RSB PMC1-GSE2<br/>           - MB96F353ASB PMC1-GSE2<br/>           (after)<br/>           - CY96F55RSBPMC-GS-UJE2<br/>           - CY96F355RSBPMC1-GS-UJE2<br/>           - CY96F353ASBPMC1-GS-UJE2</p> <p>Changed and deleted the parts number in Note.<br/>           (before)<br/>           MB96F356YSA, MB96F356RSA, MB96F356YWA, MB96F356RWA,<br/>           MB96F356ASA, MB96F356AWA,<br/>           MB96F353RSA, MB96F353RWA, MB96F355RSA, MB96F355RWA,<br/>           MB96F353ASA, MB96F353AWA,<br/>           MB96F355ASA, MB96F355AWA.<br/>           (after)<br/>           CY96F356YSA, CY96F356RSA, CY96F356YWA, CY96F356RWA,<br/>           CY96F356ASA, CY96F356AWA,<br/>           CY96F353RSA, CY96F353RWA, CY96F355RSA, CY96F355RWA,<br/>           CY96F353ASA, CY96F353AWA,<br/>           CY96F355ASA, CY96F355AWA.</p> |

| Page   | Section              | Change Result                                                                                                                                                                                                                                                         |
|--------|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 90     | Major Changes        | Changed section title and section number.<br>(before) MAJOR CHANGES IN THIS EDITION<br>(after) Major Changes                                                                                                                                                          |
| 95     | Document History     | Added Document History                                                                                                                                                                                                                                                |
| Rev *B |                      |                                                                                                                                                                                                                                                                       |
| 90     | Ordering Information | Added the following parts number.<br>MCU with CAN Controller<br>- CY96F356RSBPMC1-GS-UJE1<br>- CY96F356RSBPMC1-GS-UJE2<br>- CY96F356RSBPMC1-GS-UJE2<br>- CY96F356RWBPMC1-GS-UJE2<br>- CY96F356RWBPMC1-GS-UJE2<br>MCU with CAN Controller<br>- CY96F356ASBPMC1-GS-UJE2 |

## Revision History

Spanion Publication Number: **DS07-13806-3E**

| Revision | Date       | Modification                                                                                                                                                                                                                                                                                                                                                                           |
|----------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Prelim 1 | 2007-05-03 | Creation                                                                                                                                                                                                                                                                                                                                                                               |
| Prelim 2 | 2007-05-25 | Electrical characteristics update                                                                                                                                                                                                                                                                                                                                                      |
| Prelim 3 | 2007-11-27 | Package description is removed from cover page.<br>Typos corrections in product lineup. Product option details added<br>Electrical characteristics update<br>Update of the block diagram<br>Update of the IO map<br>Pin circuit type, LVD characteristics and example characteristics chapters added                                                                                   |
| Prelim 4 | 2007-12-20 | Update of the block diagram: external bus address lines, clock output function pins, AVRL removed from ADC block, re-layout.<br>RAMSTART value is corrected<br>IO map regenerated<br>Memory map and Flash configuration reworked<br>Few typos corrected across the document.<br>Flash bank renaming.<br>Ordering information: package type corrected.<br>IO circuit drawings modified. |

| Revision | Date       | Modification                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Prelim 5 | 2008-02-04 | <ul style="list-style-type: none"> <li>■ Reload Timer RLT 6 for PPGs added</li> <li>■ Block diagram corrected: ICU2 deleted, TTG2,3 deleted, TTG8,9 added</li> <li>■ Pin function description corrected with all existing pin types</li> <li>■ I/O circuit type diagrams corrected</li> <li>■ Memory map cleaned up</li> <li>■ “Flash sector configuration” replaced by corrected “User ROM Memory map for Flash devices”</li> <li>■ Parallel Flash programming spec removed</li> <li>■ IO map table regenerated: <ul style="list-style-type: none"> <li>- Port register: Naming style corrected</li> <li>- Memory control registers renamed (Main -&gt; A)</li> <li>- addresses after 000BFFh removed</li> </ul> </li> <li>■ Handling devices: AD converter items added</li> <li>■ Absolute maximum ratings: Pd and Ta specified more precisely</li> <li>■ Run and Sleep mode currents: more conditions added (1WS settings)</li> <li>■ Run mode current spec in 48/24MHz mode corrected</li> <li>■ Maximum CLKS1 frequency corrected at 1.8V</li> <li>■ External bus timings: missing conditions added and readability improved</li> <li>■ Ordering information updated</li> <li>■ Typos and formatting corrected</li> </ul> |

| Revision | Date       | Modification                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6        | 2009-01-09 | <ul style="list-style-type: none"> <li>■ Format adjusted to official Fujitsu Microelectronics datasheet standard (mainly style changes and official notes and disclaimer added)</li> <li>■ Numbering of Electrical Characteristics subchapters automated</li> <li>■ CANless devices added (MB96F356A)</li> <li>■ I/O map: Added node about reserved registers</li> <li>■ Serial programming interface: Note about handshaking pins improved</li> <li>■ specified AD converter channel offset to 4LSB</li> <li>■ package code of MB96V300 corrected in ordering information</li> <li>■ Added voltage condition to pull-up resistance spec</li> <li>■ Ordering information: column "Flash/ROM" added, column "Remarks" removed</li> <li>■ Official package dimension drawing with additional notes added</li> <li>■ Empty pages removed</li> <li>■ Handling devices: Notes added about Serial communication and about using ceramic resonators.</li> <li>■ Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor</li> <li>■ AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz</li> <li>■ VOL3 spec improved: spec valid for 3mA load for full Vcc range</li> <li>■ MB96F353/F355 added (under development)</li> <li>■ Free running timer (I/O Timer) 2 and 3 added (without clock input pin)</li> <li>■ Input capture ICU9 and ICU10 added (without input pin, only for LIN USART)</li> <li>■ C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted</li> <li>■ "Preliminary" watermark removed</li> </ul> |

| Revision | Date       | Modification                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7        | 2010-06-24 | <ul style="list-style-type: none"> <li>• AD converter <math>I_{AIN}</math> spec improved: 1uA valid up to 105deg, 1.2uA above 105deg</li> <li>• Low voltage detector: Detection levels of MB96F353/F355 updated</li> <li>• Note added that PLL phase jitter spec does not include jitter coming from Main clock</li> <li>• Note added in DC characteristics how to select driving strength of ports</li> <li>• <math>I^2C</math> AC spec updated: tof, Cb and tSP spec added, wrong footnotes and Condition removed</li> <li>• I/O Circuit type: Note added for type "N" (slew rate control according to <math>I^2C</math> spec)</li> <li>• Example characteristics updated, new figures added showing dependency of PLL Run mode current on frequency</li> <li>• Updated Power Supply current spec in Run/Sleep/Timer/Stop modes (new spec items in PLL Run/Sleep mode, small adjustment of most other values)</li> <li>• Package dimension: Added the following sentence under the figure: "Please confirm the latest Package dimension by following URL.<br/><a href="http://edevic.fujitsu.com/package/en-search/">http://edevic.fujitsu.com/package/en-search/</a>"</li> <li>• AD converter: Impact of input pin capacitance and external capacitance added to formula for calculation of the sampling time</li> <li>• Added specification of RC clock stabilization time</li> <li>• Ordering information updated: MB96F353/F355**A -&gt; MB96F353/F355**B, the device development is finished</li> <li>• Feature description <math>I^2C</math>: '8-bit addressing' corrected to '7-bit addressing'</li> <li>• Feature description PPG: 'Reload timer overflow as clock input' corrected to 'Reload timer underflow as clock input'</li> <li>• ICCLVD specification updated, at 125deg typical value is 7uA and maximum value is 20uA</li> <li>• Company name updated on the cover page: Fujitsu Microelectronics Limited -&gt; Fujitsu Semiconductor Limited</li> </ul> |

| Page       | Section                           | Change Result                                                                                                                                                                                   |
|------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Front Page | -                                 | Remove following description:<br>" *1: These devices are under development and specification is preliminary.<br>These products under development may change its specification without notice. " |
| 7          | Product Lineup                    | Remove following description:<br>" *1: These devices are under development and specification is preliminary.<br>These products under development may change its specification without notice. " |
| 13         | I/O Circuit Type                  | Error correction in Remarks of Type B.                                                                                                                                                          |
| 15         | I/O Circuit Type                  | Added Remarks in Type N.                                                                                                                                                                        |
| 52         | Handling Devices                  | Item "6. Power supply pins (Vcc/Vss)": Added note for bypass capacitor.                                                                                                                         |
| 53         | Handling Devices                  | Added new item "Clock modulator".                                                                                                                                                               |
| 54         | Electrical Characteristics        | Added output current spec for 2mA and 3mA outputs.                                                                                                                                              |
| 59         | DC Characteristics                | Added Port drive condition in Remarks.                                                                                                                                                          |
| 60 to 64   | DC Characteristics                | Added Mode Conditions.<br>Changed proper value for flash devices.                                                                                                                               |
| 66         | AC Characteristics                | Added RC clock stabilization time.<br>Added remark in "PLL Phase Jitter"                                                                                                                        |
| 67         | When using an oscillation circuit | Added Figure of Amplitude.                                                                                                                                                                      |
| 85         | $I^2C$ Timing                     | Added new parameter "Output fall time" ,"Capacitive load for each bus line" and "Pulse width of spikes".                                                                                        |
| 86         | Analog Digital Converter          | Deleted double expression for $I_{AIN}$ and corrected value.                                                                                                                                    |

| Page      | Section                                                 | Change Result                                                                                                                                                                                   |
|-----------|---------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 89        | Accuracy and setting of the A/D Converter sampling time | Changed to a more accurate estimation for sampling time by $R_{ext}$ , $C_{ext}$ , $C_{IN}$ , $R_{ADC}$ and $C_{ADC}$                                                                           |
| 90        | Low Voltage Detector characteristics                    | Added note description for inclination of the power-supply voltage.                                                                                                                             |
| 93 to 100 | Example Characteristics                                 | Added new section.                                                                                                                                                                              |
| 101, 102  | Ordering Information                                    | Remove following description:<br>" *1: These devices are under development and specification is preliminary.<br>These products under development may change its specification without notice. " |

## Document History

| Document Title: CY96F353/F355, CY96F356, F <sup>2</sup> MC-16FX, CY96350 Series, 16-bit Proprietary Microcontroller<br>Document Number: 002-04588 |         |                 |                                                                                                                                                                                                                                                                                                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                                                          | ECN     | Submission Date | Description of Change                                                                                                                                                                                                                                                                                      |
| **                                                                                                                                                | —       | 07/18/2013      | Migrated to Cypress and assigned document number 002-04588.<br>No change to document contents or format.                                                                                                                                                                                                   |
| *A                                                                                                                                                | 6213848 | 06/21/2018      | Updated to Cypress template.<br>Revised the following items:<br>Marketing Part Numbers changed from an MB prefix to a CY prefix.<br>Pin Assignments<br>Package Dimension<br>Ordering Information<br>Renamed Chapter Name of MAJOR CHANGES IN THIS EDITION<br>For details, please see Major Changes section |
| *B                                                                                                                                                | 6351866 | 10/16/2018      | Added Marketing Part Number in Ordering Information.<br>For details, please see Major Changes section                                                                                                                                                                                                      |
| *C                                                                                                                                                | 6896470 | 06/10/2020      | Added the part numbers CY96F355RSBPMC1-GSUJERE2 and CY96F356RSBPMC-GS-UJERE2 in <a href="#">Ordering Information</a> .                                                                                                                                                                                     |

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