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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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BIPOLAR ANALOG INTEGRATED CIRCUITS

μ PC815, μ PC816

ULTRA LOW OFFSET VOLTAGE, LOW DRIFT, LOW NOISE HIGH SLEW RATE, WIDEBAND, OPERATIONAL AMPLIFIER

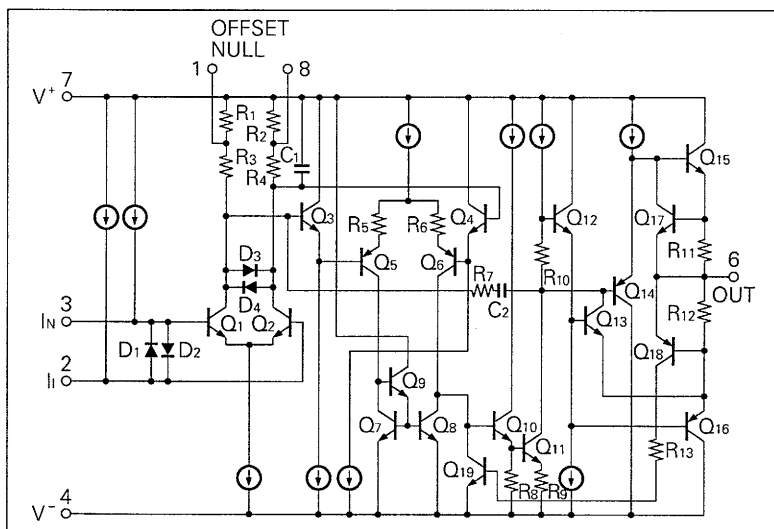
DESCRIPTION

The μ PC815, μ PC816 are high accuracy OP amps which realize 20 μ V input offset voltage and 2.8 nV/ $\sqrt{\text{Hz}}$ input noise by using advanced on-chip resistor trimming technique and ultra low noise NPN transistor for input stage. The μ PC816, high speed version of the μ PC815, realizes 25 MHz bandwidth and 7 V/ μ s slewrate with full frequency compensation characteristics by the effect of output stage high speed PNP transistors. Input stage Ib canceling circuits which minimize input bias current are also distinctive feature. By these features, the μ PC815, μ PC816 are optimum choice for instrumentation amplifier, audio pre-amplifier and buffer amplifier for high resolution DAC.

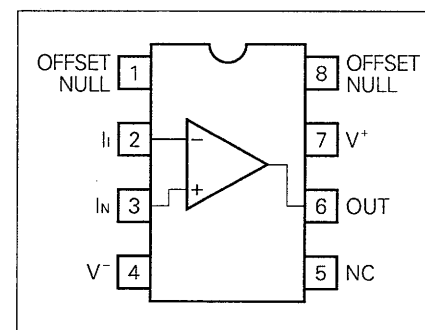
FEATURES

- Wide supply voltage range: ± 3 to ± 22 V
- Ultra low offset voltage: ± 20 μ V TYP.
- Ultra low offset voltage drift: ± 0.3 μ V/ $^{\circ}\text{C}$ TYP. (unnull)
- Ultra low noise: 2.8 nV/ $\sqrt{\text{Hz}}$ (TYP.) ($f_o = 10$ Hz)
- High slew-rate: μ PC815: 1.6 V/ μ s TYP. ($A_v = 1$)
 μ PC816: 7.6 V/ μ s TYP. ($A_v = 1$)
- Wide bandwidth product:
 μ PC815: 7 MHz TYP. ($f_o = 100$ kHz)
 μ PC816: 25 MHz TYP. ($f_o = 100$ kHz)
- Low input bias current: ± 10 nA TYP.
- Internal full frequency compensation
- Stable operation under capacitive load:
 μ PC815: 100 pF
 μ PC816: 1 000 pF

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM (Top View)



ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μ PC815D	8 PIN CERAMIC DIP (300 mil)	Standard
μ PC815D(1)		Standard
μ PC815C	8 PIN PLASTIC DIP (300 mil)	Standard
μ PC815C(1)		Standard
μ PC816D	8 PIN CERAMIC DIP (300 mil)	Standard
μ PC816C	8 PIN PLASTIC DIP (300 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25\text{ }^\circ\text{C}$)

PARAMETER	SYMBOL	μ PC815D	μ PC815C	μ PC816D	μ PC816C	UNIT
Voltage between V^+ and V^- (Note 1)	$V^+ - V^-$	-0.3 to +44				V
Differential Input Current	I_{ID}	± 25				mA
Input Voltage (Note 2)	V_I	$V^- - 0.3$ to $V^+ + 0.3$				V
Output Voltage (Note 3)	V_O	$V^- - 0.3$ to $V^+ + 0.3$				V
Power Dissipation	P_T	500 (Note 4)	350 (Note 5)	500 (Note 4)	350 (Note 5)	mW
Output Short Circuit Duration (Note 6)		Indefinite				sec
Operating Temperature Range	T_{opt}	-20 to +80	-20 to +70	-20 to +80	-20 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	-55 to +125	-55 to +150	-55 to +125	$^\circ\text{C}$

Note 1. Reverse connection of supply voltage can cause destruction.

Note 2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

Note 3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

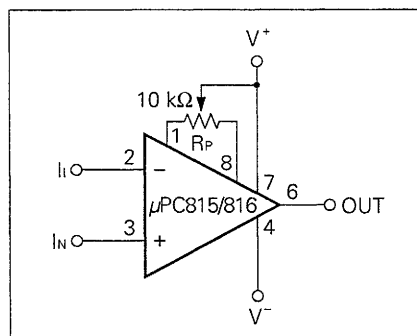
Note 4. Thermal derating factor is $-5.0\text{ mW} / ^\circ\text{C}$ when ambient temperature is higher than $50\text{ }^\circ\text{C}$.

Note 5. Thermal derating factor is $-5.0\text{ mW} / ^\circ\text{C}$ when ambient temperature is higher than $55\text{ }^\circ\text{C}$.

Note 6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V^\pm$	± 3	± 15	± 20	V
Output Current	I_O			± 25	mA
Capacitive Load ($A_v = +1$, $R_f = 0\text{ }\Omega$)	μ PC815	C_L		1000	pF
	μ PC816			100	

OFFSET VOLTAGE NULL CIRCUIT

ELECTRICAL CHARACTERISTICS ($V^{\pm} = \pm 15$ V, $T_a = 25$ °C)

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Offset Voltage		V_{IO}		± 20	± 60	μ V	$R_s \leq 100 \Omega$
Input Offset Current		I_{IO}		± 7	± 50	nA	
Input Bias Current		I_B		± 10	± 55	nA	
Input Resistance – Common Mode		R_{inCM}		3		G Ω	
Large Signal Voltage Gain		A_v	5	20		V/ μ V	$R_L \geq 2 \text{ k}\Omega$, $V_o = \pm 12$ V
Supply Current		I_{CC}		3.0	4.6	mA	$I_o = 0$ A
Common Mode Rejection Ratio		CMR	110	130		dB	
Supply Voltage Rejection Ratio		SVR	106	126		dB	$V^{\pm} = \pm 3$ V $\rightarrow \pm 18$ V
Output Voltage Swing		V_{om}	± 12.5	$+13.5$ -14.0		V	$R_L \geq 2 \text{ k}\Omega$
			± 10.5	$+12.5$ -13.5			$R_L \geq 600 \Omega$
Common Mode Input Voltage Range		V_{ICM}	± 11	$+12.5$ -13.5		V	
Slew Rate	μ PC815	SR	0.8	1.6		V/ μ s	$R_L = 2 \text{ k}\Omega$
	μ PC816		3	7.6			$R_L = 2 \text{ k}\Omega$
Gain Bandwidth Product	μ PC815	GBW	4	7		MHz	$f_o = 100 \text{ kHz}$
	μ PC816		15	25			$f_o = 100 \text{ kHz}$
Input Equivalent Noise Voltage		N_L		0.06	0.13	μ V _{p-p}	$R_s = 100 \Omega$, $f = 0.1$ to 10 Hz
Input Equivalent Noise Voltage Density		e_n		2.8	4.5	nV/ $\sqrt{\text{Hz}}$	$f_o = 10 \text{ Hz}$
				2.7	4.0		$f_o = 100 \text{ Hz}$
				2.7	3.8		$f_o = 1\,000 \text{ Hz}$
Input Equivalent Noise Current Density		i_n		1.5	4.0	pA/ $\sqrt{\text{Hz}}$	$f_o = 10 \text{ Hz}$
				0.4	0.6		$f_o = 1\,000 \text{ Hz}$
V _{IO} Adjustment Range				± 3		mV	$R_p = 10 \text{ k}\Omega$
Long Term V _{IO} Stability (Note 7)				± 0.2	± 1.0	μ V/Mo	

Note 7. Long term input offset voltage stability refers to the average trend line of offset vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during 30 days are typically 2.5 μ V – refer to typical performance curve.

$-20 \leq T_a \leq 80$ °C (μ PC815D, 816D), $-20 \leq T_a \leq 70$ °C (μ PC815C, 816C), $V^{\pm} = \pm 15$ V

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Offset Voltage		V_{IO}		± 20	± 110	μ V	$R_s \leq 100 \Omega$
Input Offset Current		I_{IO}		± 7	± 70	nA	
Input Bias Current		I_B		± 10	± 75	nA	
Large Signal Voltage Gain		A_v	2.5	20		V/ μ V	$R_L \geq 2 \text{ k}\Omega$, $V_o = \pm 10$ V
Supply Current		I_{CC}		3	5	mA	
Common Mode Rejection Ratio		CMR	106	130		dB	$V^{\pm} = \pm 3$ V $\rightarrow \pm 18$ V
Supply Voltage Rejection Ratio		SVR	102	126		dB	$R_L \geq 2 \text{ k}\Omega$
Output Voltage Swing		V_{om}	± 12	$+13.5$ -14.0		V	
Common Mode Input Voltage Range		V_{ICM}	± 10.5	$+12.5$ -13.5		V	
Average V _{IO} Temperature Drift		$\Delta V_{IO}/\Delta T$		± 0.3	± 1.5	μ V/°C	$R_s \leq 100 \Omega$

The μ PC815D(1) & 815C(1) are temperature drift sorted for high accuracy application. The $\Delta V_{IO}/\Delta T$ spec is shown below.

μ PC815D(1), 815C(1)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$			± 0.8	$\mu V/^{\circ}C$	$R_s \leq 100 \Omega$

APPLICATION INFORMATION

1. Over differential input voltage application

The μ PC815/816 contain the input protection back-to-back diodes at input stage. However the input current limit resistors are not used in order to achieve ultra low noise. (See EQUIVALENT CIRCUIT)

Therefore, when the over differential input voltage is applied, the differential input current should be kept less than 25 mA by inserting the series resistors at the inputs.

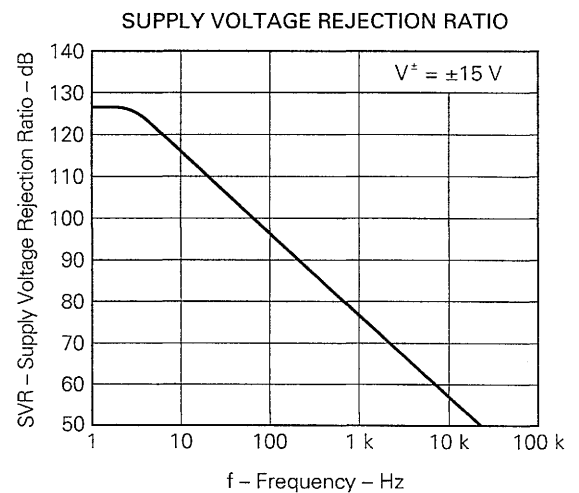
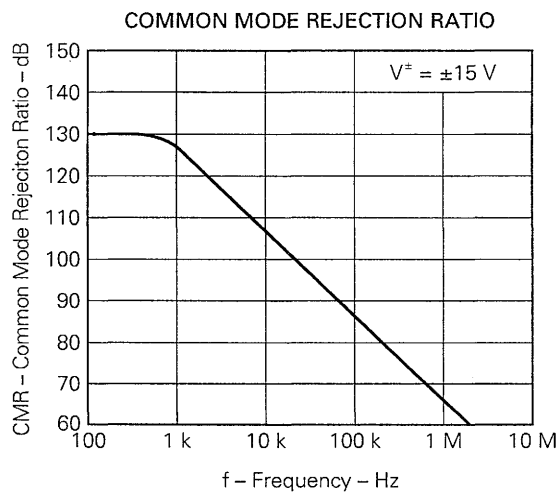
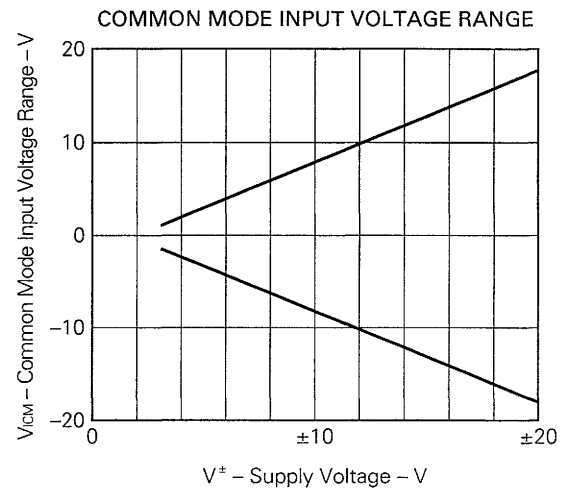
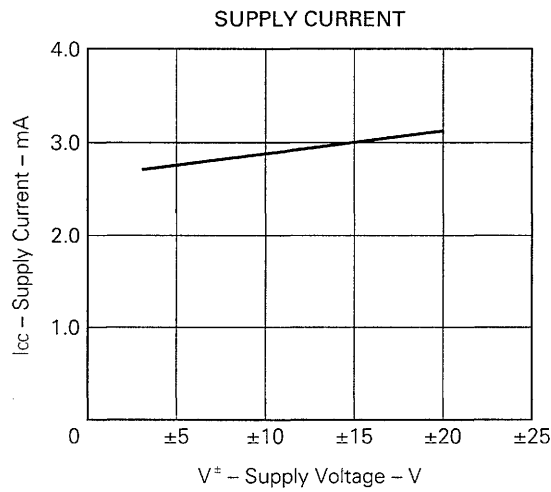
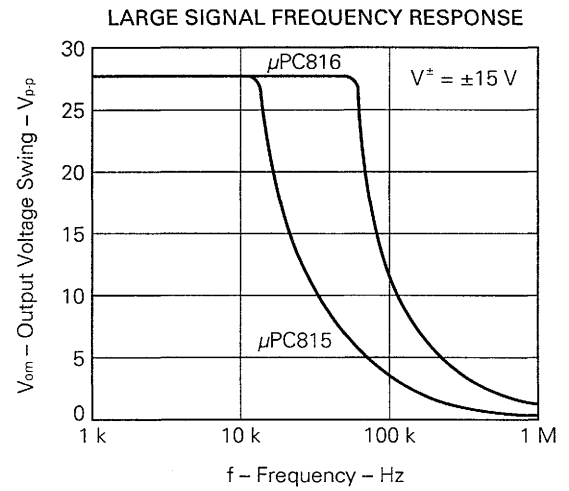
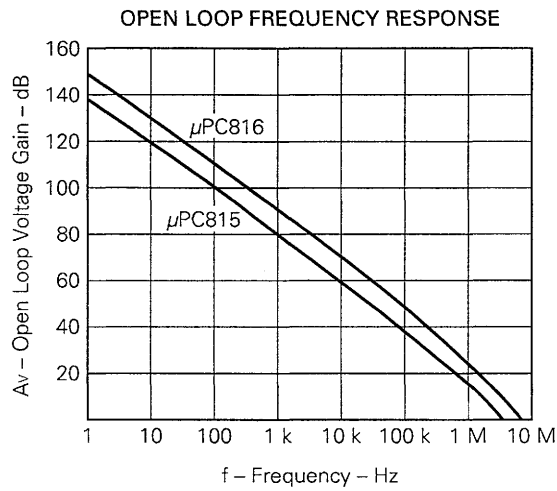
2. Unity gain buffer application

When the input is driven faster than the Slew Rate under the condition of R_f & $R_s = 0 \Omega$, the input protection diodes will short the input to the output, and the input current is limited only by the output drive capability. The solution of this problem is inserting the feedback resistor $R_f \gg 1 k\Omega$, or the source resistor $R_s \gg 1 k\Omega$ to limit the input short current.

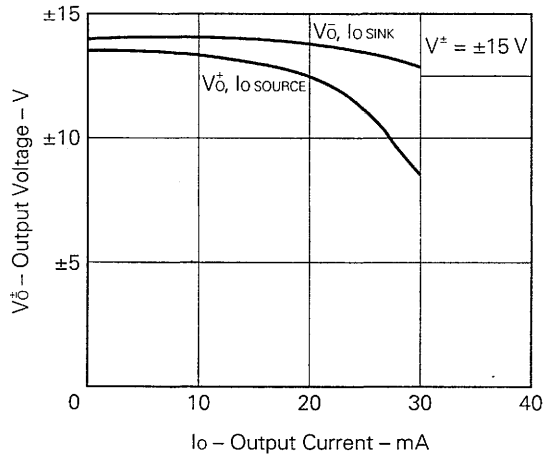
If the feedback resistor R_f becomes bigger, a pole created with R_f and C_{in} (input capacitance) at $f = \frac{1}{2\pi R_f C_{in}}$ reduces the phase margin. Considering the worst case, the oscillation will occur.

The solution of this problem is connecting the small capacitor (several 10 pF) in parallel with R_f .

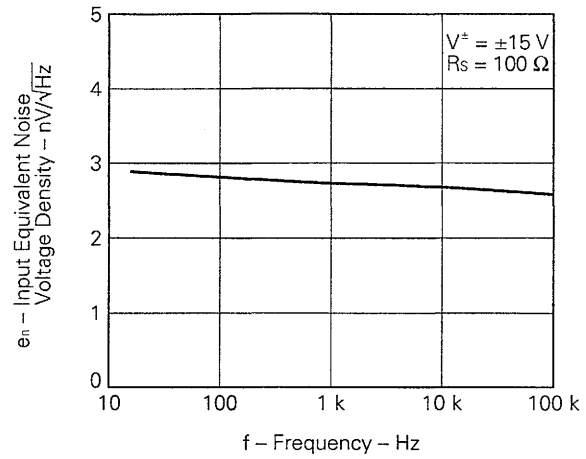
TYPICAL PERFORMANCE CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



OUTPUT CURRENT LIMIT

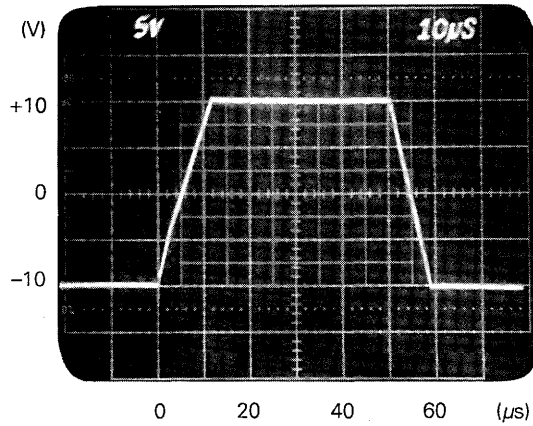


INPUT EQUIVALENT NOISE VOLTAGE DENSITY



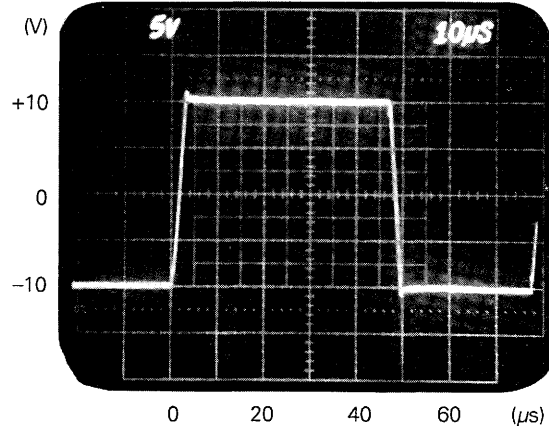
VOLTAGE FOLLOWER PULSE RESPONSE μ PC815

($V^\pm = \pm 15$ V, $A_v = +1$)
($R_f = 1 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$)

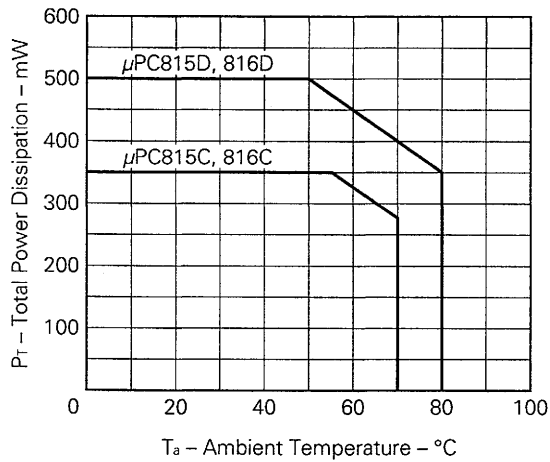


VOLTAGE FOLLOWER PULSE RESPONSE μ PC816

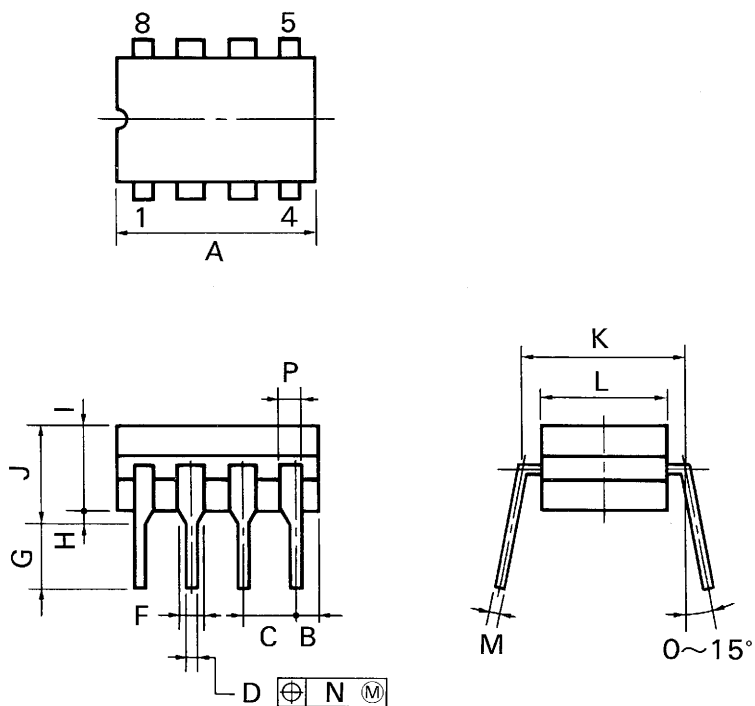
($V^\pm = \pm 15$ V, $A_v = +1$)
($R_f = 1 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$)



POWER DISSIPATION



8PIN CERAMIC DIP (300 mil)



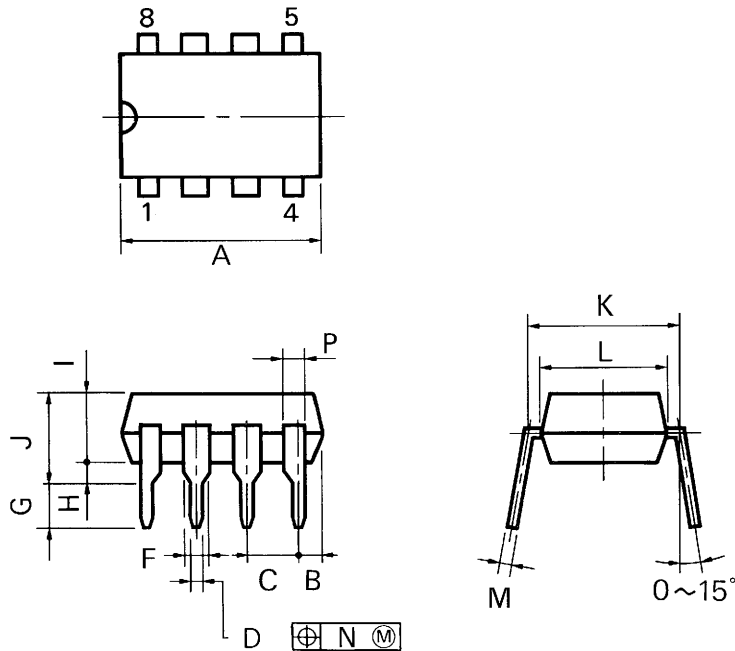
P8DH-100-300A,B

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.46 ^{±0.05}	0.018 ^{±0.002}
F	1.42 MIN.	0.055 MIN.
G	3.0 ^{±0.3}	0.118 ^{±0.012}
H	0.51 MIN.	0.020 MIN.
I	3.80	0.150
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.30	0.248
M	0.25 ^{±0.05}	0.010 ^{±0.002 -0.003}
N	0.25	0.01
P	0.89 MIN.	0.035 MIN.

8PIN PLASTIC DIP (300 mil)



P8C-100-300B,C

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ^{+0.10} _{-0.05}	0.020 ^{+0.004} _{-0.005}
F	1.4 MIN.	0.055 MIN.
G	3.2 ^{±0.3}	0.126 ^{+0.012} _{-0.010}
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF THROUGH HOLE DEVICE

[μ PC815D, μ PC815C, μ PC816D, μ PC816C]

Soldering method	Soldering conditions	Recommended condition symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

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