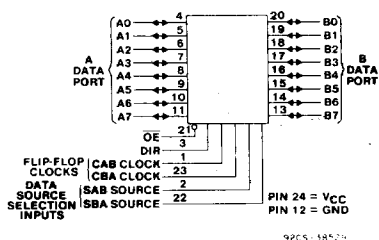


Advance Information

CD54/74AC647, CD54/74AC649 CD54/74ACT647, CD54/74ACT649

Octal-Bus Transceiver/Registers, with Open Drain

CD54/74AC/ACT647 - Non-Inverting
CD54/74AC/ACT649 - Inverting



FUNCTIONAL DIAGRAM

Type Features:

- Buffered inputs
- Typical propagation delay:
7 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

The RCA CD54/74AC647 and CD54/74AC649 and the CD54/74ACT647 and CD54/74ACT649 open-drain, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC649 and CD54/74ACT649 have inverting outputs. The CD54/74AC647 and CD54/74ACT647 have non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable (OE) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable (OE) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable (OE) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

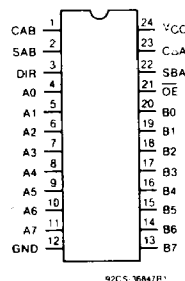
The CD74AC/ACT647 and CD74AC/ACT649 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to $+85^\circ\text{C}$); and Extended Industrial/Military (-55 to $+125^\circ\text{C}$).

The CD54AC/ACT647 and CD54AC/ACT649, available in chip form (H suffix), are operable over the -55 to $+125^\circ\text{C}$ temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.



TERMINAL ASSIGNMENT

9

CD54/74AC647, CD54/74AC649

CD54/74ACT647, CD54/74ACT649

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
OE	DIR	CAB	CBA	SAB	SBA	AD THRU A7	B0 THRU B7	647	649
X	X		X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X		X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X			X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\bar{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Store $\bar{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\bar{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\bar{A}$ Data to B Bus

#The data output functions may be enabled or disabled by various signals at the $\bar{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10 k Ω resistors.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	± 50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND})	± 100 mA*
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A)	-55 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum	$+265^\circ\text{C}$
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} *, (For T_A = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, V_I , V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC647, CD54/74AC649

CD54/74ACT647, CD54/74ACT649

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V _{cc} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V _i (V)	I _o (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V _{IH}			1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage V _{IL}			1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
Low-Level Output Voltage V _{OL}	V _{OL} or V _{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, * {	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I _I	V _{cc} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Off-State Leakage Current I _{OZ}	V _{IH} or V _{IL} V _O = V _{cc} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I _{cc}	V _{cc} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC647, CD54/74AC649

CD54/74ACT647, CD54/74ACT649

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V _{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
Low-Level Output Voltage	V _{OL}	V _{OL} or V _{IL} #,* }	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Off-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
$\overline{OE}$	1.17
A_n, B_n	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC647, CD54/74AC649

CD54/74ACT647, CD54/74ACT649

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f _{max}	1.5 3.3* 5†	11 101 143	— — —	10 89 125	— — —	MHz
Setup Time Data to Clock	t _{SU}	1.5 3.3 5	15.8 3.1 2.2	— — —	18 3.5 2.5	— — —	ns
Hold Time Data to Clock	t _H	1.5 3.3 5	2 2 2	— — —	2 2 2	— — —	ns
Clock Pulse Width	t _w	1.5 3.3 5	44 4.9 3.5	— — —	50 5.6 4	— — —	ns

*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:		1.5	—	154	—	169	
Stored A Data to B Bus 647	t _{PZL}	3.3*	5.2	18.4	5.1	20.2	ns
Stored B Data to A Bus		5†	3.5	12.3	3.4	13.5	
Stored A Data to B Bus 649		1.5	—	166	—	183	
Stored B Data to A Bus	t _{PLZ}	3.3	4.7	18.6	4.6	18.3	ns
		5	3.8	13.3	3.7	14.6	
A Data to B Bus 647		1.5	—	125	—	138	
B Data to A Bus	t _{PZL}	3.3	4.2	15	4.1	16.5	ns
		5	2.8	10	2.8	11	
A Data to B Bus 649		1.5	—	137	—	151	
B Data to A Bus	t _{PLZ}	3.3	3.9	13.7	3.8	15.1	ns
		5	3.1	11	3	12.1	
Select to Data 647, 649		1.5	—	136	—	150	
	t _{PZL}	3.3	4.6	16.4	4.5	18	ns
		5	3.1	10.9	3	12	
		1.5	—	149	—	164	
	t _{PLZ}	3.3	4.2	14.9	4.6	16.4	ns
		5	3.4	11.9	3.3	13.1	
Enable, Disable Times		1.5	—	154	—	169	
Bus to Output or	t _{PZL}	3.3	5.2	18.4	5.1	20.2	ns
Register to Output	t _{PLZ}	5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C _{PD} §	—	150 Typ.		150 Typ.		pF
Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C _I	—	—	10	—	10	pF
Off-State Output Capacitance	C _O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V†5 V: min. is @ 5.5 V
max. is @ 4.5 V§C_{PD} is used to determine the dynamic power consumption, per package.
$$P_D = V_{CC}^2 C_{PD} f_i + \sum V_{CC}^2 C_{L_o} f_o$$

where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC647, CD54/74AC649 **CD54/74ACT647, CD54/74ACT649**

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f _{max}	5*	125	—	110	—	MHz
Setup Time Data to Clock	t _{su}	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t _h	5	2	—	2	—	ns
Clock Pulse Width	t _w	5	3.9	—	4.5	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3$ ns, $C_L = 50$ pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Stored A Data to B Bus 647 Stored B Data to A Bus Stored A Data to B Bus 649 Stored B Data to A Bus	t _{PZL} t _{PLZ}	5* 5	4 4.3	14.1 15.1	3.9 4.2	15.5 16.6	ns ns
A Data to B Bus 647 B Data to A Bus A Data to B Bus 649 B Data to A Bus	t _{PZL} t _{PLZ}	5 5	3.2 3.5	11.4 12.4	3.1 3.4	12.5 13.6	ns ns
Select to Data 647, 649	t _{PZL}	5	4	14.1	3.9	15.5	ns
	t _{PLZ}	5	4.3	15.1	4.2	16.6	ns
Enable, Disable Times Bus to Output or Register to Output	t _{PZL} t _{PLZ}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C _{PD§}	—	150 Typ.		150 Typ.		pF
Max. (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C _I	—	—	10	—	10	pF
Off-State Output Capacitance	C _O	—	—	15	—	15	pF

*5 V min. is @ 5.5 V
max. is @ 4.5 V

$\S C_{PD}$ is used to determine the dynamic power consumption, per package.

$P_D = V_{CC}^2 C_{PD} f_i + \sum V_{CC}^2 C_L f_o + V_{CC} I_{CC}$ where f_i = input frequency

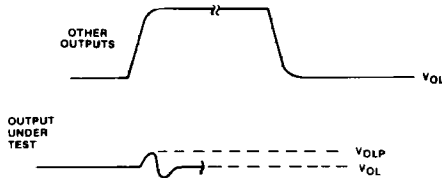
f_o = output frequency

C_L = output load capacitance

V_{CC} = supply voltage.

CD54/74AC647, CD54/74AC649 CD54/74ACT647, CD54/74ACT649

PARAMETER MEASUREMENT INFORMATION

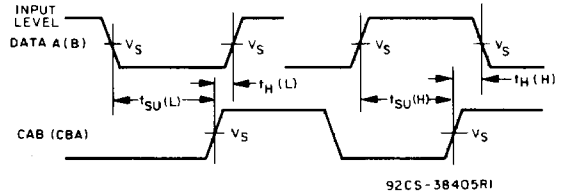


NOTES:

1. V_{OLP} IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
 $PRR \leq 1 \text{ MHz}$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.
 IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH $0.1 \mu\text{F}$ CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

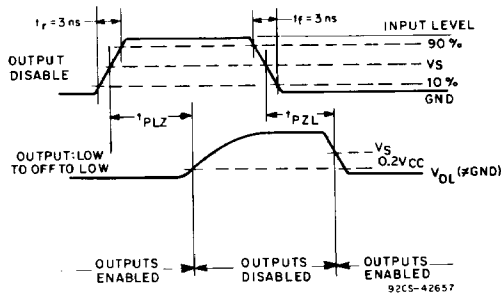
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Fig. 1 - Simultaneous switching transient waveforms.

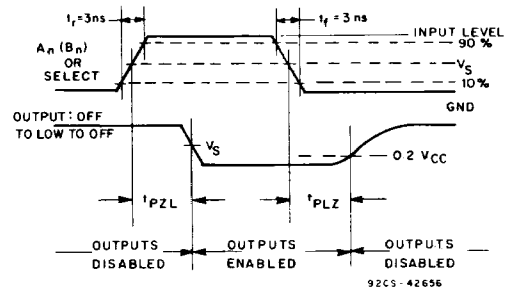


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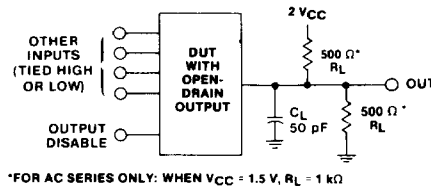
Fig. 2 - Data setup and hold times.



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92CS-42656



*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5 \text{ V}$, $R_L = 1 \text{ k}\Omega$

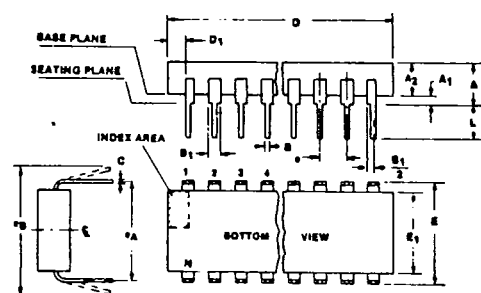
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Fig. 3 - Open-drain propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Dual-In-Line Plastic Packages

T-90-20

(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E₁ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead lip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D₁ at the left end of the package must equal dimension D₁ at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

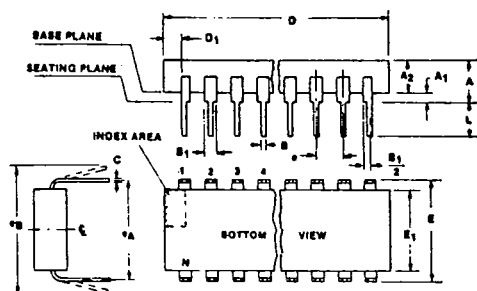
(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

Dual-In-Line Plastic Packages

T-90-20

(E) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

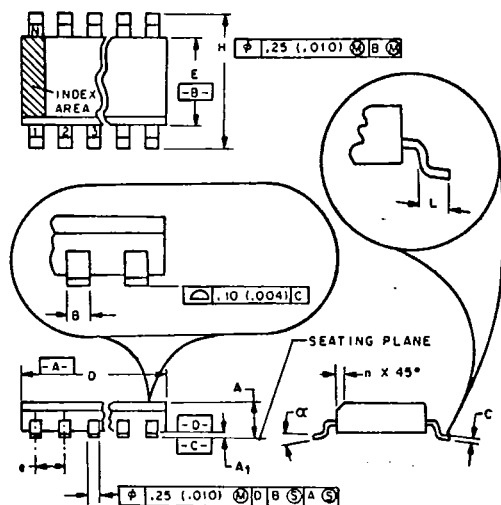
$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E₁ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around

center line shown in end view.

8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D₁ at the left end of the package must equal dimension D₁ at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

13

T-90-20



14-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A ₁	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38924R2

16-Lead Dual-In-Line, Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0888	1.35	1.75	
A ₁	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38925R2

20-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A ₁	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4861	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
h	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38926R2

24-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A ₁	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39037R2