

SN54AHC16540, SN74AHC16540 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS331F – MARCH 1996 – REVISED JANUARY 2000

- Members of the Texas Instruments **Widebus™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

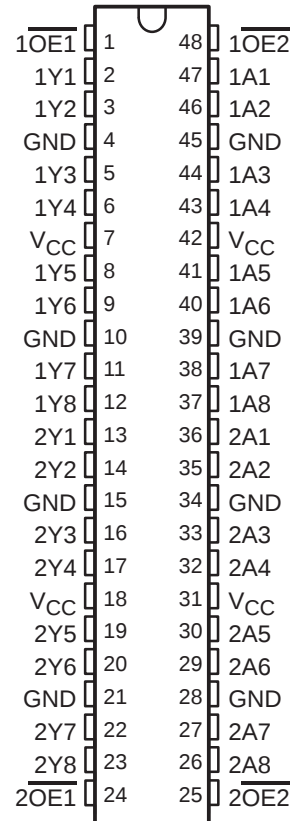
These 16-bit buffers and bus drivers provide a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC16540 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC16540 is characterized for operation from -40°C to 85°C .

SN54AHC16540 . . . WD PACKAGE
SN74AHC16540 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 8-bit buffer/driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z



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**TEXAS
INSTRUMENTS**

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$\overline{10E1}$	1				
$\overline{10E2}$	48		EN1		
$\overline{20E1}$	24		&		
$\overline{20E2}$	25		EN2		
1A1	47	1	1 ▽	2	1Y1
1A2	46			3	1Y2
1A3	44			5	1Y3
1A4	43			6	1Y4
1A5	41			8	1Y5
1A6	40			9	1Y6
1A7	38			11	1Y7
1A8	37			12	1Y8
2A1	36			13	2Y1
2A2	35	1	2 ▽	14	2Y2
2A3	33			16	2Y3
2A4	32			17	2Y4
2A5	30			19	2Y5
2A6	29			20	2Y6
2A7	27			22	2Y7
2A8	26			23	2Y8

logic diagram (positive logic)



Supply voltage range, V_{CC}		-0.5 V to 7 V
Input voltage range, V_I (see Note 1)		-0.5 V to 7 V
Output voltage range, V_O (see Note 1)		-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)		-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		± 25 mA
Continuous current through each V_{CC} or GND		± 75 mA
Package thermal impedance, θ_{JA} (see Note 2):		
DGG package		70°C/W
DGV package		58°C/W
DL package		63°C/W

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

			SN54AHC16540		SN74AHC16540		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 3 V	2.1		2.1		
		V _{CC} = 5.5 V	3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 3 V		0.9		0.9	
		V _{CC} = 5.5 V		1.65		1.65	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		−50		−50	μA
		V _{CC} = 3.3 V ± 0.3 V		−4		−4	mA
		V _{CC} = 5 V ± 0.5 V		−8		−8	
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 3.3 V ± 0.3 V		4		4	mA
		V _{CC} = 5 V ± 0.5 V		8		8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V _{CC} = 5 V ± 0.5 V		20		20	
T _A	Operating free-air temperature		−55	125	−40	85	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC16540		SN74AHC16540		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I _{OZ}	V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH}	5.5 V			±0.25		±2.5		±2.5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	µA
C _i	V _I = V _{CC} or GND	5 V		2	10				10	pF
C ₀	V _O = V _{CC} or GND	5 V		3						pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC16540		SN74AHC16540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF		4.8**	8.4**	1**	10**	1	10	ns
t _{PHL}					4.8**	8.4**	1**	10**	1	10	
t _{PZH}	$\overline{\text{OE}}$	Y	C _L = 15 pF		6.8**	10.6**	1**	12.5**	1	12.5	ns
t _{PZL}					6.8**	10.6**	1**	12.5**	1	12.5	
t _{PHZ}	$\overline{\text{OE}}$	Y	C _L = 15 pF		6.8**	11.5**	1**	12.5**	1	12.5	ns
t _{PLZ}					6.8**	11.5**	1**	12.5**	1	12.5	
t _{PLH}	A	Y	C _L = 50 pF		7.7	11	1	12.5	1	12.5	ns
t _{PHL}					7.3	11	1	12.5	1	12.5	
t _{PZH}	$\overline{\text{OE}}$	Y	C _L = 50 pF		9.7	14.1	1	16	1	16	ns
t _{PZL}					7.1	14.1	1	16	1	16	
t _{PHZ}	$\overline{\text{OE}}$	Y	C _L = 50 pF		9.4	14	1	16	1	16	ns
t _{PLZ}					9.7	14	1	16	1	16	
t _{sk(0)}			C _L = 50 pF			1.5***				1.5	ns

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

*** On products compliant to MIL-PRF-38535, this parameter does not apply.

SN54AHC16540, SN74AHC16540
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16540		SN74AHC16540		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.7*	6*		1*	7*	1	7	ns
t_{PHL}				3.7*	6*		1*	7*	1	7	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	4.7*	7.3*		1*	8.5*	1	8.5	ns
t_{PZL}				4.7*	7.3*		1*	8.5*	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	4.5*	7.2*		1*	8.5*	1	8.5	ns
t_{PLZ}				4.5*	7.2*		1*	8.5*	1	8.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.2	8		1	9	1	8.5	ns
t_{PHL}				5.2	8		1	9	1	8.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.2	9.3		1	10.5	1	10.5	ns
t_{PZL}				6.2	9.3		1	10.5	1	10.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6	9.2		1	10.5	1	10.5	ns
t_{PLZ}				6	9.2		1	10.5	1	10.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1**					1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHC16540			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

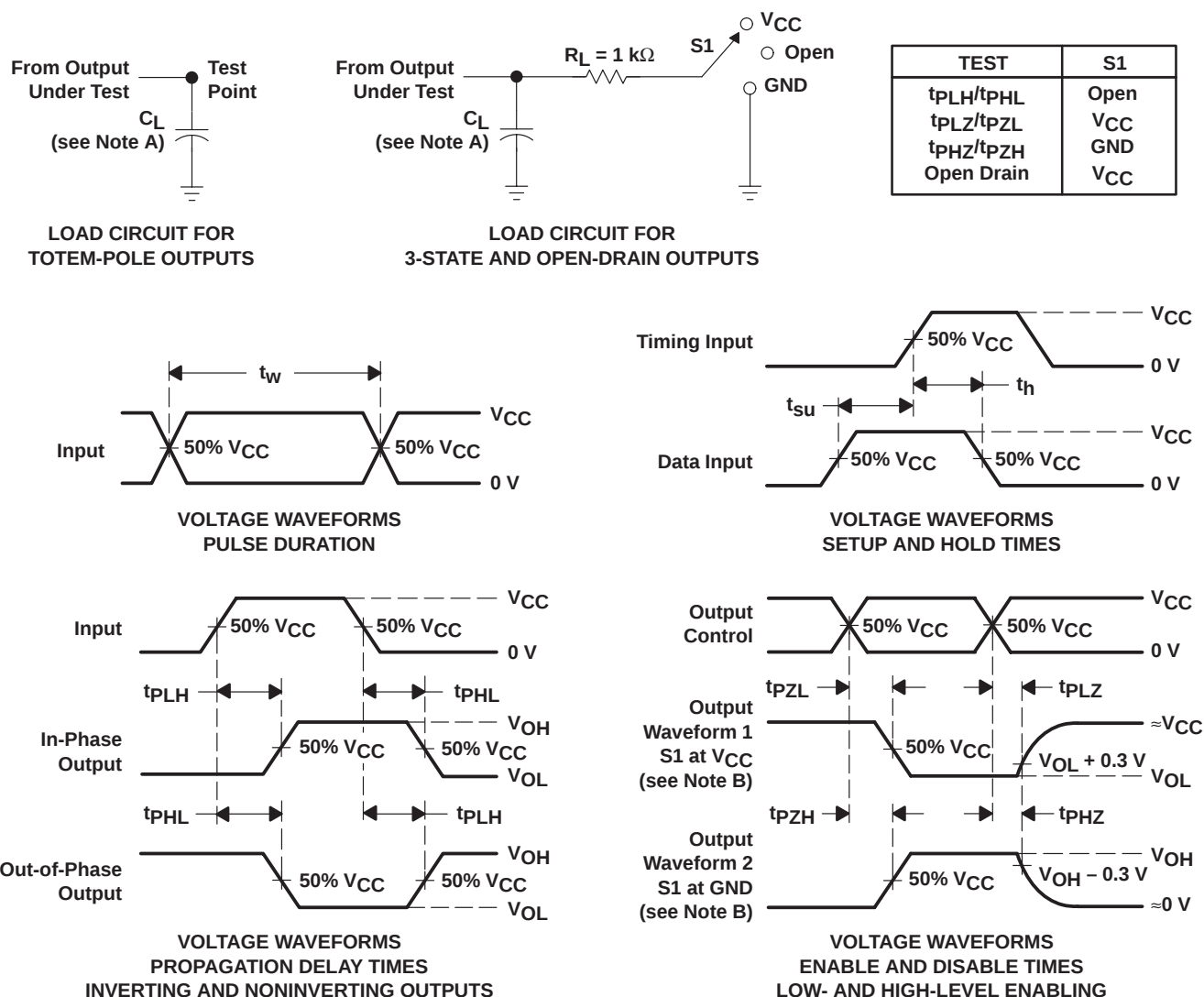
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	13	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AHC16540DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16540DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16540DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74AHC16540DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16540DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16540DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16540DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC16540DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC16540DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74AHC16540DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



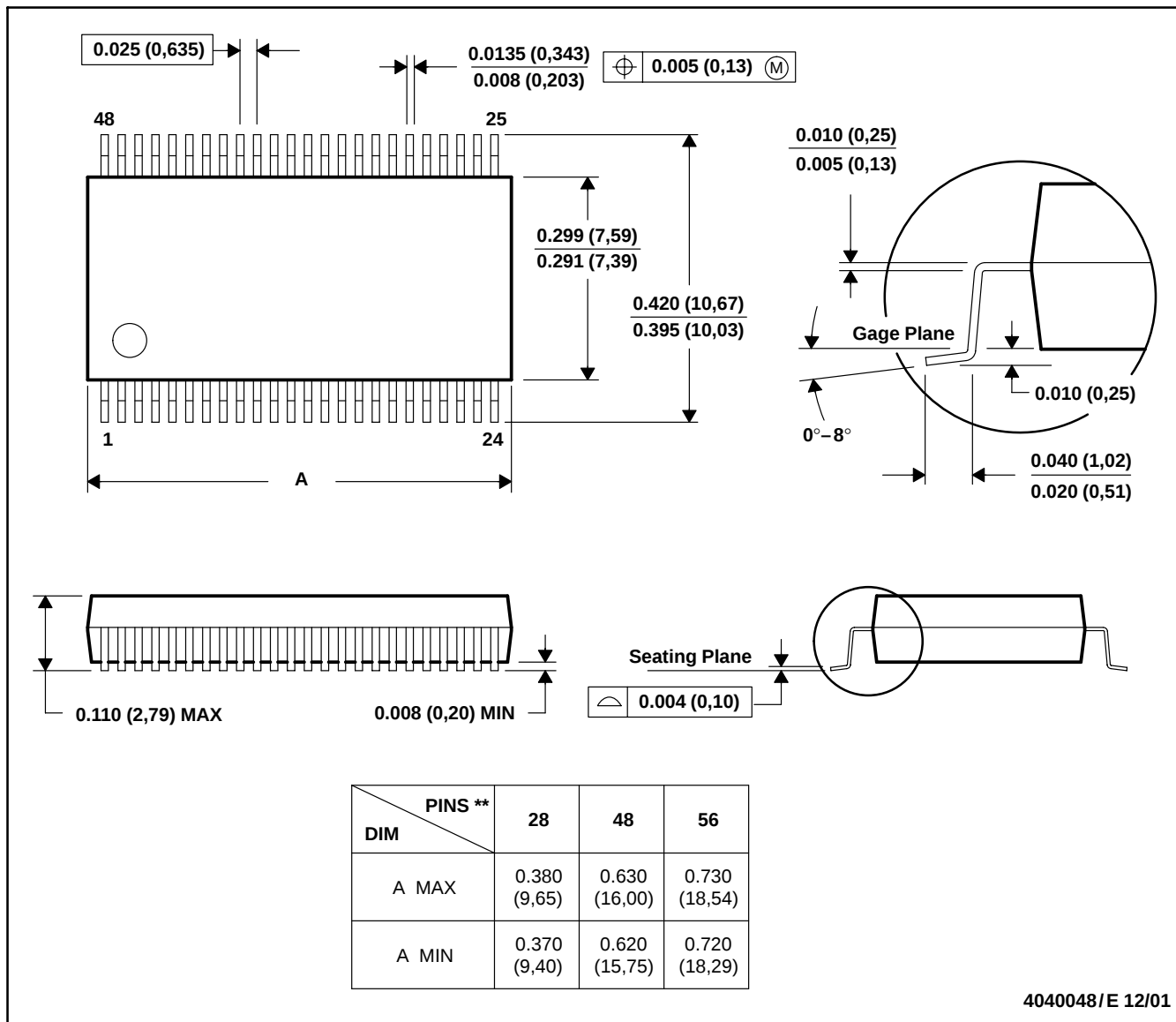
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC16540DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74AHC16540DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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