ISL84582

Low-Voltage, Single and Dual Supply, Differential 4-to-1 Multiplexer

FN6213
Rev 3.00
May 6, 2009

The Intersil ISL84582 device is made of precision, bi-directional, analog switches configured as a differential 4-Channel multiplexer/demultiplexer. It is designed to operate from a single +2V to +12V supply or from a ±2V to ±6V dual supplies. The device has an inhibit pin to simultaneously open all signal paths.

ON-resistance of 39Ω with a ±5V supply and 125Ω with a single +3.3V supply. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 0.02nA at +25°C or 0.2nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS logic compatibility when using a single 3.3V or +5V supply or dual ±5V supplies.

The ISL84582 is a differential 4-to-1 multiplexer device. Table 1 summarizes the performance of this part.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	DIFF 4:1 Mux
±5V r_{ON}	39Ω
±5V t_{ON}/t_{OFF}	32ns/18ns
12V r_{ON}	32Ω
12V t_{ON}/t_{OFF}	23ns/15ns
5V r_{ON}	65Ω
5V t_{ON}/t_{OFF}	43ns/20ns
3.3V r_{ON}	125Ω
3.3V t_{ON}/t_{OFF}	70ns/32ns
Package	16 Ld TSSOP

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”
- Application Note AN520 “CMOS Analog Multiplexers and Switches; Specifications and Application Considerations.”
- Application Note AN1034 “Analog Switch and Multiplexer Applications”

Features

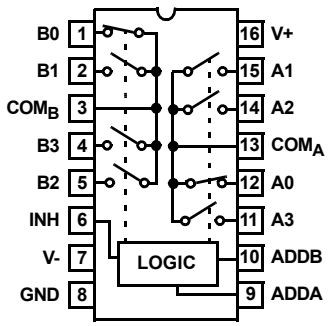
- Pb-Free (RoHS Compliant)
- Fully Specified at 3.3V, 5V, ±5V, and 12V Supplies for 10% Tolerances
- ON-resistance (r_{ON}), V_S = ±4.5V 44Ω
- ON-resistance (r_{ON}), V_S = +3V 175Ω
- r_{ON} Matching Between Channels, V_S = ±5V . . . . . <2Ω
- Low Charge Injection, V_S = ±5V . . . . . 1pC (Max)
- Single Supply Operation . . . . . +2V to +12V
- Dual Supply Operation . . . . . ±2V to ±6V
- Low Power Consumption (P_D) . . . . . <3µW
- Fast Switching Action (V_S = +5V)
  - t_{ON} 43ns
  - t_{OFF} 20ns
- Guaranteed Max Off-Leakage 2.5nA
- Guaranteed Break-Before-Make
- TTL, CMOS Compatible

Applications

- Battery Powered, Handheld, and Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrastructure
  - ADSL, VDSL Modems
- Test Equipment
  - Medical Ultrasound
  - Magnetic Resonance Image
  - CT and PET Scanners (MRI)
  - ATE
  - Electrocardiograph
- Audio and Video Signal Routing
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

Pinout

ISL84582
(16 LD TSSOP)
TOP VIEW



Truth Table

ISL84582			
INH	**ADDB**	**ADDA**	**SWITCH ON**
1	X	X	NONE
0	0	0	A0, B0
0	0	1	A1, B1
0	1	0	A2, B2
0	1	1	A3, B3

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V, with V+ between 3V and 10V. X = Don’t Care.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL84582IVZ	84582 IVZ	-40 to +85	16 Ld TSSOP	M16.173
ISL84582IVZ-T*	84582 IVZ	-40 to +85	16 Ld TSSOP Tape and Reel	M16.173

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

PIN	FUNCTION
V+	Positive Power Supply Pin
V-	Negative Power Supply Pin. Connect to GND for Single Supply Configurations.
GND	Ground Connection
INH	Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off.
COMx	Analog Mux Common Pin
Ax, Bx	Analog Mux Signal Pin
ADDx	Address Input Pin

Absolute Maximum Ratings

V+ to V- . . . . . -0.3 to 15V
V+ to GND . . . . . -0.3 to 15V
V- to GND. . . . . -15 to 0.3V
Input Voltages
INH, NO, NC, ADD (Note 1). . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 1). . . . . -0.3 to ((V+) + 0.3V)
Continuous Current (Any Terminal) . . . . . ±30mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating
Human Body Model (Per Mil-STD-883, Method 3015.7) . . . >2kV

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
16 Ld TSSOP Package	150

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. Signals on NC, NO, COM, ADD, INH exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications: ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 10)	TYP	MAX (Notes 4, 10)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}	(Note 9)	Full	V-	-	V+	V
ON-resistance, r_{ON}	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = 3V, (See Figure 5)	25	-	44	60	Ω
		Full	-	-	80	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = 3V, (Note 5)	25	-	1.3	4	Ω
		Full	-	-	6	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±4.5V, I_{COM} = 2mA, V_{NO} or V_{NC} = ±3V, 0.1V, (Note 6)	25	-	7.5	9	Ω
		Full	-	-	12	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V, (Note 7)	25	-	0.02	-	nA
		Full	-	0.2	-	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V, (Note 7)	25	-	0.02	-	nA
		Full	-	0.2	-	nA
COM ON Leakage Current, $I_{COM(ON)}$	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V, (Note 7)	25	-	0.02	-	nA
		Full	-	0.2	-	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INHH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INHL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, I_{INHH}, I_{INHL}	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+, (Note 9)	Full	-0.5	0.03	0.5	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (see Figure 1, Note 9)	25	-	35	50	ns
		Full	-	-	60	ns
Inhibit Turn-OFF Time, t_{OFF}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (see Figure 1, Note 9)	25	-	22	35	ns
		Full	-	-	40	ns
Address Transition Time, t_{TRANS}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3 (see Figure 1, Note 9)	25	-	43	60	ns
		Full	-	-	70	ns

Electrical Specifications: ±5V Supply Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 10)	TYP	MAX (Notes 4, 10)	UNITS
Break-Before-Make Time, t_{BBM}	V_S = ±5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (see Figure 3, Note 9)	Full	2	7	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (see Figure 2, Note 9)	25	-	0.3	1	pC
NO/NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	3	-	pF
COM OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	12	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (see Figure 7)	25	-	18	-	pF
OFF-Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} = $1V_{RMS}$ (see Figures 4, 6 and 19)	25	-	92	-	dB
Crosstalk, (Note 8)		25	-	≤110	-	dB
All Hostile Crosstalk, (Note 8)		25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	±4.5	-	±5.5	V
Positive Supply Current, I+	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off, (Note 9)	Full	-1	-	1	µA
Negative Supply Current, I-		Full	-1	-	1	µA

Electrical Specifications: 12V Supply Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 10)	TYP	MAX (Notes 4, 10)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}	(Note 9)	Full	0	-	V+	V
ON-resistance, r_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V, (See Figure 5)	25	-	37	45	Ω
		Full	-	-	55	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 9V, (Note 5)	Full	-	1.2	2	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 10.8V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, 6V, 9V, (Note 6)	Full	-	5	-	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 13.2V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 12V, 1V, (Note 7)	25	-	0.02	-	nA
		Full	-	0.2	-	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	V+ = 13.2V, V_{COM} = 12V, 1V, V_{NO} or V_{NC} = 1V, 12V, (Note 7)	25	-	0.02	-	nA
		Full	-	0.2	-	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 13.2V, V_{COM} = 1V, 12V, V_{NO} or V_{NC} = 1V, 12V, or floating, (Note 7)	25	-	0.02	-	nA
		Full	-	0.2	-	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INHH}, V_{ADDH}		Full	3.7	-	-	V
Input Voltage Low, V_{INHL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, I_{INHH}, I_{INHL}	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA

Electrical Specifications: 12V Supply Test Conditions: V+ = +10.8V to +13.2V, GND = 0V, V_{INH} = 4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 10)	TYP	MAX (Notes 4, 10)	UNITS
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4, (See Figure 1, Note 9)	25	-	24	40	ns
		Full	-	-	45	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4, (See Figure 1, Note 9)	25	-	15	30	ns
		Full	-	-	35	ns
Address Transition Time, t_{TRANS}	V+ = 10.8V, V_{NO} or V_{NC} = 10V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 4, (See Figure 1, Note 9)	25	-	27	50	ns
		Full	-	-	55	ns
Break-Before-Make Time Delay, t_D	V+ = 13.2V, R_L = 300Ω, C_L = 35pF, V_{NO} or V_{NC} = 10V, V_{IN} = 0 to 4, (See Figure 3, Note 9)	Full	2	5	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2, Note 9)	25	-	2.7	5	pC
OFF-Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, (See Figure 4, 6 and 19)	25	-	92	-	dB
Crosstalk, (Note 8)		25	-	≤110	-	dB
All Hostile Crosstalk, (Note 8)		25	-	-105	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (See Figure 7)	25	-	3	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (See Figure 7)	25	-	12	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (See Figure 7)	25	-	18	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	10.8	-	13.2	V
Positive Supply Current, I+	V+ = 13.2V, V_{INH}, V_{ADD} = 0V or V+, all channels on or off (Note 9)	Full	-1	-	1	µA

Electrical Specifications: 5V Supply Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 10)	TYP	MAX (Notes 4, 10)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}	(Note 9)	Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V, (See Figure 5)	25	-	81	100	Ω
		Full	-	-	120	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3V, (Note 5)	25	-	2.2	4	Ω
		Full	-	-	6	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V, (Note 6)	Full	-	11.5	-	Ω
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INHH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INHL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, I_{INHH}, I_{INHL}	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+, (Note 9)	Full	-0.5	-	0.5	µA

Electrical Specifications: 5V Supply Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 10)	TYP	MAX (Notes 4, 10)	UNITS
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (see Figure 1, Note 9)	25	-	43	60	ns
		Full	-	-	70	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (see Figure 1, Note 9)	25	-	20	35	ns
		Full	-	-	40	ns
Address Transition Time, t_{TRANS}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (see Figure 1, Note 9)	25	-	51	70	ns
		Full	-	-	85	ns
Break-Before-Make Time, t_{BBM}	V+ = 5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (See Figure 3, Note 9)	Full	2	9	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2, Note 9)	25	-	0.6	1.5	pC
OFF-Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NOx} = 1V_{RMS} (see Figures 4, 6 and 19)	25	-	92	-	dB
Crosstalk, (Note 8)		25	-	≤110	-	dB
All Hostile Crosstalk, (Note 8)		25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	4.5	-	5.5	V
Positive Supply Current, I+	V+ = 5.5V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off, (Note 9)	Full	-1	-	1	µA

Electrical Specifications: 3.3V Supply Test Conditions: V+ = +3V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3) Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 10)	TYP	MAX (Notes 4, 10)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}	(Note 9)	Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V (See Figure 5)	25	-	175	180	Ω
		Full	-	-	200	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V, (Note 5)	25	-	3.4	8	Ω
		Full	-	-	10	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.0V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 0.5V, 1V, 2V, (Note 6)	Full	-	55	-	Ω
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INHH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INHL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{ADDH}, I_{ADDL}, I_{INHH}, I_{INHL}	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+, (Note 9)	Full	-0.5	-	0.5	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (see Figure 1, Note 9)	25	-	82	100	ns
		Full	-	-	120	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (see Figure 1, Note 9)	25	-	37	50	ns
		Full	-	-	60	ns
Address Transition Time, t_{TRANS}	V+ = 3.0V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (see Figure 1, Note 9)	25	-	96	120	ns
		Full	-	-	145	ns

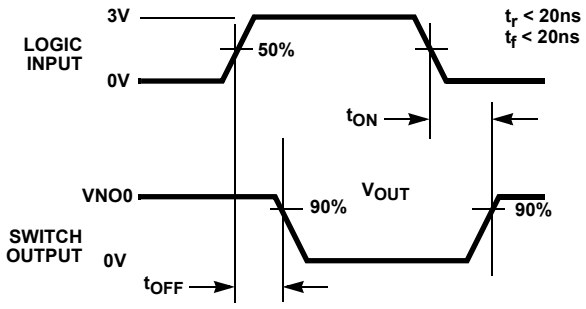
Electrical Specifications: 3.3V Supply Test Conditions: V+ = +3V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 3) Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 4, 10)	TYP	MAX (Notes 4, 10)	UNITS
Break-Before-Make Time, t_{BBM}	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V (see Figure 3, Note 9)	Full	3	13	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2, Note 9)	25	-	0.3	1	pC
OFF-Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$ (see Figures 4, 6 and 19)	25	-	92	-	dB
Crosstalk, (Note 8)		25	-	≤110	-	dB
All Hostile Crosstalk, (Note 8)		25	-	-105	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	3.0	-	3.6	V
Positive Supply Current, I+	V+ = 3.6V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off, (Note 9)	Full	-1	-	1	µA

NOTES:

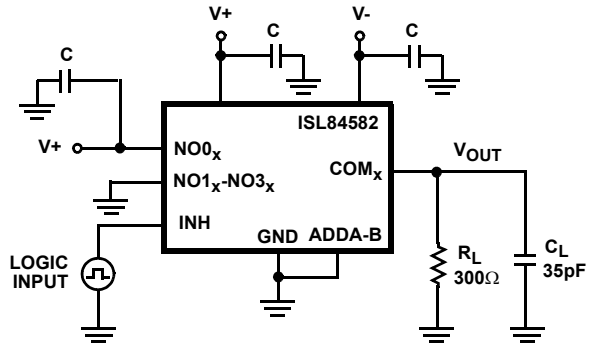
3. V_{IN} = Input logic voltage to configure the device in a given state.
4. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. $\Delta r_{ON} = r_{ON}$ (MAX) - r_{ON} (MIN).
6. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
7. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at +25°C.
8. Between any two switches.
9. Limits established by characterization and are not production tested.
10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. INHIBIT t_{ON}/t_{OFF} MEASUREMENT POINTS

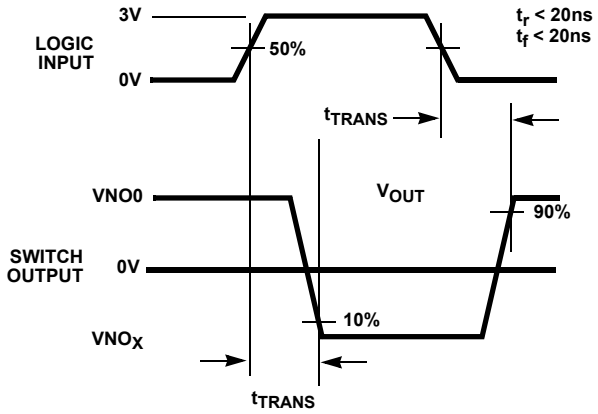


Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{(ON)}}$$

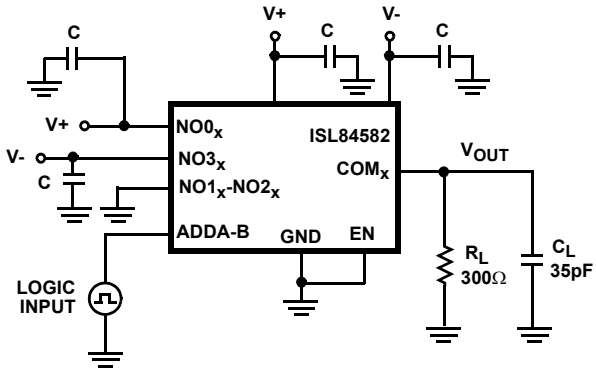
FIGURE 1B. INHIBIT t_{ON}/t_{OFF} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1D. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

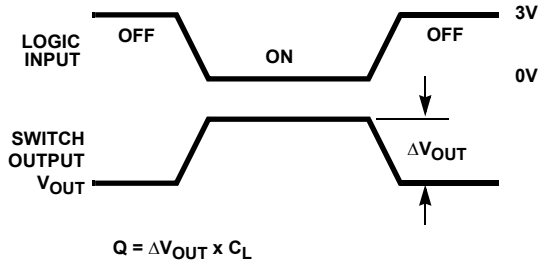
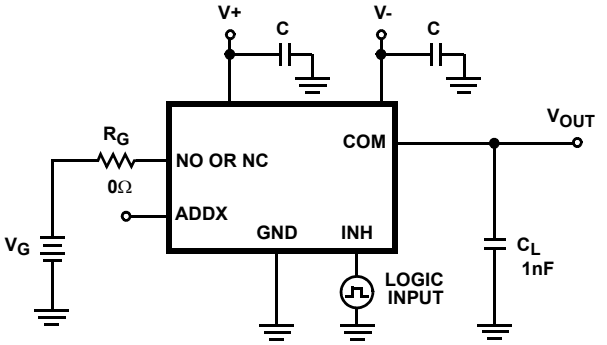


FIGURE 2A. Q MEASUREMENT POINTS



Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

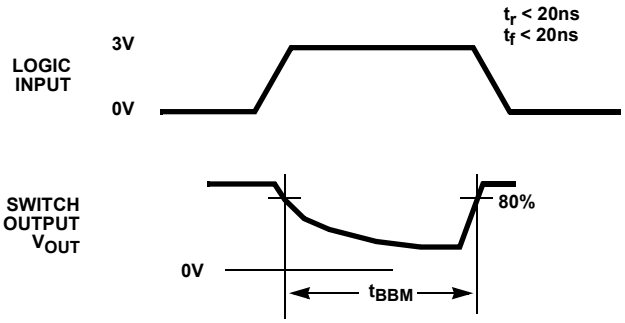
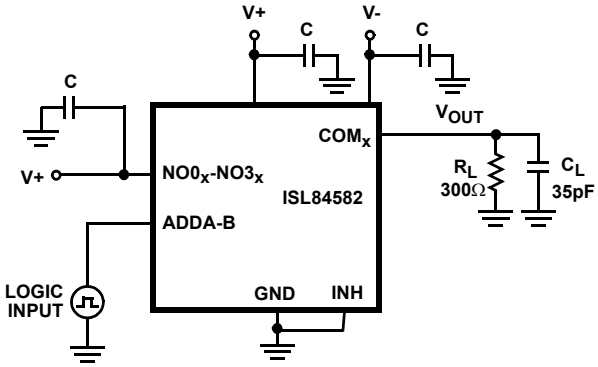


FIGURE 3A. t_{BBM} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

FIGURE 3B. t_{BBM} TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)

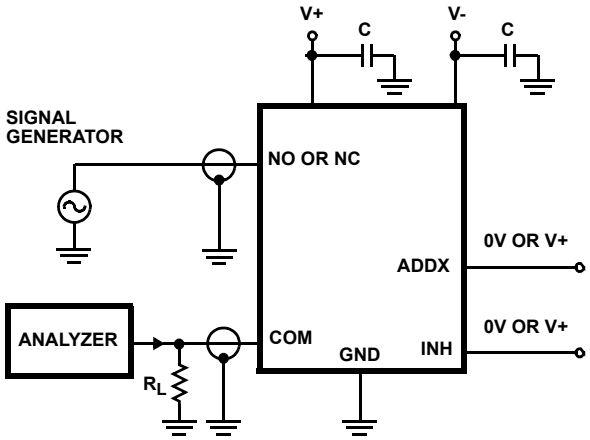


FIGURE 4. OFF-ISOLATION TEST CIRCUIT

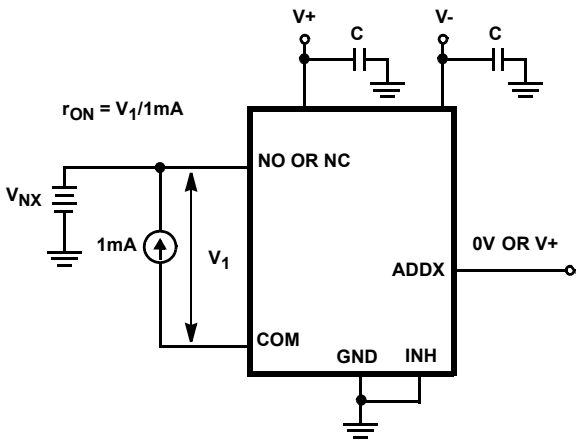


FIGURE 5. r_{ON} TEST CIRCUIT

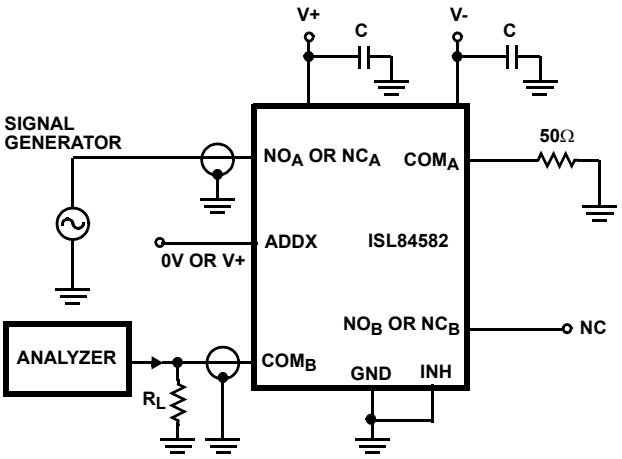


FIGURE 6. CROSSTALK TEST CIRCUIT

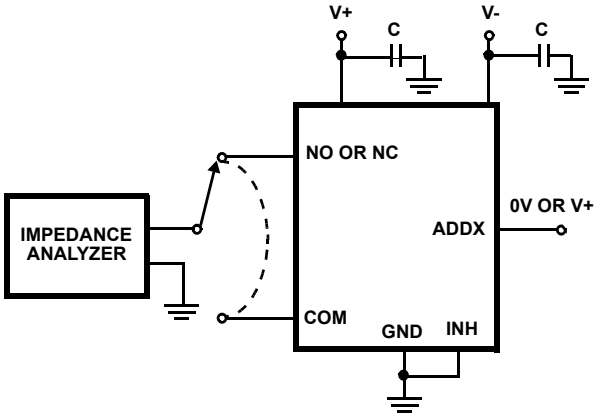


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL84582 multiplexer offers precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply with low ON-resistance (39Ω) and high speed operation (t_{ON} = 38ns, t_{OFF} = 19ns) with dual 5V supplies. The device is especially well suited to portable battery-powered equipment thanks to the low operating supply voltage (2V), low power consumption (3µW), low leakage currents (0.2nA). High frequency applications also benefit from the wide bandwidth, and the very high off-isolation and crosstalk rejection.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 8). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

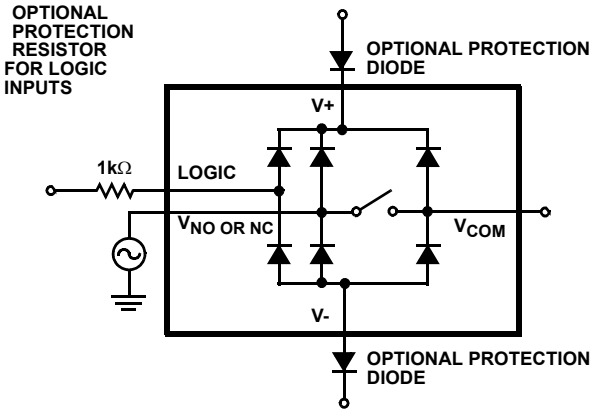


FIGURE 8. INPUT OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL84582 construction is typical of most CMOS analog switches, in that they have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V absolute maximum voltage, the ISL84582 15V absolute maximum voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

The ISL84582 performs equally well when operated with bipolar or single voltage supplies. The minimum recommended supply voltage is 2V or ±2V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the "Electrical Specification" tables beginning on page 5 and "Typical Performance Curves" beginning on page 11 for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This ISL84582 is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.7V to 10V. At 12V the V_{IH} level is about 3.3V. This is still below the CMOS guaranteed high output minimum level of 4V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 4V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 100MHz (see Figures 17 and 18). Figures 17 and 18 also illustrates that the frequency response is very consistent over varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off-Isolation is the resistance to this feed-through, while Crosstalk indicates the amount of feed through from one switch to another. Figure 19 details the high Off-Isolation and Crosstalk rejection provided by this family. At 10MHz, Off-Isolation is about 55dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off-Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

Typical Performance Curves

T_A = +25°C, Unless Otherwise Specified.

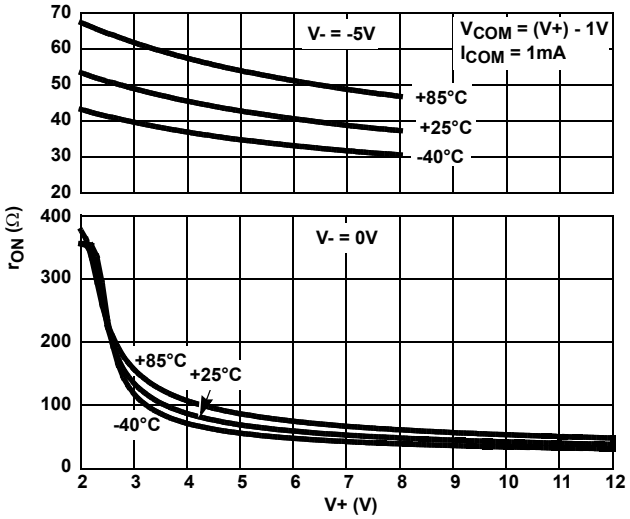


FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE

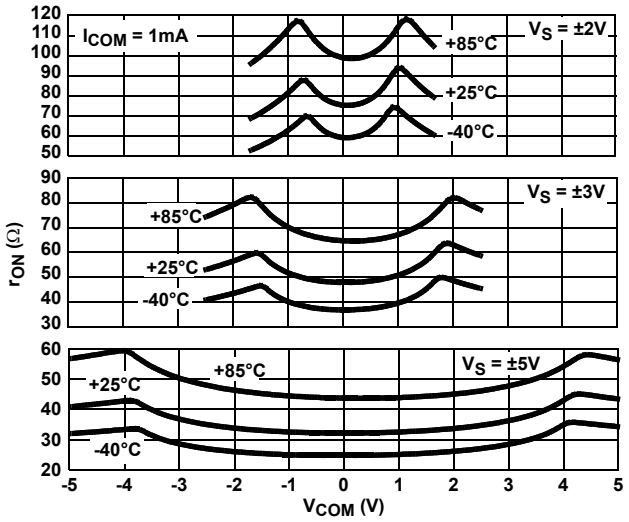


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

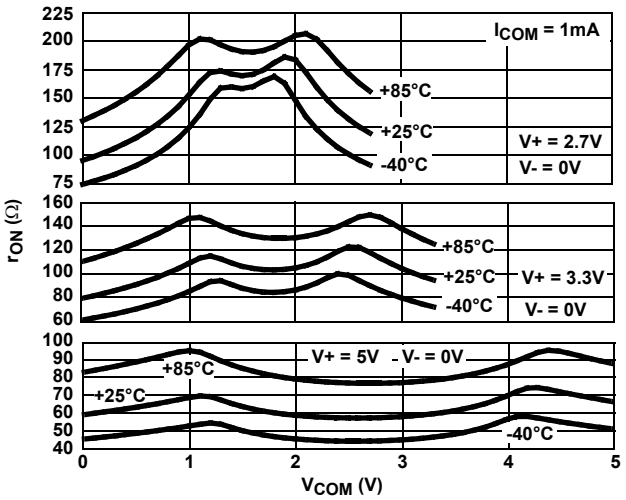


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

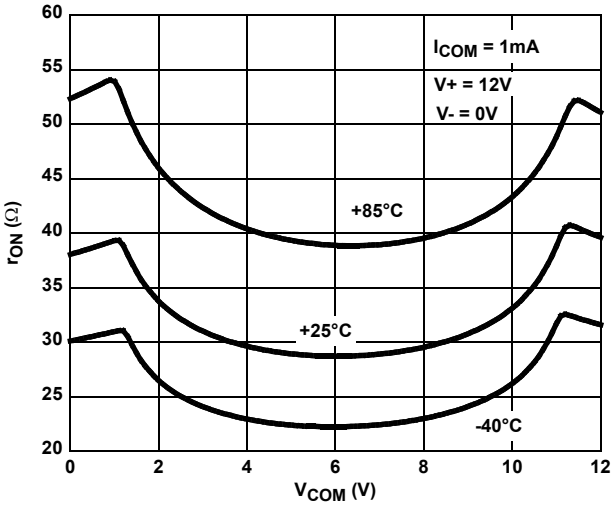


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

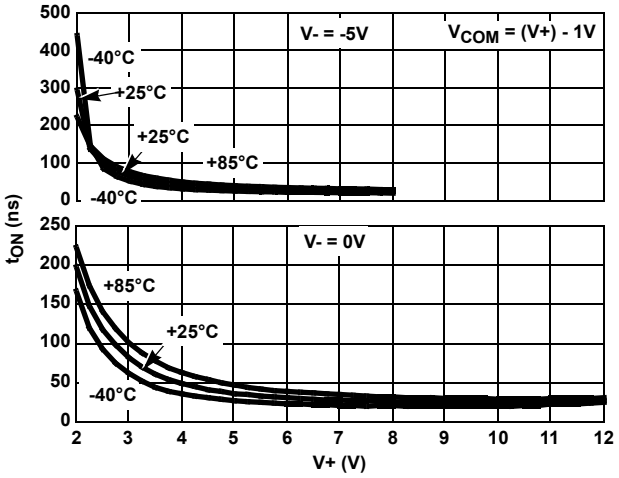


FIGURE 13. INHIBIT TURN-ON TIME vs SUPPLY VOLTAGE

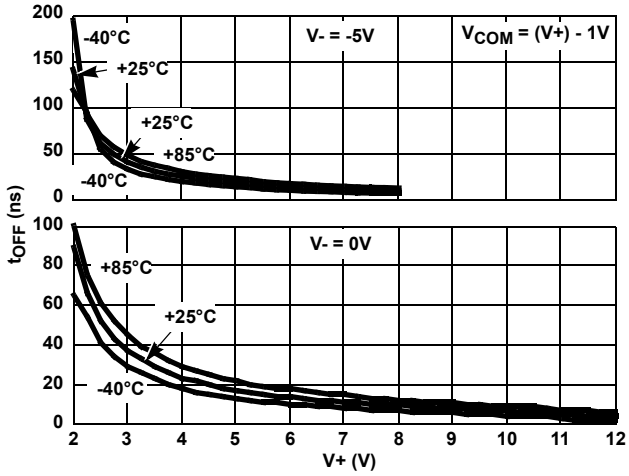


FIGURE 14. INHIBIT TURN-OFF TIME vs SUPPLY VOLTAGE

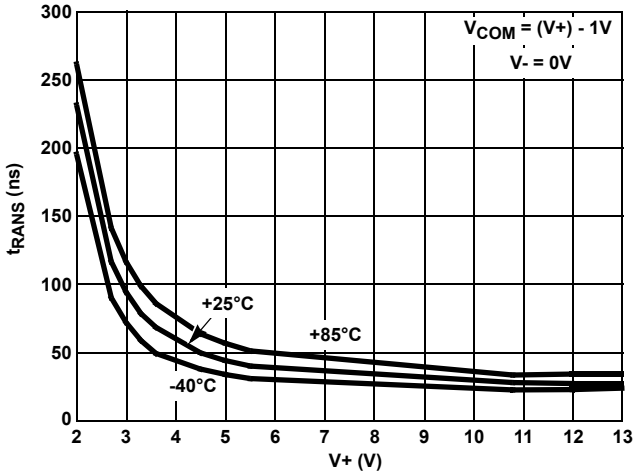


FIGURE 15. ADDRESS TRANS TIME vs SINGLE SUPPLY VOLTAGE

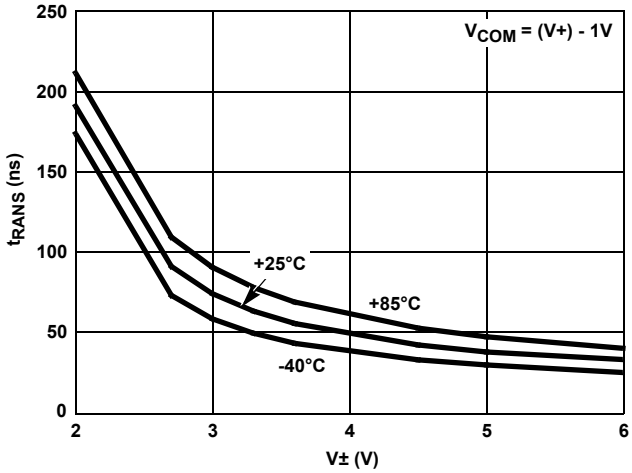


FIGURE 16. ADDRESS TRANS TIME vs DUAL SUPPLY VOLTAGE

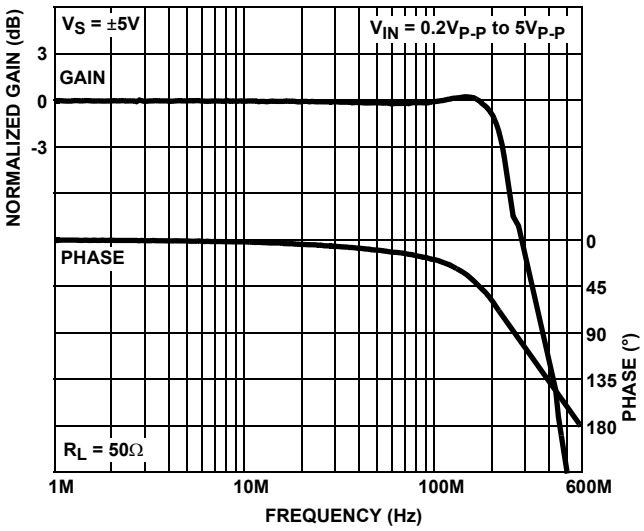


FIGURE 17. FREQUENCY RESPONSE

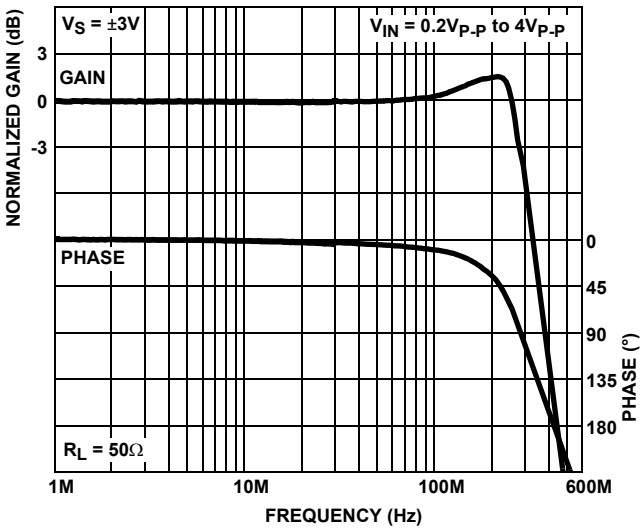


FIGURE 18. FREQUENCY RESPONSE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

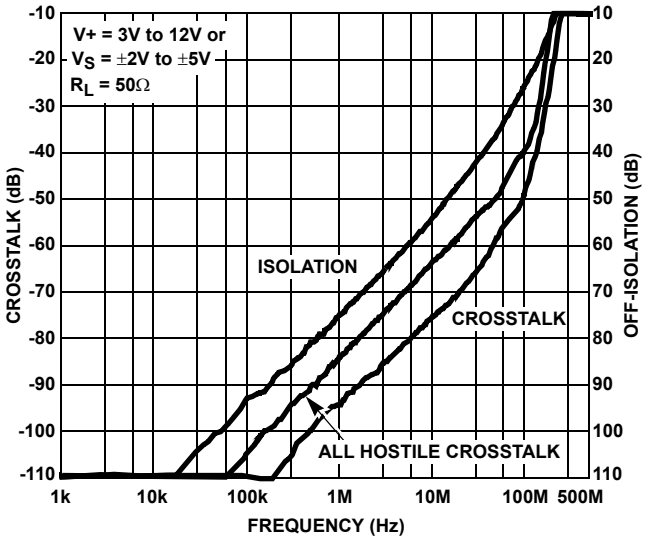


FIGURE 19. CROSSTALK AND OFF-ISOLATION

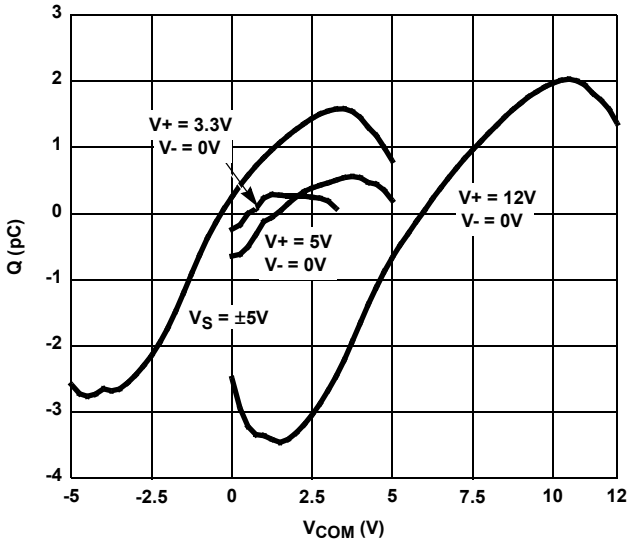


FIGURE 20. CHARGE INJECTION vs SWITCH VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

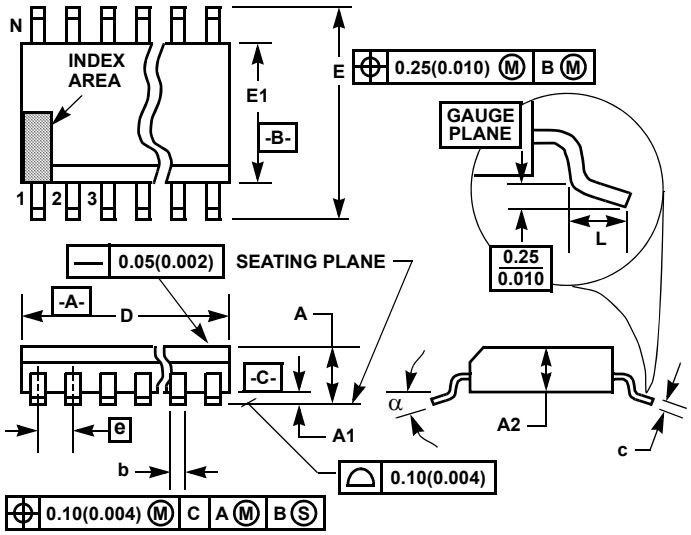
TRANSISTOR COUNT:

ISL84582: 193

PROCESS:

Si Gate CMOS

Thin Shrink Small Outline Plastic Packages (TSSOP)



M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 2/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

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