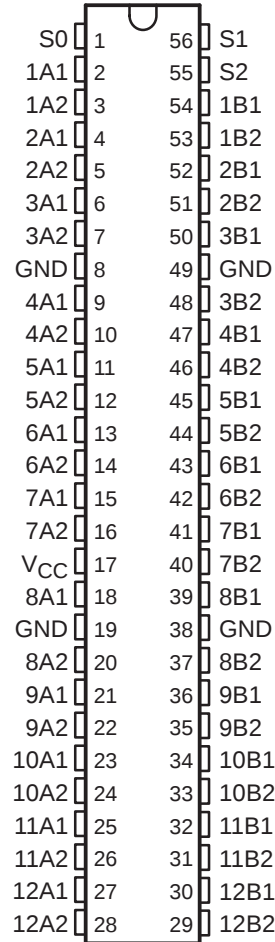


SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

SCDS007M – NOVEMBER 1992 – REVISED SEPTEMBER 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), and Shrink Small-Outline (DL) Packages, and Ceramic Flat (WD) Package

SN54CBT16212A . . . WD PACKAGE
SN74CBT16212A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'CBT16212A devices provide 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Each device operates as a 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

The SN54CBT16212A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74CBT16212A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1 port	Z	A1 port = B1 port
L	H	L	B2 port	Z	A1 port = B2 port
L	H	H	Z	B1 port	A2 port = B1 port
H	L	L	Z	B2 port	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1 port	B2 port	A1 port = B1 port A2 port = B2 port
H	H	H	B2 port	B1 port	A1 port = B2 port A2 port = B1 port



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

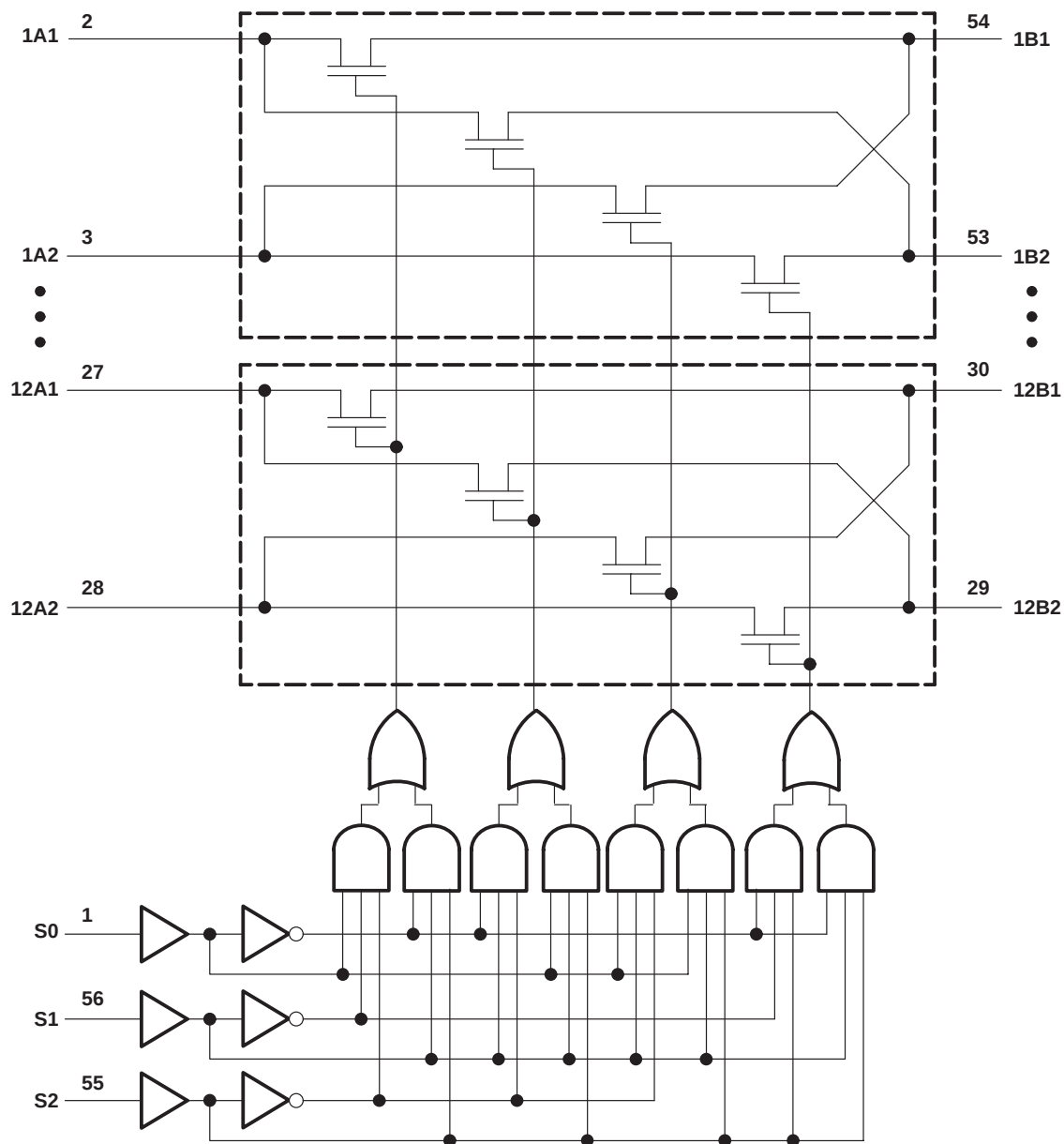
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SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

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logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, and DL packages.

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Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DGG package	81°C/W
DGV package	86°C/W
DL package	74°C/W
Storage temperature range, T_{Stg}	−65°C to 150°C

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51.

		SN54CBT16212A		SN74CBT16212A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4	5.5	4	5.5	V
V _{IH}	High-level control input voltage	2		2		V
V _{IL}	Low-level control input voltage		0.8		0.8	V
T _A	Operating free-air temperature	−55	125	−40	85	°C

PARAMETER		TEST CONDITIONS		SN54CBT16212A		SN74CBT16212A		UNIT	
				MIN	TYP [‡]	MAX	MIN		TYP [‡]
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2		−1.2		V	
I _I		V _{CC} = 0, V _I = 5.5 V		10		10		μA	
		V _{CC} = 5.5 V, V _I = 5.5 V or GND		±1		±1			
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		3.2		3		μA	
ΔI _{CC} [§]	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		2.5		2.5		mA	
C _i	Control inputs	V _I = 3 V or 0		2.5		2.5		pF	
C _{io} (OFF)		V _O = 3 V or 0, S0, S1, or S2 = V _{CC}		7.5		7.5		pF	
r _{on} [¶]		V _{CC} = 4 V, TYP at V _{CC} = 4 V		V _I = 2.4 V, I _I = 15 mA		14 20		Ω	
		V _{CC} = 4.5 V		V _I = 0		I _I = 64 mA			4 10
						I _I = 30 mA			4 10
				V _I = 2.4 V, I _I = 15 mA		6 14			6 12

† Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

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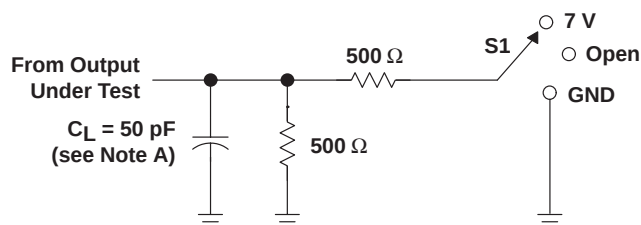
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16212A				SN74CBT16212A				UNIT
			V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} [†]	A or B	B or A			0.8*		0.35		0.25		ns
t _{pd}	S	A or B	14		1.5	13	10		1.5	9.1	ns
t _{en}	S	A or B	15		1.5	13.7	10.4		1.5	9.7	ns
t _{dis}	S	A or B	14.2		1.5	13.5	9.2		1.5	8.8	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

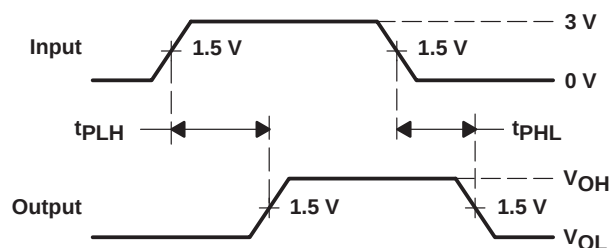
† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

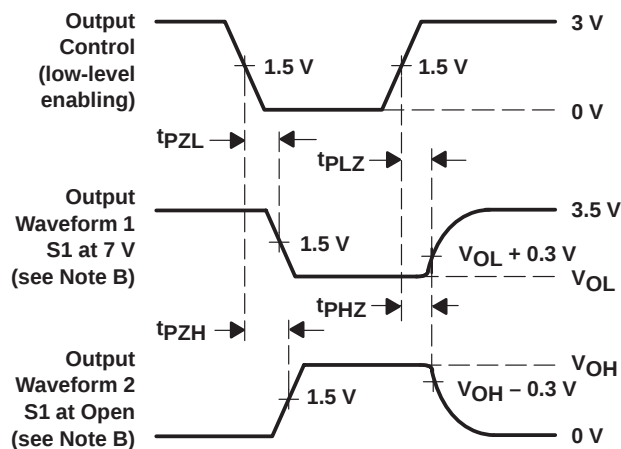


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50$ Ω , $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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