

MC74HC390A

Dual 4-Stage Binary Ripple Counter with $\div 2$ and $\div 5$ Sections

High-Performance Silicon-Gate CMOS

The MC74HC390A is identical in pinout to the LS390. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five section. The divide-by-two and divide-by-five counters have separate clock inputs, and can be cascaded to implement various combinations of $\div 2$ and/or $\div 5$ up to a $\div 100$ counter.

Flip-flops internal to the counters are triggered by high-to-low transitions of the clock input. A separate, asynchronous reset is provided for each 4-bit counter. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or strobes except when gated with the Clock of the HC390A.

Features

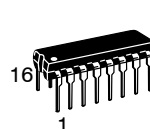
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
- Chip Complexity: 244 FETs or 61 Equivalent Gates
- Pb-Free Packages are Available*



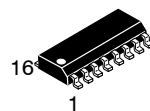
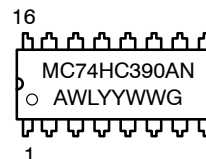
ON Semiconductor®

<http://onsemi.com>

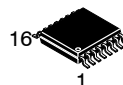
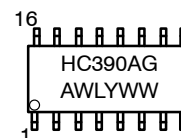
MARKING DIAGRAMS



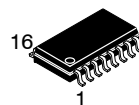
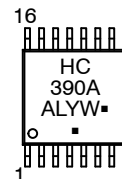
PDIP-16
N SUFFIX
CASE 648



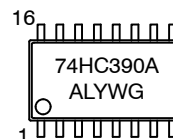
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
F SUFFIX
CASE 966



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G = Pb-Free Package
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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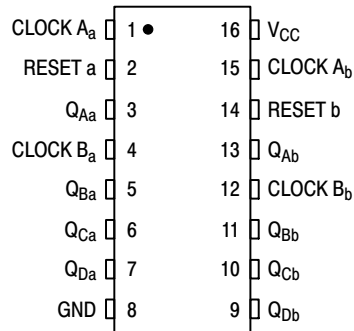


Figure 1. Pin Assignment

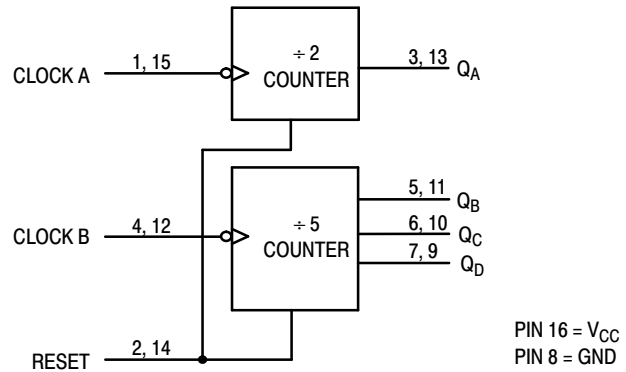


Figure 2. Logic Diagram

FUNCTION TABLE

Clock		Reset	Action
A	B		
X	X	H	Reset ÷ 2 and ÷ 5
↘	X	L	Increment ÷ 2
X	↘	L	Increment ÷ 5

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC390AN	PDIP-16	500 Units / Rail
MC74HC390ANG	PDIP-16 (Pb-Free)	500 Units / Rail
MC74HC390AD	SOIC-16	48 Units / Rail
MC74HC390ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC390ADR2	SOIC-16	2500 Units / Reel
MC74HC390ADR2G	SOIC-16 (Pb-Free)	2500 Units / Reel
MC74HC390ADTR2	TSSOP-16*	2500 Units / Reel
MC74HC390ADTR2G	TSSOP-16*	2500 Units / Reel
MC74HC390AF	SOEIAJ-16	50 Units / Rail
MC74HC390AFG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC74HC390AFEL	SOEIAJ-16	2000 Units / Reel
MC74HC390AFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ 0 $V_{CC} = 3.0 \text{ V}$ 0 $V_{CC} = 4.5 \text{ V}$ 0 $V_{CC} = 6.0 \text{ V}$ 0	1000 600 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 2.4 \text{ mA}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 2.4 \text{ mA}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	10	9	8	MHz
		3.0	15	14	12	
		4.5	30	28	25	
		6.0	50	45	40	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock A to QA (Figures 1 and 3)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	24	30	36	
		6.0	20	26	31	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock A to QC (QA connected to Clock B) (Figures 1 and 3)	2.0	200	250	300	ns
		3.0	160	185	210	
		4.5	58	65	70	
		6.0	49	62	68	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QB (Figures 1 and 3)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	26	33	39	
		6.0	22	28	33	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QC (Figures 1 and 3)	2.0	90	105	180	ns
		3.0	56	70	100	
		4.5	37	46	56	
		6.0	31	39	48	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock B to QD (Figures 1 and 3)	2.0	70	80	90	ns
		3.0	40	45	50	
		4.5	26	33	39	
		6.0	22	28	33	
t _{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0	80	95	110	ns
		3.0	48	65	75	
		4.5	30	38	44	
		6.0	26	33	39	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	15	19	
C _{in}	Maximum Input Capacitance	–	10	10	10	pF

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Counter)*	Typical @ 25°C, V _{CC} = 5.0 V	pF
		35	

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock A or Clock B (Figure 4)	2.0	25	30	40	ns
		3.0	15	20	30	
		4.5	10	13	15	
		6.0	9	11	13	
t_w	Minimum Pulse Width, Clock A, Clock B (Figure 3)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	15	19	22	
		6.0	13	15	19	
t_w	Minimum Pulse Width, Reset (Figure 4)	2.0	75	95	110	ns
		3.0	27	32	36	
		4.5	20	24	30	
		6.0	18	22	28	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 3)	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS

INPUTS

Clock A (Pins 1, 15) and Clock B (Pins 4, 15)

Clock A is the clock input to the ÷ 2 counter; Clock B is the clock input to the ÷ 5 counter. The internal flip-flops are toggled by high-to-low transitions of the clock input.

CONTROL INPUTS

Reset (Pins 2, 14)

Asynchronous reset. A high at the Reset input prevents counting, resets the internal flip-flops, and forces Q_A through Q_D low.

OUTPUTS

Q_A (Pins 3, 13)

Output of the ÷ 2 counter.

Q_B, Q_C, Q_D (Pins 5, 6, 7, 9, 10, 11)

Outputs of the ÷ 5 counter. Q_D is the most significant bit. Q_A is the least significant bit when the counter is connected for BCD output as in Figure 6. Q_B is the least significant bit when the counter is operating in the bi-quinary mode as in Figure 7.

SWITCHING WAVEFORMS

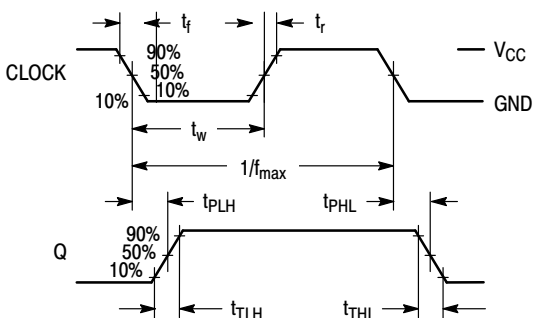


Figure 3.

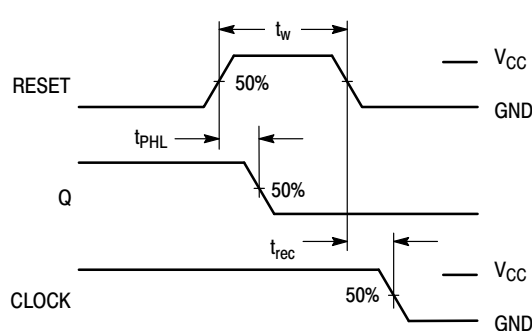
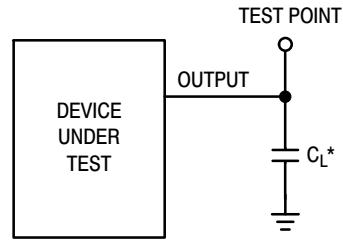


Figure 4.

MC74HC390A

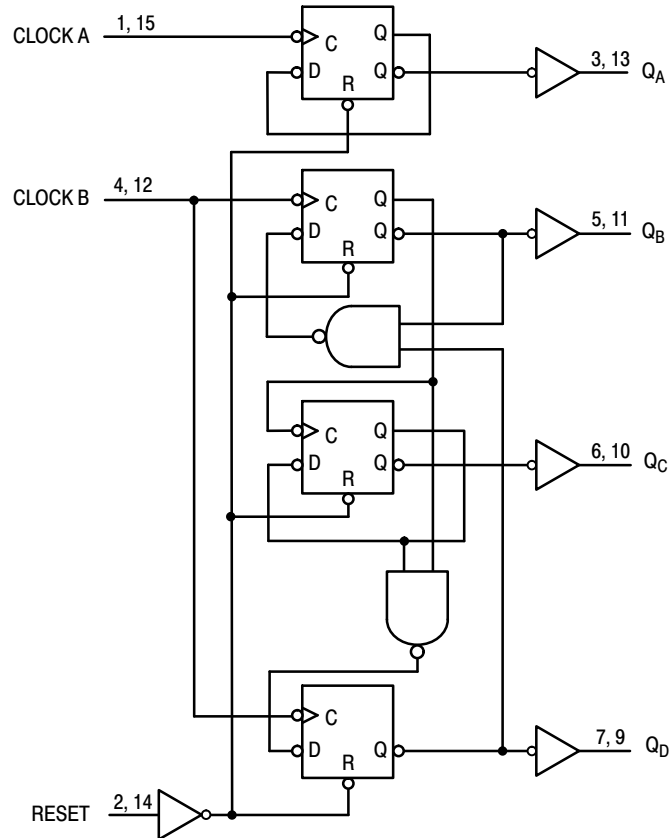
TEST CIRCUIT



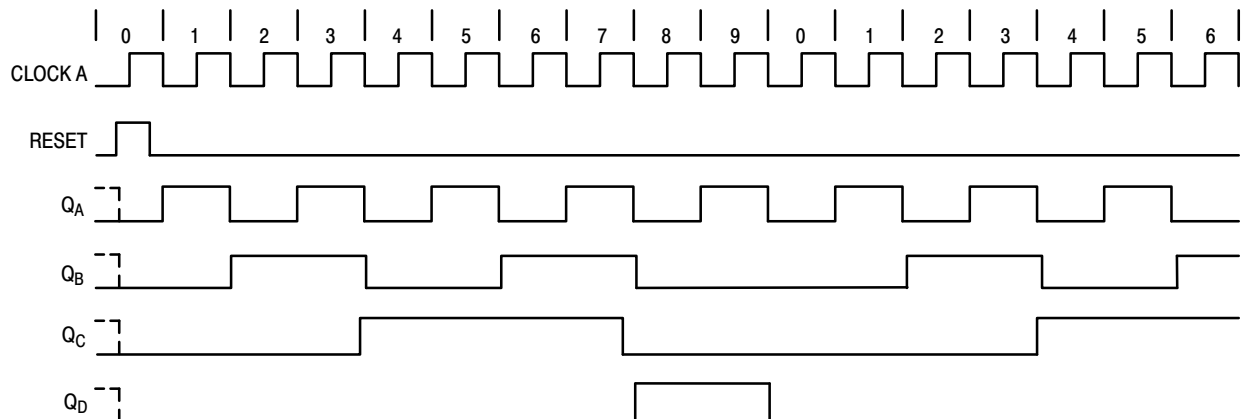
*Includes all probe and jig capacitance

Figure 5.

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM (Q_A Connected to Clock B)



MC74HC390A

APPLICATIONS INFORMATION

Each half of the MC54/74HC390A has independent $\div 2$ and $\div 5$ sections (except for the Reset function). The $\div 2$ and $\div 5$ counters can be connected to give BCD or bi-quinary (2–5) count sequences. If Output Q_A is connected to the Clock B input (Figure 4), a decade divider with BCD output is obtained. The function table for the BCD count sequence is given in Table 1.

Table 1. BCD Count Sequence*

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

* Q_A connected to Clock B input.

To obtain a bi-quinary count sequence, the input signals connected to the Clock B input, and output Q_D is connected to the Clock A input (Figure 7). Q_A provides a 50% duty cycle output. The bi-quinary count sequence function table is given in Table 2.

Table 2. Bi-Quinary Count Sequence**

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L

** Q_D connected to Clock A input.

CONNECTION DIAGRAMS

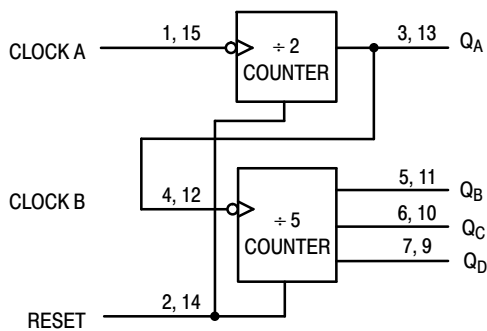


Figure 6. BCD Count

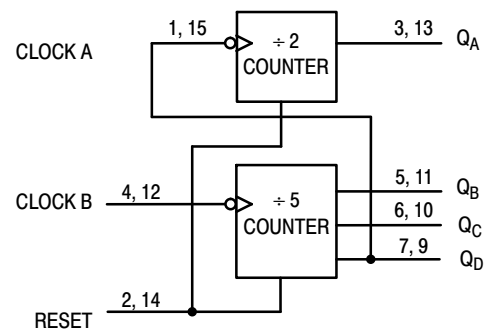
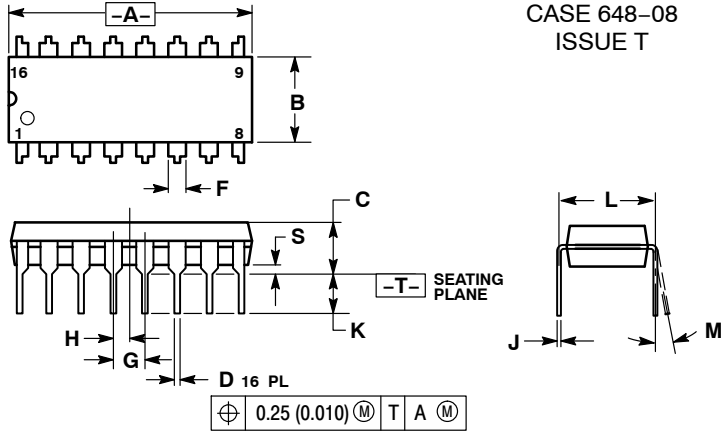


Figure 7. Bi-Quinary Count

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PACKAGE DIMENSIONS

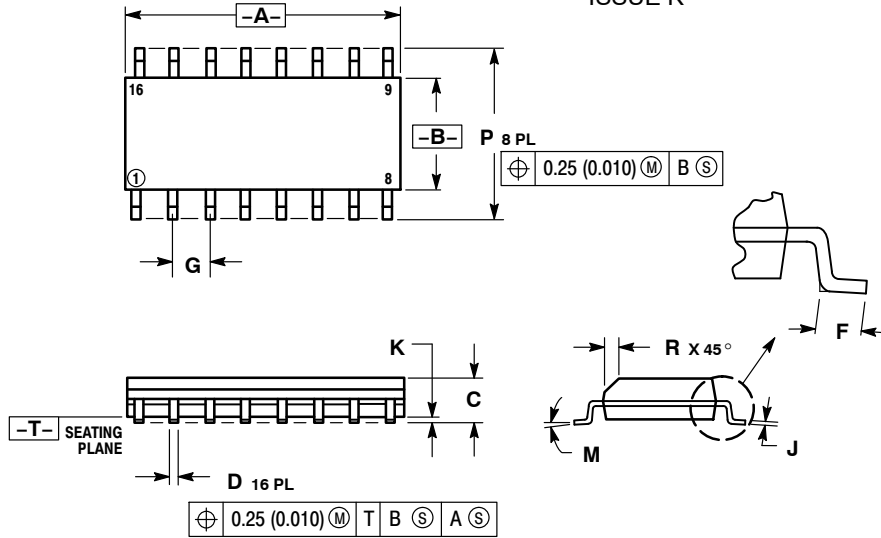
PDIP-16 N SUFFIX CASE 648-08 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

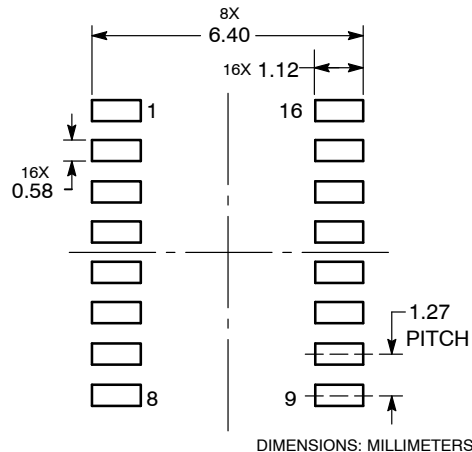
SOIC-16 D SUFFIX CASE 751B-05 ISSUE K



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

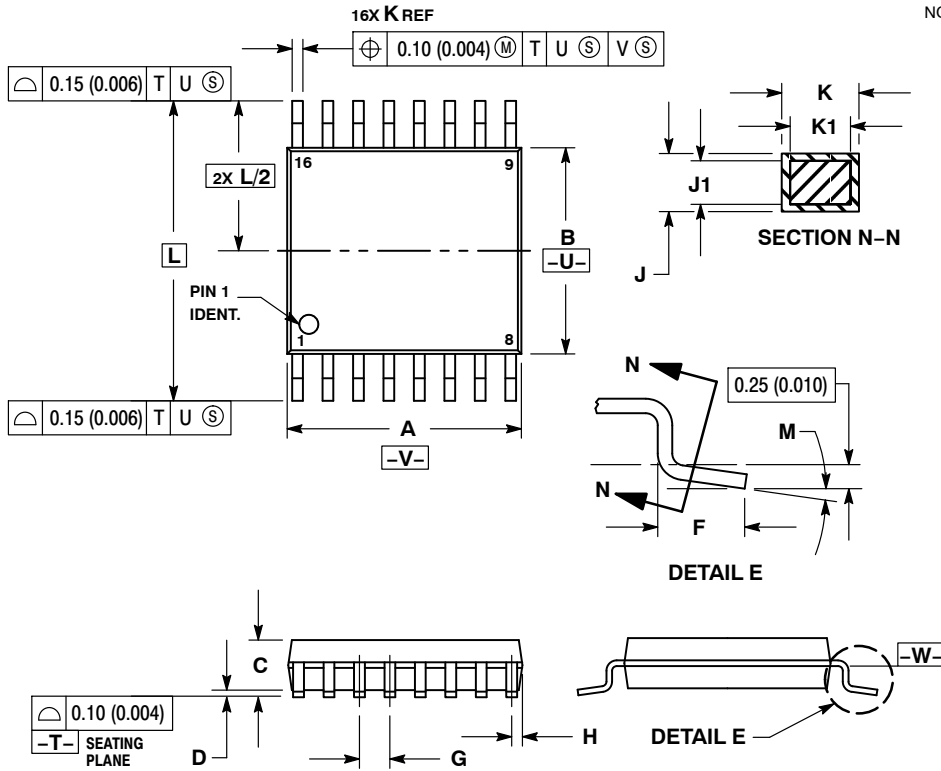
SOLDERING FOOTPRINT



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PACKAGE DIMENSIONS

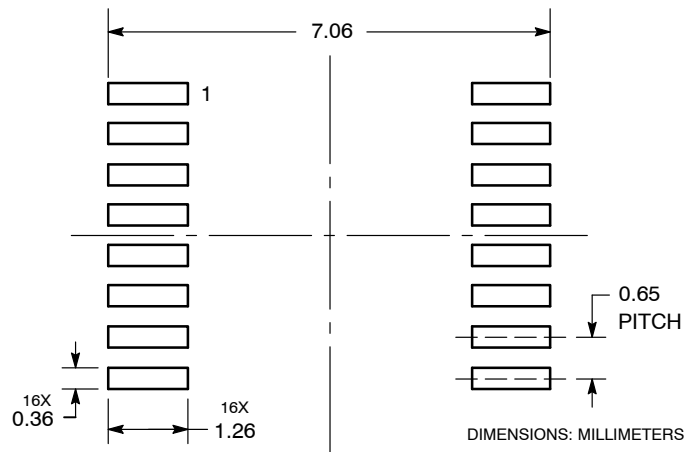
TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

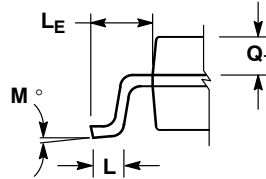
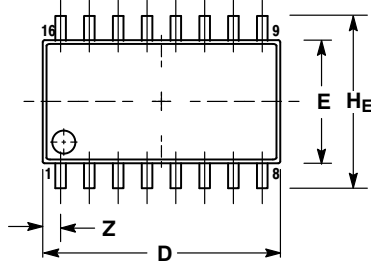
SOLDERING FOOTPRINT



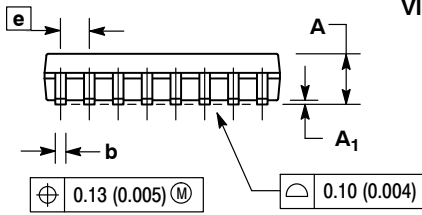
MC74HC390A

PACKAGE DIMENSIONS

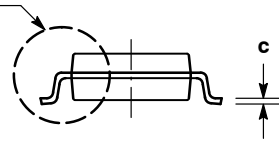
SOEIAJ-16
F SUFFIX
CASE 966-01
ISSUE A



DETAIL P



VIEW P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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