PTN3331

High speed differential line driver

Rev. 01 — 06 August 2002 **Product data**

1. Description

The PTN3331 is a differential line driver that implements the electrical characteristics of Low-Voltage Differential Signaling (LVDS) that meets or exceeds the requirements of the ANSI *TIA/EIA-644 Standard*. LVDS is used to achieve higher data rates on commonly used media. LVDS overcomes the limitations of achievable slew rates and EMI restrictions of previous differential signaling techniques. The PTN3331 operates at 3.3 volt supply levels and current mode output drivers. The output drivers will deliver a minimum of 247 mV into a 100 Ω load when enabled.

The intended application of this device is for point-to-point baseband transmission rates over a controlled impedance media of approximately 100 Ω. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media selected and the noise coupling to the environment.

The PTN3331 is designed to function over the full industrial temperature range of –40 °C to +85 °C.

2. Features

- Meets or exceeds the requirements of ANSI *TIA/EIA-644 Standard*
- Low-Voltage Differential Signaling with output voltage of 350 mV across a 100 Ω load
- 300 ps maximum channel to channel output skew
- 500 ps typical output voltage rise and fall times
- Power dissipation of 100 mW typical at 200 MHz
- Driver at high impedance when disabled or with V_{CC} = 0 V
- 5 volt tolerant inputs with Low Voltage TTL (LVTTL) logic input levels
- Pin-compatible with AM26LS31 and SN65LVDS31.

3. Applications

- Low voltage, low EMI, high speed differential signaling
- Point-to-point high speed data transmission
- High performance switches and routers.

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4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PTN3331DH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PTN3331D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

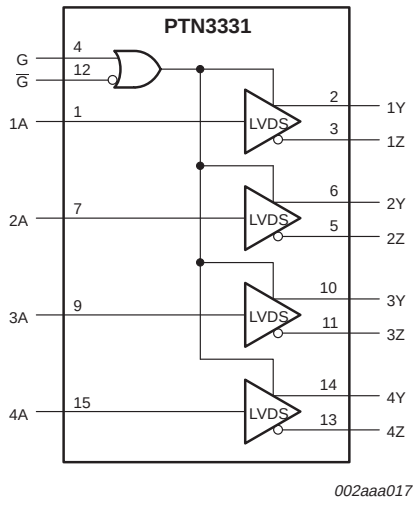


Fig 1. Functional diagram.

6. Pinning information

6.1 Pinning

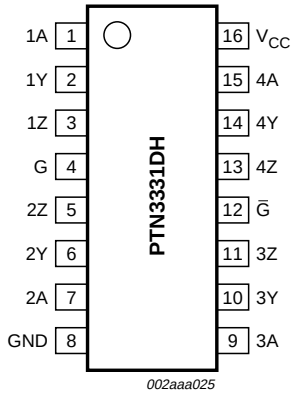


Fig 2. TSSOP16 pin configuration.

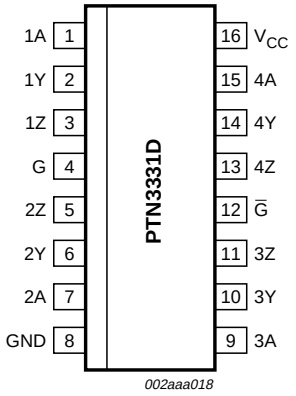


Fig 3. SO16 pin configuration.

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
1A	1	LVTTL input
1Y	2	LVDS non-inverting output
1Z	3	LVDS inverting output
G	4	Enable (active-HIGH)
2Z	5	LVDS inverting output
2Y	6	LVDS non-inverting output
2A	7	LVTTL input
GND	8	Ground
3A	9	LVTTL input
3Y	10	LVDS non-inverting output
3Z	11	LVDS inverting output
$\overline{G}$	12	Enable (active-LOW)
4Z	13	LVDS inverting output
4Y	14	LVDS non-inverting output
4A	15	LVTTL input
V_{CC}	16	Supply

7. Functional description

7.1 Function table

Table 3: Function table

H = HIGH level; L = LOW level; X = irrelevant; Z = high impedance.

Input	Enables		Outputs	
A	**G**	**$\overline{G}$**	**Y**	**Z**
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{CC}	supply voltage	–0.5	4.0	V
V_I	input voltage	–0.5	V_{CC} + 0.5	V
	short circuit duration	Continuous		sec
T_{amb}	operating ambient temperature range	–40	+85	°C
T_j	operating junction temperature	–40	+150	°C
T_{stg}	storage temperature range	–65	+150	°C
	ESD	>2	-	kV

[1] Values beyond absolute maximum ratings can cause the device to be prematurely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

9. Recommended operating conditions

Table 5: Recommended operating conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{CC}	supply voltage	3	3.3	3.6	V
V_{IH}	HIGH-level input voltage	2	-	-	V
V_{IL}	LOW-level input voltage	-	-	0.8	V

10. Static characteristics

Table 6: DC electrical characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{OD}	differential output voltage	R_L = 100 Ω See Figure 4.	247	340	454	mV
ΔV_{OD}	change in differential voltage magnitude between logic states		–50	-	+50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50	-	+50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		-	50	150	mV
I_{CC}	Supply current	V_I = 0.8 or 2 V; enabled, no load	-	22	30	mA
		V_I = 0.8 or 2 V; enabled, R_L = 100 Ω	-	25	35	mA
		V_I = 0 V or V_{CC}; disabled	-	0.25	1	mA
I_{IH}	HIGH-level input current	V_{IH} = 2 V	-	4	20	µA
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	-	0.1	10	µA
I_{OS}	Output short circuit current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0 V	-	–4	–24	mA
I_{OZ}	High-impedance output current	V_{OD} = 0 V or 2.4 V	-	±1	-	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 0 V; V_O = 2.4 V	1	-	–1	µA
C_i	Input capacitance		-	3	-	pF

[1] All typical values are at T_{amb} = 25 °C and V_{CC} = 3.3 V.

11. Dynamic characteristics

Table 7: AC electrical characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{PLH}	Propagation delay, LOW-to-HIGH level output	R_L = 100 Ω; C_L = 10 pF See Figure 5.		0.5	1.4	2	ns
t_{PHL}	Propagation delay, HIGH-to-LOW level output			1	1.7	2.5	ns
t_r	Differential output rise time (20 to 80%)		[4]	0.4	0.5	0.6	ns
t_f	Differential output fall time (80 to 20%)		[4]	0.4	0.5	0.6	ns
$t_{sk(p)}$	Pulse skew ($t_{PHL} - t_{PLH}$)			-	0.3	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew		[2], [4]	-	0	0.3	ns
$t_{sk(p-p)}$	Part-to-part skew		[3], [4]	-	-	800	ps
t_{PZH}	Propagation delay, high-impedance to HIGH-level output	See Figure 6.		-	5.4	15	ns
t_{PZL}	Propagation delay, high-impedance to LOW-level output			-	2.5	15	ns
t_{PHZ}	Propagation delay, HIGH-level to high-impedance output			-	8.1	15	ns
t_{PLZ}	Propagation delay, LOW-level to high-impedance output			-	7.3	15	ns

[1] All typical values are at T_{amb} = 25 °C, and V_{CC} = 3.3 V.

[2] $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

[3] $t_{sk(p-p)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

[4] Guaranteed by design and characterization.

12. Test figures

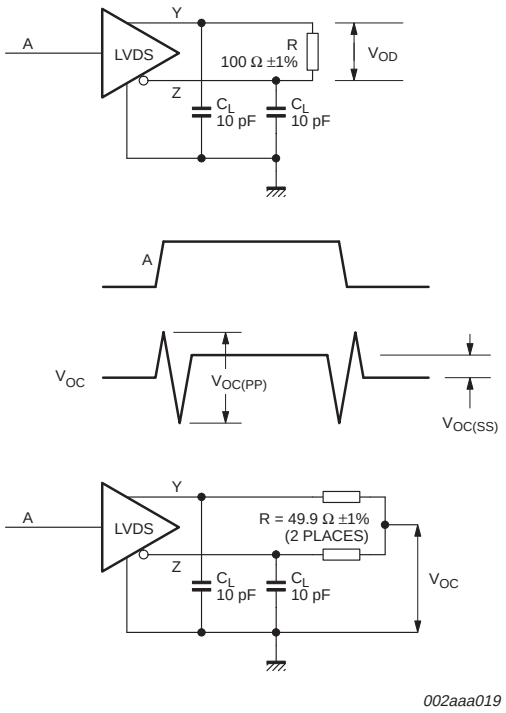


Fig 4. Test circuit and voltage definitions.

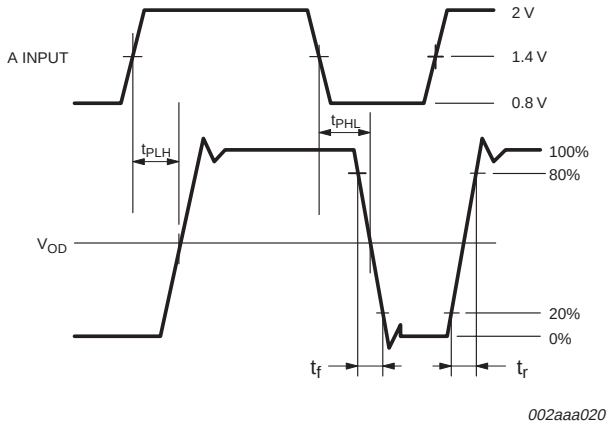


Fig 5. Propagation delay definitions.

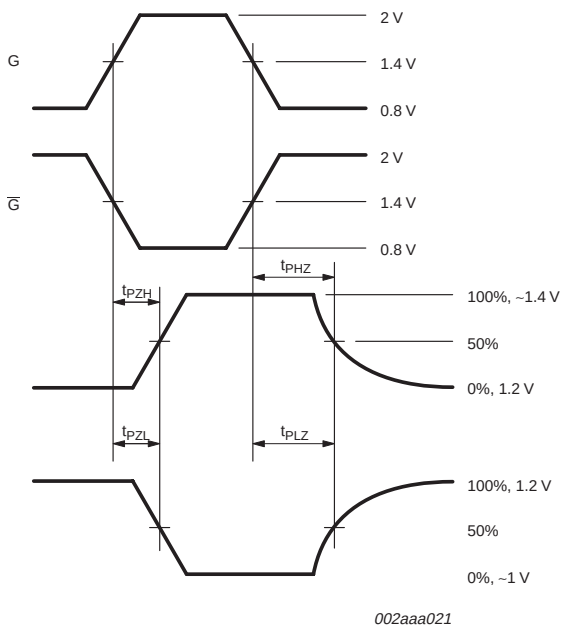
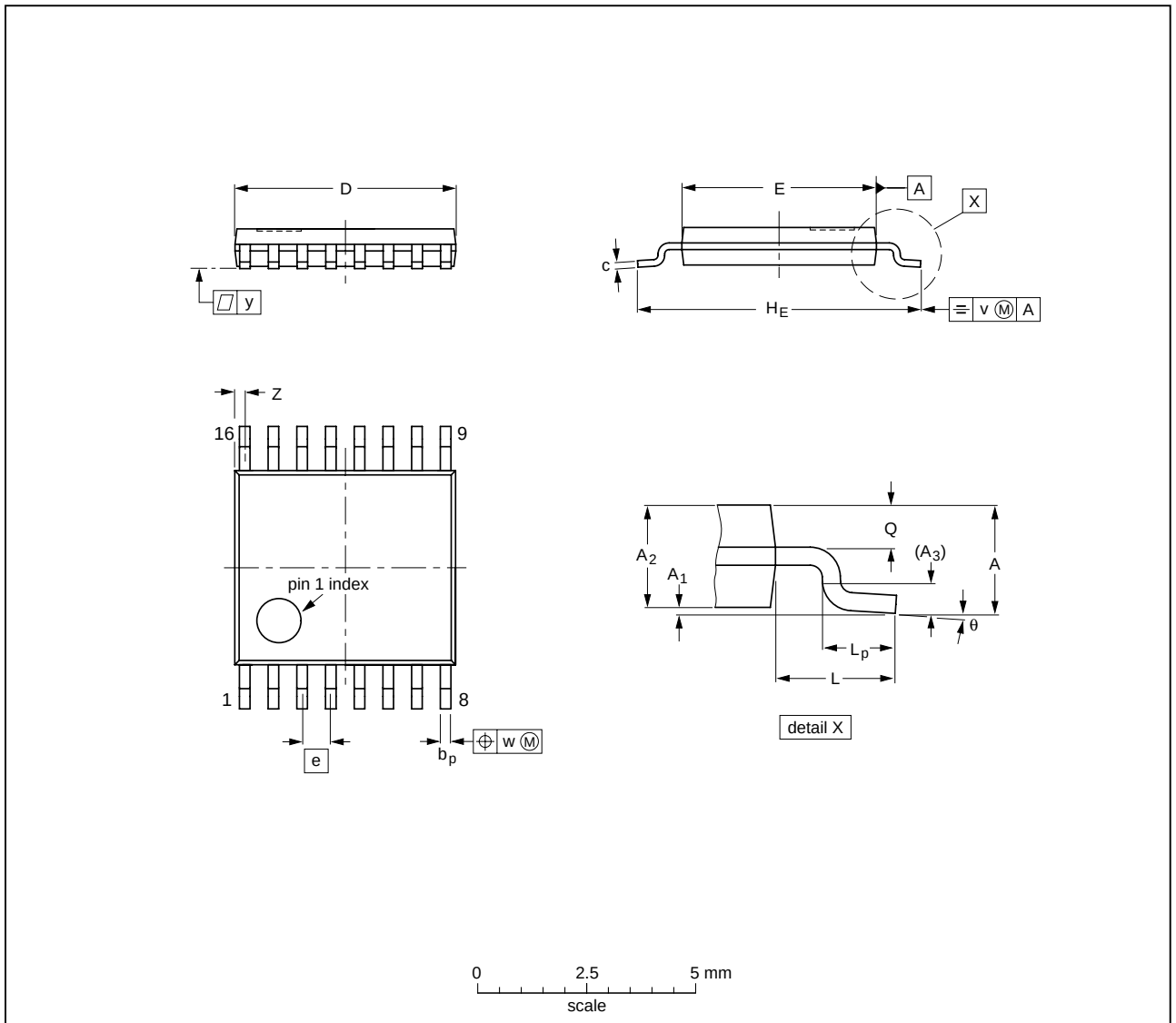


Fig 6. Enable and disable time definitions.

13. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

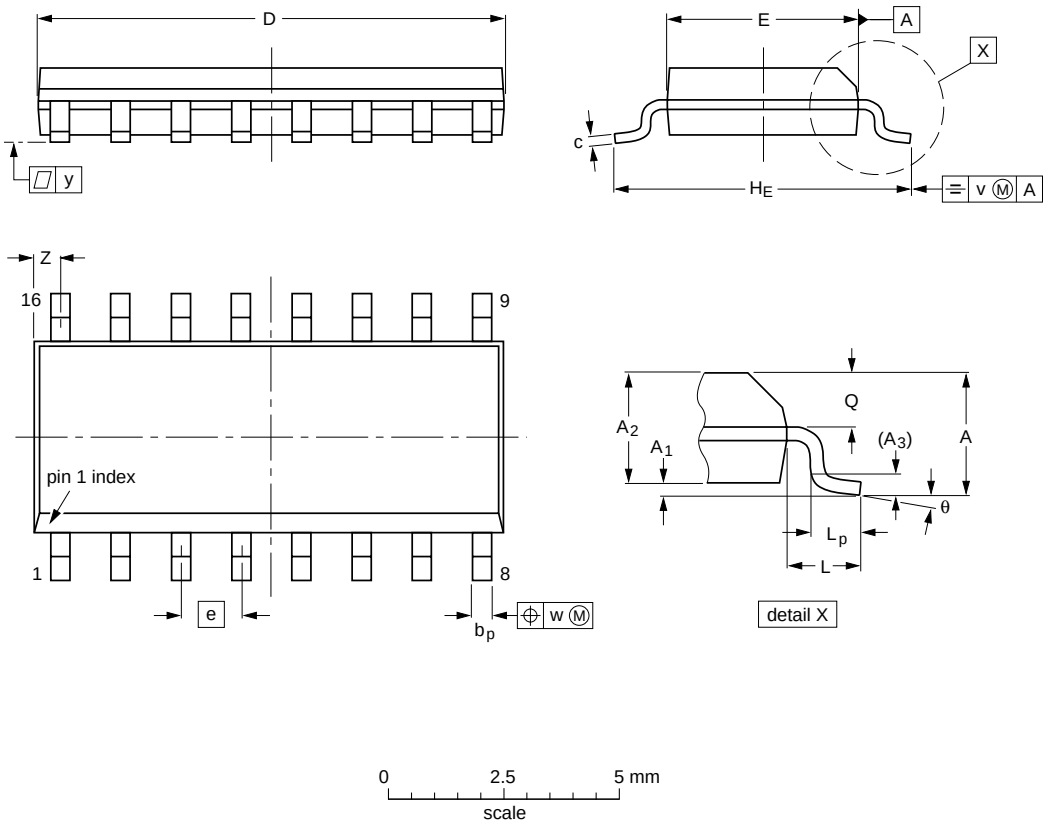
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

Fig 7. TSSOP16 package outline (SOT403-1).

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

Fig 8. SO16 package outline (SOT109-1).

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Package related soldering information

Table 8: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15. Revision history

Table 9: Revision history

Rev	Date	CPCN	Description
01	**20020806**	**-**	**Product data. Initial version. Engineering Change Notice 853-2362 28701 dated 2002 August 06.**

16. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**. **Fax: +31 40 27 24825**

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Contents

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