

VFC32

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- OPERATION UP TO 500kHz
- EXCELLENT LINEARITY
 $\pm 0.01\%$ max at 10kHz FS
 $\pm 0.05\%$ max at 100kHz FS
- V/F OR F/V CONVERSION
- MONOTONIC
- VOLTAGE OR CURRENT INPUT

APPLICATIONS

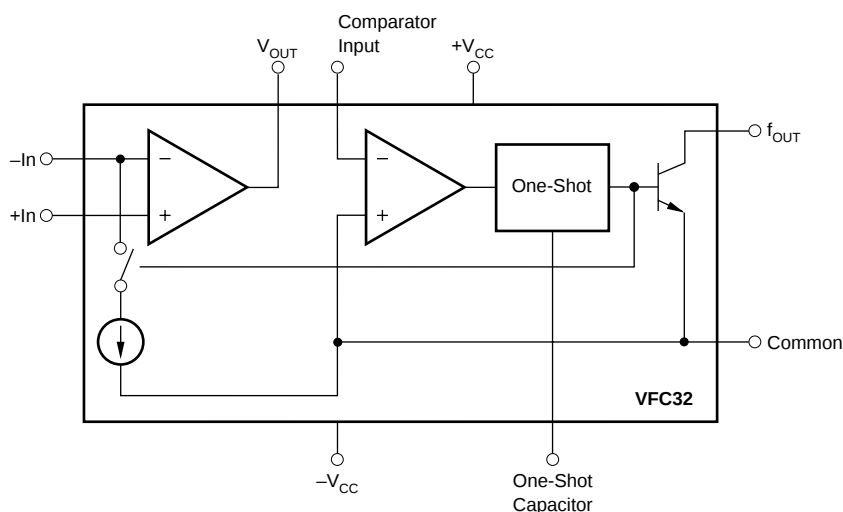
- INTEGRATING A/D CONVERTER
- SERIAL FREQUENCY OUTPUT
- ISOLATED DATA TRANSMISSION
- FM ANALOG SIGNAL MOD/DEMODO
- MOTOR SPEED CONTROL
- TACHOMETER

DESCRIPTION

The VFC32 voltage-to-frequency converter provides an output frequency accurately proportional to its input voltage. The digital open-collector frequency output is compatible with all common logic families. Its integrating input characteristics give the VFC32 excellent noise immunity and low nonlinearity.

Full-scale output frequency is determined by an external capacitor and resistor and can be scaled over a wide range. The VFC32 can also be configured as a frequency-to-voltage converter.

The VFC32 is available in 14-pin plastic DIP, SO-14 surface-mount, and metal TO-100 packages. Commercial, industrial, and military temperature range models are available.



SPECIFICATIONS

At $T_A = +25^\circ\text{C}$ and $V_{CC} = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS	VFC32KP, KU			VFC32BM			VFC32SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT (V/F CONVERTER) $F_{OUT} = V_{IN}/7.5 R_1 C_1$											
Voltage Range ⁽¹⁾ Positive Input		>0		+0.25mA x R_1	*		*	*		*	V
Negative Input		>0		-10	*		*	*		*	V
Current Range ⁽¹⁾ Bias Current		>0		+0.25	*		*	*		*	mA
Inverting Input			20	100		*	*		*	*	nA
Noninverting Input			100	250		*	*		*	*	nA
Offset Voltage ⁽²⁾			1	4		*	*		*	*	mV
Differential Impedance		300 10	650 10		*	*		*	*		k Ω pF
Common-mode Impedance		300 3	500 3		*	*		*	*		M Ω pF
INPUT (F/V CONVERTER) $V_{OUT} = 7.5 R_1 C_1 F_{IN}$											
Impedance		50 10	150 10		*	*		*	*		k Ω pF
Logic "1"			+1.0		*		*	*		*	V
Logic "0"			-0.05		*		*	*		*	V
Pulse-width Range		0.1		150k/ F_{MAX}	*		*	*		*	μ s
ACCURACY											
Linearity Error ⁽³⁾	0.01Hz $\leq$ Oper Freq $\leq$ 10kHz		± 0.005	$\pm 0.010^{(4)}$		*	*		*	*	% of FSR ⁽⁵⁾
	0.1Hz $\leq$ Oper Freq $\leq$ 100kHz		± 0.025	± 0.05		*	*		*	*	% of FSR
	0.5Hz $\leq$ Oper Freq $\leq$ 500kHz		± 0.05			*			*		% of FSR
Offset Error Input Offset Voltage ⁽²⁾			1	4		*	*		*	*	mV
Offset Drift ⁽⁶⁾			± 3			*			*		ppm of FSR/ $^{\circ}$ C
Gain Error ⁽²⁾			5			*			*		% of FSR
Gain Drift ⁽⁶⁾	f = 10kHz		± 75			± 50	± 100		± 70	± 150	ppm/ $^{\circ}$ C
Full Scale Drift (offset drift and gain drift) ^(6, 7)	f = 10kHz		± 75			± 50	± 100		± 70	± 150	ppm of FSR/ $^{\circ}$ C
Power Supply Sensitivity	f = DC, $\pm V_{CC}$ = 12VDC to 18VDC			± 0.015			*			*	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	$I_{SINK} = 8$ mA	0	0.2	0.4	*	*	*	*	*	*	V
Leakage Current, Logic "1"	$V_o = 15$ V		0.01	1.0		*	*		*	*	μ A
Voltage, Logic "1"	External Pull-up Resistor Required (see Figure 4)			V_{PU}		*	*			*	V
Pulse Width	For Best Linearity		0.25/ F_{MAX}			*			*		s
Fall Time	$I_{OUT} = 5$ mA, $C_{LOAD} = 500$ pF			400		*	*		*	*	ns
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	$I_o \leq 7$ mA	0 to +10			*			*			V
Current	$V_o \leq 7$ VDC	+10			*			*			mA
Impedance	Closed Loop			1			*			*	Ω
Capacitive Load	Without Oscillation			100			*			*	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500 ⁽⁸⁾	*			*			kHz
Dynamic Range		6			*			*			decades
Settling Time	(V/F) to Specified Linearity for a Full Scale Input Step < 50% Overload		⁽⁹⁾			*			*		
Overload Recovery			⁽⁹⁾			*			*		
POWER SUPPLY											
Rated Voltage			± 15								V
Voltage Range		± 11		± 20					*		V
Quiescent Current			± 5.5	± 6.0		*	*		*		mA
TEMPERATURE RANGE											
Specification		0		+70	-25		+85	-55		+125	$^{\circ}$ C
Operating		-25		+85	-55		+125	-55		+125	$^{\circ}$ C
Storage		-25		+85	-65		+150	-65		+150	$^{\circ}$ C

* Specification the same as VFC32KP.

NOTES: (1) A 25% duty cycle (0.25mA input current) is recommended for best linearity. (2) Adjustable to zero. See Offset and Gain Adjustment section. (3) Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85 $^\circ\text{C}$. (4) $\pm 0.015\%$ of FSR for negative inputs shown in Figure 5. Positive inputs are shown in Figure 1. (5) FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage). (6) Exclusive of external components' drift. (7) Positive drift is defined to be increasing frequency with increasing temperature. (8) For operations above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections. (9) One pulse of new frequency plus 1 μs .

ABSOLUTE MAXIMUM RATINGS

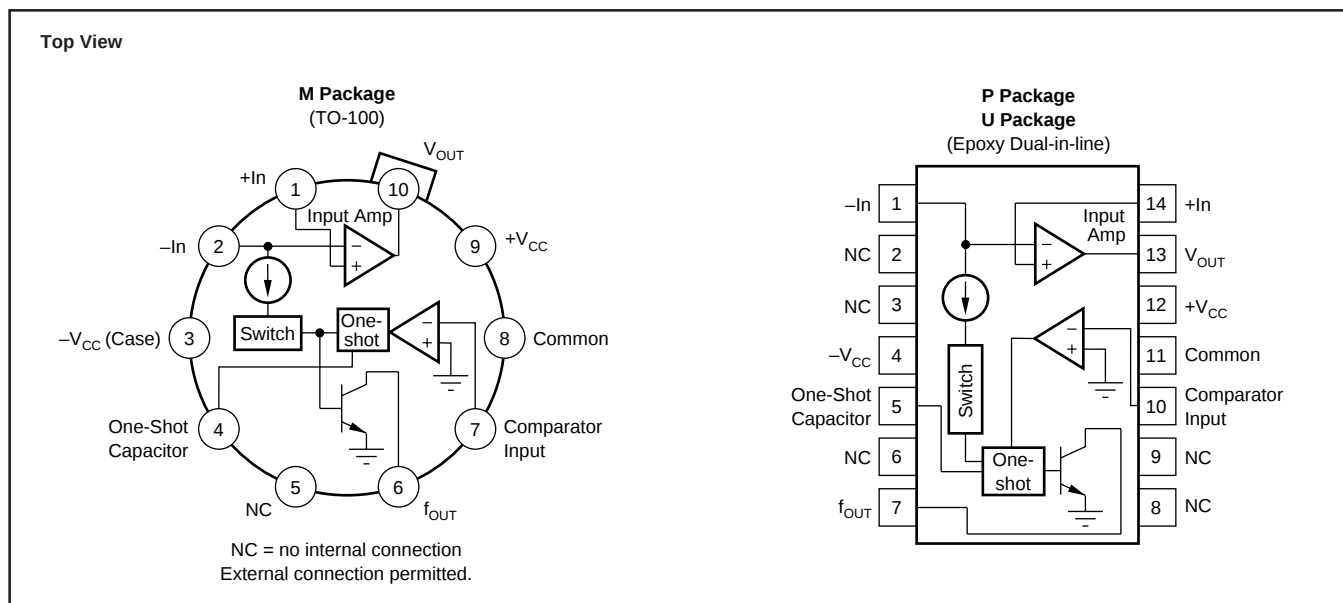
Supply Voltage	±22V
Output Sink Current (F_{OUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, -Input	±Supply
Input Voltage, +Input	±Supply
Comparator Input	±Supply
Storage Temperature Range:	
VFC32BM, SM	-65°C to +150°C
VFC32KP, KU	-25°C to +85°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
VFC32KP	14-Pin Plastic DIP	010	0°C to 70°C
VFC32BM	TO-100 Metal	007	-25°C to +85°C
VFC32SM	TO-100 Metal	007	-55°C to +125°C
VFC32KU	SO-14 SOIC	235	0°C to +70°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

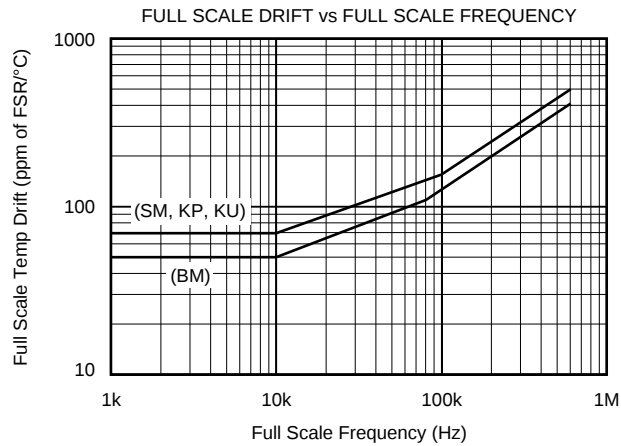
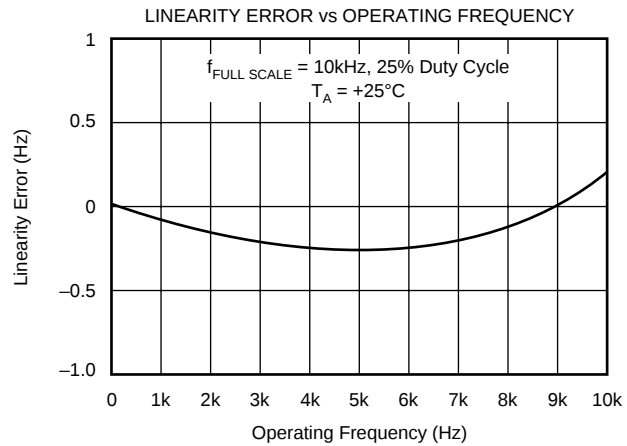
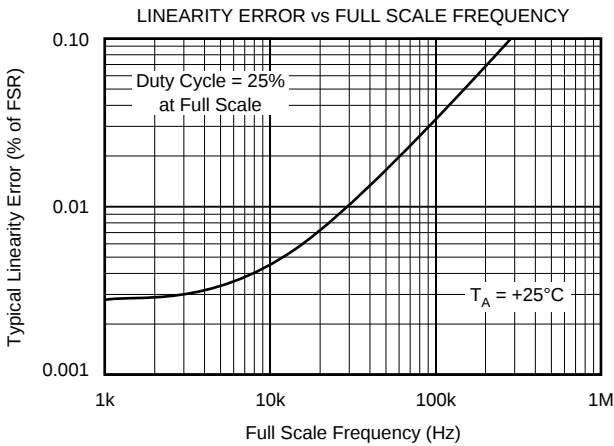
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

TYPICAL PERFORMANCE CURVES

At $T_A = +25^{\circ}\text{C}$ and $V_{CC} = \pm 15\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for frequency-to-voltage conversion. R_1 sets the input voltage range. For a 10V full-scale input, a 40k Ω input resistor is recommended. Other input voltage ranges can be achieved by changing the value of R_1 .

$$R_1 = \frac{V_{FS}}{0.25\text{mA}} \quad (1)$$

R_1 should be a metal film type for good stability. Manufacturing tolerances can produce approximately $\pm 10\%$ variation in output frequency. Full-scale output frequency can be trimmed by adjusting the value of R_1 —see Figure 3.

The full-scale output frequency is determined by C_1 . Values shown in Figure 1 are for a full-scale output frequency of 10kHz. Values for other full-scale frequencies can be read from Figure 2. Any variation in C_1 —tolerance, temperature drift, aging—directly affect the output frequency. Ceramic NPO or silver-mica types are a good choice.

For full-scale frequencies above 200kHz, use larger capacitor values as indicated in Figure 2, with $R_1 = 20\text{k}\Omega$.

The value of the integrating capacitor, C_2 , does not directly influence the output frequency, but its value must be chosen within certain bounds. Values chosen from Figure 2 produce

approximately 2.5Vp-p integrator voltage waveform. If C_2 's value is made too low, the integrator output voltage can exceed its linear output swing, resulting in a nonlinear response. Using C_2 values larger than shown in Figure 2 is acceptable.

Accuracy or temperature stability of C_2 is not critical because its value does not directly affect the output frequency. For best linearity, however, C_2 should have low leakage and low dielectric absorption. Polycarbonate and other film capacitors are generally excellent. Many ceramic types are adequate, but some low-voltage ceramic capacitor types may degrade nonlinearity. Electrolytic types are not recommended.

FREQUENCY OUTPUT PIN

The frequency output terminal is an open-collector logic output. A pull-up resistor is usually connected to a 5V logic supply to create standard logic-level pulses. It can, however, be connected to any power supply up to $+V_{CC}$. Output pulses have a constant duration and positive-going during the one-shot period. Current flowing in the open-collector output transistor returns through the Common terminal. This terminal should be connected to logic ground.

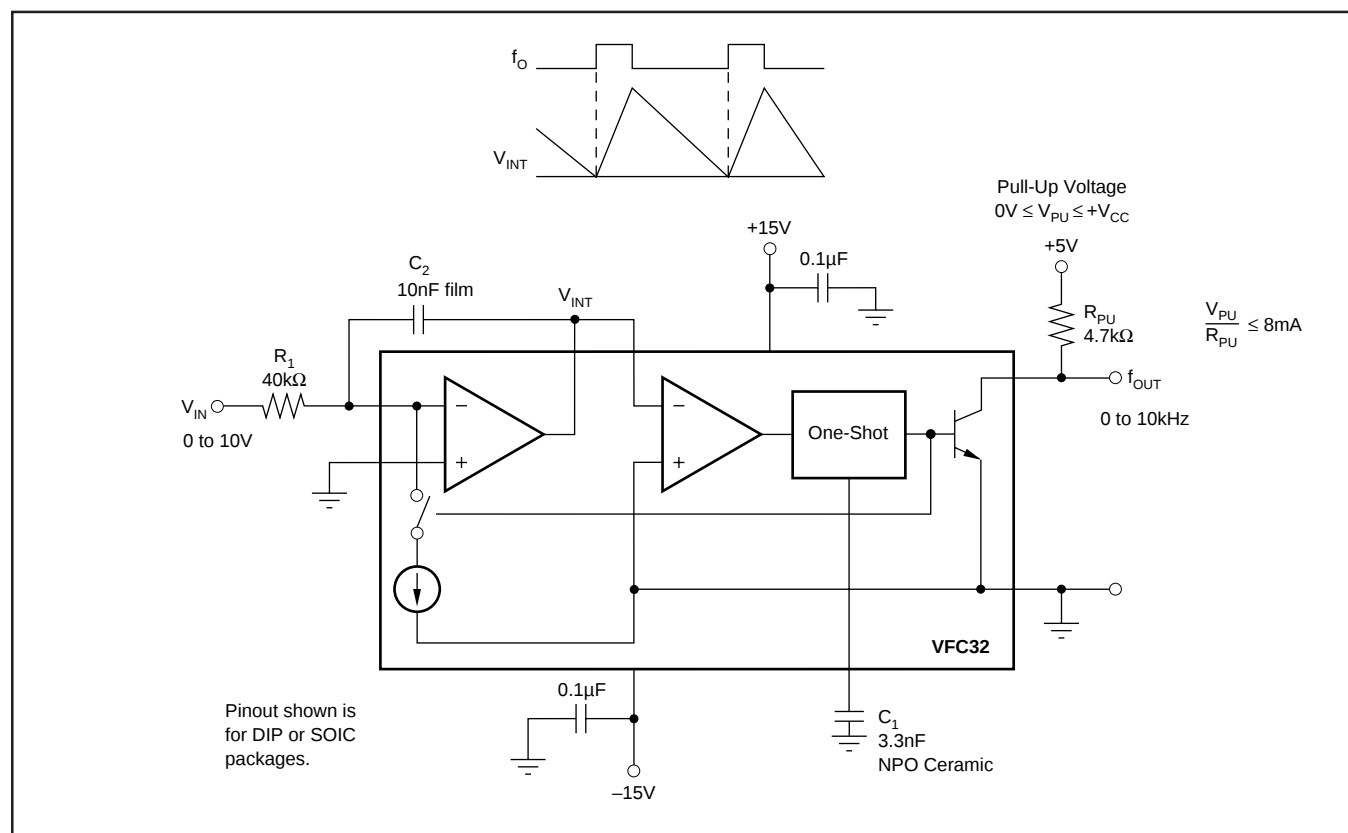


FIGURE 1. Voltage-to-Frequency Converter Circuit.

FREQUENCY-TO-VOLTAGE CONVERSION

Figure 4 shows the VFC32 connected as a frequency-to-voltage converter. The capacitive-coupled input network C_3 , R_6 and R_7 allow standard 5V logic levels to trigger the comparator input. The comparator triggers the one-shot on the falling edge of the frequency input pulses. Threshold voltage of the comparator is approximately $-0.7V$. For frequency input waveforms less than 5V logic levels, the R_6/R_7 voltage divider can be adjusted to a lower voltage to assure that the comparator is triggered.

The value of C_1 is chosen from Figure 2 according to the full-scale input frequency. C_2 smooths the output voltage waveform. Larger values of C_2 reduce the ripple in the output voltage. Smaller values of C_2 allow the output voltage to settle faster in response to a change in input frequency. Resistor R_1 can be trimmed to achieve the desired output voltage at the full-scale input frequency.

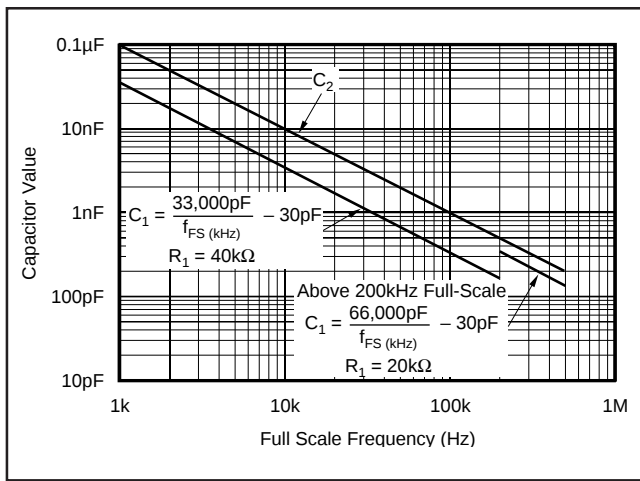


FIGURE 2. Capacitor Value Selection.

PRINCIPLES OF OPERATION

The VFC32 operates on a principle of charge balance. The signal input current is equal to V_{IN}/R_1 . This current is integrated by input op amp and C_2 , producing a downward ramping integrator output voltage. When the integrator output ramps to the threshold of the comparator, the one-shot is triggered. The 1mA reference current is switched to the integrator input during the one-shot period, causing the integrator output ramp upward. After the one-shot period, the integrator again ramps downward.

The oscillation process forces a long-term balance of charge (or average current) between the input signal current and the reference current. The equation for charge balance is:

$$I_{IN} = I_{R(AVERAGE)} \quad (2)$$

$$\frac{V_{IN}}{R_1} = f_O t_{OS} (1mA) \quad (3)$$

Where:

f_O is the output frequency

t_{OS} is the one-shot period, equal to

$$t_{OS} = 7500 C_1 (\text{Farads}) \quad (4)$$

The values suggested for R_1 and C_1 are chosen to produce a 25% duty cycle at full-scale frequency output. For full-scale frequencies above 200kHz, the recommended values produce a 50% duty cycle.

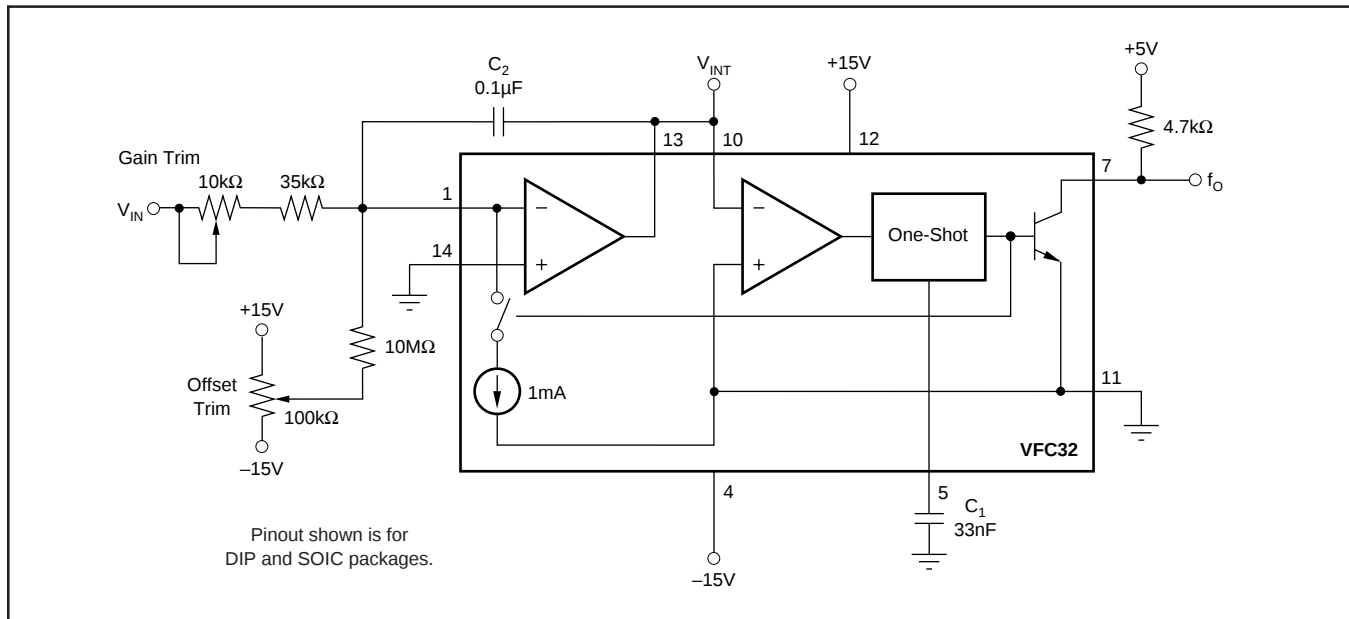


FIGURE 3. Gain and Offset Voltage Trim Circuit.

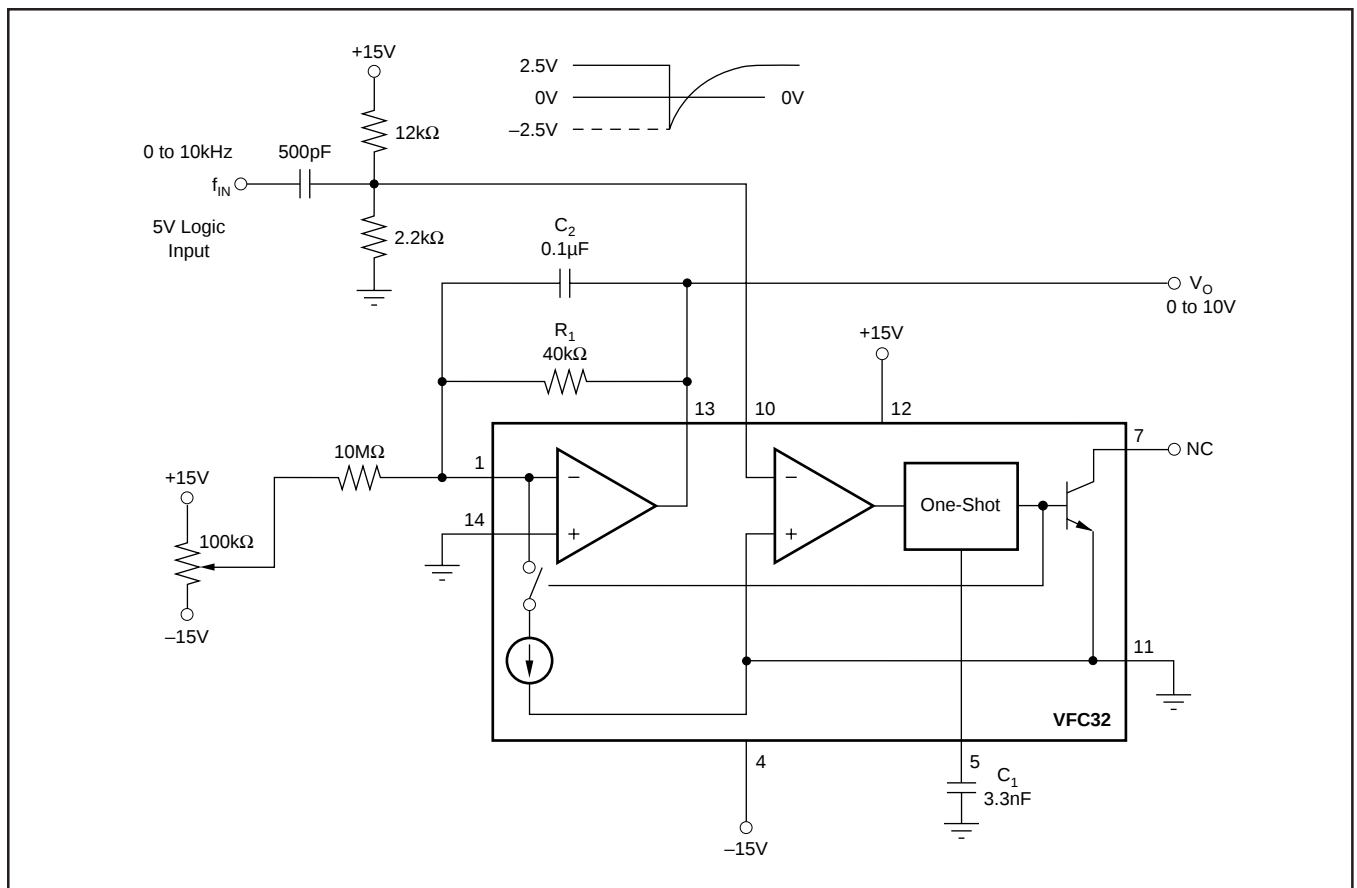


FIGURE 4. Frequency-to-Voltage Converter Circuit.

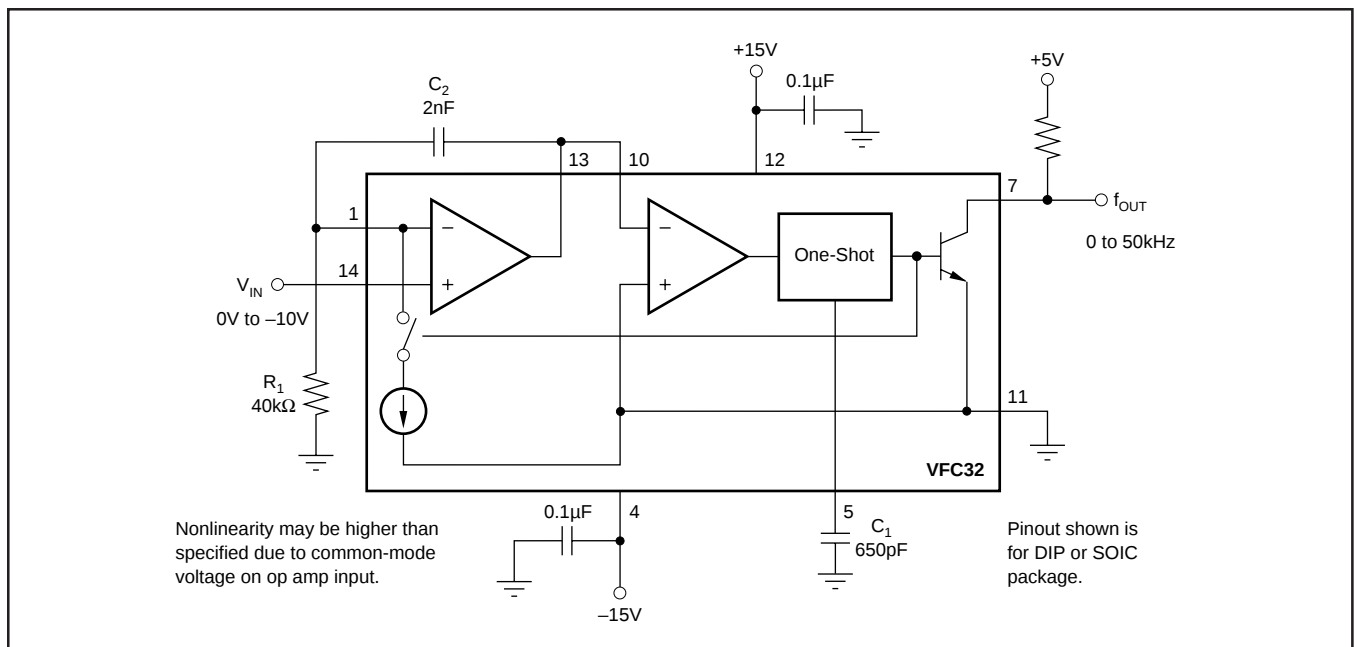


FIGURE 5. V/F Converter—Negative Input Voltage.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VFC32KP	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	VFC32KP	Samples
VFC32KPG4	LIFEBUY	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	VFC32KP	
VFC32KU	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU	Samples
VFC32KU/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU	Samples
VFC32KUE4	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	VFC32KU	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VFC32KU/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VFC32KU/2K5	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
VFC32KP	N	PDIP	14	25	506	13.97	11230	4.32
VFC32KPG4	N	PDIP	14	25	506	13.97	11230	4.32
VFC32KU	D	SOIC	14	50	506.6	8	3940	4.32
VFC32KUE4	D	SOIC	14	50	506.6	8	3940	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated