December 1, 2010

SCAN90004

4-Channel LVDS Buffer/Repeater with Pre-Emphasis

General Description

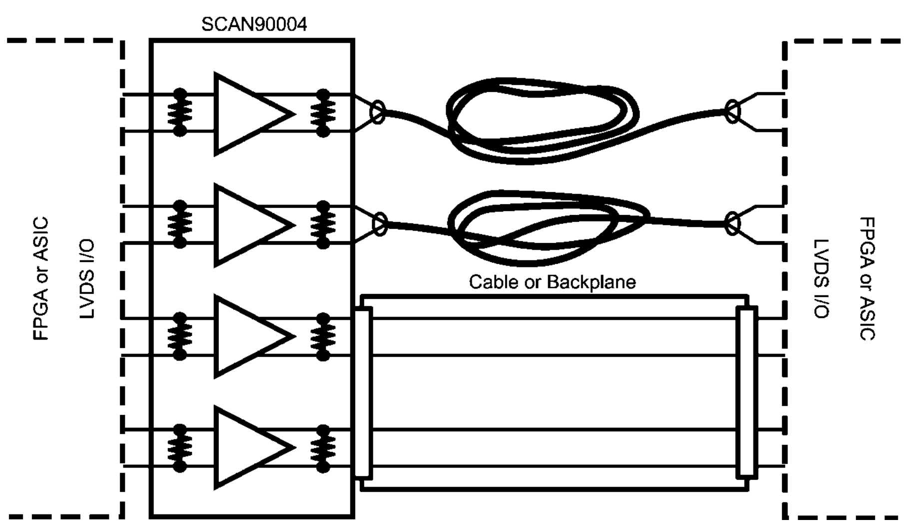
The SCAN90004 is a four channel 1.5 Gbps LVDS buffer/repeater. High speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while configurable pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs interface to LVDS, and Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs and outputs are internally terminated with a 100Ω resistor to improve performance and minimize board space. The repeater function is especially useful for boosting signals for longer distance transmission over lossy cables and backplanes.

Integrated testability circuitry supports IEEE1149.1 (JTAG) on single-ended LVTTL/CMOS I/O and limited IEEE1149.6 capability on high-speed differential LVDS interconnects. The 3.3V supply, CMOS process, and LVDS I/O ensure stable high performance at low power over the entire industrial -40 to +85°C temperature range.

Features

- 1.5 Gbps maximum data rate per channel
- Configurable pre-emphasis drives lossy backplanes and cables
- Low output skew and jitter
- LVDS/CML/LVPECL compatible input, LVDS output
- On-chip 100Ω input and output termination
- 12 kV ESD protection on LVDS Outputs
- IEEE 1149.1 JTAG interface
- IEEE 1149.6 limited capability
- Fault Insertion
- Single 3.3V supply
- Very low power consumption
- Industrial -40 to +85°C temperature range
- Small TQFP Package Footprint
- See DS90LV004 for non-JTAG version

Typical Application



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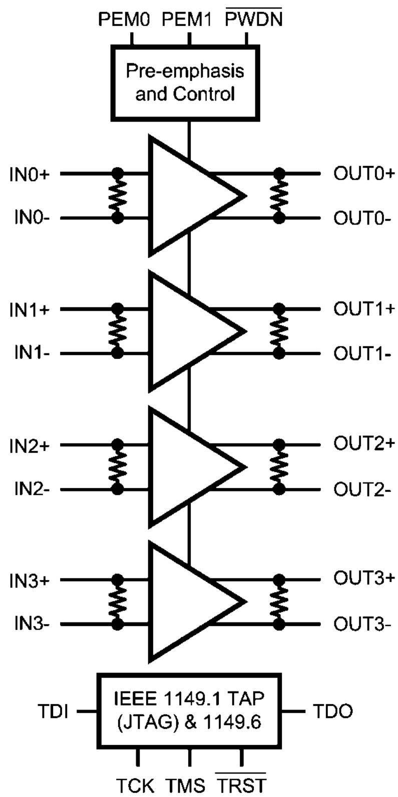
Block and Connection Diagrams



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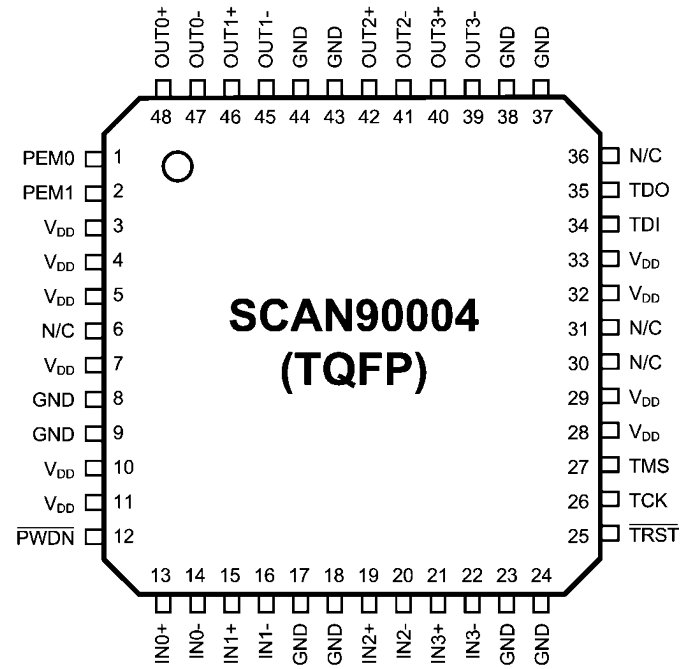
SCAN90004 Block Diagram



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Pinout - Top View

Pin Descriptions

Pin Name	TQFP Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS			
IN0+ IN0−	13 14	I, LVDS	Channel 0 inverting and non-inverting differential inputs.
IN1+ IN1−	15 16	I, LVDS	Channel 1 inverting and non-inverting differential inputs.
IN2+ IN2−	19 20	I, LVDS	Channel 2 inverting and non-inverting differential inputs.
IN3+ IN3−	21 22	I, LVDS	Channel 3 inverting and non-inverting differential inputs.
DIFFERENTIAL OUTPUTS			
OUT0+ OUT0−	48 47	O, LVDS	Channel 0 inverting and non-inverting differential outputs. (*Note 1*)
OUT1+ OUT1−	46 45	O, LVDS	Channel 1 inverting and non-inverting differential outputs. (*Note 1*)
OUT2+ OUT2−	42 41	O, LVDS	Channel 2 inverting and non-inverting differential outputs. (*Note 1*)
OUT3+ OUT3-	40 39	O, LVDS	Channel 3 inverting and non-inverting differential outputs. (*Note 1*)
DIGITAL CONTROL INTERFACE			
$\overline{\text{PWDN}}$	12	I, LVTTL	A logic low at $\overline{\text{PWDN}}$ activates the hardware power down mode.
PEM0 PEM1	1 2	I, LVTTL	Pre-emphasis Control Inputs (affects all Channels)
TDI	34	I, LVTTL	Test Data Input to support IEEE 1149.1 features
TDO	35	O, LVTTL	Test Data Output to support IEEE 1149.1 features
TMS	27	I, LVTTL	Test Mode Select to support IEEE 1149.1 features
TCK	26	I, LVTTL	Test Clock to support IEEE 1149.1 features
$\overline{\text{TRST}}$	25	I, LVTTL	Test Reset to support IEEE 1149.1 features
POWER			
V_{DD}	3, 4, 5, 7, 10, 11, 28, 29, 32, 33	I, Power	V_{DD} = 3.3V, ±5%
GND	8, 9, 17, 18, 23, 24, 37, 38, 43, 44	I, Power	Ground
N/C	6, 30, 31, 36		No Connect

Note 1: The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the SCAN90004 device have been optimized for point-to-point backplane and cable applications.

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{DD})	−0.3V to +4.0V
CMOS Input Voltage	-0.3V to (V_{DD}+0.3V)
LVDS Input Voltage (Note 3)	-0.3V to (V_{DD}+0.3V)
LVDS Output Voltage	-0.3V to (V_{DD}+0.3V)
LVDS Output Short Circuit Current	+40 mA
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Solder, 4sec)	260°C
Max Pkg Power Capacity @ 25°C	1.64W
Thermal Resistance (θ_{JA})	76°C/W
Package Derating above +25°C	13.2mW/°C
ESD Last Passing Voltage (LVDS output pins)	
HBM, 1.5kΩ, 100pF	12kV
EIAJ, 0Ω, 200pF	250V
ESD Last Passing Voltage (All other pins)	
HBM, 1.5kΩ, 100pF	8kV
EIAJ, 0Ω, 200pF	250V

Recommended Operating Conditions

Supply Voltage (V_{DD})	3.15V to 3.45V
Input Voltage (V_I) (Note 3)	0V to V_{DD}
Output Voltage (V_O)	0V to V_{DD}
Operating Temperature (T_A)	
Industrial	−40°C to +85°C

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of products outside of recommended operation conditions.

Note 3: V_{ID} max < 2.4V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
LVTTL DC SPECIFICATIONS ($\overline{PWDN}$, PEM0, PEM1, TDI, TDO, TCK, TMS, $\overline{TRST}$)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10		+10	μA
I_{ILR}	Low Level Input Current	TDI, TMS, $\overline{TRST}$	-40		-200	μA
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		3.5		pF
C_{OUT1}	Output Capacitance	Any Digital Output Pin to V_{SS}		5.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.8		V
V_{OH}	High Level Output Voltage (TDO)	I_{OH} = −12 mA, V_{DD} = 3.15 V	2.4			V
		I_{OH} = −100 μA, V_{DD} = 3.15 V	V_{DD}-0.2			V
V_{OL}	Low Level Output Voltage (TDO)	I_{OL} = 12 mA, V_{DD} = 3.15 V			0.5	V
		I_{OL} = 100 μA, V_{DD} = 3.15 V			0.2	V
I_{OS}	Output Short Circuit Current	TDO	−15		−125	mA
I_{OZ}	Output TRI-STATE® Current	TDO	−10		+10	μA
LVDS INPUT DC SPECIFICATIONS (INn±)						
V_{TH}	Differential Input High Threshold (Note 5)	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V		0	100	mV
V_{TL}	Differential Input Low Threshold (Note 5)	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V	100		2400	mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.45V	0.05		3.40	V
C_{IN2}	Input Capacitance	IN+ or IN− to V_{SS}		5.2		pF
I_{IN}	Input Current	V_{IN} = 3.45V, $V_{DD} = V_{DDMAX}$	−10		+10	μA
		V_{IN} = 0V, $V_{DD} = V_{DDMAX}$	−10		+10	μA

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
LVDS OUTPUT DC SPECIFICATIONS (OUTn±)						
V_{OD}	Differential Output Voltage, 0% Pre-emphasis (Note 5)	R_L = 100Ω external resistor between OUT+ and OUT−	250	500	600	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		-35		35	mV
V_{OS}	Offset Voltage (Note 6)		1.05	1.18	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		-35		35	mV
I_{OS}	Output Short Circuit Current	OUT+ or OUT− Short to GND		−60	−90	mA
C_{OUT2}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE		5.5		pF
SUPPLY CURRENT (Static)						
I_{CC}	Supply Current	All inputs and outputs enabled and active, terminated with external differential load of 100Ω between OUT+ and OUT-, 0% pre-emphasis		117	140	mA
I_{CCZ}	Supply Current - Power Down Mode	$\overline{\text{PWDN}}$ = L, 0% pre-emphasis		2.7	6	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V_{OD}. (Note 11)		210	300	ps
t_{HLT}	Differential High to Low Transition Time			210	300	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V_{OD} between input to output.		2.0	3.2	ns
t_{PHLD}	Differential High to Low Propagation Delay			2.0	3.2	ns
t_{SKD1}	Pulse Skew	$\lvert t_{PLHD} - t_{PHLD} \rvert$ (Note 11)		25	80	ps
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels. (Note 11)		50	125	ps
t_{SKP}	Part to Part Skew (Note 11)	Common edge, parts at same temp and V_{CC} (Note 11)			1.1	ns
t_{JIT}	Jitter (0% Pre-emphasis) (Note 7)	RJ - Alternating 1 and 0 at 750 MHz (Note 8)		1.1	1.5	psrms
		DJ - K28.5 Pattern, 1.5 Gbps (Note 9)		43	62	psp-p
		TJ - PRBS 2^{23}-1 Pattern, 1.5 Gbps (Note 10)		35	85	psp-p
t_{ON}	LVDS Output Enable Time	Time from $\overline{\text{PWDN}}$ to OUT± change from TRI-STATE to active.			300	ns
t_{OFF}	LVDS Output Disable Time	Time from $\overline{\text{PWDN}}$ to OUT± change from active to TRI-STATE.			12	ns

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
SWITCHING CHARACTERISTICS—SCAN FEATURES						
f_{MAX}	Maximum TCK Clock Frequency	$R_L = 500\Omega$, $C_L = 35$ pF	25.0			MHz
t_S	TDI to TCK, H or L		3.0			ns
t_H	TDI to TCK, H or L		0.5			ns
t_S	TMS to TCK, H or L		2.5			ns
t_H	TMS to TCK, H or L		0.5			ns
t_W	TCK Pulse Width, H or L		10.0			ns
t_W	$\overline{\text{TRST}}$ Pulse Width, L		2.5			ns
t_{REC}	Recovery Time, $\overline{\text{TRST}}$ to TCK		1.0			ns

Note 4: Typical parameters are measured at $V_{DD} = 3.3V$, $T_A = 25°C$. They are for reference purposes, and are not production-tested.

Note 5: Differential output voltage V_{OD} is defined as ABS(OUT+–OUT–). Differential input voltage V_{ID} is defined as ABS(IN+–IN–).

Note 6: Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

Note 7: Jitter is not production tested, but guaranteed through characterization on a sample basis.

Note 8: Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = V_{ID} = 500mV, 50% duty cycle at 750MHz, $t_r = t_f$ = 50ps (20% to 80%).

Note 9: Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = V_{ID} = 500mV, K28.5 pattern at 1.5 Gbps, $t_r = t_f$ = 50ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

Note 10: Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = V_{ID} = 500mV, 2^{23}-1 PRBS pattern at 1.5 Gbps, $t_r = t_f$ = 50ps (20% to 80%).

Note 11: Not production tested. Guaranteed by a statistical analysis on a sample basis at the time of characterization.

Feature Descriptions

INTERNAL TERMINATIONS

The SCAN90004 has integrated termination resistors on both the input and outputs. The inputs have a 100Ω resistor across the differential pair, placing the receiver termination as close as possible to the input stage of the device. The LVDS outputs also contain an integrated 100Ω ohm termination resistor, this resistor is used to reduce the effects of Near End Crosstalk (NEXT) and does not take the place of the 100 ohm termination at the inputs to the receiving device. The integrated terminations improve signal integrity and decrease the external component count resulting in space savings.

OUTPUT CHARACTERISTICS

The output characteristics of the SCAN90004 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

POWERDOWN MODE

The $\overline{\text{PWDN}}$ input activates a hardware powerdown mode. When the powerdown mode is active ($\overline{\text{PWDN}}$=L), all input and output buffers and internal bias circuitry are powered off and disabled. Outputs are tri-stated in powerdown mode. JTAG Circuitry is active per the IEEE standard, but does not switch unless TCK is toggling. When exiting powerdown mode, there is a delay associated with turning on bandgap references and input/output buffer circuits as indicated in the LVDS Output Switching Characteristics

Upon asserting the power down function ($\overline{\text{PWDN}}$ = Low), and if the Pre-emphasis feature is enable, it is possible for the driver output to source current for a short amount of time lifting the output common mode to V_{DD}. To prevent this occurrence, a load discharge pull down path can be used on either output (1 kΩ to ground recommended). Alternately, a commonly deployed external failsafe network will also provide this path (see INPUT FAILSAFE BIASING). The occurrence of this is application dependant, and parameters that will affect if this is of concern include: AC coupling, use of the powerdown feature, presence of the discharge path, presence of the failsafe biasing, the usage of the pre-emphasis feature, and input characteristics of the downstream LVDS Receiver.

PRE-EMPHASIS

Pre-emphasis dramatically reduces ISI jitter from long or lossy transmission media. Two pins are used to select the pre-emphasis level for all outputs: off, low, medium, or high.

Pre-emphasis Control Selection Table

PEM1	PEM0	Pre-Emphasis
0	0	Off
0	1	Low
1	0	Medium
1	1	High

INPUT FAILSAFE BIASING

Failsafe biasing of the LVDS link should be considered if the downstream Receiver is ON and enabled when the source is in TRI-STATE, powered off, or removed. This will set a valid known input state to the active receiver. This is accomplished by using a pull up resistor to V_{DD} on the 'plus' line, and a pull down resistor to GND on the 'minus' line. Resistor values are in the 750 Ω to several k Ω range. The exact value depends upon the desired common mode bias point, termination resistor(s) and desired input differential voltage setting. Please refer to application note AN-1194 "Failsafe Biasing of LVDS interfaces" for more information and a general discussion.

Design-for-Test (DfT) Features

IEEE 1149.1 (JTAG) SUPPORT

The SCAN90004 supports a fully compliant IEEE 1149.1 interface. The Test Access Port (TAP) provides access to boundary scan cells at each LVTTL I/O on the device for interconnect testing. Differential pins are included in the same boundary scan chain but instead contain IEEE1149.6 cells. IEEE1149.6 is the improved IEEE standard for testing high-speed differential signals.

Refer to the BSDL file located on National's website for the details of the SCAN90004 IEEE 1149.1 implementation.

IEEE 1149.6 SUPPORT

AC-coupled differential interconnections on very high speed (1+ Gbps) data paths are not testable using traditional IEEE 1149.1 techniques. The IEEE 1149.1 structures and methods are intended to test static (DC-coupled), single ended networks. IEEE 1149.6 is targeted for the testing of high-speed differential (including AC coupled) networks. The SCAN90004 includes circuitry to support AC-coupled testing on all differential inputs and outputs and offers limited test capability. The limitations are due to several application specific factors (board layout, capacitor value, data rate etc.), and also IO compliance (LVDS links in general are DC coupled). The SCAN90004 has not been tested for full compliance or full compatibility to the IEEE1149.6 standard. Testing of the device in the targeted application with the appropriate JTAG software will determine what extent of IEEE 1149.6 support is provided by the device.

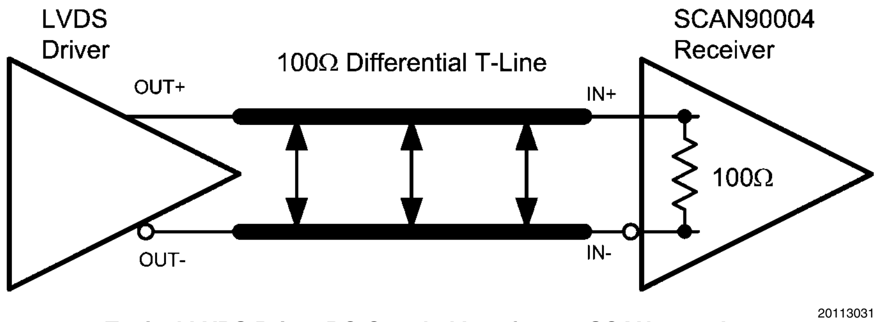
FAULT INSERTION

Fault Insertion is a technique used to assist in the verification and debug of diagnostic software. During system testing faults are "injected" to simulate hardware failure and thus help verify the monitoring software can detect and diagnose these faults. In the SCAN90004 an IEEE1149.1 "stuck-at" instruction can create a stuck-at condition, either high or low, on any pin or combination of pins. A more detailed description of the stuck-at feature can be found in NSC Applications note AN-1313.

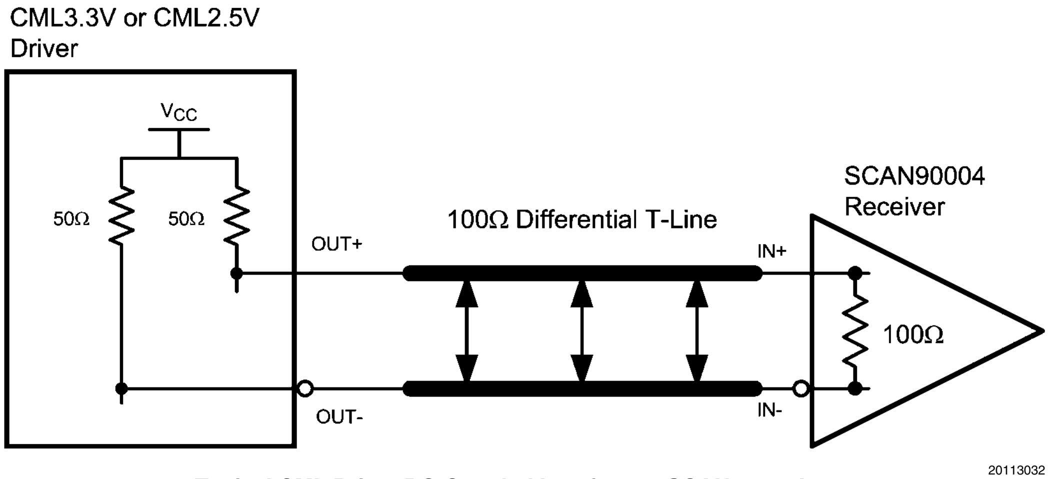
Application Information

INPUT INTERFACING

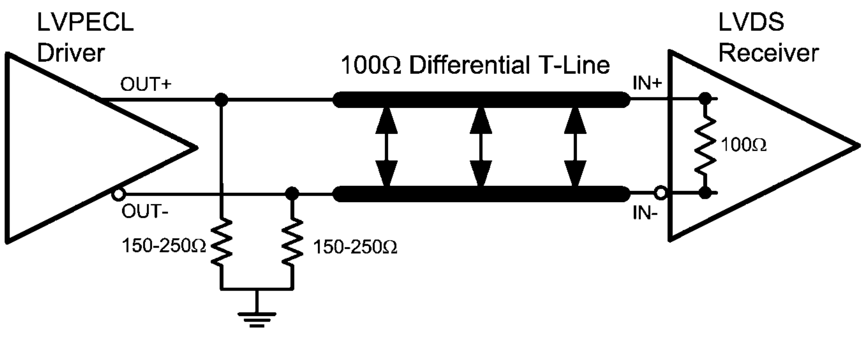
The SCAN90004 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the SCAN90004 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the SCAN90004 inputs are internally terminated with a 100Ω resistor.



Typical LVDS Driver DC-Coupled Interface to SCAN90004 Input



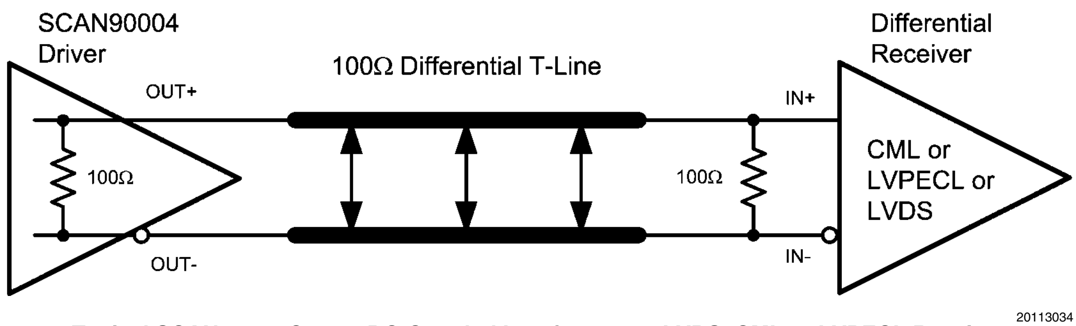
Typical CML Driver DC-Coupled Interface to SCAN90004 Input



Typical LVPECL Driver DC-Coupled Interface to SCAN90004 Input

OUTPUT INTERFACING

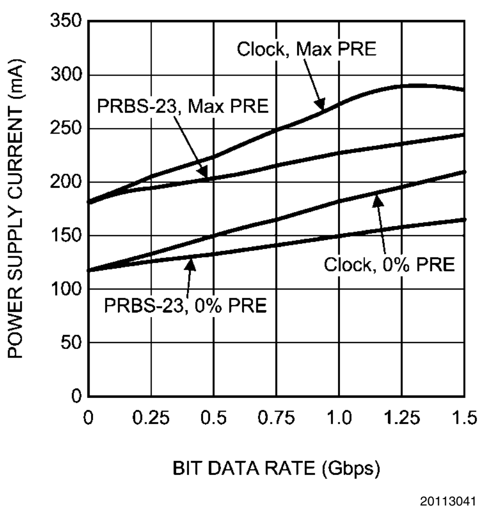
The SCAN90004 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



Typical SCAN90004 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

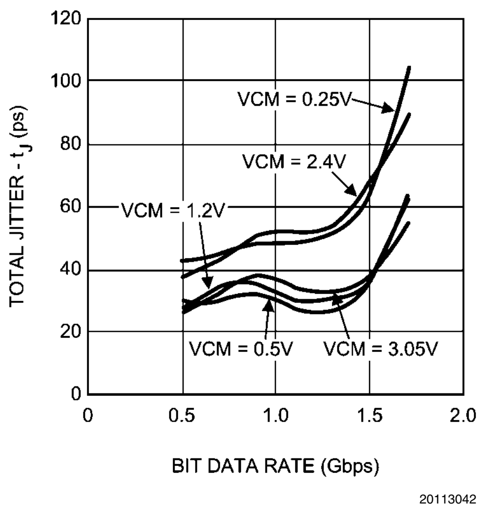
Typical Performance Characteristics

Power Supply Current vs. Bit Data Rate



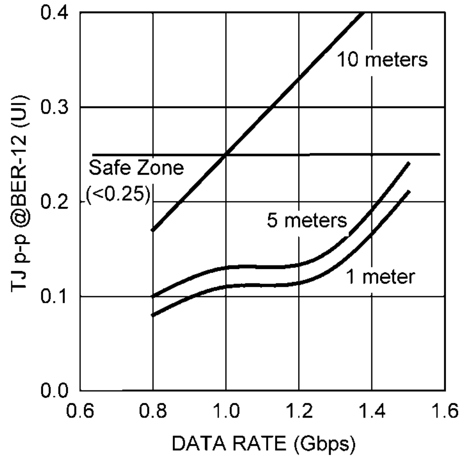
Dynamic power supply current was measured while running a clock or PRBS 2^23-1 pattern with all 4 channels active.
V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, V_{CM} = 1.2V

Total Jitter (T_J) vs. Bit Data Rate



Total Jitter measured at 0V differential while running a PRBS 2^23-1 pattern with a single channel active.
V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, 0% Pre-emphasis

Total Jitter (U.I.) vs. Bit Data Rate
SCAN90004 as Driver



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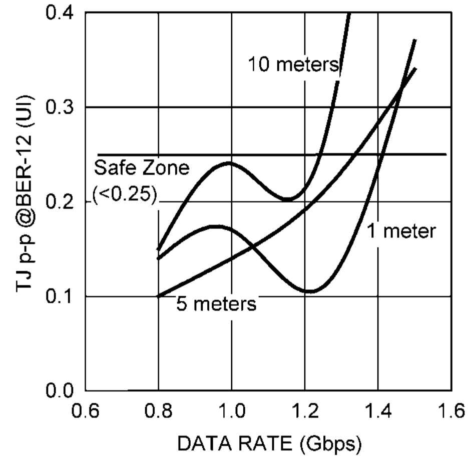
Total Jitter measured while SCAN90004 output is driving a PRBS 2^7-1 NRZ pattern with a single active channel across a Belden 1700A cable. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, 0% Pre-emphasis. Data measured at end of specified cable length.

Total Jitter (U.I.) vs. Bit Data Rate
SCAN90004 as Receiver



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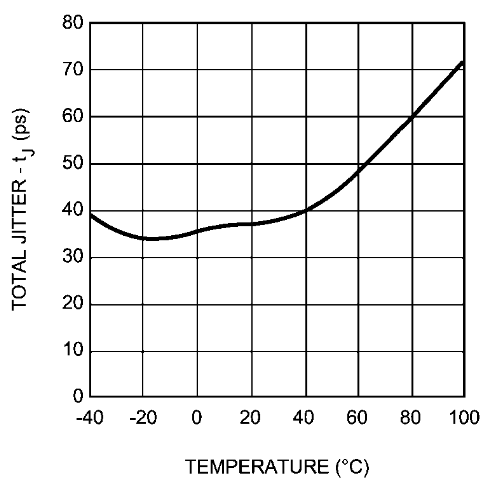
Total Jitter measured at SCAN90004 receiver outputs after receiving a PRBS 2^7-1 NRZ pattern over the specified cable length. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, data collected at receiver outputs, receiver located at end of specified Belden 1700A cable length.

Total Jitter (T_J) vs. Temperature



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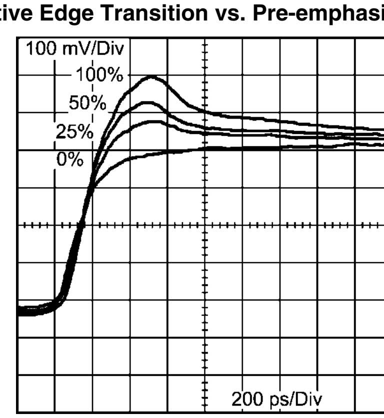
Total Jitter measured at 0V differential while running a PRBS 2^23-1 pattern with a single channel active. V_{CC} = 3.3V, V_{ID} = 0.5V, V_{CM} = 1.2V, 1.5 Gbps data rate, 0% Pre-emphasis

Positive Edge Transition vs. Pre-emphasis Level



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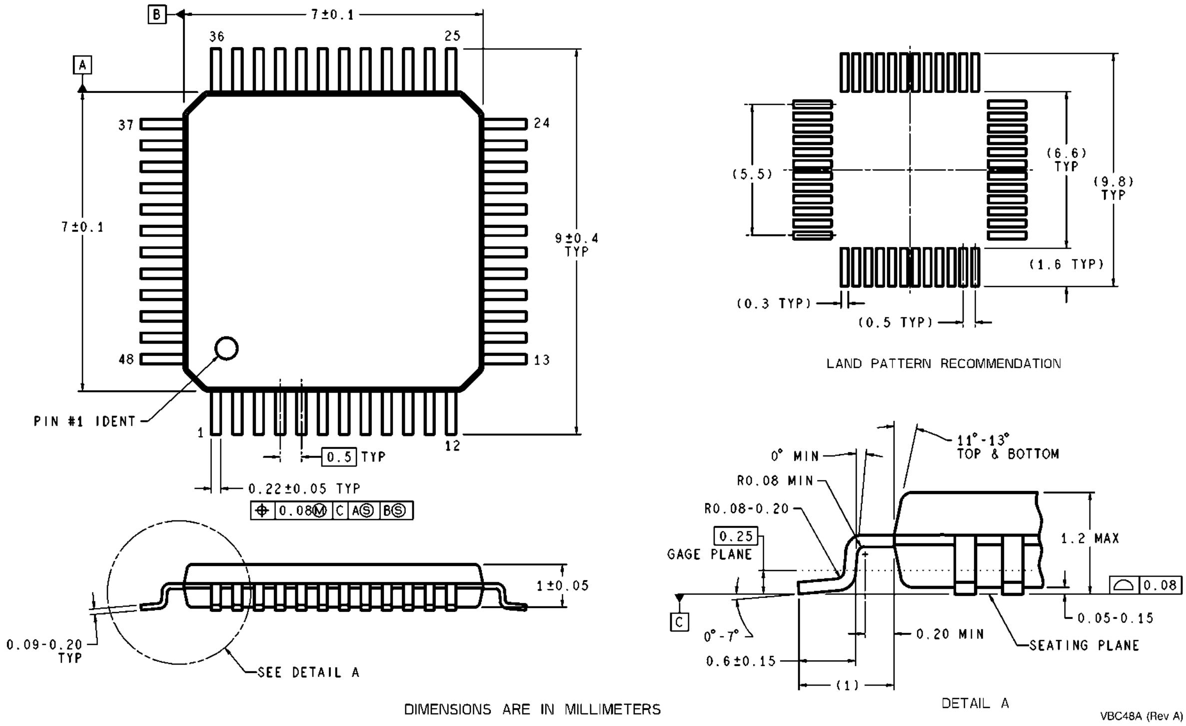
Physical Dimensions inches (millimeters) unless otherwise noted



48-TQFP
NS Package Number VBC48a
Order Number SCAN90004TVS (250 piece Tray)

Notes

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