

## Single-chip Type with Built-in FET Switching Regulator Series

# Boost and Inverted Output Power Supply for TFT-LCD Displays

## BD83850GWL

### General Description

BD83850GWL is a boost switching regulator and charge pump inverter for small TFT-LCD Displays. It has a wide input voltage range of 2.5V to 4.5V that is suitable for portable applications. In addition, its small package design is ideal for miniaturizing the power supply.

### Features

- Wide input voltage range of 2.5V to 4.5V
- High frequency operation
- Output Discharge Independent ON/OFF signal(STBYP, STBYN)
- Circuit protection
  - Over Current Protection (OCP)
  - Short Current Protection (SCP)
  - Under Voltage Lock Out (UVLO)
  - Thermal Shutdown (TSD)

### Applications

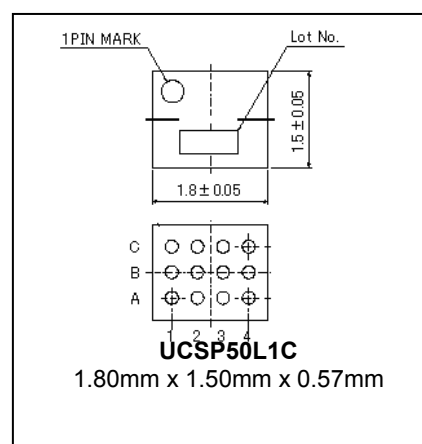
- TFT LCD Smart phones
- TFT LCD Tablets

### Key Specifications

|                           |              |
|---------------------------|--------------|
| ■ Input Voltage Range     | 2.5V to 4.5V |
| ■ Output Boost Voltage    | 5.0V(typ)    |
| ■ Output Inverted Voltage | -5.0V(typ)   |
| ■ Maximum Current         | 50mA(max)    |
| ■ Operating Frequency     | 1.0MHz(typ)  |
| ■ Efficiency              | >85 % (typ)  |
| ■ Output Voltage Accuracy | ±2 % (typ)   |
| ■ Standby Current         | 1μA(max)     |

### Package

W(Typ) x D(Typ) x H(Max)



### Typical Application Circuit

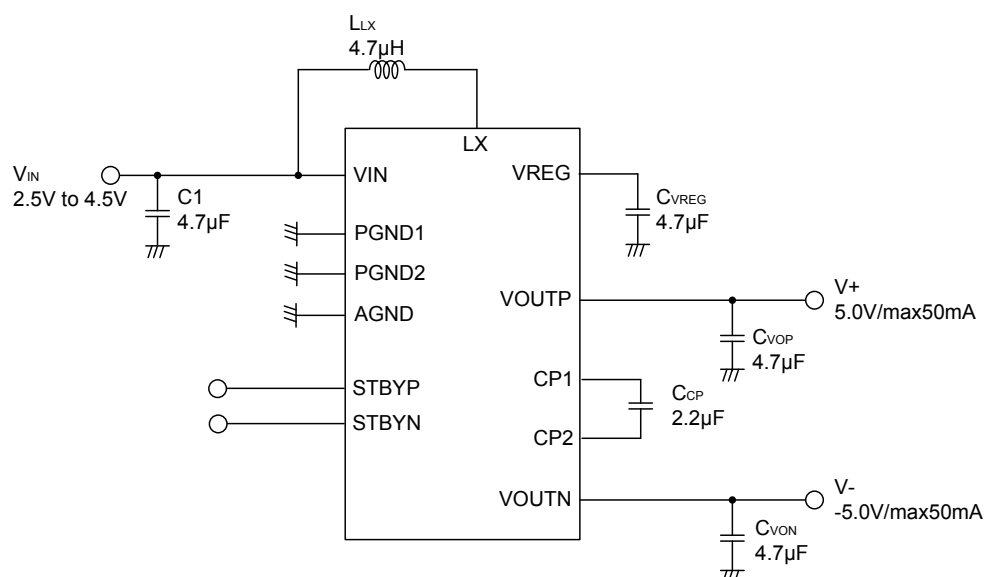


Figure 1. Application Circuit

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## Pin Configuration

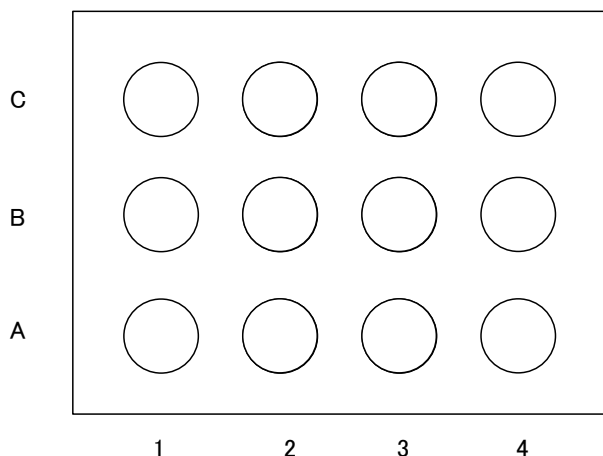


Figure 2. Pin assignment (Bottom view)

## Pin Description

| Pin No. | Pin Name | Function                                        |
|---------|----------|-------------------------------------------------|
| B-1     | CP2      | Negative charge pump flying capacitor           |
| A-3     | PGND1    | Boost Power ground                              |
| B-2     | PGND2    | Charge pump Power ground                        |
| C-1     | CP1      | Negative charge pump flying capacitor           |
| B-4     | VREG     | Boost converter output                          |
| C-4     | VOOTP    | LDO output (V+)                                 |
| A-1     | VOUTN    | Charge pump inverter (V-) output                |
| C-2     | AGND     | Analog ground                                   |
| B-3     | STBYN    | Charge pump inverter (V-) enable (only STBYP=H) |
| C-3     | STBYP    | LDO enable (V+)                                 |
| A-2     | VIN      | Input voltage supply                            |
| A-4     | LX       | Boost converter switch                          |

## Block Diagram

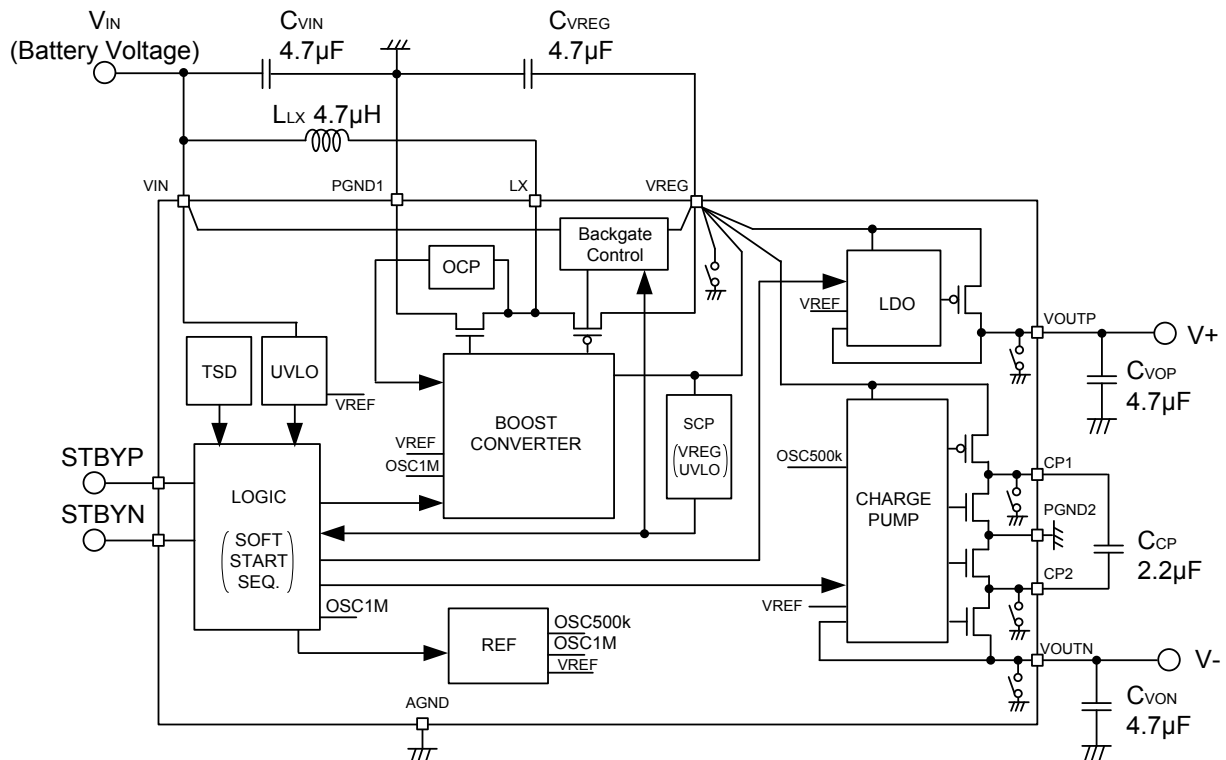


Figure 3. Block diagram

## Absolute Maximum Ratings (Ta = 25°C)

| Parameter                            | Symbol      | Rating      | Unit |
|--------------------------------------|-------------|-------------|------|
| Maximum power supply voltage         | VIN         | -0.3 to 7.0 | V    |
|                                      | STBYP,STBYN | -0.3 to 7.0 | V    |
| Voltage range                        | LX          | -0.3 to 7.0 | V    |
|                                      | VOUTP       | -0.3 to 7.0 | V    |
| Power dissipation <sup>(note1)</sup> | Pd          | 0.69        | W    |
| Storage temperature range            | Tstg        | -55 to +150 | °C   |
| Junction temperature                 | Tjmax       | +150        | °C   |

(Note 1) Derate by 5.5mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

## Recommended Operating Conditions

| Parameter                   | Symbol | Standard value |     |     | Units |
|-----------------------------|--------|----------------|-----|-----|-------|
|                             |        | MIN            | TYP | MAX |       |
| Power supply voltage        | VDD    | 2.5            | -   | 4.5 | V     |
| Operating temperature range | Topr   | -40            | 25  | 85  | °C    |

Electrical Characteristics (Unless otherwise specified  $V_{IN}=3.7V$   $T_a=25^{\circ}C$ )

| Parameter                        | Symbol              | Standard value    |        |        | Unit            | Conditions                             |  |
|----------------------------------|---------------------|-------------------|--------|--------|-----------------|----------------------------------------|--|
|                                  |                     | MIN               | TYP    | MAX    |                 |                                        |  |
| 【Power Supply】                   |                     |                   |        |        |                 |                                        |  |
| Input Voltage Range              | V <sub>IN</sub>     | 2.5               | -      | 4.5    | V               |                                        |  |
| UVLO Detect Voltage              | V <sub>UVLO1</sub>  | 2.20              | 2.26   | -      | V               |                                        |  |
| UVLO UnDetect Voltage            | V <sub>UVLO2</sub>  | -                 | 2.39   | 2.50   | V               |                                        |  |
| UVLO Hysteresis Voltage          | V <sub>HYS</sub>    | -                 | 0.13   | -      | V               |                                        |  |
|                                  |                     |                   |        |        |                 |                                        |  |
| 【Soft Start Sequence】            |                     |                   |        |        |                 |                                        |  |
| VOUTP Soft Start Time            | t <sub>SSVP</sub>   | 0.4               | 0.5    | 1.0    | ms              | C <sub>VOP</sub> =4.7μF+4.7μF          |  |
| VOUTN Soft Start Time            | t <sub>SSVN</sub>   | 3.7               | 4.1    | 4.6    | ms              | C <sub>VON</sub> =4.7μF+6.8μF          |  |
|                                  |                     |                   |        |        |                 |                                        |  |
| 【Boost Converter】                |                     |                   |        |        |                 |                                        |  |
| LX Switching Frequency           | f <sub>SWLX</sub>   | 0.90              | 1.00   | 1.10   | MHz             |                                        |  |
| LX OCP Current                   | OCPLXL              | 0.6               | -      | -      | A               |                                        |  |
| VREG Output Voltage              | V <sub>VREG</sub>   | 5.10              | 5.25   | 5.40   | V               |                                        |  |
| VREGUVLO Voltage 1               | V <sub>RUVLO1</sub> | 1.9               | 2.1    | 2.3    | V               | Among Soft Start Operation             |  |
| VREGUVLO Voltage 2               | V <sub>RUVLO2</sub> | 4.35              | 4.55   | 4.75   | V               |                                        |  |
|                                  |                     |                   |        |        |                 |                                        |  |
| 【Output VOUTP】                   |                     |                   |        |        |                 |                                        |  |
| Output Voltage                   | V <sub>OUTP</sub>   | 4.900             | 5.000  | 5.100  | V               |                                        |  |
| Output Voltage Accuracy          | V <sub>OUTPAQ</sub> | -2                | -      | 2      | %               |                                        |  |
| Maximum Output Current           | I <sub>OUTP</sub>   | -                 | -      | 50     | mA              |                                        |  |
| Line Regulation                  | V <sub>OPLINE</sub> | -                 | 0.1    | -      | %/V             | I <sub>out</sub> =10mA                 |  |
| Load Regulation                  | V <sub>OPLOAD</sub> | -                 | 10     | -      | mV              | I <sub>out</sub> =50mA                 |  |
| Discharge Resistor               | R <sub>OPDIS</sub>  | 20                | 40     | 80     | Ω               | VREG=5.25V                             |  |
|                                  |                     |                   |        |        |                 |                                        |  |
| 【Output VOUTN】                   |                     |                   |        |        |                 |                                        |  |
| CP Switching Frequency           | f <sub>SWCP</sub>   | 450               | 500    | 550    | kHz             |                                        |  |
| Output Voltage                   | V <sub>OUTN</sub>   | -5.100            | -5.000 | -4.900 | V               |                                        |  |
| Output Voltage Accuracy          | V <sub>OUTNAQ</sub> | -2                | -      | 2      | %               |                                        |  |
| Maximum Output Current           | I <sub>OUTN</sub>   | -                 | -      | 50     | mA              |                                        |  |
| Line Regulation                  | V <sub>ONLINE</sub> | -                 | 0.1    | -      | %/V             | I <sub>out</sub> =10mA                 |  |
| Load Regulation                  | V <sub>ONLOAD</sub> | -                 | 10     | -      | mV              | I <sub>out</sub> =50mA                 |  |
| Discharge Resistor               | R <sub>ONDIS</sub>  | 10                | 20     | 40     | Ω               | VREG=5.25V                             |  |
|                                  |                     |                   |        |        |                 |                                        |  |
| 【STBYP,STBYN】                    |                     |                   |        |        |                 |                                        |  |
| STBY pin Control voltage         | Active              | V <sub>STBH</sub> | 1.5    | -      | V <sub>IN</sub> | V                                      |  |
|                                  | Non-active          | V <sub>STBL</sub> | -0.3   | -      | 0.3             | V                                      |  |
| STBY pin pull down resistance    | R <sub>STB1</sub>   | 500               | 800    | 1100   | kΩ              |                                        |  |
|                                  |                     |                   |        |        |                 |                                        |  |
| 【Circuit current】                |                     |                   |        |        |                 |                                        |  |
| Standby current                  | I <sub>STB</sub>    | -                 | 0      | 1      | μA              | STBYP=STBYN=L                          |  |
| Circuit current of operation VIN | I <sub>DD</sub>     | 1.3               | 2.5    | 5.0    | mA              | STBYP=STBYN=H<br>VOUTP IL=0,VOUTN IL=0 |  |

Typical Performance Curves

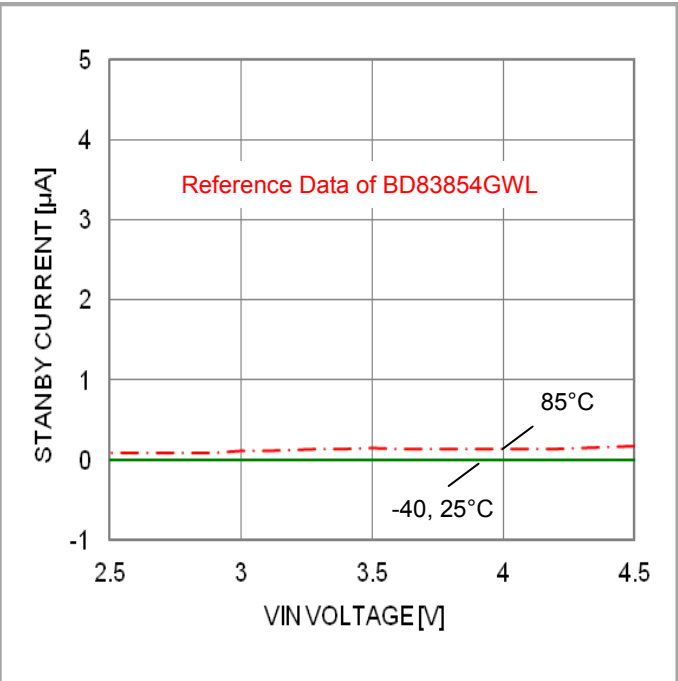


Figure 4. Standby Current vs VIN Voltage  
(Ta -40, 25, 85°C)

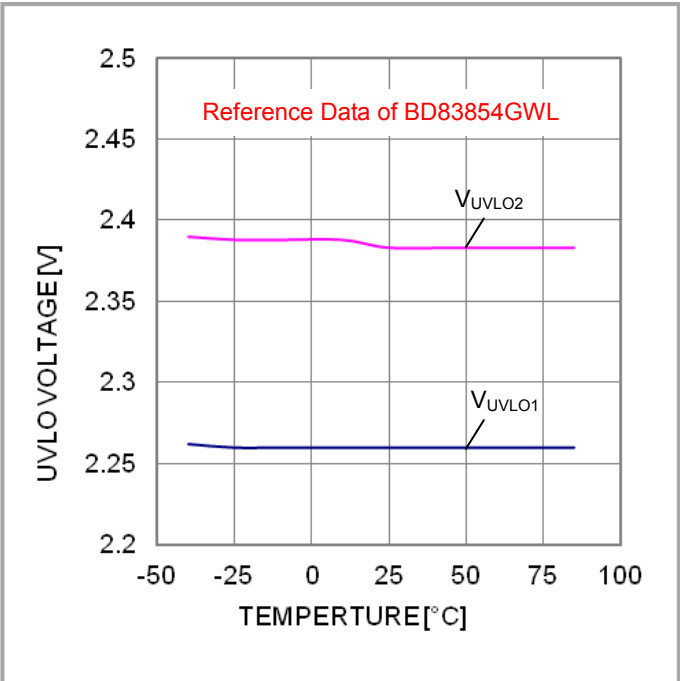


Figure 5. VIN UVLO Voltage vs Temperature

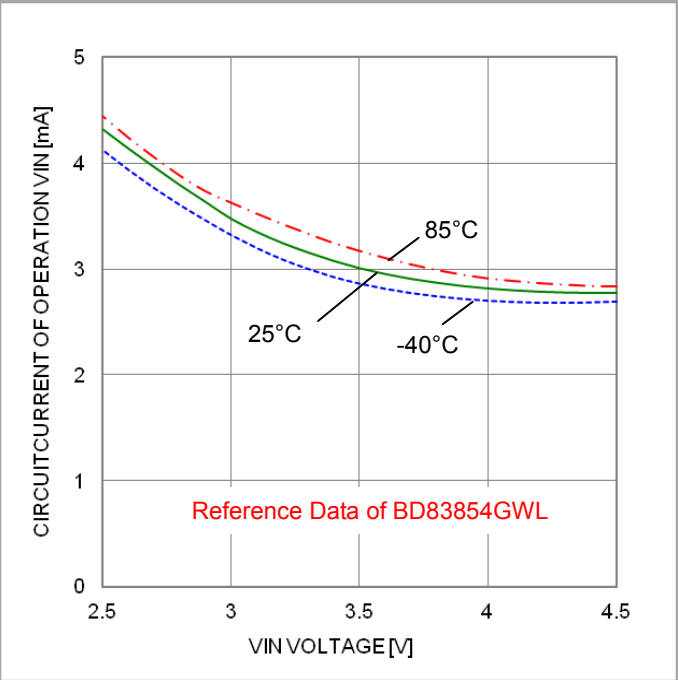


Figure 6. Circuit Current of Operation VIN vs VIN Voltage  
(Ta -40, 25, 85°C)

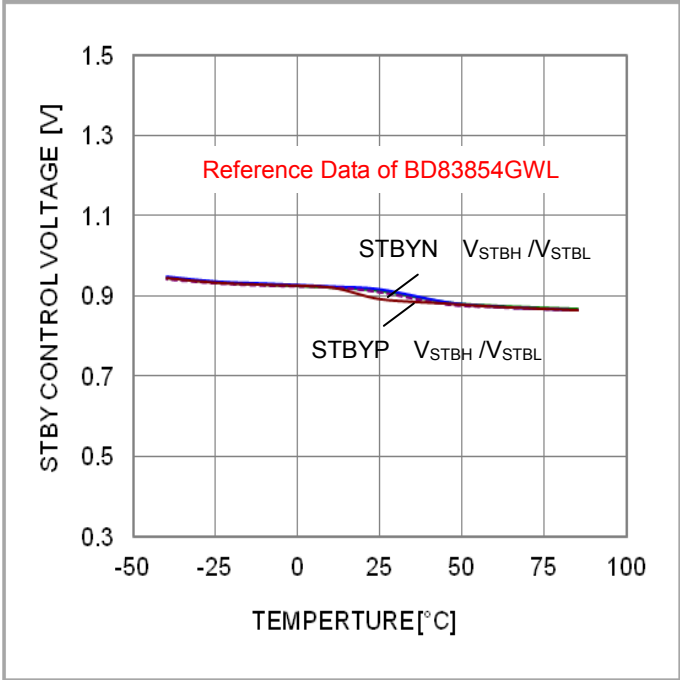


Figure 7. STBY Control Voltage vs Temperature  
(VIN =3.7V)

## Typical Performance Curves – continued

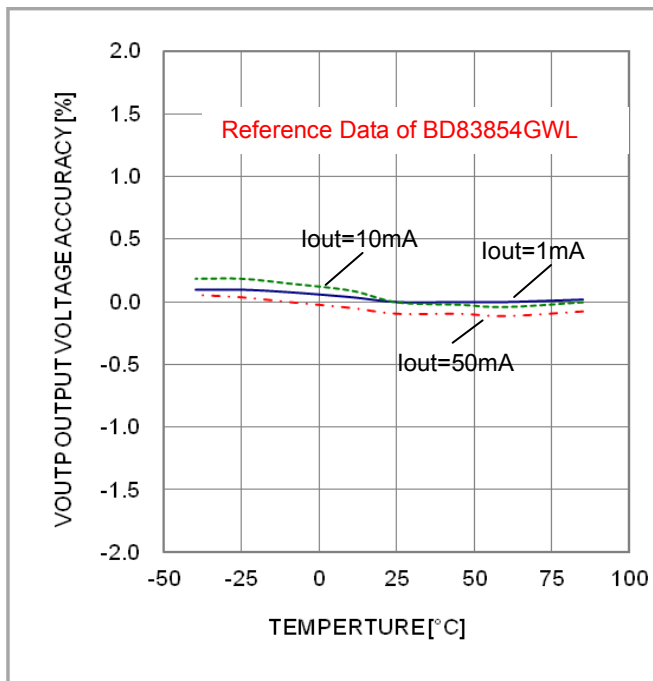


Figure 8. VOUTP Output Voltage vs Temperature  
( $V_{IN} = 3.7V$ ,  $I_{out} = 1m, 10m, 50mA$ )

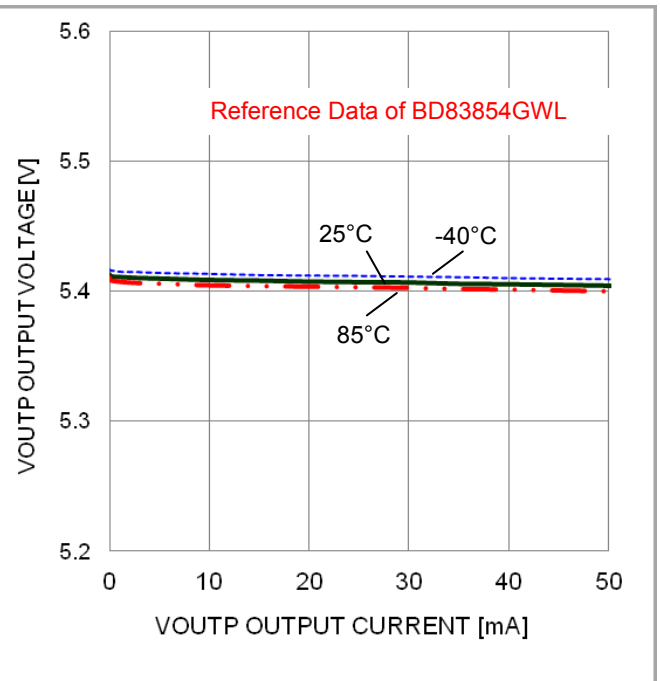


Figure 9. VOUTP Load Regulation  
( $T_a = -40^{\circ}C, 25^{\circ}C, 85^{\circ}C$ )

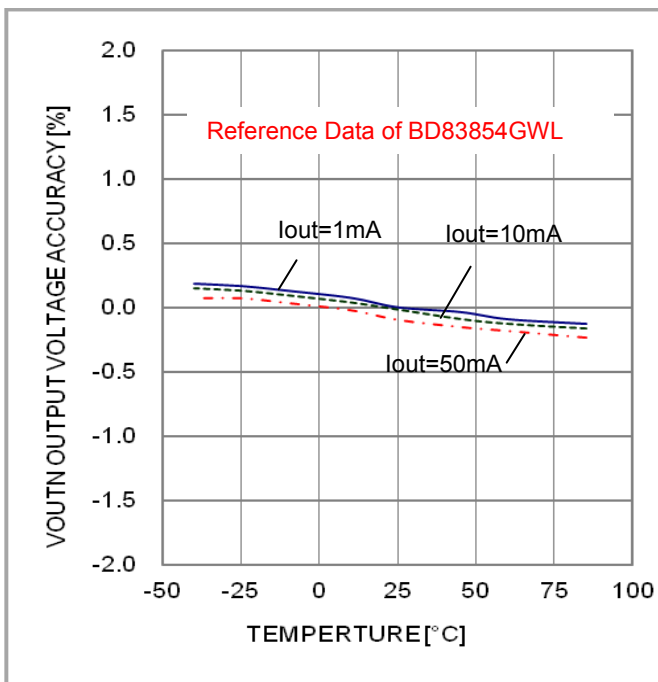


Figure 10. VOUTN Output Voltage vs Temperature  
( $V_{IN} = 3.7V$ ,  $I_{out} = 1m, 10m, 50mA$ )

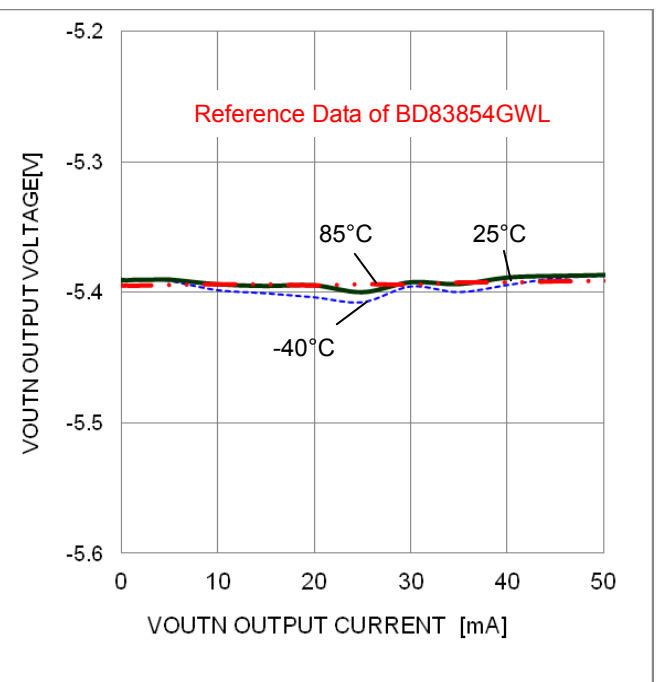


Figure 11. VOUTN Load Regulation  
( $T_a = -40, 25, 85^{\circ}C$ )

## Typical Performance Curves – continued

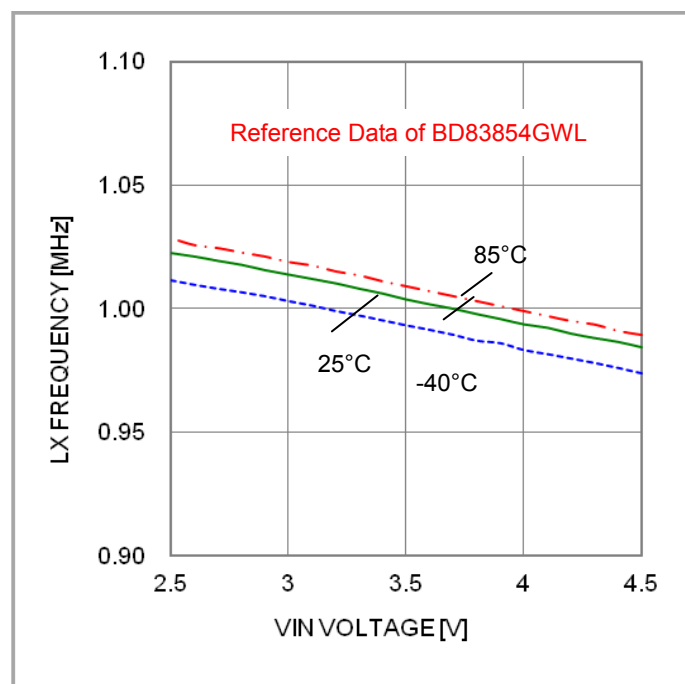


Figure 12. LX Frequency vs VIN Voltage  
(Ta -40, 25, 85°C)

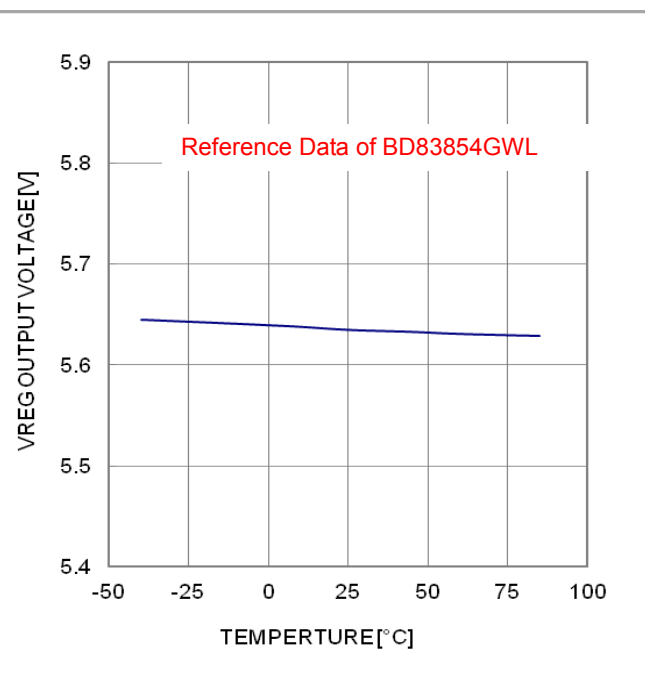


Figure 13. VREG Output Voltage vs Temperature  
(VIN =3.7V, Iout=0)

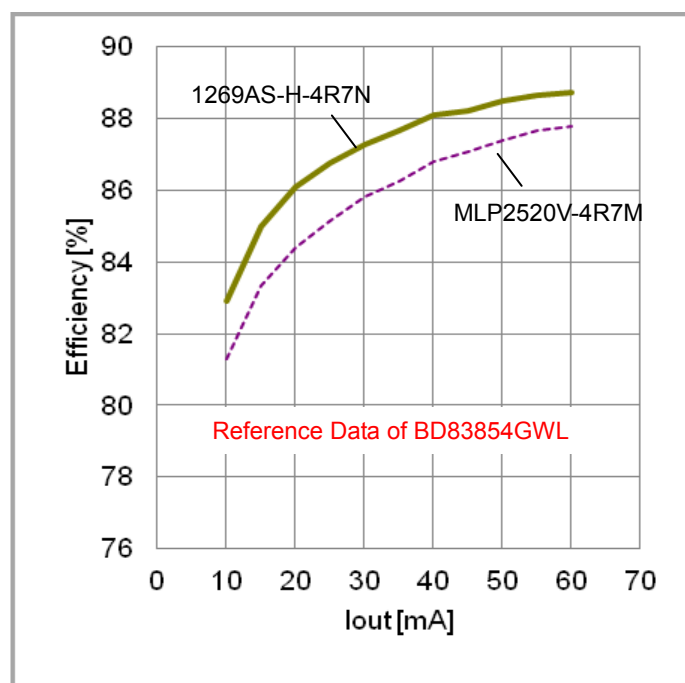


Figure 14. Efficiency vs Iout  
(VIN =3.7V, Ta 25°C)

$$\text{Efficiency} = (\text{VOUTP} \times \text{Iout} - \text{VOUTN} \times \text{Iout}) / (\text{VIN} \times \text{Idd})$$

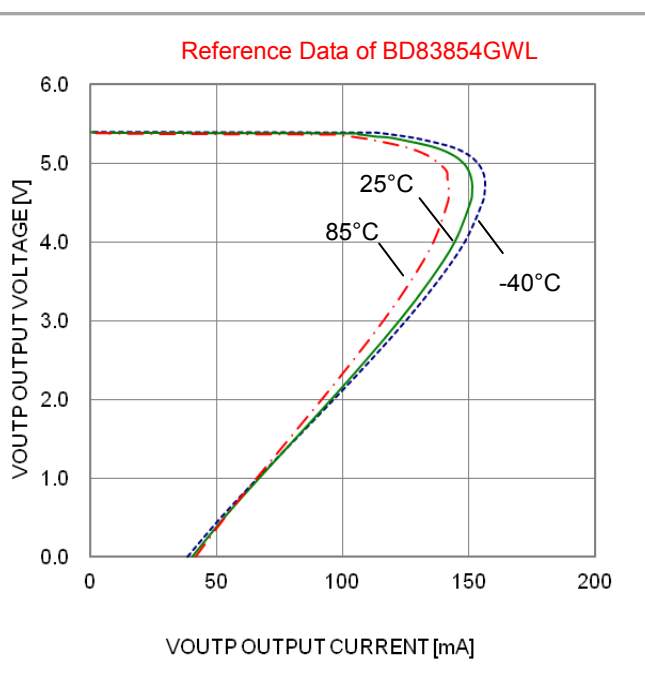


Figure 15. VOUTP vs IVOUTP  
(Ta -40, 25, 85°C)

## Timing Chart

## Recommended Power ON Sequence (STBYP has same timing as STBYN)

STBYP & STBYN are recommended simultaneously to be in H when after VIN becomes more than 2.5V (working range voltage). The through rate should be less than 100 $\mu$ s when STBYP and STBYN are set H simultaneously. It is not relating to soft start but to prevent chattering. STBYN must be high within 5ms from STBYP=H.

Table 1. Function of STBYP and STBYN

| STBYP | STBYN | VOUTP | VOUTN | Function Description                                                                                                           |
|-------|-------|-------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| L     | L     | +0V   | -0V   | The output of VOUTP/N stay "L" before STBYP become "H"                                                                         |
| L     | L→H   | +0V   | -0V   |                                                                                                                                |
| L→H   | L     | +5.0V | -0V   |                                                                                                                                |
| H→L   | L     | +0V   | -0V   | VOUTP can be controlled independently when STBYN is "L"                                                                        |
| L→H   | L→H   | +5.0V | -5.0V | STBYP and STBYN should be controlled almost at the same timing<br>Gap of STBYP/N should less than 5ms                          |
| H     | L→H   | +0V   | -0V   | VOUTP will be driven to "L" when setting STBYN to "H" later more than 5ms<br>Otherwise the internal sequence will be disrupted |

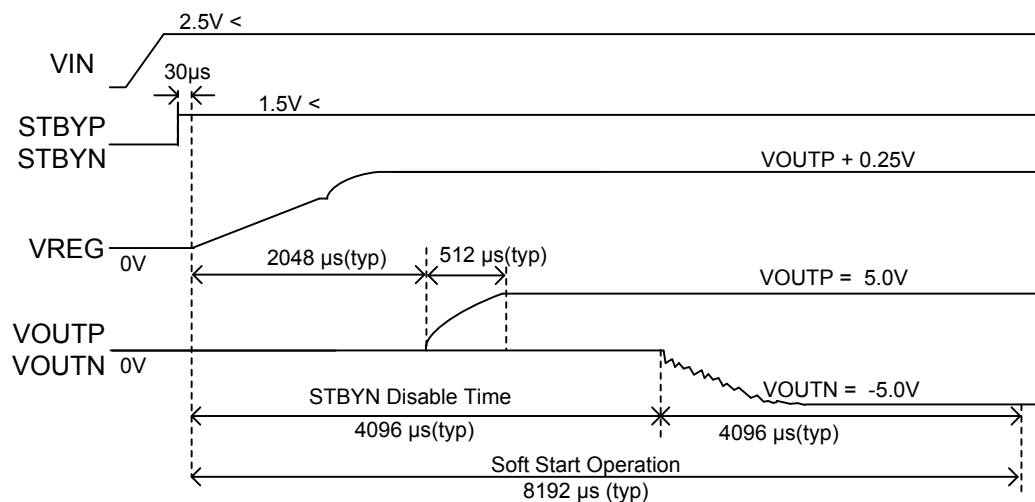


Figure 16. Power ON Sequence Timing (STBYP=STBYN)

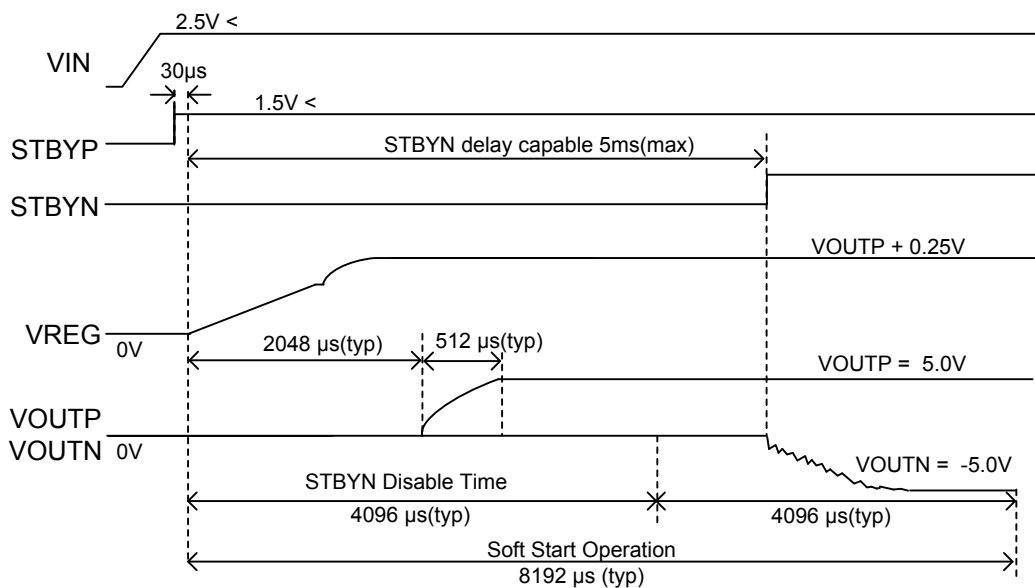


Figure 17. Power ON Sequence Timing (STBYP≠STBYN)

Recommended OFF Sequence (STBYP has same timing as STBYN)

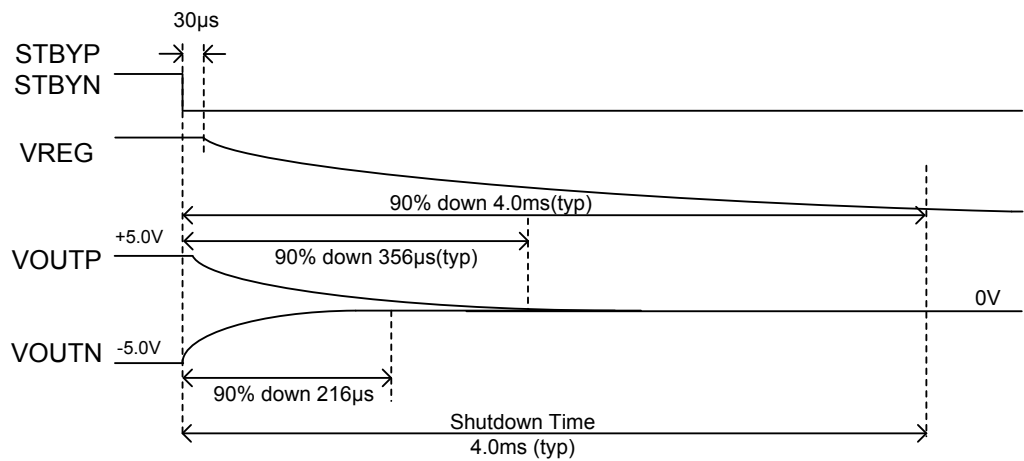


Figure 18. OFF Sequence Timing (STBYP=STBYN)

Recommended OFF Sequence

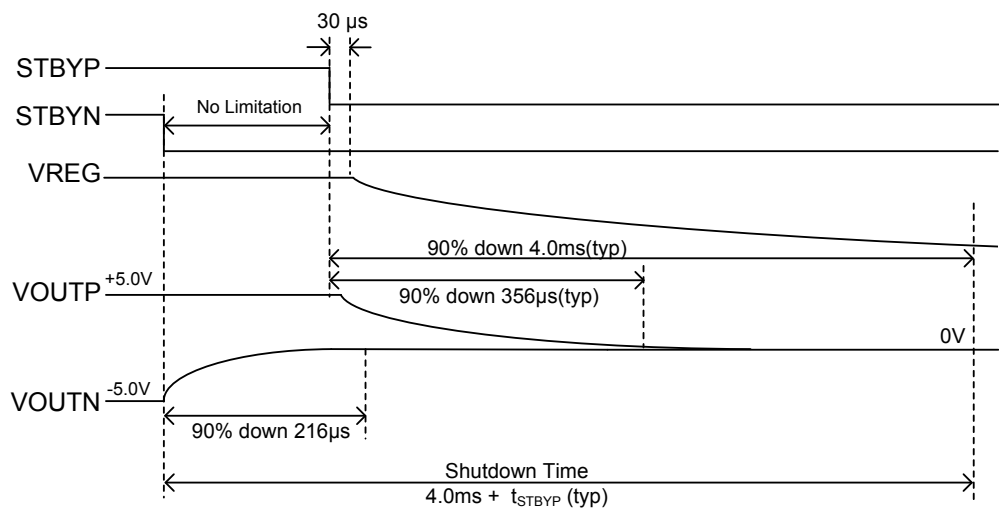


Figure 19. OFF Sequence Timing

## Application Information

### Description of Protection Circuits

#### (1) UVLO

Circuit for preventing malfunction at low voltage input.

This circuit prevents malfunction at the start of DC/DC converter operation when there is low input voltage by monitoring the voltage at VIN pin. If VIN voltage is lower than 2.2V, all DC/DC converter outputs are turned OFF, and the timer latch for soft-start circuit is reset.

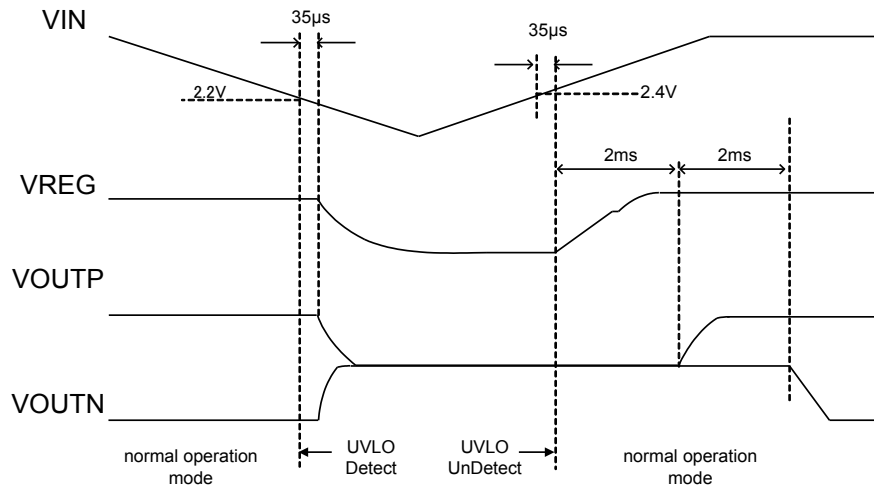


Figure 20. UVLO Detect and Release Sequence Timing

#### (2) LX OCP (BOOST CONVERTER)

Circuit for preventing malfunction at over-current.

If input inductor current being supplied by VIN exceeds rated electrical characteristics, LX Lside terminal of DC/DC converter turns OFF.

#### (3) SCP

Short-circuit protection(SCP) function based on latch system that monitor VREG voltage among ON state.

The SCP detection level will be change from 2.1V to 4.55V after Soft Start Operation. When VREG pin voltage is lower than the SCP detection level, the internal SCP circuit turns OFF all DC/DC converter outputs. To reset the latch output circuit, turn OFF STBYP and STBYN pins once then turn it ON or power up the supply again.

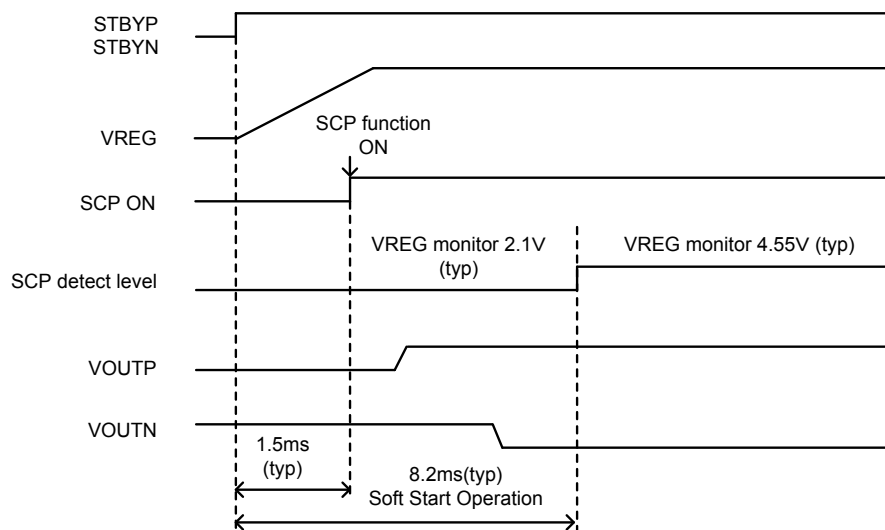


Figure 21. SCP function ON Sequence Timing

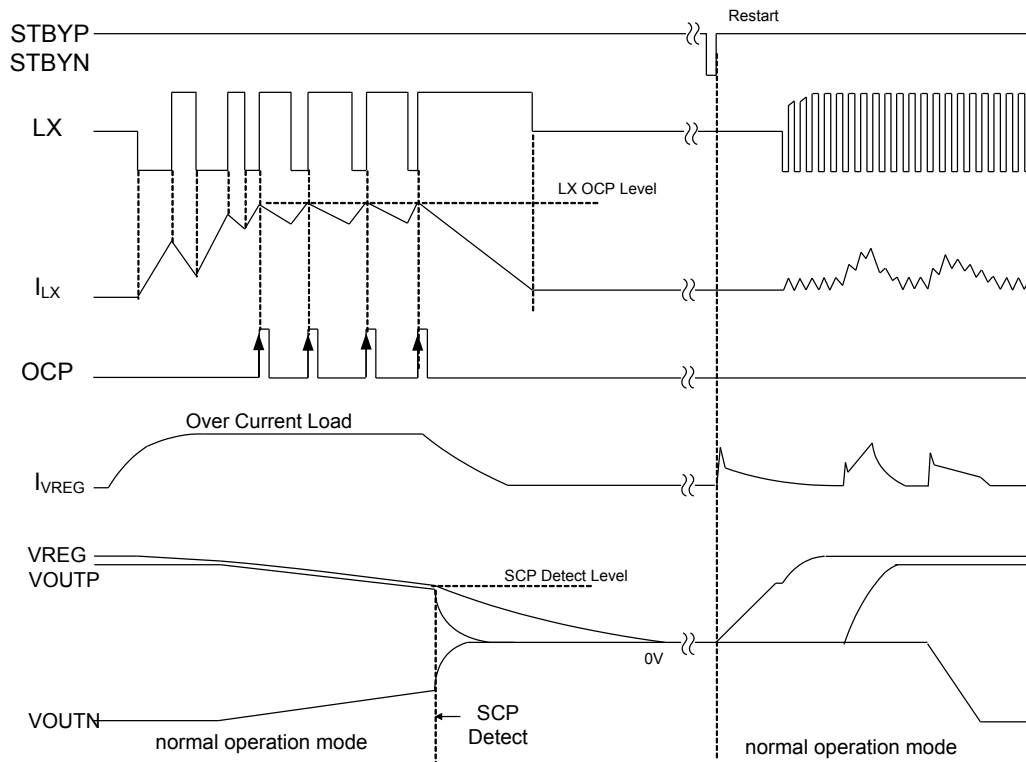


Figure 22. OCP and SCP Detect Sequence Timing

## (4) TSD

Circuit for preventing malfunction at high Temperature.

When it detects an abnormal temperature exceeding Maximum Junction Temperature ( $T_j=150^{\circ}\text{C}$ ), all outputs are turned OFF.

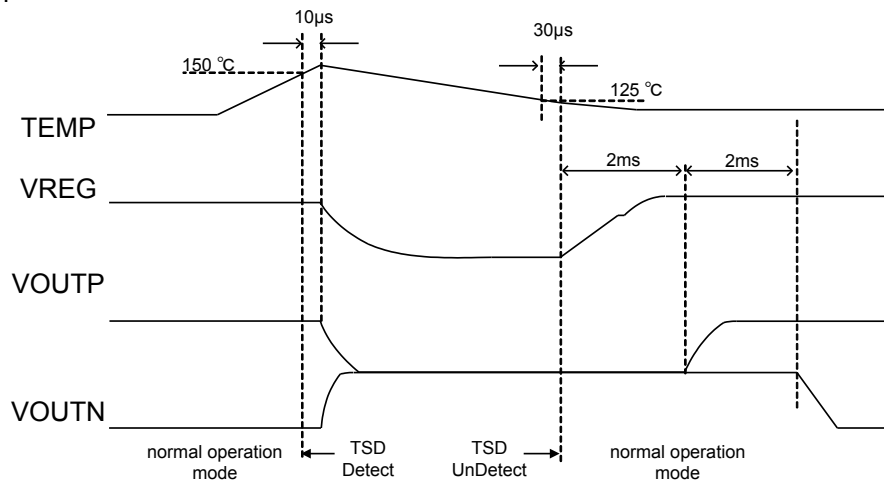


Figure 23. TSD Detect and Release Sequence Timing

## (5) VOUTP OCP (LDO)

Circuit for preventing malfunction at over-current.

If VOUTP load current exceeds 200mA, over-current protection circuit is activated and output current of LDO is decreased with respect to VOUTP voltage. If short or overload condition is removed from VOUTP, then the output returns to normal voltage regulation mode.

Application Example

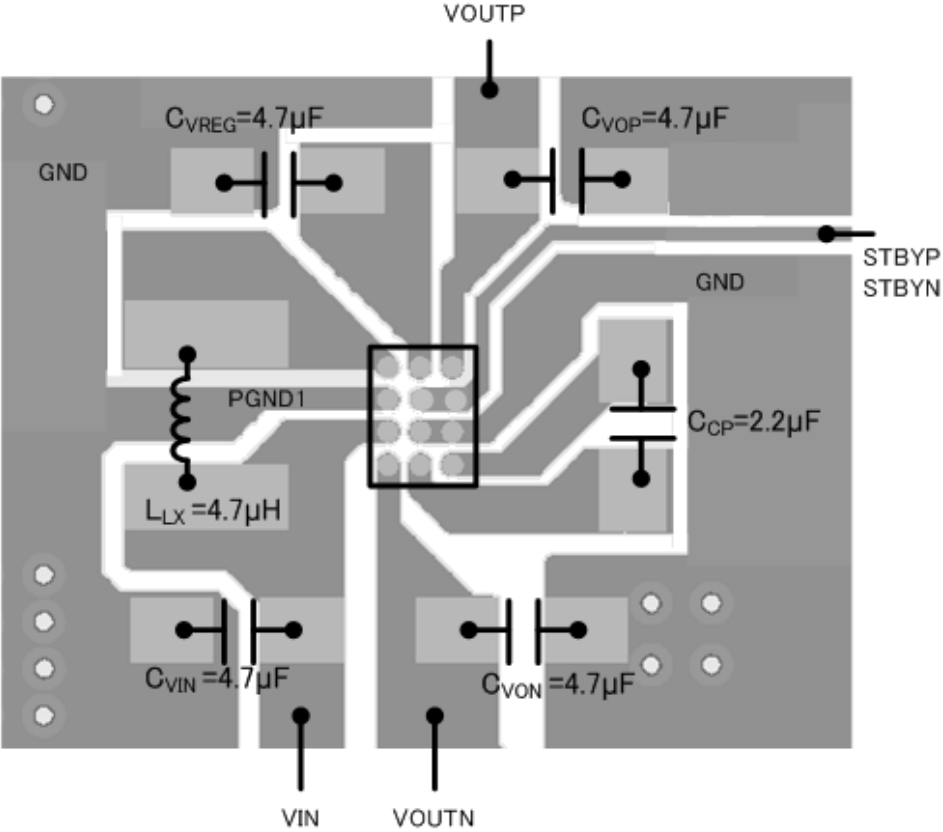


Figure 24. Suggested Layout

Selection of External Components

Table 2. Inductor Selection

| Component Code | Inductor [µH] | Vendor | EIA Size (Thickness max.) | DCR (Typ.) [Ω] |
|----------------|---------------|--------|---------------------------|----------------|
| 1269AS-H-4R7N  | 4.7           | Toko   | 1008(1.0mm)               | 0.25           |
| MLP2520V-4R7M  | 4.7           | TDK    | 1008(1.0mm)               | 0.24           |

Table 3. Capacitor Selection

| Component Code    | Capacitor [µF] | Vendor | EIA Size (Thickness max.) | Voltage Rating [V] |
|-------------------|----------------|--------|---------------------------|--------------------|
| GRM188R61C225KAAD | 2.2            | Murata | 0603 (0.9mm)              | 16                 |
| GRM188R61C475KAAJ | 4.7            | Murata | 0603 (0.9mm)              | 16                 |

## Power Dissipation

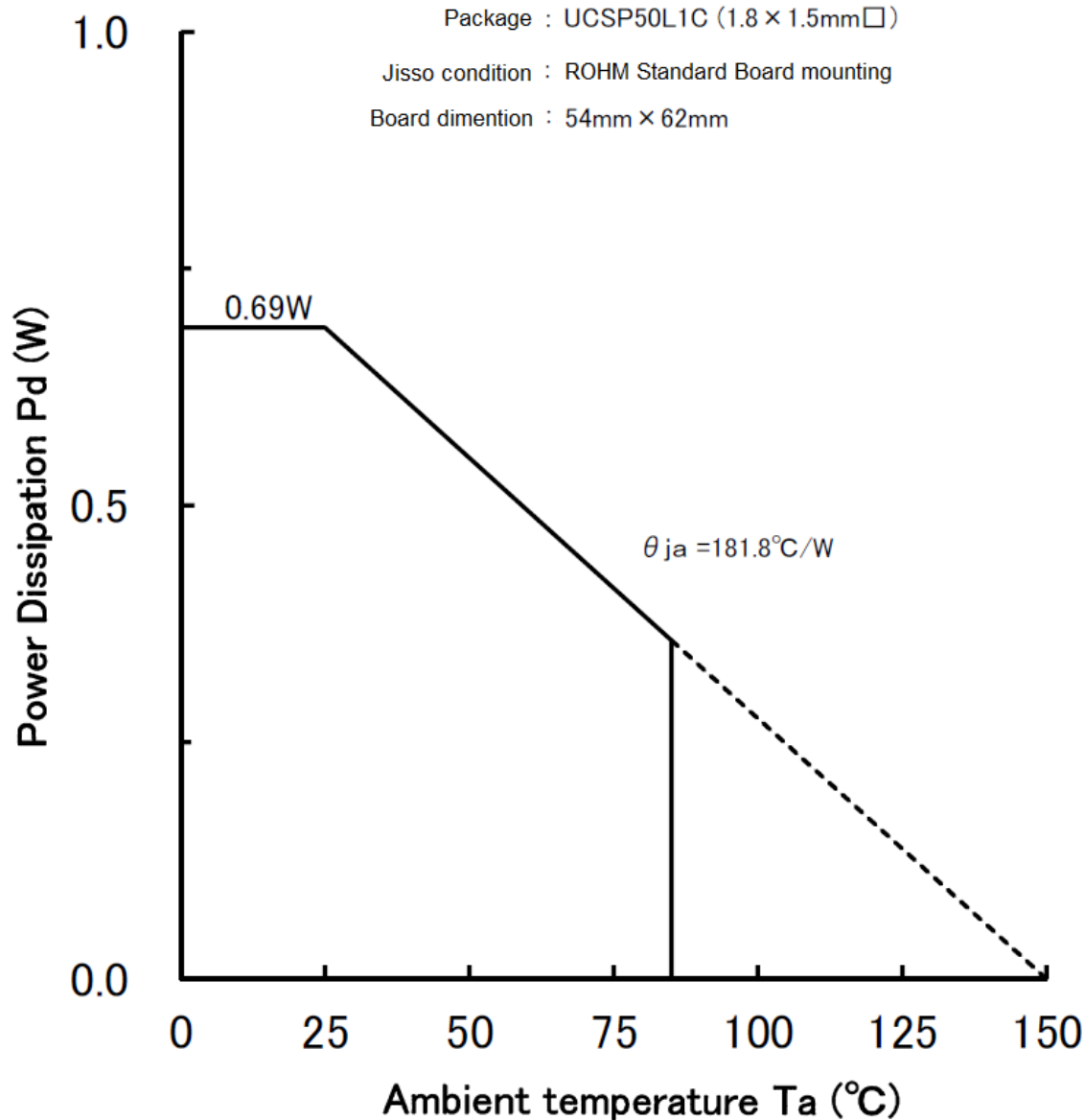
## REFERENCE DATA

## BD83850GWL

Package : UCSP50L1C (1.8 × 1.5mm□)

Jisro condition : ROHM Standard Board mounting

Board dimention : 54mm × 62mm



Notes) These values are actual measurements and are not guarantee values.

## I/O Equivalence Circuit

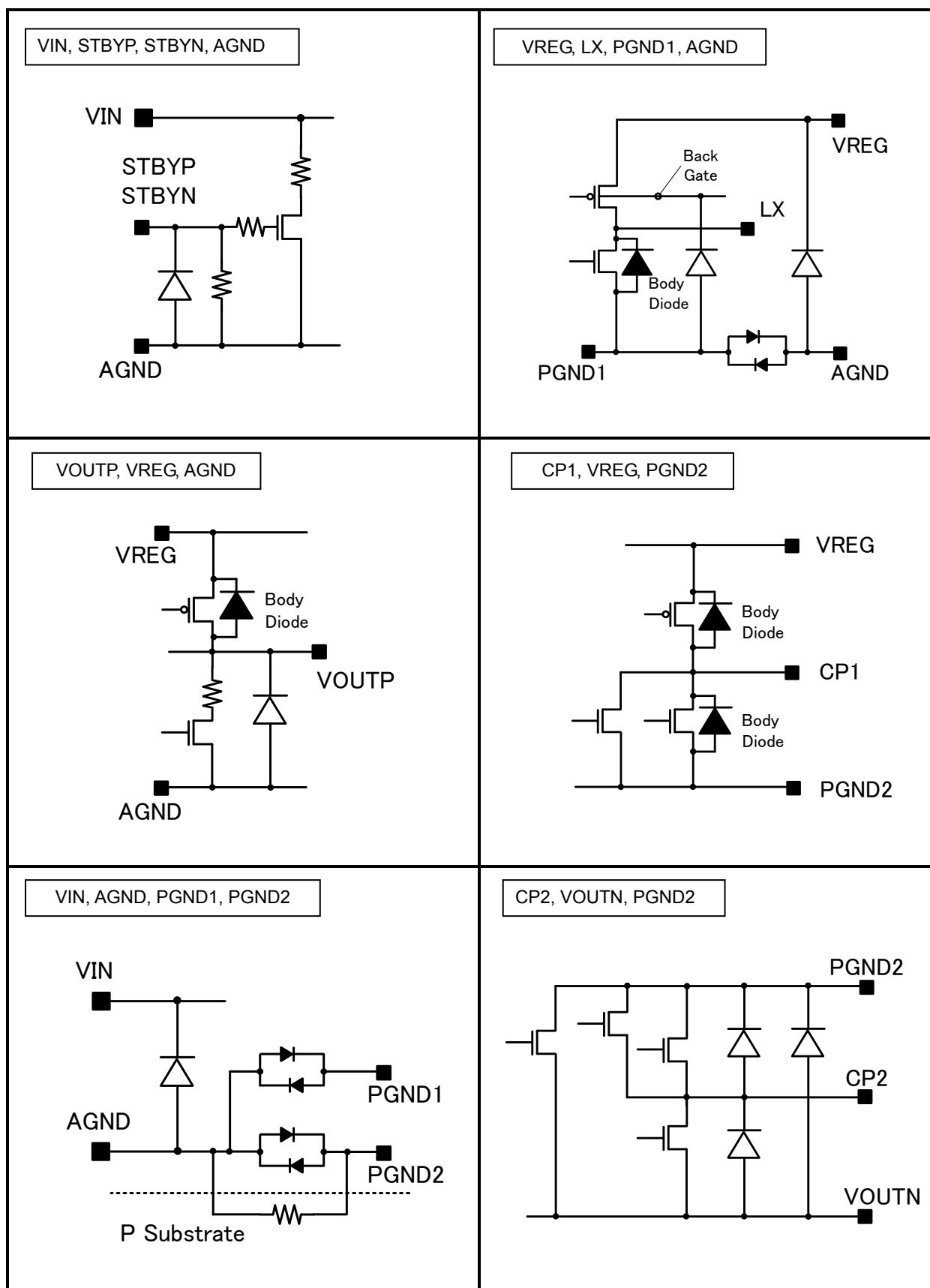


Figure 25. I/O Equivalent Circuit

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Except for pins the output the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### Operational Notes – continued

## 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## 12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin\ A$  and  $GND > Pin\ B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin\ A$  and  $GND > Pin\ B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

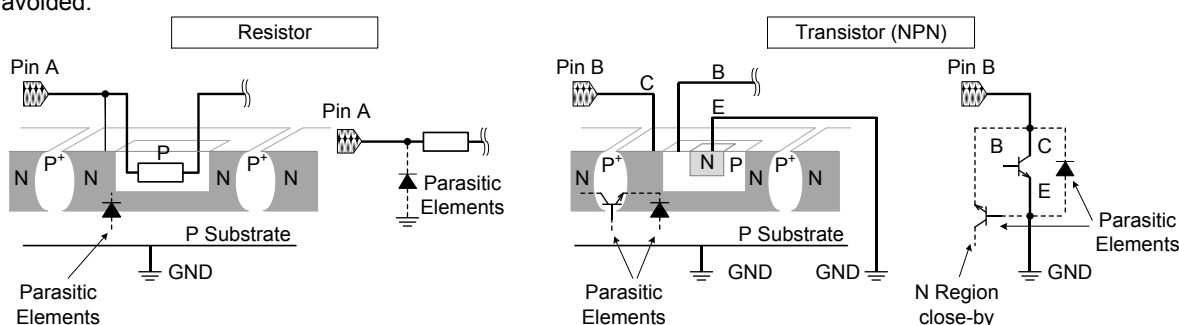


Figure 26. Example of monolithic IC structure

### 13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

#### 14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

### 15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

## 16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

## 17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information

|          |   |          |   |   |   |                          |   |   |   |                                                                   |    |
|----------|---|----------|---|---|---|--------------------------|---|---|---|-------------------------------------------------------------------|----|
| B        | D | 8        | 3 | 8 | 5 | 0                        | G | W | L | -                                                                 | E2 |
| Part No. |   | Part No. |   |   |   | Package<br>MUV:UCSP50L1C |   |   |   | Packaging and forming specification<br>E2: Embossed tape and reel |    |

Physical Dimension, Tape and Reel Information

|              |                       |
|--------------|-----------------------|
| Package Name | UCSP50L1C(BD83850GWL) |
|--------------|-----------------------|

Unit: mm

|                               |                                                                                                                                                  |
|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| < Tape and Reel Information > |                                                                                                                                                  |
| Tape                          | Embossed carrier tape                                                                                                                            |
| Quantity                      | 3,000 pcs                                                                                                                                        |
| Direction of feed             | E2<br>The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand |

Revision History

| Date        | Revision | Changes     |
|-------------|----------|-------------|
| 28.Jan.2015 | 001      | New Release |

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(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN     | USA       | EU         | CHINA     |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV  |           | CLASS III  |           |

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  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

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## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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