

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC4051AP, TC74HC4051AF, TC74HC4051AFT TC74HC4052AP, TC74HC4052AF, TC74HC4052AFT TC74HC4053AP, TC74HC4053AF, TC74HC4053AFT

TC74HC4051AP/AF/AFT

8-Channel Analog
Multiplexer/Demultiplexer

TC74HC4052AP/AF/AFT

Dual 4-Channel Analog
Multiplexer/Demultiplexer

TC74HC4053AP/AF/AFT

Triple 2-Channel Analog
Multiplexer/Demultiplexer

The TC74HC4051A/4052A/4053A are high speed CMOS ANALOG MULTIPLEXER/DEMUTIPLEXER fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4051A has an 8 channel configuration, the TC74HC4052A has a 4 channel × 2 configuration and the TC74HC4053A has a 2 channel × 3 configuration.

The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal ($V_{CC} - V_{EE}$) can then be switched by the small logical amplitude ($V_{CC} - GND$) control signal.

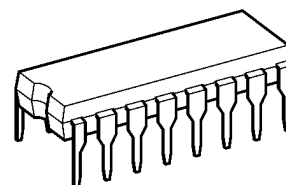
For example, in the case of $V_{CC} = 5\text{ V}$, $GND = 0\text{ V}$, $V_{EE} = -5\text{ V}$, signals between -5 V and $+5\text{ V}$ can be switched from the logical circuit with a single power supply of 5 V . As the ON-resistance of each switch is low, they can be connected to circuits with low input impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

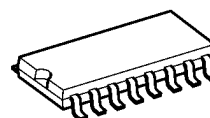
- High speed: $t_{pd} = 15\text{ ns}$ (typ.) at $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$
- Low power dissipation: $I_{CC} = 4\text{ }\mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Low ON resistance: $R_{ON} = 50\text{ }\Omega$ (typ.) at $V_{CC} - V_{EE} = 9\text{ V}$
- High noise immunity: $THD = 0.02\%$ (typ.) at $V_{CC} - V_{EE} = 9\text{ V}$
- Pin and function compatible with 4051/4052/4053B

TC74HC4051AP, TC74HC4052AP,
TC74HC4053AP



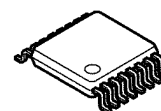
DIP16-P-300-2.54A

TC74HC4051AF, TC74HC4052AF,
TC74HC4053AF



SOP16-P-300-1.27A

TC74HC4051AFT, TC74HC4052AFT,
TC74HC4053AFT



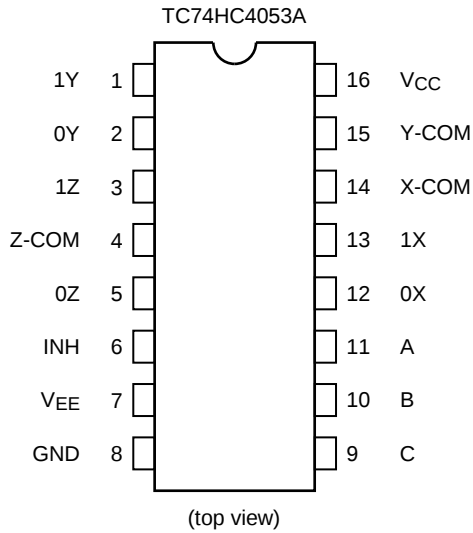
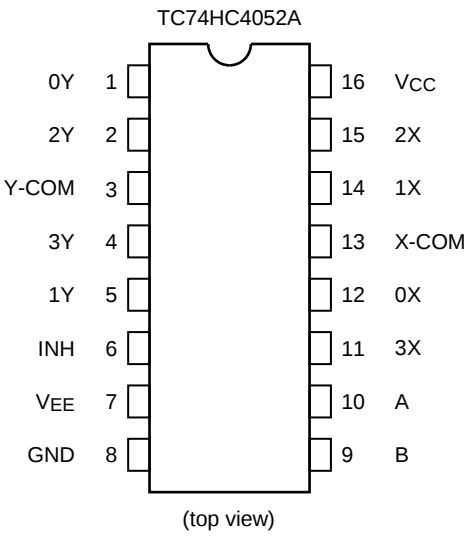
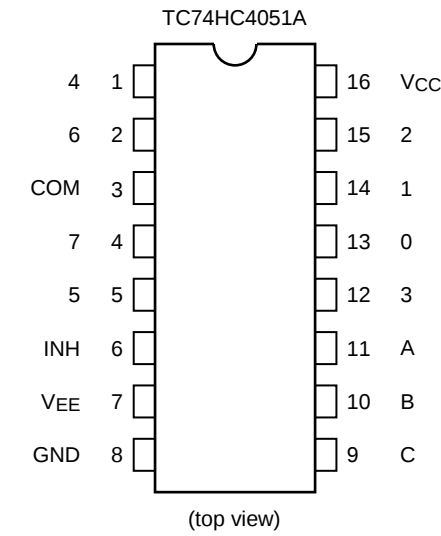
TSSOP16-P-0044-0.65A

Weight

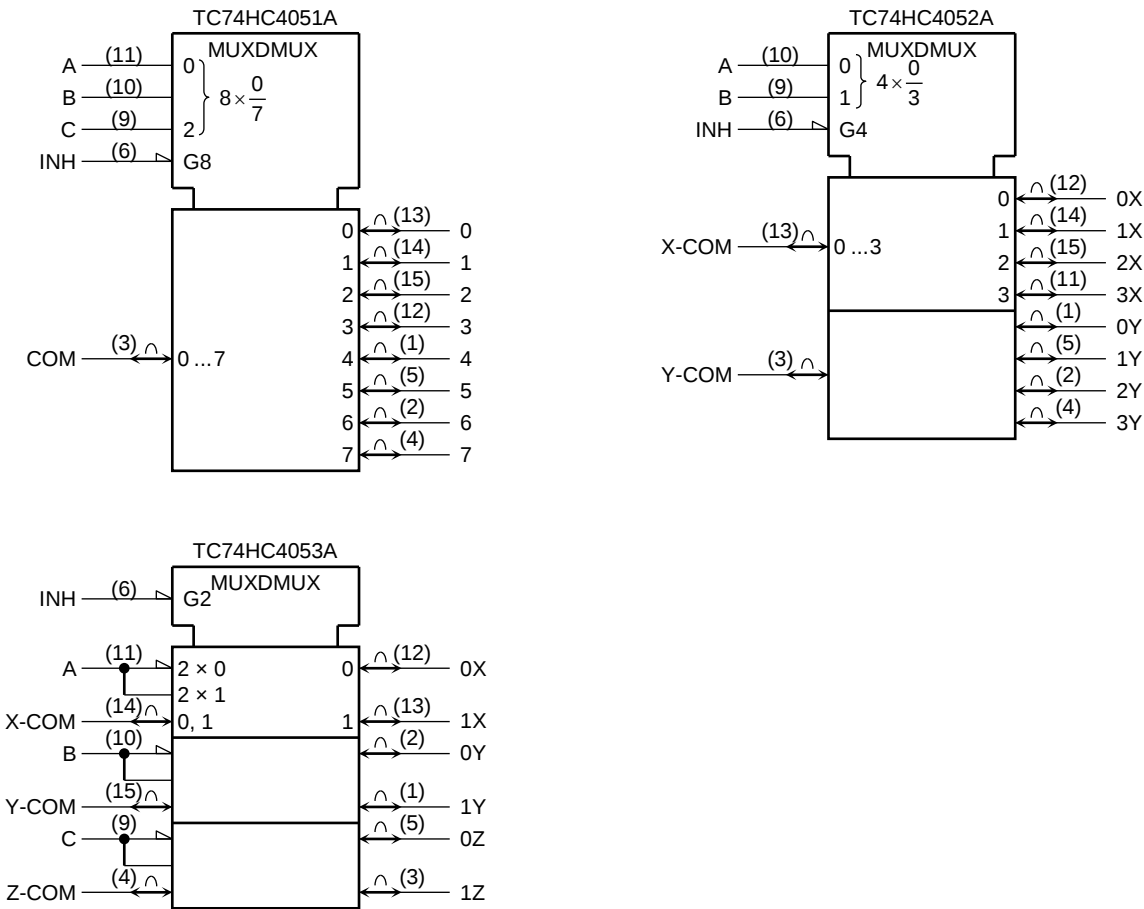
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)

Start of commercial production
1986-05

Pin Assignment



IEC Logic Symbol



Truth Table

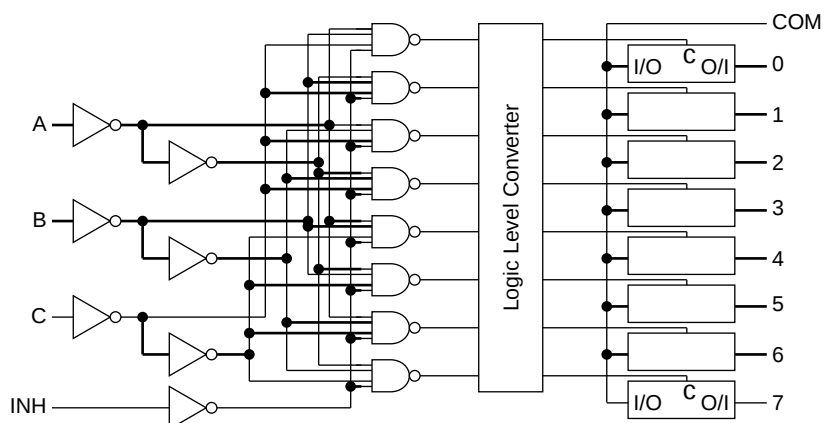
Control Inputs				“ON” Channel		
Inhibit	C*	B	A	HC4051A	HC4052A	HC4053A
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	X	X	X	None	None	None

X: Don't care

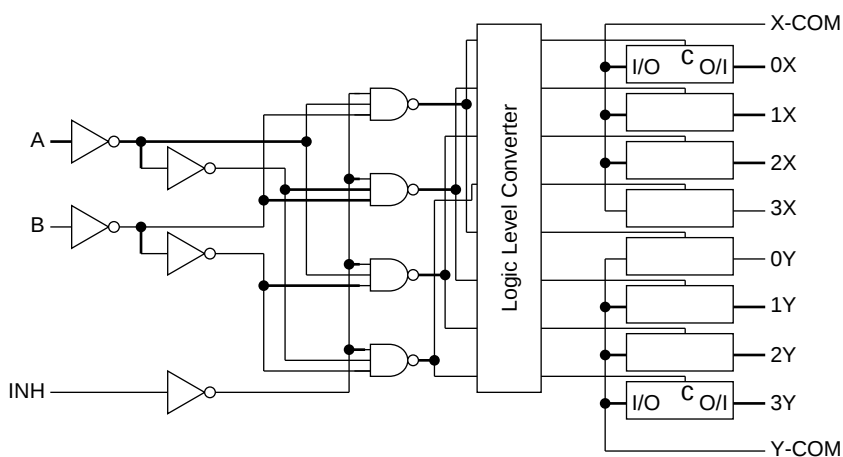
*: Except HC4052A

System Diagram

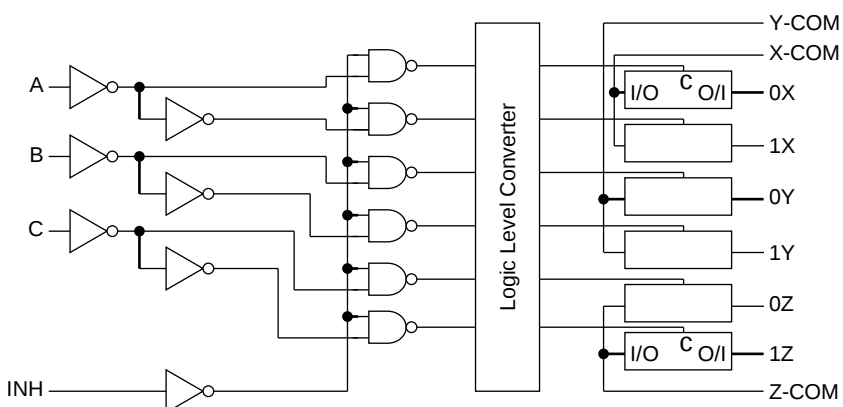
TC74HC4051A



TC74HC4052A



TC74HC4053A



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
Supply voltage range	$V_{CC}-V_{EE}$	-0.5 to 13	V
Control input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Switch I/O voltage	$V_{I/O}$	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
Control input diode current	I_{CK}	± 20	mA
I/O diode current	I_{IOK}	± 20	mA
Switch through current	I_T	± 25	mA
DC V_{CC} or ground current	I_{CC}	± 50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of $-10 \text{ mW}/^\circ\text{C}$ should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	2 to 6	V
Supply voltage range	V_{EE}	-6 to 0	V
Supply voltage range	$V_{CC}-V_{EE}$	2 to 12	V
Control input voltage	V_{IN}	0 to V_{CC}	V
Switch I/O voltage	$V_{I/O}$	V_{EE} to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Control input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0 \text{ V}$) 0 to 500 ($V_{CC} = 4.5 \text{ V}$) 0 to 400 ($V_{CC} = 6.0 \text{ V}$)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused control inputs must be tied to either V_{CC} or GND.

Electrical Characteristics
DC Characteristics

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit	
			V _{EE} (V)	V _{CC} (V)	Min	Typ.	Max	Min	Max		
High-level control input voltage	V _{IHC}	—			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low-level control input voltage	V _{ILC}	—			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
ON resistance	R _{ON}	V _{IN} = V _{ILC} or V _{IHC}	GND	4.5	—	85	180	—	225	Ω	
		V _{I/O} = V _{CC} to V _{EE}	-4.5	4.5	—	55	120	—	150		
		I _{I/O} ≤ 2 mA	-6.0	6.0	—	50	100	—	125		
		V _{IN} = V _{ILC} or V _{IHC}	GND	2.0	—	150	—	—	—		
		V _{I/O} = V _{CC} or V _{EE}	GND	4.5	—	70	150	—	190		
		I _{I/O} ≤ 2 mA	-4.5	4.5	—	50	100	—	125		
Difference of ON resistance between switches	ΔR _{ON}	V _{IN} = V _{ILC} or V _{IHC}	GND	4.5	—	10	30	—	35	Ω	
		V _{I/O} = V _{CC} to V _{EE}	-4.5	4.5	—	5	12	—	15		
		I _{I/O} ≤ 2 mA	-6.0	6.0	—	5	10	—	12		
Input/output leakage current (switch off)	I _{OFF}	V _{OS} = V _{CC} or GND V _{IS} = GND or V _{CC} V _{IN} = V _{ILC} or V _{IHC}	GND -6.0	6.0 6.0	— —	— —	±60 ±100	— —	±600 ±1000	nA	
Switch input leakage current (switch on, output open)	I _{IZ}	V _{OS} = V _{CC} or GND V _{IN} = V _{ILC} or V _{IHC}	GND -6.0	6.0 6.0	— —	— —	±60 ±100	— —	±600 ±1000	nA	
Control input current	I _{IN}	V _{IN} = V _{CC} or GND	GND	6.0	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	GND -6.0	6.0 6.0	— —	— —	4.0 8.0	— —	40.0 80.0	μA	

AC Characteristics (CL = 50 pF, input: tr = tf = 6 ns, GND = 0 V)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{EE} (V)	V _{CC} (V)	Min	Typ.	Max	Min	Max	
Phase difference between input and output	φ _{I/O}	All types	GND	2.0	—	25	60	—	75	ns
			GND	4.5	—	6	12	—	15	
			GND	6.0	—	5	10	—	13	
			-4.5	4.5		4	—	—	—	
Output enable time	t _{pZL} t _{pZH}	4051A (Note 1)	GND	2.0	—	64	225	—	280	ns
			GND	4.5	—	18	45	—	56	
			GND	6.0	—	15	38	—	48	
			-4.5	4.5		18	—	—	—	
		4052A (Note 1)	GND	2.0	—	64	225	—	280	
			GND	4.5	—	18	45	—	56	
			GND	6.0	—	15	38	—	48	
			-4.5	4.5		18	—	—	—	
		4053A (Note 1)	GND	2.0	—	50	225	—	280	
			GND	4.5	—	14	45	—	56	
			GND	6.0	—	12	38	—	48	
			-4.5	4.5		14	—	—	—	
Output disable time	t _{pLZ} t _{pHZ}	4051A (Note 1)	GND	2.0	—	100	250	—	315	ns
			GND	4.5	—	33	50	—	63	
			GND	6.0	—	28	43	—	54	
			-4.5	4.5		29	—	—	—	
		4052A (Note 1)	GND	2.0	—	100	250	—	315	
			GND	4.5	—	33	50	—	63	
			GND	6.0	—	28	43	—	54	
			-4.5	4.5		29	—	—	—	
		4053A (Note 1)	GND	2.0	—	95	225	—	280	
			GND	4.5	—	30	45	—	56	
			GND	6.0	—	26	38	—	48	
			-4.5	4.5		26	—	—	—	
Control input capacitance	C _{IN}	All types	—	—	—	5	10	—	10	pF
COMMON terminal capacitance	C _{IS}	4051A			—	36	70	—	70	pF
		4052A	-5.0	5.0	—	19	40	—	40	
		4053A			—	11	20	—	20	
SWITCH terminal capacitance	C _{OS}	4051A			—	7	15	—	15	pF
		4052A	-5.0	5.0	—	7	15	—	15	
		4053A			—	7	15	—	15	
Feedthrough capacitance	C _{IOS}	4051A			—	0.95	2	—	2	pF
		4052A	-5.0	5.0	—	0.85	2	—	2	
		4053A			—	0.75	2	—	2	
Power dissipation capacitance	C _{PD}	4051A (Note 2)			—	70	—	—	—	pF
		4052A (Note 2)	GND	5.0	—	71	—	—	—	
		4053A (Note 2)			—	67	—	—	—	

Note 1: RL = 1 kΩ

Note 2: CPD is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

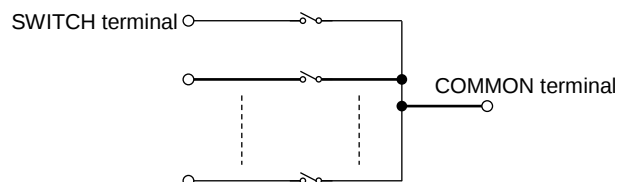
Analog Switch Characteristics (GND = 0 V, Ta = 25°C) (Note 1)

Characteristics	Symbol	Test Condition				Typ.	Unit
			V _{EE} (V)	V _{CC} (V)			
Sine wave distortion (T.H.D)		R _L = 10 kΩ,	V _{IN} = 4.0 V _{p-p}	-2.25	2.25	0.025	%
		C _L = 50 pF	V _{IN} = 8.0 V _{p-p}	-4.5	4.5	0.020	
		f _{IN} = 1 kHz	V _{IN} = 11.0 V _{p-p}	-6.0	6.0	0.018	
Frequency response (switch on)	f _{max}	Adjust f _{IN} voltage to obtain 0dBm at V _{OS} Increase f _{IN} frequency until dB meter reads -3dB R _L = 50 Ω, C _L = 10 pF f _{IN} = 1 MHz, sine wave	All (Note 2)	-2.25	2.25	120	MHz
			4051A (Note 3)			45	
			4052A (Note 3)			70	
			4053A (Note 3)			95	
			All (Note 2)	-4.5	4.5	190	
			4051A (Note 3)			70	
			4052A (Note 3)			110	
			4053A (Note 3)			150	
			All (Note 2)	-6.0	6.0	200	
			4051A (Note 3)			85	
			4052A (Note 3)			140	
			4053A (Note 3)			190	
Feed through attenuation (switch off)		V _{IN} is centered at (V _{CC} - V _{EE})/2 Adjust input for 0dBm R _L = 600 Ω, C _L = 50 pF f _{IN} = 1 MHz, sine wave	-2.25	2.25	-50	dB	
			-4.5	4.5	-50		
			-6.0	6.0	-50		
Crosstalk (control input to signal output)		R _L = 600 Ω, C _L = 50 pF f _{IN} = 1 MHz, square wave (t _r = t _f = 6 ns)	-2.25	2.25	60	mV	
			-4.5	4.5	140		
			-6.0	6.0	200		
Crosstalk (between any switches)		Adjust V _{IN} to obtain 0dBm at input R _L = 600 Ω, C _L = 50 pF f _{IN} = 1 MHz, sine wave	-2.25	2.25	-50	dB	
			-4.5	4.5	-50		
			-6.0	6.0	-50		

Note 1: These characteristics are determined by design of devices.

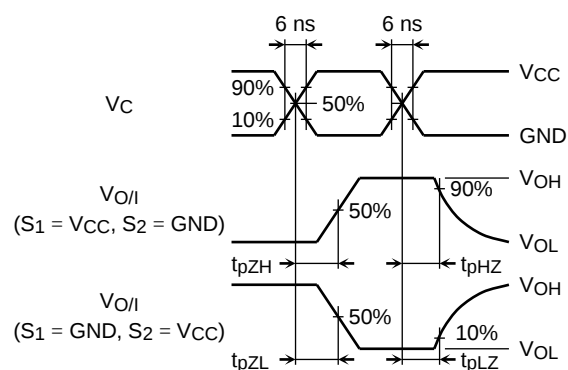
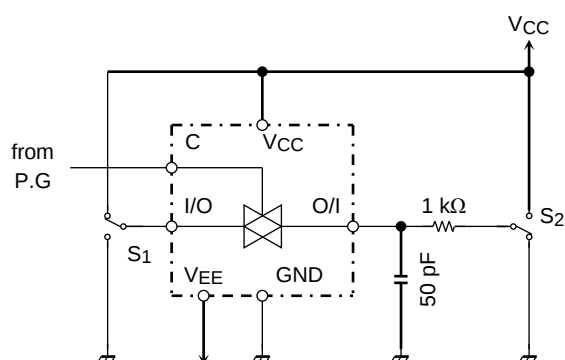
Note 2: Input COMMON terminal, and measured at SWITCH terminal.

Note 3: Input SWITCH terminal, and measured at COMMON terminal.

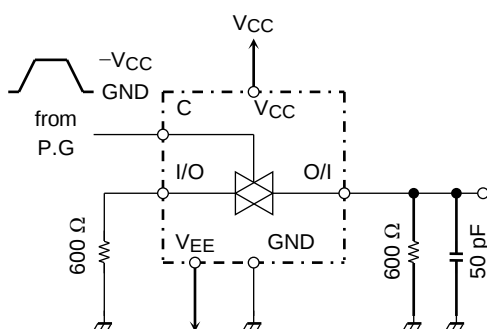


Switching Characteristics Test Circuits

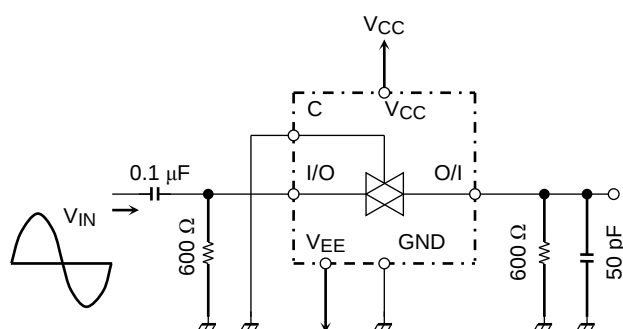
1. t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}



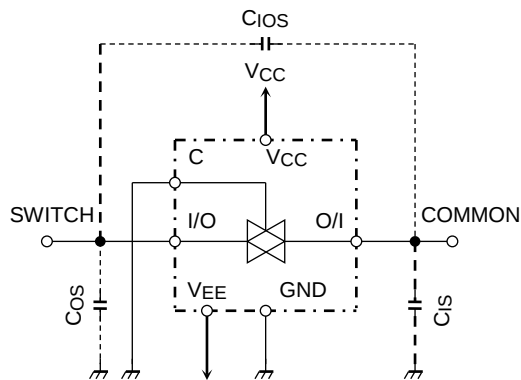
2. Cross Talk (control input-switch output) $f_{IN} = 1$ MHz duty = 50% $t_r = t_f = 6$ ns



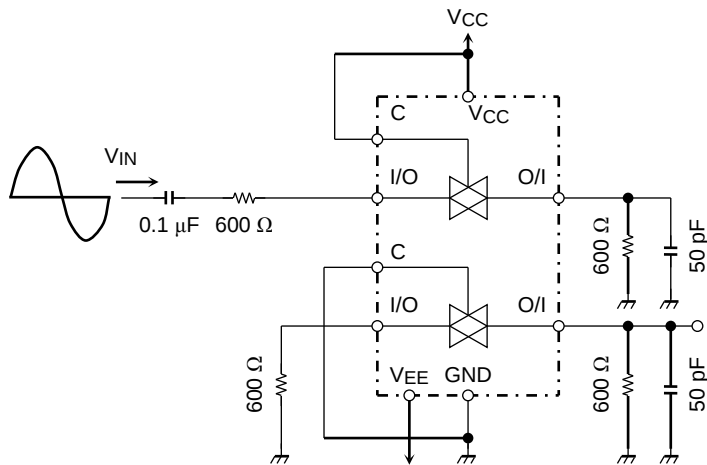
3. Feedthrough Attenuation



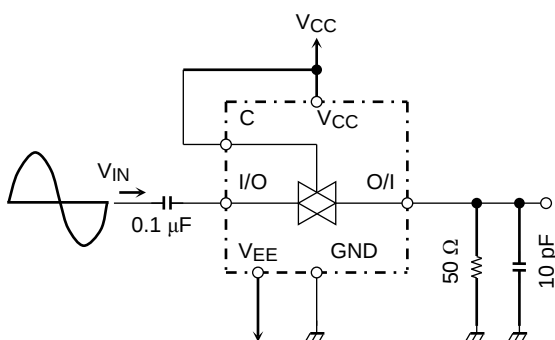
4. Cios, Cis, Cos



5. Cross Talk (between any two switches)



6. Frequency Response (switch on)



DIP16-P-300-2.54A

Technical drawing of the 16-pin connector showing three views: top, side, and pin detail.

Top View: Shows a rectangular connector with 16 pins (8 on each side). Pin numbers 1, 8, 9, and 16 are indicated. The width is 6.4 ± 0.2 .

Side View: Shows the profile of the connector. The height is 7.62 . The pins are angled at $0 \sim 15^\circ$. The pin thickness is $0.25^{+0.1}_{-0.05}$.

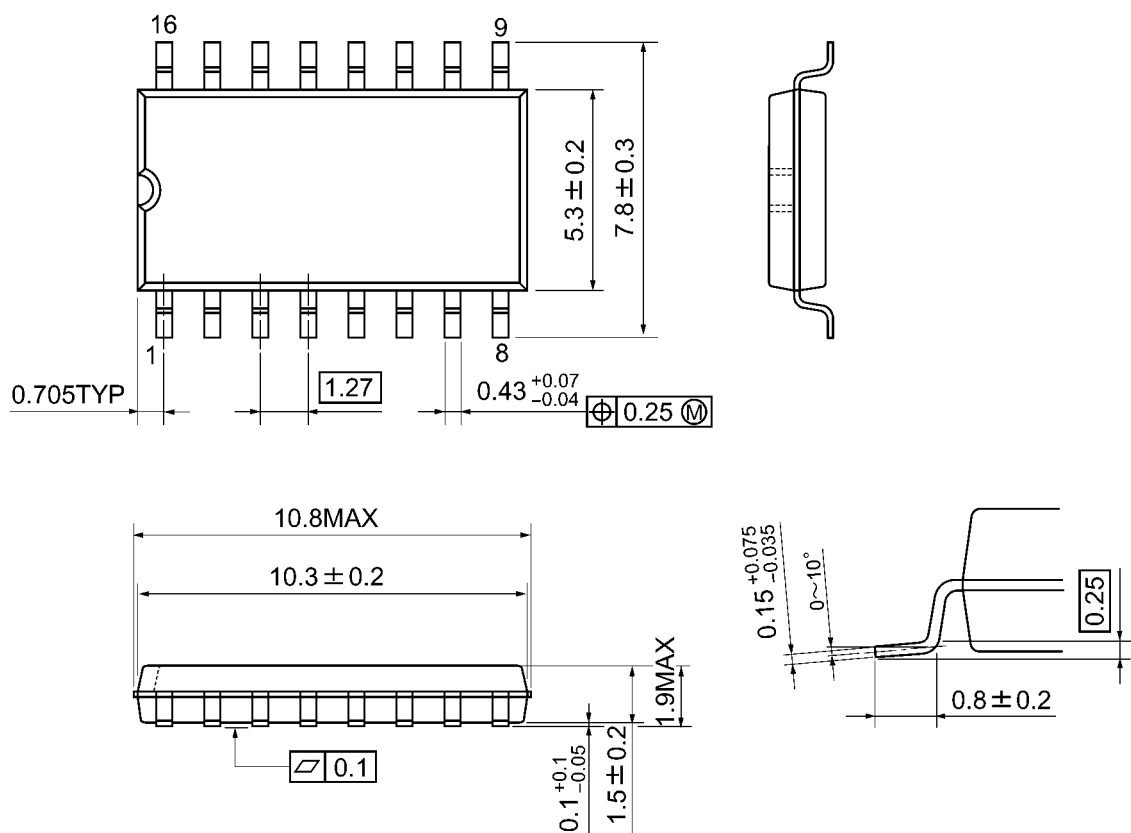
Pin Detail View: Shows the dimensions of the pins. The total length is 19.75 MAX . The length of the pin body is 19.25 ± 0.2 . The pin diameter is 0.95 ± 0.1 . The pin thickness is 0.735 TYP . The pin pitch is 2.54 . The pin length from the base to the tip is 1.4 ± 0.1 . The pin thickness at the base is 0.5 ± 0.1 . The pin thickness at the base is 0.51 MIN . The pin thickness at the base is 3.5 ± 0.2 . The pin thickness at the base is 4.15 ± 0.3 . The pin thickness at the base is 3.3 ± 0.3 . The pin thickness at the base is 0.25 (M) .

2016-10-18

Package Dimensions

SOP16-P-300-1.27A

Unit: mm

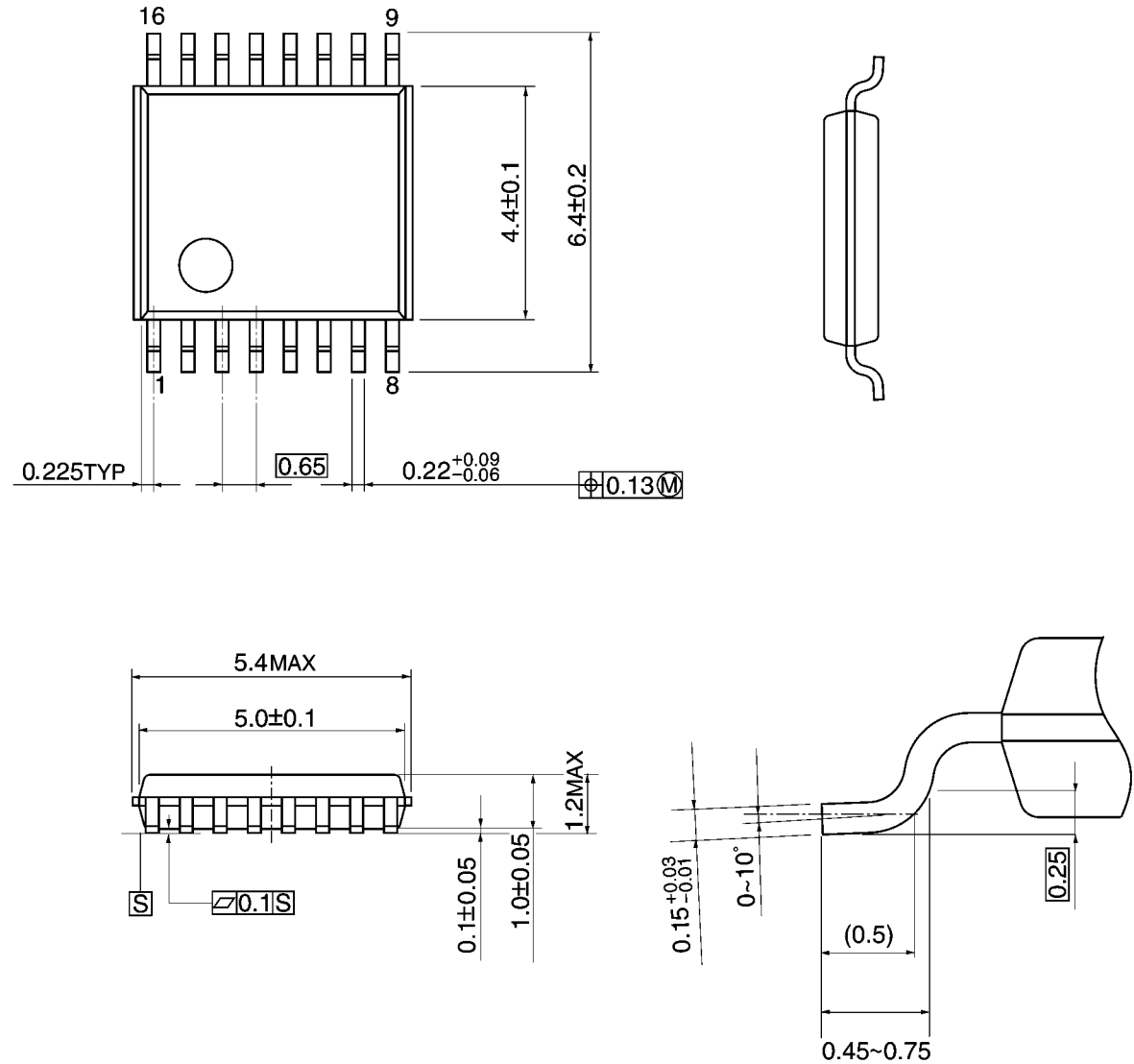


Weight: 0.18 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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