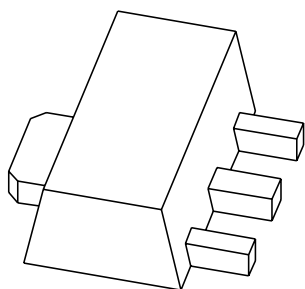


DATA SHEET



PBSS4540X

40 V, 5 A

NPN low V_{CEsat} (BISS) transistor

Product specification
Supersedes data of 2004 Jun 11

2004 Nov 04

40 V, 5 A

NPN low V_{CEsat} (BISS) transistor

PBSS4540X

FEATURES

- High h_{FE} and low V_{CEsat} at high current operation
- High collector current capability: I_C maximum 4 A
- High efficiency leading to less heat generation.

APPLICATIONS

- Medium power peripheral drivers (e.g. fan and motor)
- Strobe flash units for DSC and mobile phones
- Inverter applications (e.g. TFT displays)
- Power switch for LAN and ADSL systems
- Medium power DC-to-DC conversion
- Battery chargers.

DESCRIPTION

NPN low V_{CEsat} transistor in a medium power SOT89 (SC-62) package.

PNP complement: PBSS5540X.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PBSS4540X	*1B

Note

- * = p: made in Hong Kong.
* = t: made in Malaysia.
* = W: made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	40	V
I_C	collector current (DC)	4	A
I_{CM}	peak collector current	10	A
R_{CEsat}	equivalent on-resistance	71	mΩ

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base

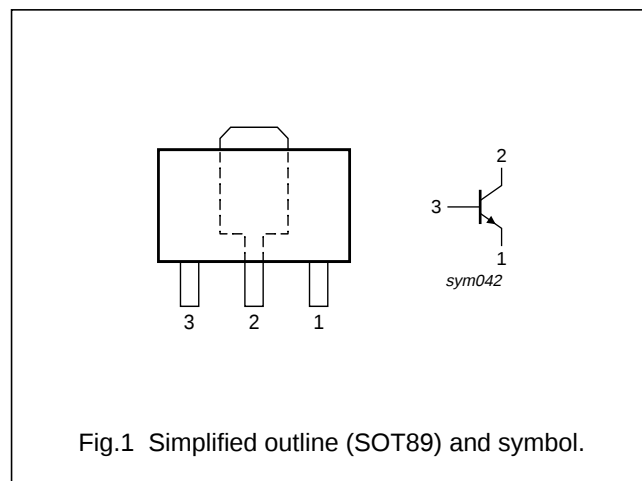


Fig.1 Simplified outline (SOT89) and symbol.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS4540X	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89

40 V, 5 A NPN low V_{CEsat} (BISS) transistor

PBSS4540X

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

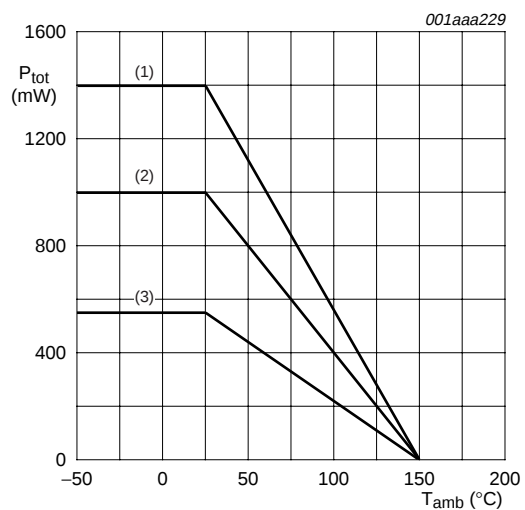
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	40	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	4	A
I_{CRM}	maximum repetitive collector current	notes 1 and 2	–	5	A
I_{CM}	peak collector current	$t_p \leq 1$ ms	–	10	A
I_B	base current (DC)		–	1	A
I_{BM}	peak base current	$t_p \leq 1$ ms	–	2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
		notes 1 and 2	–	2.5	W
		note 2	–	0.55	W
		note 3	–	1	W
		note 4	–	1.4	W
		note 5	–	1.6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Operated under pulsed conditions; pulse width $t_p \leq 10$ ms; duty cycle $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².
5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated. For other mounting conditions, see “*Thermal considerations for SOT89 in the General Part of associated Handbook*”.

40 V, 5 A
NPN low V_{CEsat} (BISS) transistor

PBSS4540X



- (1) FR4 PCB; 6 cm² mounting pad for collector.
- (2) FR4 PCB; 1 cm² mounting pad for collector.
- (3) FR4; standard footprint.

Fig.2 Power derating curves.

40 V, 5 A
NPN low V_{CEsat} (BISS) transistor

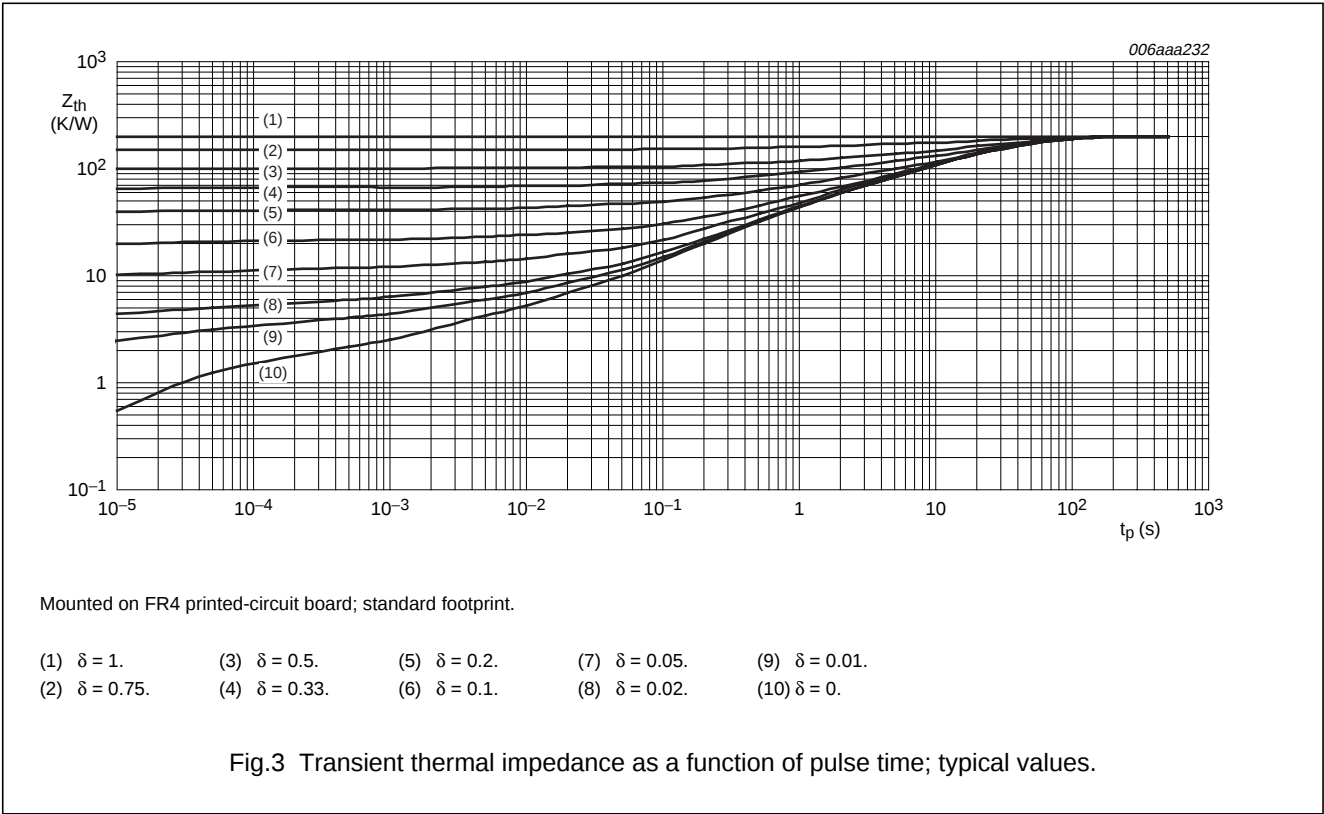
PBSS4540X

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	from junction to ambient	in free air		
		notes 1 and 2	50	K/W
		note 2	225	K/W
		note 3	125	K/W
		note 4	90	K/W
		note 5	80	K/W
$R_{th(j-s)}$	from junction to soldering point		16	K/W

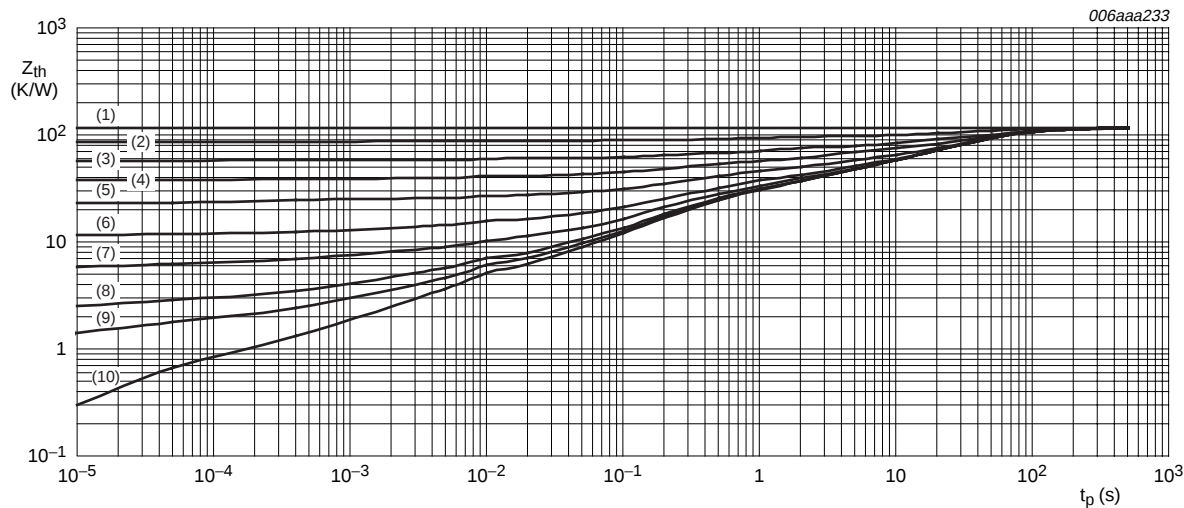
Notes

1. Operated under pulsed conditions; pulse width $t_p \leq 10$ ms; duty cycle $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².
5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated. For other mounting conditions, see “Thermal considerations for SOT89 in the General Part of associated Handbook”.



40 V, 5 A
NPN low V_{CEsat} (BISS) transistor

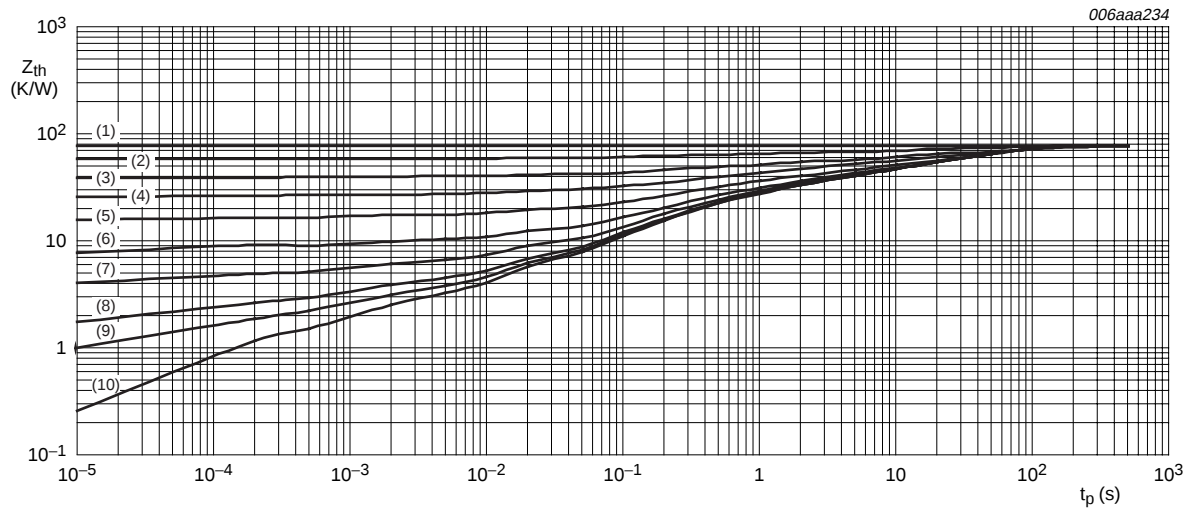
PBSS4540X



Mounted on FR4 printed-circuit board; mounting pad for collector 1 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.4 Transient thermal impedance as a function of pulse time; typical values.



Mounted on FR4 printed-circuit board; mounting pad for collector 6 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.5 Transient thermal impedance as a function of pulse time; typical values.

40 V, 5 A

NPN low V_{CEsat} (BISS) transistor

PBSS4540X

CHARACTERISTICS $T_{amb} = 25\text{ °C}$ unless otherwise specified.

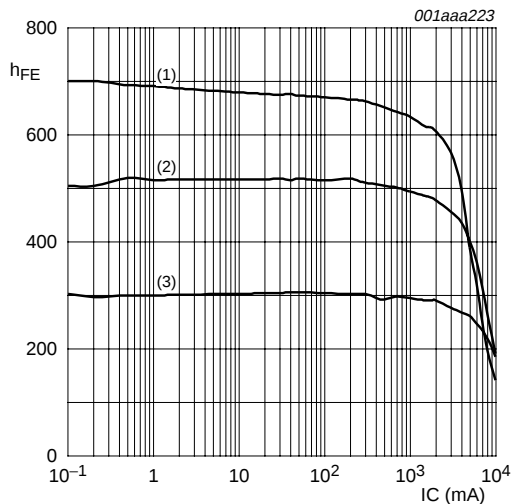
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = 30\text{ V}; I_E = 0\text{ A}$	–	–	100	nA
		$V_{CB} = 30\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ °C}$	–	–	50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; V_{BE} = 0\text{ V}$	–	–	0.1	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	–	–	100	nA
h_{FE}	DC current gain	$V_{CE} = 2\text{ V}; I_C = 0.5\text{ A}$	300	–	–	
		$V_{CE} = 2\text{ V}; I_C = 1\text{ A}; \text{note 1}$	300	–	–	
		$V_{CE} = 2\text{ V}; I_C = 2\text{ A}; \text{note 1}$	250	–	–	
		$V_{CE} = 2\text{ V}; I_C = 5\text{ A}; \text{note 1}$	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 0.5\text{ A}; I_B = 5\text{ mA}$	–	–	90	mV
		$I_C = 1\text{ A}; I_B = 10\text{ mA}$	–	–	120	mV
		$I_C = 2\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	–	–	150	mV
		$I_C = 4\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	–	–	290	mV
		$I_C = 5\text{ A}; I_B = 500\text{ mA}; \text{note 1}$	–	–	355	mV
R_{CEsat}	equivalent on-resistance	$I_C = 5\text{ A}; I_B = 500\text{ mA}; \text{note 1}$	–	40	71	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = 4\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	–	–	1.1	V
		$I_C = 5\text{ A}; I_B = 500\text{ mA}; \text{note 1}$	–	–	1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 2\text{ V}; I_C = 2\text{ A}$	–	–	1.1	V
f_T	transition frequency	$V_{CE} = 10\text{ V}; I_C = 0.1\text{ A};$ $f = 100\text{ MHz}$	70	–	–	MHz
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = I_C = 0\text{ A};$ $f = 1\text{ MHz}$	–	–	75	pF

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

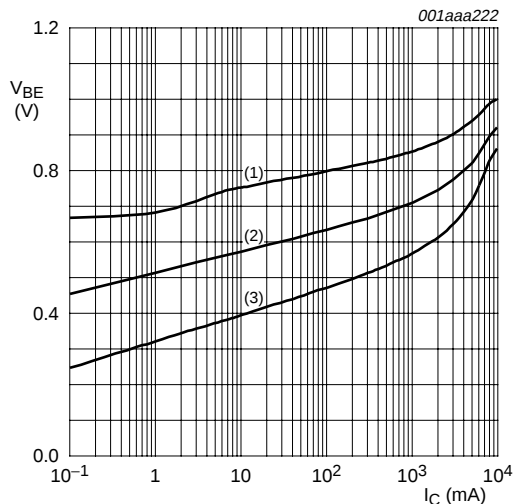
40 V, 5 A
NPN low V_{CEsat} (BISS) transistor

PBSS4540X



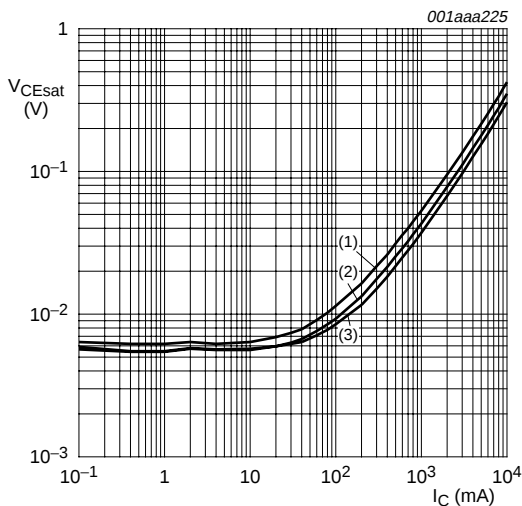
$V_{CE} = 2\text{ V}$.
(1) $T_{amb} = 100^\circ\text{C}$.
(2) $T_{amb} = 25^\circ\text{C}$.
(3) $T_{amb} = -55^\circ\text{C}$.

Fig.6 DC current gain as a function of collector current; typical values.



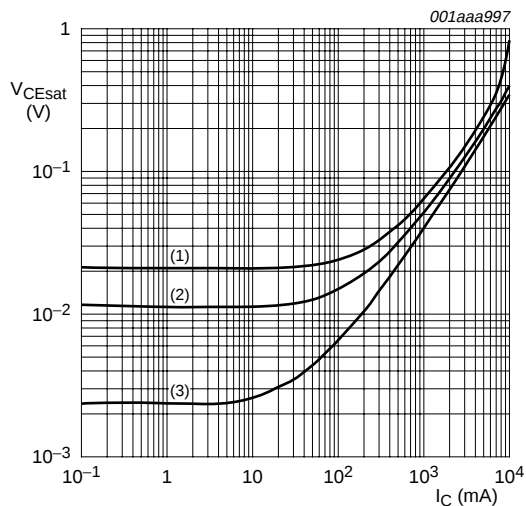
$V_{CE} = 2\text{ V}$.
(1) $T_{amb} = 55^\circ\text{C}$.
(2) $T_{amb} = 25^\circ\text{C}$.
(3) $T_{amb} = 100^\circ\text{C}$.

Fig.7 Base-emitter voltage as a function of collector current; typical values.



$I_C/I_B = 20$.
(1) $T_{amb} = 100^\circ\text{C}$.
(2) $T_{amb} = 25^\circ\text{C}$.
(3) $T_{amb} = -55^\circ\text{C}$.

Fig.8 Collector-emitter saturation voltage as a function of collector current; typical values.

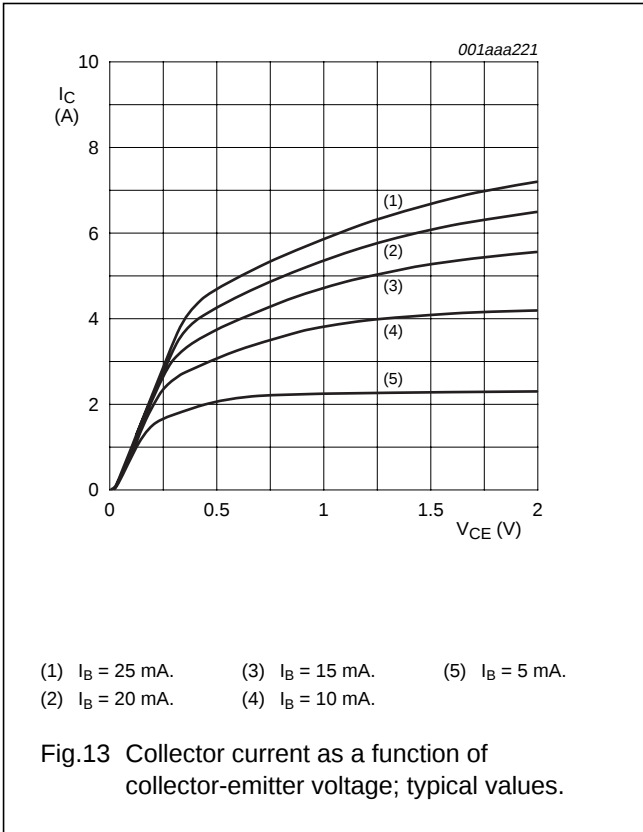
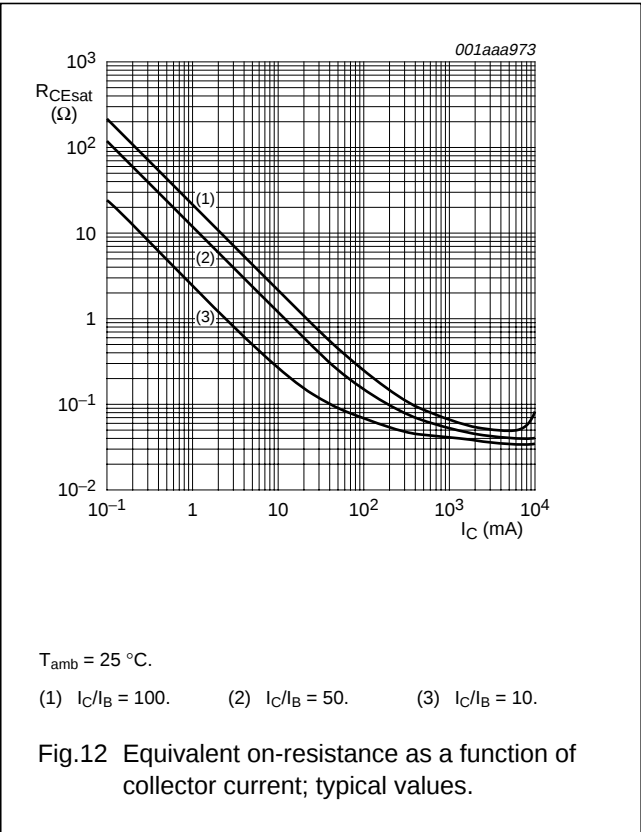
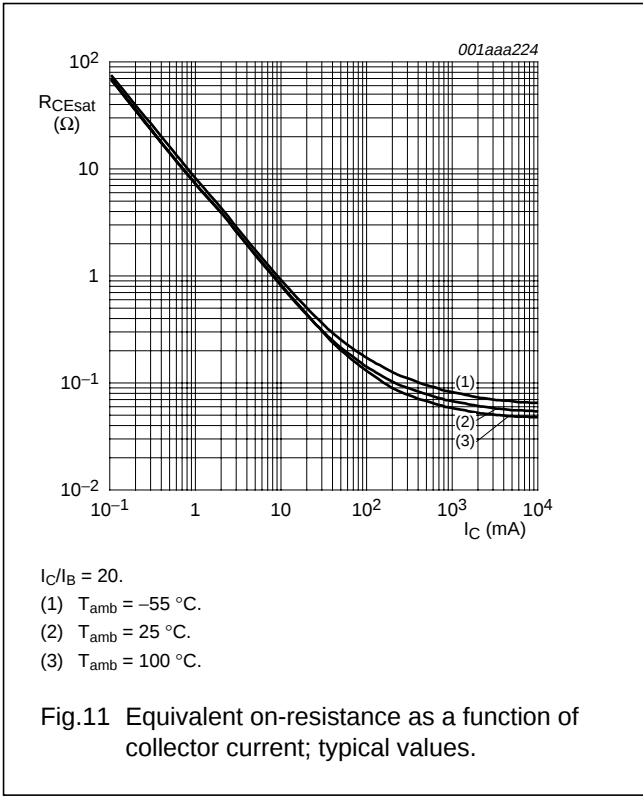
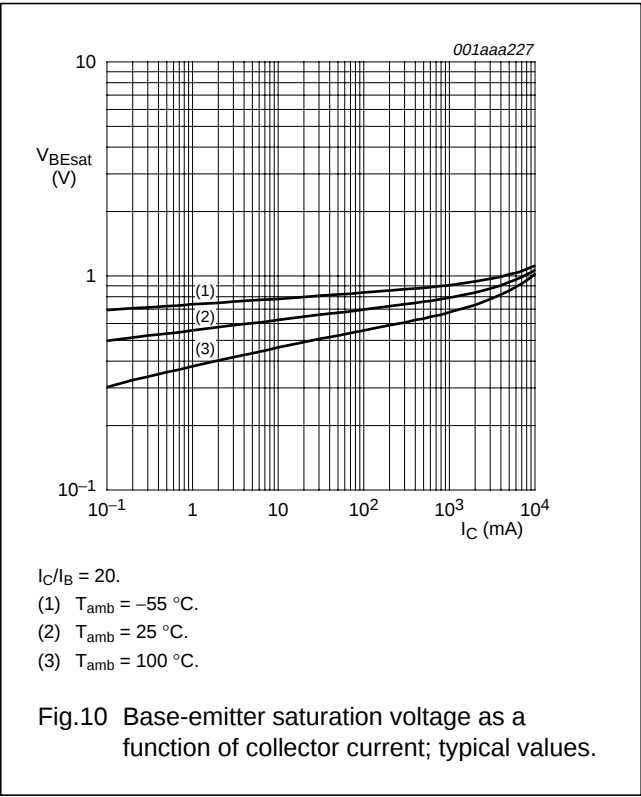


$T_{amb} = 25^\circ\text{C}$.
(1) $I_C/I_B = 100$.
(2) $I_C/I_B = 50$.
(3) $I_C/I_B = 10$.

Fig.9 Collector-emitter saturation voltage as a function of collector current; typical values.

40 V, 5 A
NPN low V_{CEsat} (BISS) transistor

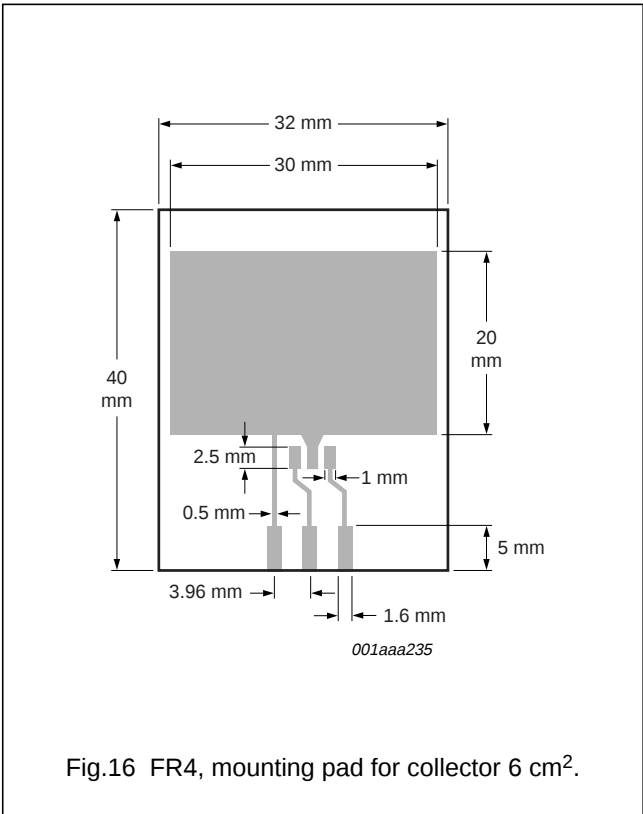
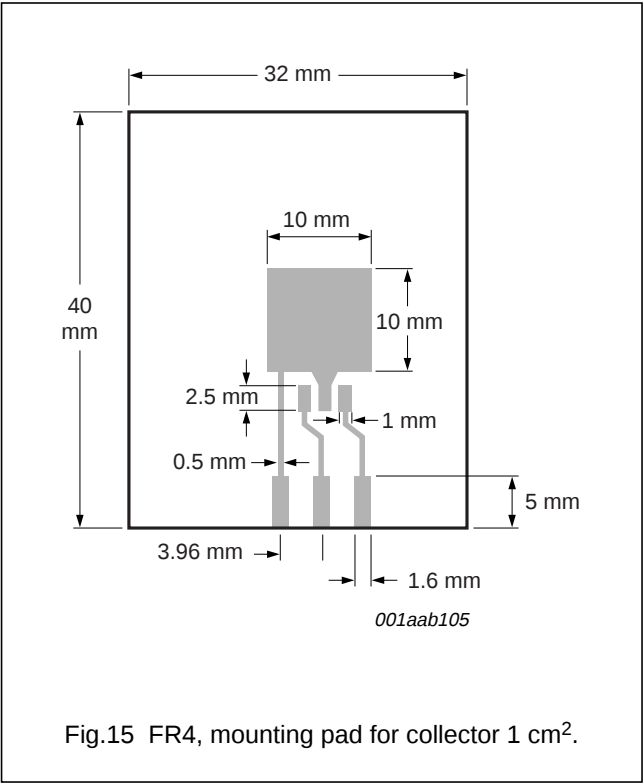
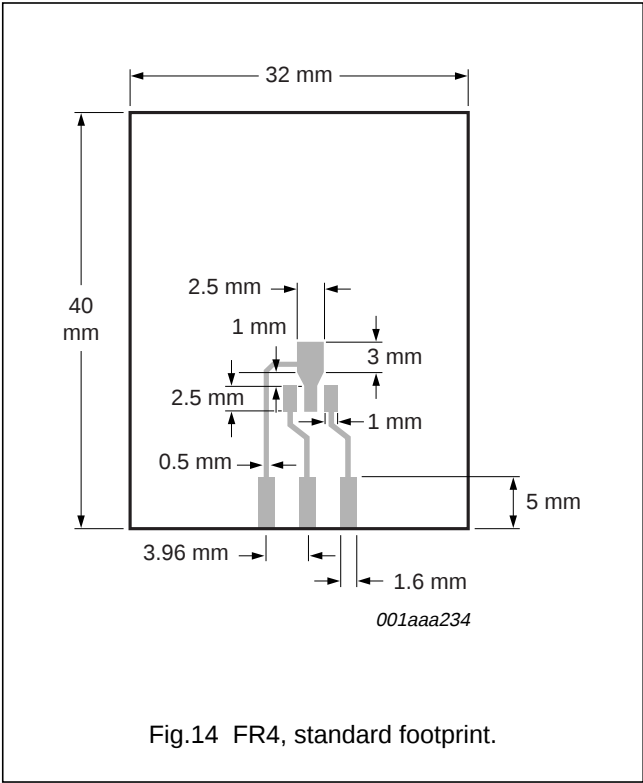
PBSS4540X



40 V, 5 A
NPN low V_{CEsat} (BISS) transistor

PBSS4540X

Reference mounting conditions



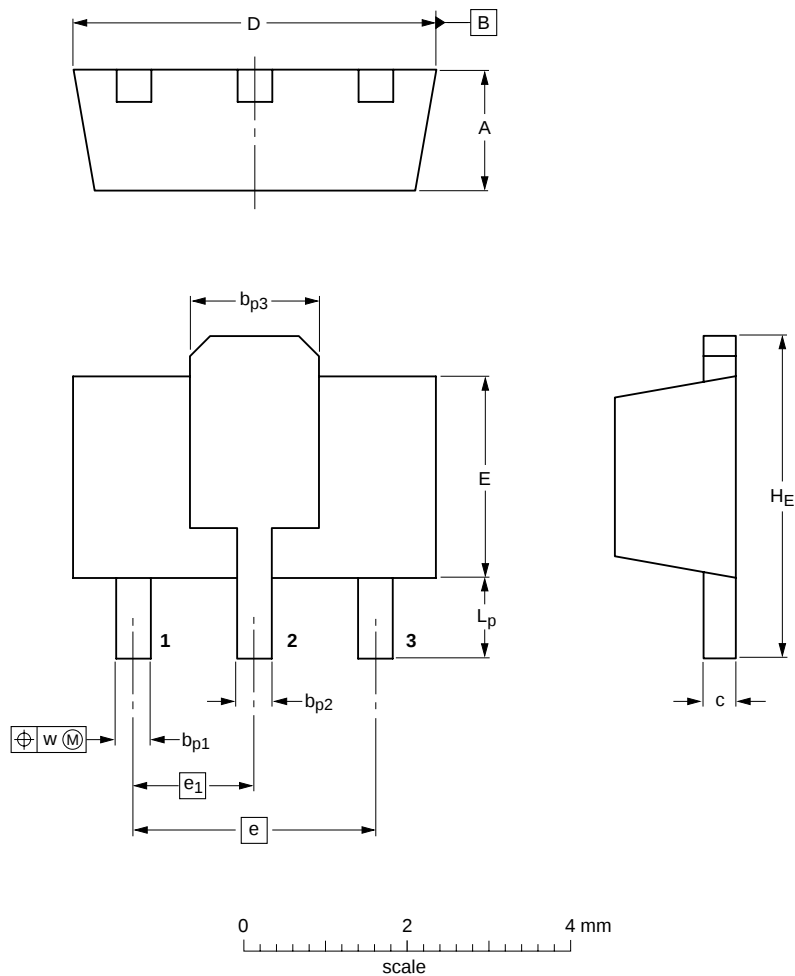
40 V, 5 A
NPN low V_{CEsat} (BISS) transistor

PBSS4540X

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_{p1}	b_{p2}	b_{p3}	c	D	E	e	e_1	H_E	L_p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			99-09-13 04-08-03

40 V, 5 A

NPN low V_{CEsat} (BISS) transistor

PBSS4540X

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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