

CDx4AC245, CDx4ACT245 Octal-Bus Transceiver, Three-State, Non-Inverting

1 Features

- Buffered inputs
- Typical propagation delay
 - 4ns at $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50pF$
- SCR-latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST™/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ± 24 mA output drive current
 - Fanout to 15 FAST™ ICs
 - Drives 50 Ω transmission line

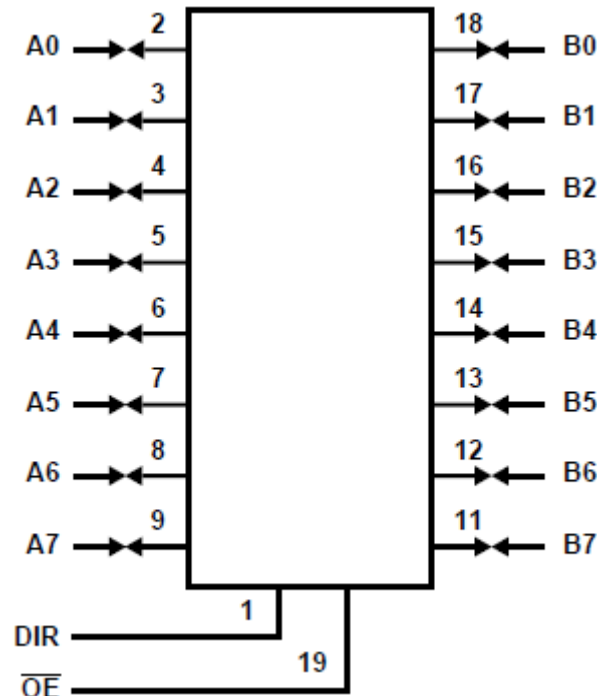
2 Description

The 'AC245 and 'ACT245 are octal-bus transceivers that utilize Advanced CMOS Logic technology.

Package Information

PART NUMBER	PACKAGE ¹	BODY SIZE (NOM)
CD74AC245/ CD74ACT245	N (PDIP, 20)	24.33 mm × 6.35 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
CD54AC245/ CD54ACT245	J (CDIP, 20)	24.2 mm × 6.92 mm
CD74ACT245	DB (SSOP, 20)	7.2 mm × 5.3 mm

1. For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)



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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2002) to Revision C (May 2023)	Page
• Added <i>Package Information</i> table, <i>Pin Functions</i> table, and <i>Thermal Information</i> table.....	1

4 Pin Configuration and Functions

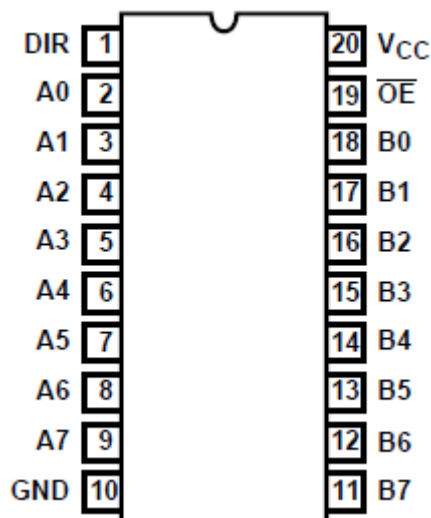


Figure 4-1. CD54AC245, CD54ACT245 (CERDIP), CD74AC245, CD74ACT245 (PDIP, SOIC, SSOP) Top View

Pin Functions

PIN		TYPE ¹	DESCRIPTION
NO.	NAME		
1	DIR	I/O	Direction Pin
2	A0	I/O	A1 Input/Output
3	A1	I/O	A2 Input/Output
4	A2	I/O	A3 Input/Output
5	A3	I/O	A4 Input/Output
6	A4	I/O	A5 Input/Output
7	A5	I/O	A6 Input/Output
8	A6	I/O	A7 Input/Output
9	A7	I/O	A8 Input/Output
10	GND	—	Ground Pin
11	B7	I/O	B7 Input/Output
12	B6	I/O	B6 Input/Output
13	B5	I/O	B5 Input/Output
14	B4	I/O	B4 Input/Output
15	B3	I/O	B3 Input/Output
16	B2	I/O	B2 Input/Output
17	B1	I/O	B1 Input/Output
18	B0	I/O	B0 Input/Output
19	$\overline{OE}$	I/O	Output Enable
20	V _{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	6	V
I _{IK}	Input diode current	V _I < -0.5V or V _I > V _{CC} + 0.5V		± 20	mA
I _{OK}	Output diode current	V _O < -0.5V or V _O > V _{CC} + 0.5V		± 50	mA
I _O	Output source or sink current per output pin	V _O > -0.5V or V _O < V _{CC} + 0.5V		± 50	mA
I _{OK}	V _{CC} or ground current	I _{CC} or I _{GND}		± 100	mA
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		CDx4AC245		CDx4ACT245		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage ³	1.5V	5.5V	4.5V	5.5V	V
V _I , V _O	Input or Output Voltage	0V	V _{CC}	0V	V _{CC}	V
dt/dv	Input Rise and Fall Slew Rate	1.5V to 3V	50			ns
		3.6V to 5.5V	20			
		4.5V to 5.5V			10	
T _A	Temperature range	-55	125	-55	125	°C

- (1) Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		CDx4AC14/ CDx4ACT14			UNIT
		E	M	SM	
		20 PINS			
R _{θJA}	Junction-to-ambient thermal resistance	69	58	70	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
	V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES										
V _{IH}	High-level input voltage			1.5	1.2	1.2	1.2		V	
				3	2.1	2.1	2.1			
				5.5	3.85	3.85	3.85			
V _{IL}	Low-level input voltage	V _{IL}		1.5	0.3	0.3	0.3		V	
				3	0.9	0.9	0.9			
				5.5	1.65	1.65	1.65			
V _{OH}	High-level output voltage	V _{IH} or V _{IL}	-0.05	1.5	1.4	1.4	1.4		V _{VOH}	
			-0.05	3	2.9	2.9	2.9			
			-0.05	4.5	4.4	4.4	4.4			
			-4	3	2.58	2.48	2.4			
			-24	4.5	3.94	3.8	3.7			
			-75	5.5		3.85				
			-50	5.5			3.85			
V _{OL}	Low-level output voltage	V _{IH} or V _{IL}	0.05	1.5 V	0.1	0.1	0.1		V	
			0.05	3 V	0.1	0.1	0.1			
			0.05	4.5 V	0.1	0.1	0.1			
			12	3 V	0.36	0.44	0.5			
			24	4.5 V	0.36	0.44	0.5			
			75 ¹	5.5 V		1.65				
			50 ¹	5.5 V			1.65			
I _I	Input leakage current	V _{CC} or GND		5.5	± 0.1	± 1	± 1	μ A		
I _{OZ}	Three-state leakage current	V _{IH} or V _{IL} , V _O = V _{CC} or GND		5.5 V	± 0.5	± 5	± 10	μ A		
I _{CC}	Quiescent supply current MSI	V _{CC} or GND	0	5.5 V	8	80	160	μ A		
ACT TYPES										
V _{IH}	High-level input voltage			4.5 V to 5.5 V	2	2	2		V	
V _{IL}	Low-level input voltage			4.5 V to 5.5 V	0.8	0.8	0.8		V	
V _{OH}	High-level output voltage	V _{IH} or V _{IL}	-0.05	4.5 V	4.4	4.4	4.4	0.8	V	
			-24	4.5 V	3.94	3.8	3.7			
			-75 ¹	5.5 V		3.85				
			-50	5.5 V			3.85			

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$		$-40^\circ\text{C TO } 85^\circ\text{C}$		$-55^\circ\text{C TO } 125^\circ\text{C}$		UNIT
	V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL} Low-level output voltage	V_{IH} or V_{IL}	0.05	4.5		0.1		0.1		0.1	V
		24	4.5		0.36		0.44		0.5	
		75 ¹	5.5				1.65			
		50 ¹	5.5						1.65	
										V
I_I Input leakage current	V_{CC} or GND		5.5 V		± 0.1		± 1		± 1	μA
I_{OZ} Three-state or leakage current	V_{IH} or V_{IL} , $V_O = V_{CC}$ or GND		5.5 V		± 0.5		± 5		± 10	μA
I_{CC} Quiescent supply current MSI	V_{CC} or GND	0	5.5 V		8		80		160	μA
ΔI_{CC} Additional supply current per input pin TTL inputs high 1 unit load	$V_{CC} - 2.1$		4.5 to 5.5		2.4		2.8		3	mA

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C , 75Ω at 125°C .

5.5 Switching Characteristics

Input t_r , $t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case). Over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER		V _{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
t _{PLH} , t _{PHL}	Propagation delay, data to output	1.5	96			106			ns
		3.3	3.2	10.8	3	11.9			
		5	2.2	7.7	2.1	8.5			
t _{PLZ} , t _{PHZ}	Propagation delay, output disable to output	1.5	159			175			ns
		3.3	4.7	15.9	4.4	17.5			
		5	3.7	12.7	3.5	14			
t _{PZL} , t _{PZH}	Propagation delay, output enable to output	1.5	159			175			ns
		3.3	5.6	19	5.3	21			
		5	3.7	12.7	3.5				
V _{OHV}	Minimum (Valley) V _{OH} During switching of other outputs (output under test not switching)	5	4 at 25°C			4 at 25°C			V

Input t_r , t_f = 3ns, C_L = 50pF (Worst Case). Over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

See Load Circuit and Voltage Waveforms)

PARAMETER		V _{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OLP}	Maximum (Peak) V _{OL} During switching of other outputs (output under test not switching)	5	1 at 25°C			1 at 25°C			V
C _O	Three-state output capacitance		15			15			pF
C _I	Input capacitance		10			10			pF
C _{PD}	Power dissipation capacitance		57			57			pF
ACT TYPES									
t _{PLH} , t _{PHL}	Propagation delay, data to output	5	2.7			2.5	10		ns
t _{PLZ} , t _{PHZ}	Propagation delay, output disable to output	5	3.7			3.5	14		ns
t _{PZL} , t _{PZH}	Propagation delay, output enable to output	5	3.8			3.6	14.4		ns
V _{OHV}	Minimum (Valley) V _{OH} During switching of other outputs (output under test not switching)	5	4 at 25°C			4 at 25°C			V
V _{OLP}	Maximum (Peak) V _{OL} During switching of other outputs (output under test not switching)	5	1 at 25°C			1 at 25°C			V
C _O	Three-state output capacitance		15			15			pF
C _I	Input capacitance		10			10			pF
C _{PD}	Power dissipation capacitance		57			57			pF

- Limits tested 100%
- 3.3V Min is at 3.6V, Max is at 3V
- 5V Min is at 5.5V, Max is at 4.5V
- CPD is used to determine the dynamic power consumption per channel
 - AC: $PD = VCC^2 f_i (CPD + CL)$
 - ACT: $PD = VCC^2 f_i (CPD + CL) + VCC \Delta ICC$ where f_i = input frequency, CL = output load capacitance, VCC = supply voltage

5.6 Timing Diagrams

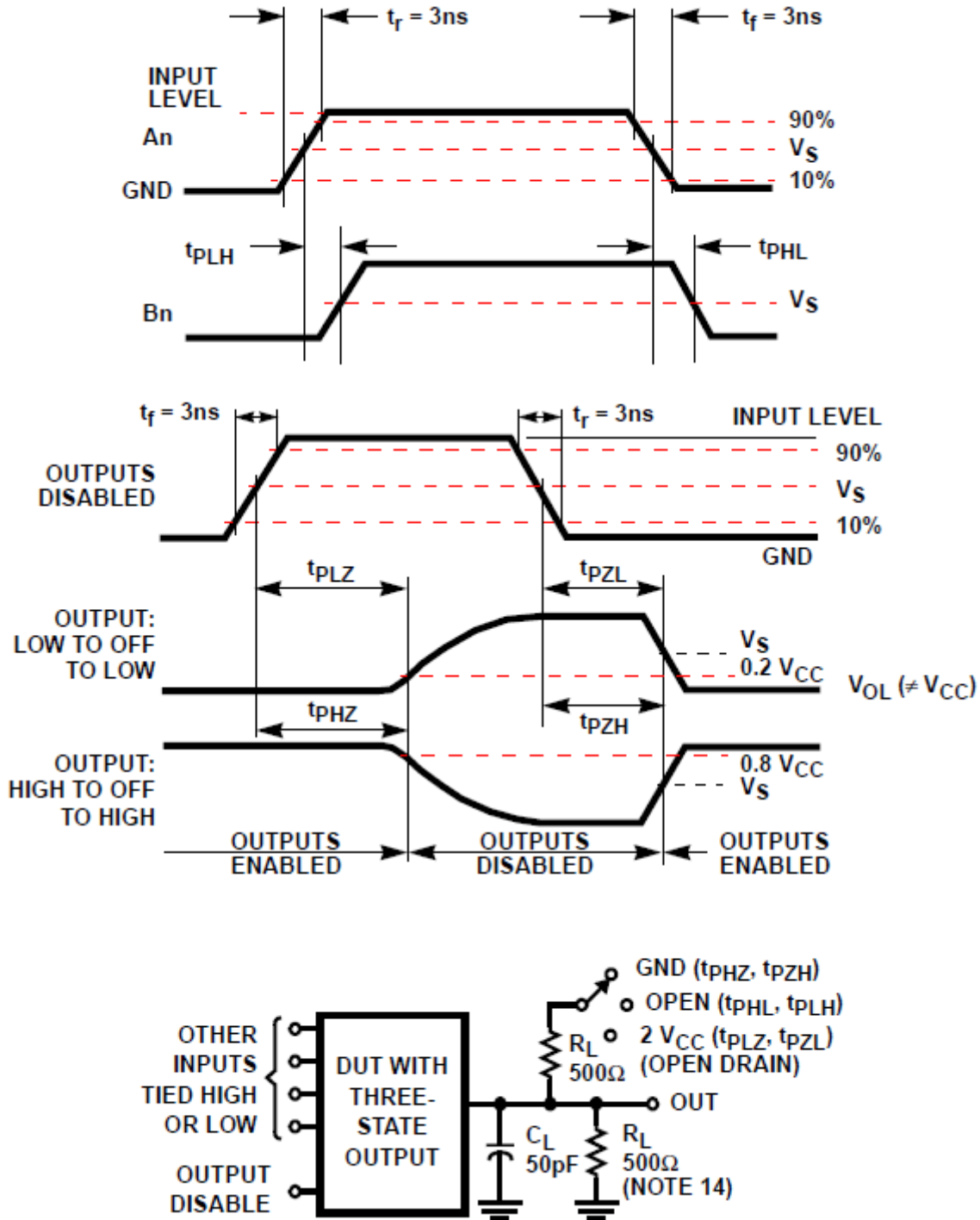


Figure 5-1. THREE-STATE PROPAGATION DELAY TIMES AND TEST CIRCUIT

Figure 5-1. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

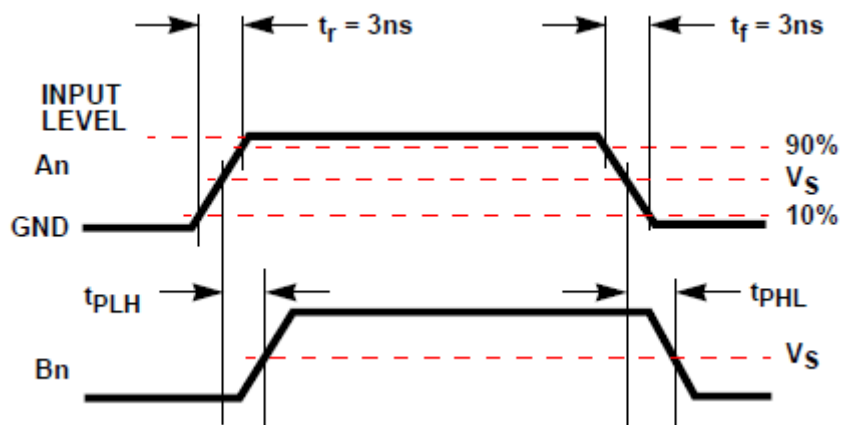
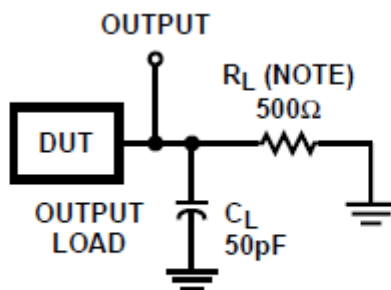


Figure 5-3. PROPAGATION DELAY TIMES



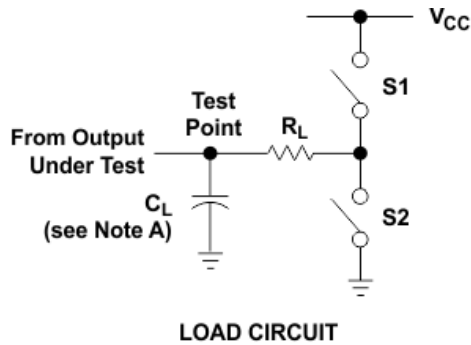
NOTE: For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

Table 5-1.

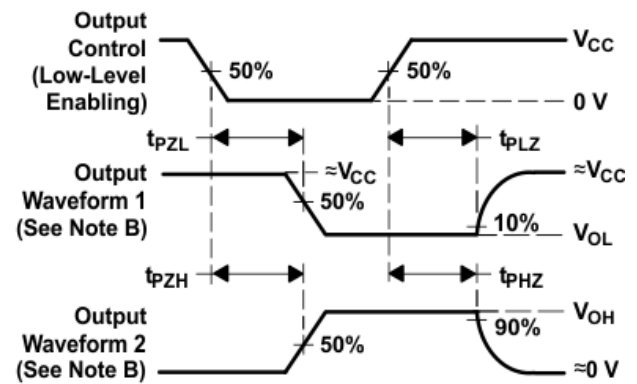
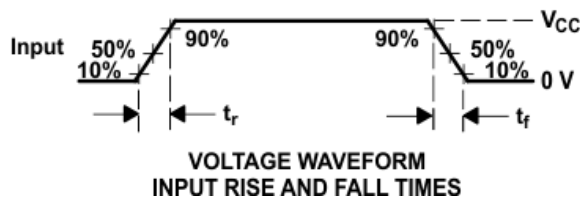
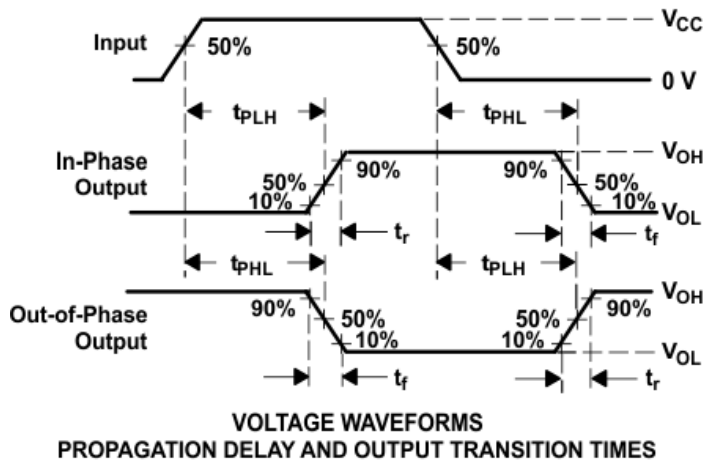
	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$

Figure 5-4. PROPAGATION DELAY TIMES

6 Parameter Measurement Information



PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{pZH}	1 k Ω	50 pF or 150 pF	Open	Closed
	t_{pZL}			Closed	Open
t_{dis}	t_{pHZ}	1 k Ω	50 pF	Open	Closed
	t_{pLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open



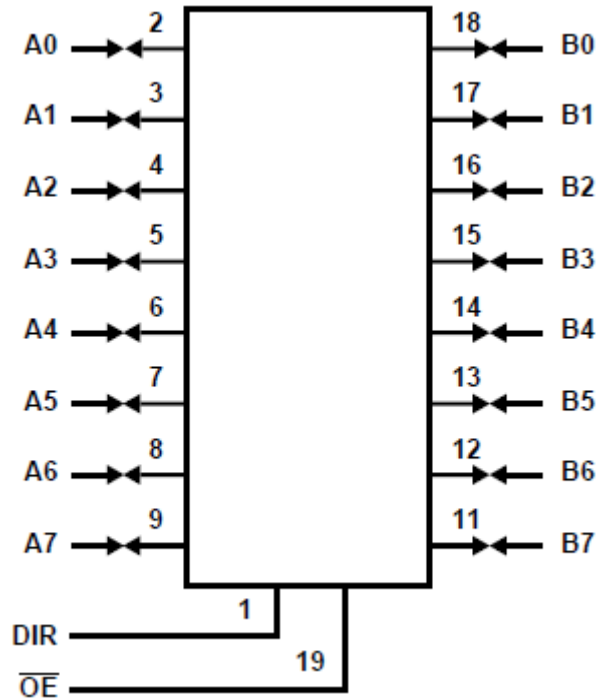
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

7 Detailed Description

7.1 Overview

The 'AC245 and 'ACT245 are non-inverting three-state bidirectional transceiver-buffers intended for two-way transmission from “A” bus to “B” bus or “B” bus to “A”. The logic level present on the direction input (DIR) determines the data direction. When the output enable input ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Device Functional Modes

[Function Table](#) lists the function modes of the CDx4AC245, CDx4ACT245.

Table 7-1. Function Table

INPUTS ⁽¹⁾		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

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