

### FEATURES

18-bit resolution with no missing codes

Throughput: 250 kSPS

INL

$\pm 0.75$  LSB typical

$\pm 1.5$  LSB minimum/maximum at  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

$-2.7$  LSB/ $+2$  LSB minimum/maximum at  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$

Dynamic range: 102 dB typical

Oversampled dynamic range: 125 dB at 1 kSPS

Noise-free code resolution: 20 bits at 1 kSPS

Effective resolution: 22.7 bits at 1 kSPS

SINAD: 101 dB typical at  $f_{\text{IN}} = 1$  kHz,  $V_{\text{REF}} = 5$  V

THD:  $-125$  dB typical at  $f_{\text{IN}} = 1$  kHz,  $V_{\text{REF}} = 5$  V

True differential analog input range:  $\pm V_{\text{REF}}$

0 V to  $V_{\text{REF}}$  with  $V_{\text{REF}}$  up to VDD on both inputs

No pipeline delay

Single-supply 2.3 V to 5 V operation with 1.8 V/2.5 V/3 V/5 V logic interface

Serial interface SPI/QSPI™-/MICROWIRE™-/DSP-compatible

Ability to daisy-chain multiple ADCs

Optional busy indicator feature

Power dissipation

1.35 mW at VDD = 2.5 V, 100 kSPS throughput

4.24 mW at VDD = 5 V, 100 kSPS throughput

1.4  $\mu\text{W}$  at VDD = 2.5 V, 100 SPS throughput

Standby current: 1 nA

10-lead MSOP

Pin-for-pin compatible with the 18-bit [AD7690](#) and 16-bit [AD7693](#), [AD7688](#), and [AD7687](#)

### ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)

Military temperature range:  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$

Controlled manufacturing baseline

One assembly/test site

One fabrication site

Enhanced product change notification

Qualification data available on request

### APPLICATIONS

Battery-powered equipment

Data acquisitions

Seismic data acquisition systems

Instrumentation

Medical instruments

### APPLICATION DIAGRAM

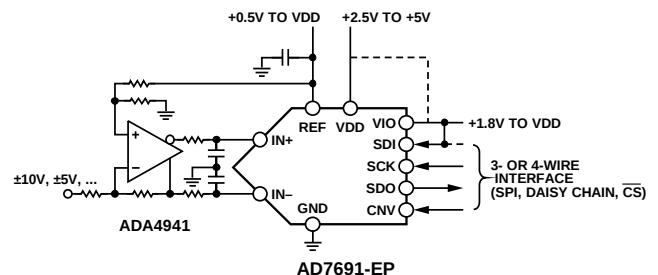


Figure 1.

### GENERAL DESCRIPTION

The [AD7691-EP](#) is an 18-bit, charge redistribution, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD, between 2.3 V and 5 V. It contains a low power, high speed, 18-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. On the CNV rising edge, it samples the voltage difference between the IN+ and IN- pins. The voltages on these pins swing in opposite phases between 0 V and REF.

The reference voltage, REF, is applied externally and can be set up to the supply voltage.

The power of the [AD7691-EP](#) scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus and provides an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate VIO supply.

The [AD7691-EP](#) is housed in a 10-lead MSOP with operation specified from  $-55^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ . Additional application and technical information can be found in the [AD7691](#) data sheet.

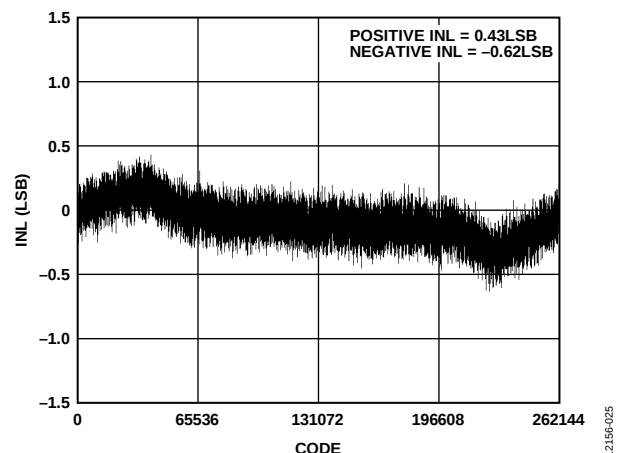


Figure 2. Integral Nonlinearity vs. Code, 5 V

Rev. A

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REVISION HISTORY

|                                               |   |
|-----------------------------------------------|---|
| 8/15—Rev. 0 to Rev. A                         |   |
| Added Enhanced Product Features Section ..... | 1 |
| 9/14—Revision 0: Initial Version              |   |

## SPECIFICATIONS

VDD = 2.3 V to 5.25 V, VIO = 2.3 V to VDD, VREF = VDD, all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

Table 1.

| Parameter                                         | Test Conditions/Comments                        | Min                       | Typ                 | Max                       | Unit             |
|---------------------------------------------------|-------------------------------------------------|---------------------------|---------------------|---------------------------|------------------|
| RESOLUTION                                        |                                                 | 18                        |                     |                           | Bits             |
| ANALOG INPUT                                      |                                                 |                           |                     |                           |                  |
| Voltage Range, V <sub>IN</sub>                    | IN+ – (IN–)                                     | –V <sub>REF</sub>         |                     | +V <sub>REF</sub>         | V                |
| Absolute Input Voltage Range                      | IN+, IN–                                        | –0.1                      |                     | V <sub>REF</sub> + 0.1    | V                |
| Common-Mode Input Range                           | IN+, IN–                                        | V <sub>REF</sub> /2 – 0.1 | V <sub>REF</sub> /2 | V <sub>REF</sub> /2 + 0.1 | V                |
| Analog Input Common-Mode Rejection Ratio (CMRR)   | f <sub>IN</sub> = 250 kHz                       |                           | 65                  |                           | dB               |
| Leakage Current at 25°C                           | Acquisition phase                               |                           | 1                   |                           | nA               |
| Input Impedance <sup>1</sup>                      |                                                 |                           |                     |                           |                  |
| THROUGHPUT                                        |                                                 |                           |                     |                           |                  |
| Conversion Rate                                   | VDD = 4.5 V to 5.25 V                           | 0                         |                     | 250                       | kSPS             |
|                                                   | VDD = 2.3 V to 4.5 V                            | 0                         |                     | 180                       | kSPS             |
| Transient Response                                | Full-scale step                                 |                           |                     | 1.8                       | μs               |
| ACCURACY                                          |                                                 |                           |                     |                           |                  |
| No Missing Codes                                  |                                                 | 18                        |                     |                           | Bits             |
| Integral Linearity Error                          | –55°C to +105°C                                 | –2.7                      | ±0.75               | +2                        | LSB <sup>2</sup> |
|                                                   | –40°C to +85°C                                  | –1.5                      | ±0.75               | +1.5                      | LSB <sup>2</sup> |
| Differential Linearity Error                      |                                                 | –1                        | ±0.5                | +1.25                     | LSB <sup>2</sup> |
| Transition Noise                                  | REF = VDD = 5 V                                 |                           | 0.75                |                           | LSB <sup>2</sup> |
| Gain Error <sup>3</sup>                           | VDD = 4.5 V to 5.25 V                           | –40                       | ±2                  | +40                       | LSB <sup>2</sup> |
|                                                   | VDD = 2.3 V to 4.5 V                            | –80                       | ±2                  | +80                       | LSB <sup>2</sup> |
| Gain Error Temperature Drift                      |                                                 |                           | ±0.3                |                           | ppm/°C           |
| Zero Error <sup>3</sup>                           | VDD = 4.5 V to 5.25 V                           | –0.8                      | ±0.1                | +0.8                      | mV               |
|                                                   | VDD = 2.3 V to 4.5 V                            | –3.5                      | ±0.7                | +3.5                      | mV               |
| Zero Temperature Drift                            |                                                 |                           | ±0.3                |                           | ppm/°C           |
| Power Supply Sensitivity                          | VDD = 5 V ± 5%                                  |                           | ±0.25               |                           | LSB <sup>2</sup> |
| AC ACCURACY <sup>4</sup>                          |                                                 |                           |                     |                           |                  |
| Dynamic Range                                     | V <sub>REF</sub> = 5 V                          | 101                       | 102                 |                           | dB               |
| Oversampled Dynamic Range <sup>5</sup>            | f <sub>IN</sub> = 1 kSPS                        |                           | 125                 |                           | dB               |
| Signal-to-Noise                                   |                                                 |                           |                     |                           |                  |
| f <sub>IN</sub> = 1 kHz, V <sub>REF</sub> = 5 V   | –55°C to +105°C                                 | 98.5                      | 101                 |                           | dB               |
|                                                   | –40°C to +85°C                                  | 100                       | 101.5               |                           | dB               |
| f <sub>IN</sub> = 1 kHz, V <sub>REF</sub> = 2.5 V | –55°C to +105°C                                 | 94                        | 96                  |                           | dB               |
|                                                   | –40°C to +85°C                                  | 95                        | 96.5                |                           | dB               |
| Spurious-Free Dynamic Range                       | f <sub>IN</sub> = 1 kHz, V <sub>REF</sub> = 5 V |                           | –125                |                           | dB               |
| Total Harmonic Distortion                         | f <sub>IN</sub> = 1 kHz, V <sub>REF</sub> = 5 V |                           | –118                |                           | dB               |
| Signal-to-Noise-and-Distortion Ratio (SINAD)      |                                                 |                           |                     |                           |                  |
| f <sub>IN</sub> = 1 kHz, V <sub>REF</sub> = 5 V   | –55°C to +105°C                                 | 98.5                      | 101                 |                           | dB               |
|                                                   | –40°C to +85°C                                  | 100                       | 101.5               |                           | dB               |
| f <sub>IN</sub> = 1 kHz, V <sub>REF</sub> = 2.5 V | –55°C to +105°C                                 | 94                        | 96                  |                           | dB               |
|                                                   | –40°C to +85°C                                  | 95                        | 96.5                |                           | dB               |
| Intermodulation Distortion <sup>6</sup>           |                                                 |                           | 115                 |                           | dB               |

<sup>1</sup> See the Analog Inputs section of the [AD7691](#) data sheet.

<sup>2</sup> LSB means least significant bit. With the ±5 V input range, one LSB is 38.15 μV.

<sup>3</sup> See the Terminology section of the [AD7691](#) data sheet. These specifications include full temperature range variation but not the error contribution from the external reference.

<sup>4</sup> All ac accuracy specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

<sup>5</sup> Dynamic range obtained by oversampling the ADC running at a throughput f<sub>s</sub> of 250 kSPS, followed by postdigital filtering with an output word rate f<sub>o</sub>.

<sup>6</sup> f<sub>IN1</sub> = 21.4 kHz and f<sub>IN2</sub> = 18.9 kHz, with each tone at –7 dB below full scale.

VDD = 2.3 V to 5.25 V, VIO = 2.3 V to VDD, V<sub>REF</sub> = VDD, all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

Table 2.

| Parameter                       | Test Conditions/Comments                 | Min       | Typ  | Max        | Unit      |
|---------------------------------|------------------------------------------|-----------|------|------------|-----------|
| REFERENCE                       |                                          |           |      |            |           |
| Voltage Range                   |                                          | 0.5       |      | VDD + 0.3  | V         |
| Load Current                    | 250 kSPS, REF = 5 V                      |           | 60   |            | μA        |
| SAMPLING DYNAMICS               |                                          |           |      |            |           |
| –3 dB Input Bandwidth           |                                          |           | 2    |            | MHz       |
| Aperture Delay                  | VDD = 5 V                                |           | 2.5  |            | ns        |
| DIGITAL INPUTS                  |                                          |           |      |            |           |
| Logic Levels                    |                                          |           |      |            |           |
| V <sub>IL</sub>                 |                                          | –0.3      |      | +0.3 × VIO | V         |
| V <sub>IH</sub>                 |                                          | 0.7 × VIO |      | VIO + 0.3  | V         |
| I <sub>IL</sub>                 |                                          | –1        |      | +1         | μA        |
| I <sub>IH</sub>                 |                                          | –1        |      | +1         | μA        |
| DIGITAL OUTPUTS                 |                                          |           |      |            |           |
| Data Format                     | Serial 18-bit, twos complement           |           |      |            |           |
| Pipeline Delay <sup>1</sup>     |                                          |           |      |            |           |
| V <sub>OL</sub>                 | I <sub>SINK</sub> = +500 μA              |           |      | 0.4        | V         |
| V <sub>OH</sub>                 | I <sub>SOURCE</sub> = –500 μA            | VIO – 0.3 |      |            | V         |
| POWER SUPPLIES                  |                                          |           |      |            |           |
| VDD Range                       | Specified performance                    | 2.3       |      | 5.25       | V         |
| VIO Range                       | Specified performance                    | 2.3       |      | VDD + 0.3  | V         |
| VIO Range                       | Functional operation                     | 1.8       |      | VDD + 0.3  | V         |
| Standby Current <sup>2, 3</sup> | VDD and VIO = 5 V, T <sub>A</sub> = 25°C |           | 1    | 50         | nA        |
| Power Dissipation               | VDD = 2.5 V, 100 SPS throughput          |           | 1.4  |            | μW        |
|                                 | VDD = 2.5 V, 100 kSPS throughput         |           | 1.35 |            | mW        |
|                                 | VDD = 2.5 V, 180 kSPS throughput         |           | 2.4  |            | mW        |
|                                 | VDD = 5 V, 100 kSPS throughput           |           | 4.24 | 5          | mW        |
|                                 | VDD = 5 V, 250 kSPS throughput           |           | 10.6 | 12.5       | mW        |
| Energy per Conversion           |                                          |           | 50   |            | nJ/sample |
| TEMPERATURE RANGE <sup>4</sup>  |                                          |           |      |            |           |
| Specified Performance           | T <sub>MIN</sub> to T <sub>MAX</sub>     | –55       |      | +105       | °C        |

<sup>1</sup> Conversion results are available immediately after completed conversion.

<sup>2</sup> With all digital inputs forced to VIO or GND as required.

<sup>3</sup> During acquisition phase.

<sup>4</sup> Contact an Analog Devices, Inc., sales representative for the extended temperature range.

**TIMING SPECIFICATIONS**

VDD = 4.5 V to 5.25 V, VIO = 2.3 V to VDD, VREF = VDD, all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. See Figure 3 and Figure 4 for load conditions.

**Table 3.**

| Parameter                                                                                     | Symbol               | Min | Typ | Max | Unit |
|-----------------------------------------------------------------------------------------------|----------------------|-----|-----|-----|------|
| Conversion Time: CNV Rising Edge to Data Available                                            | t <sub>CONV</sub>    | 0.5 |     | 2.2 | μs   |
| Acquisition Time                                                                              | t <sub>ACQ</sub>     | 1.8 |     |     | μs   |
| Time Between Conversions                                                                      | t <sub>CYC</sub>     | 4   |     |     | μs   |
| CNV Pulse Width ( $\overline{\text{CS}}$ Mode)                                                | t <sub>CNVH</sub>    | 10  |     |     | ns   |
| SCK Period ( $\overline{\text{CS}}$ Mode)                                                     | t <sub>SCK</sub>     | 15  |     |     | ns   |
| SCK Period (Chain Mode)                                                                       | t <sub>SCK</sub>     |     |     |     |      |
| VIO Above 4.5 V                                                                               |                      | 17  |     |     | ns   |
| VIO Above 3 V                                                                                 |                      | 18  |     |     | ns   |
| VIO Above 2.7 V                                                                               |                      | 19  |     |     | ns   |
| VIO Above 2.3 V                                                                               |                      | 20  |     |     | ns   |
| SCK Low Time                                                                                  | t <sub>SCKL</sub>    | 7   |     |     | ns   |
| SCK High Time                                                                                 | t <sub>SCKH</sub>    | 7   |     |     | ns   |
| SCK Falling Edge to Data Remains Valid                                                        | t <sub>HSDO</sub>    | 4   |     |     | ns   |
| SCK Falling Edge to Data Valid Delay                                                          | t <sub>DSDO</sub>    |     |     |     |      |
| VIO Above 4.5 V                                                                               |                      |     |     | 14  | ns   |
| VIO Above 3 V                                                                                 |                      |     |     | 15  | ns   |
| VIO Above 2.7 V                                                                               |                      |     |     | 16  | ns   |
| VIO Above 2.3 V                                                                               |                      |     |     | 17  | ns   |
| CNV or SDI Low to SDO D17 MSB Valid ( $\overline{\text{CS}}$ Mode)                            | t <sub>EN</sub>      |     |     |     |      |
| VIO Above 4.5 V                                                                               |                      |     |     | 15  | ns   |
| VIO Above 2.7 V                                                                               |                      |     |     | 18  | ns   |
| VIO Above 2.3 V                                                                               |                      |     |     | 23  | ns   |
| CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ( $\overline{\text{CS}}$ Mode) | t <sub>DIS</sub>     |     |     | 25  | ns   |
| SDI Valid Setup Time from CNV Rising Edge ( $\overline{\text{CS}}$ Mode)                      | t <sub>SSDICNV</sub> | 15  |     |     | ns   |
| SDI Valid Hold Time from CNV Rising Edge ( $\overline{\text{CS}}$ Mode)                       | t <sub>HSDICNV</sub> | 0   |     |     | ns   |
| SCK Valid Setup Time from CNV Rising Edge (Chain Mode)                                        | t <sub>SSCKCNV</sub> | 5   |     |     | ns   |
| SCK Valid Hold Time from CNV Rising Edge (Chain Mode)                                         | t <sub>HSCKCNV</sub> | 10  |     |     | ns   |
| SDI Valid Setup Time from SCK Falling Edge (Chain Mode)                                       | t <sub>SSDISCK</sub> | 3   |     |     | ns   |
| SDI Valid Hold Time from SCK Falling Edge (Chain Mode)                                        | t <sub>HSDISCK</sub> | 4   |     |     | ns   |
| SDI High to SDO High (Chain Mode with Busy Indicator)                                         | t <sub>DSDOSDI</sub> |     |     |     |      |
| VIO Above 4.5 V                                                                               |                      |     |     | 15  | ns   |
| VIO Above 2.3 V                                                                               |                      |     |     | 26  | ns   |

VDD = 2.3 V to 4.5 V, VIO = 2.3 V to VDD, VREF = VDD, all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. See Figure 3 and Figure 4 for load conditions.

Table 4.

| Parameter                                                                                     | Symbol               | Min | Typ | Max | Unit |
|-----------------------------------------------------------------------------------------------|----------------------|-----|-----|-----|------|
| Conversion Time: CNV Rising Edge to Data Available                                            | t <sub>CONV</sub>    | 0.5 |     | 3.7 | μs   |
| Acquisition Time                                                                              | t <sub>ACQ</sub>     | 1.8 |     |     | μs   |
| Time Between Conversions                                                                      | t <sub>CYC</sub>     | 5.5 |     |     | μs   |
| CNV Pulse Width ( $\overline{\text{CS}}$ Mode)                                                | t <sub>CNVH</sub>    | 10  |     |     | ns   |
| SCK Period ( $\overline{\text{CS}}$ Mode)                                                     | t <sub>SCK</sub>     | 25  |     |     | ns   |
| SCK Period (Chain Mode)                                                                       | t <sub>SCK</sub>     |     |     |     |      |
| VIO Above 3 V                                                                                 |                      | 29  |     |     | ns   |
| VIO Above 2.7 V                                                                               |                      | 35  |     |     | ns   |
| VIO Above 2.3 V                                                                               |                      | 40  |     |     | ns   |
| SCK Low Time                                                                                  | t <sub>SCKL</sub>    | 12  |     |     | ns   |
| SCK High Time                                                                                 | t <sub>SCKH</sub>    | 12  |     |     | ns   |
| SCK Falling Edge to Data Remains Valid                                                        | t <sub>HSDO</sub>    | 5   |     |     | ns   |
| SCK Falling Edge to Data Valid Delay                                                          | t <sub>DSDO</sub>    |     |     |     |      |
| VIO Above 3 V                                                                                 |                      |     |     | 24  | ns   |
| VIO Above 2.7 V                                                                               |                      |     |     | 30  | ns   |
| VIO Above 2.3 V                                                                               |                      |     |     | 35  | ns   |
| CNV or SDI Low to SDO D17 MSB Valid ( $\overline{\text{CS}}$ Mode)                            | t <sub>EN</sub>      |     |     |     |      |
| VIO Above 2.7 V                                                                               |                      |     |     | 18  | ns   |
| VIO Above 2.3 V                                                                               |                      |     |     | 22  | ns   |
| CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ( $\overline{\text{CS}}$ Mode) | t <sub>DIS</sub>     |     |     | 25  | ns   |
| SDI Valid Setup Time from CNV Rising Edge ( $\overline{\text{CS}}$ Mode)                      | t <sub>SSDICNV</sub> | 30  |     |     | ns   |
| SDI Valid Hold Time from CNV Rising Edge ( $\overline{\text{CS}}$ Mode)                       | t <sub>HSDICNV</sub> | 0   |     |     | ns   |
| SCK Valid Setup Time from CNV Rising Edge (Chain Mode)                                        | t <sub>SSCKCNV</sub> | 5   |     |     | ns   |
| SCK Valid Hold Time from CNV Rising Edge (Chain Mode)                                         | t <sub>HSCKCNV</sub> | 8   |     |     | ns   |
| SDI Valid Setup Time from SCK Falling Edge (Chain Mode)                                       | t <sub>SSDISCK</sub> | 8   |     |     | ns   |
| SDI Valid Hold Time from SCK Falling Edge (Chain Mode)                                        | t <sub>HSDISCK</sub> | 10  |     |     | ns   |
| SDI High to SDO High (Chain Mode with Busy Indicator)                                         | t <sub>DSDOSDI</sub> |     |     | 36  |      |

## Timing Diagrams

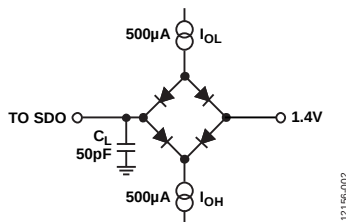
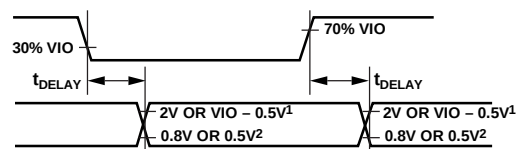


Figure 3. Load Circuit for Digital Interface Timing



<sup>1</sup>2V IF VIO ABOVE 2.5V, VIO - 0.5V IF VIO BELOW 2.5V.  
<sup>2</sup>0.8V IF VIO ABOVE 2.5V, 0.5V IF VIO BELOW 2.5V.

Figure 4. Voltage Levels for Timing

## ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter                             | Rating                                        |
|---------------------------------------|-----------------------------------------------|
| Analog Inputs (IN+, IN–) <sup>1</sup> | GND – 0.3 V to VDD + 0.3 V<br>or $\pm 130$ mA |
| REF                                   | GND – 0.3 V to VDD + 0.3 V                    |
| Supply Voltages                       |                                               |
| VDD, VIO to GND                       | –0.3 V to +7 V                                |
| VDD to VIO                            | $\pm 7$ V                                     |
| Digital Inputs to GND                 | –0.3 V to VIO + 0.3 V                         |
| Digital Outputs to GND                | –0.3 V to VIO + 0.3 V                         |
| Storage Temperature Range             | –65°C to +150°C                               |
| Junction Temperature                  | 150°C                                         |
| Lead Temperature Range                | JEDEC J-STD-20                                |

<sup>1</sup> See the Analog Inputs section of the [AD7691](#) data sheet.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|--------------|---------------|---------------|------|
| 10-Lead MSOP | 200           | 44            | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

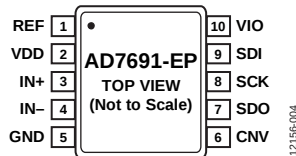


Figure 5. 10-Lead MSOP Pin Configuration

Table 7. Pin Function Descriptions

| Pin No. | Mnemonic | Type <sup>1</sup> | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------|----------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | REF      | AI                | Reference Input Voltage. The REF range is from 0.5 V to VDD. It is referred to the GND pin. Decouple this pin closely with a 10 $\mu$ F capacitor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2       | VDD      | P                 | Power Supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 3       | IN+      | AI                | Differential Positive Analog Input. Referenced to IN-. The input range for IN+ is between 0 V and $V_{REF}$ , centered about $V_{REF}/2$ and must be driven 180° out of phase with IN-.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4       | IN-      | AI                | Differential Negative Analog Input. Referenced to IN+. The input range for IN- is between 0 V and $V_{REF}$ , centered about $V_{REF}/2$ and must be driven 180° out of phase with IN+.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 5       | GND      | P                 | Power Supply Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 6       | CNV      | DI                | Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device, either chain mode or CS mode. In CS mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.                                                                                                                                                                                                                                                                                                                                                          |
| 7       | SDO      | DO                | Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 8       | SCK      | DI                | Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 9       | SDI      | DI                | Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows:<br>Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 18 SCK cycles.<br>CS mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low, and if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled. |
| 10      | VIO      | P                 | Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

<sup>1</sup>AI = analog input, DI = digital input, DO = digital output, and P = power.

## TYPICAL PERFORMANCE CHARACTERISTICS

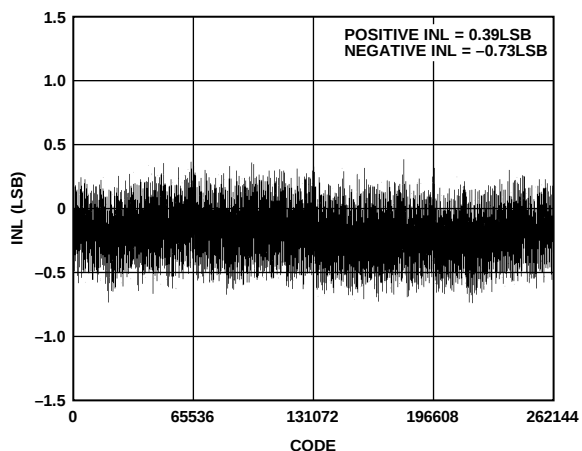


Figure 6. Integral Nonlinearity (INL) vs. Code, 2.5 V

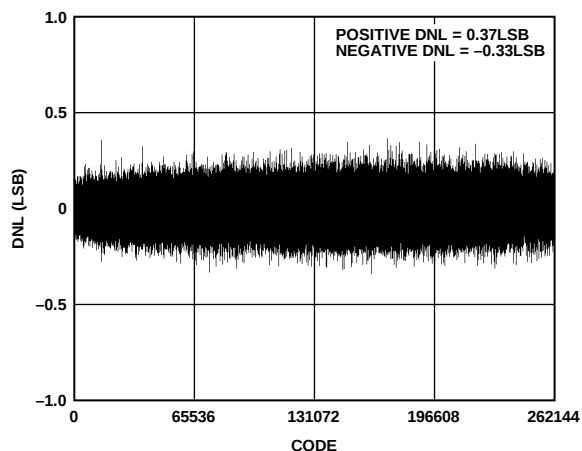


Figure 9. Differential Nonlinearity (DNL) vs. Code, 5 V

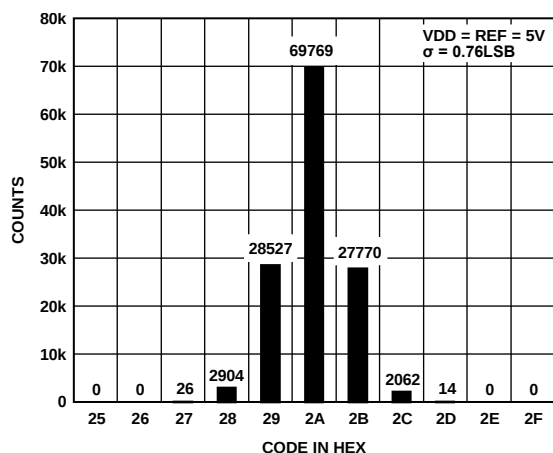


Figure 7. Histogram of a DC Input at the Code Center, 5 V

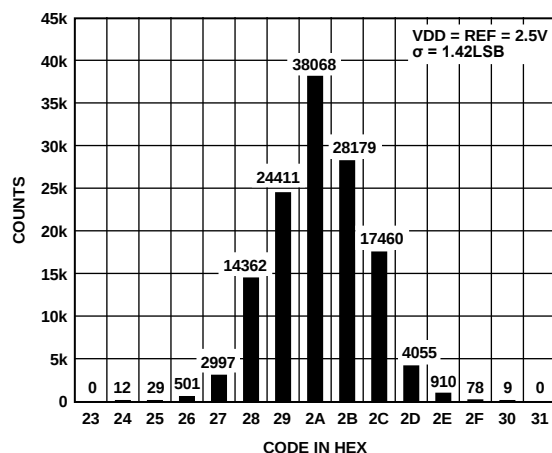


Figure 10. Histogram of a DC Input at the Code Center, 2.5 V

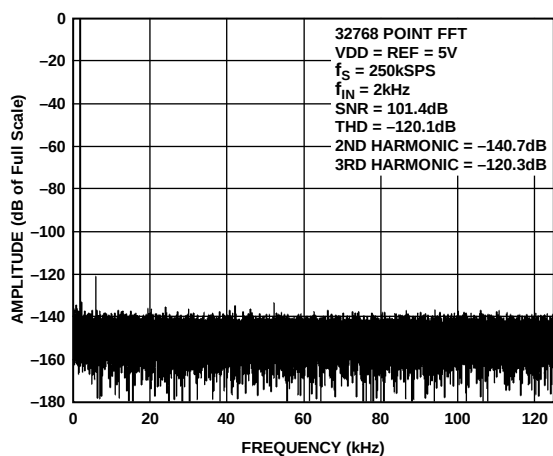


Figure 8. 2 kHz FFT Plot, 5 V

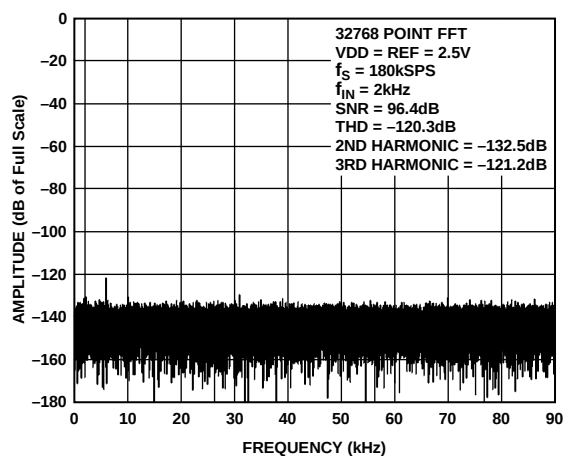


Figure 11. 2 kHz FFT Plot, 2.5 V

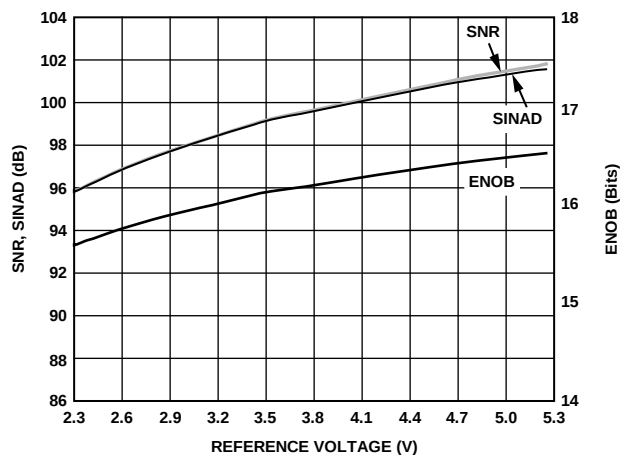


Figure 12. SNR, SINAD, and ENOB vs. Reference Voltage

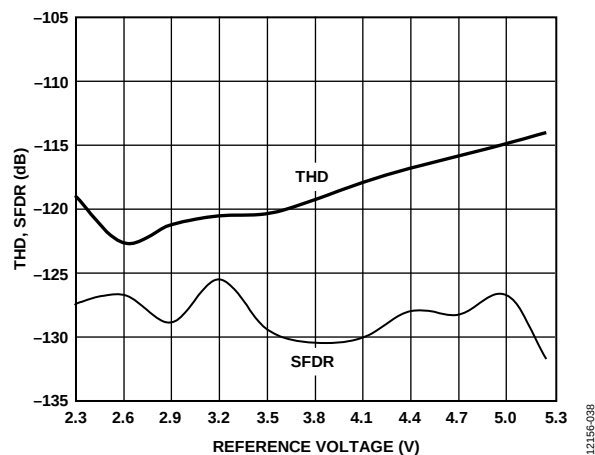


Figure 15. THD, SFDR vs. Reference Voltage

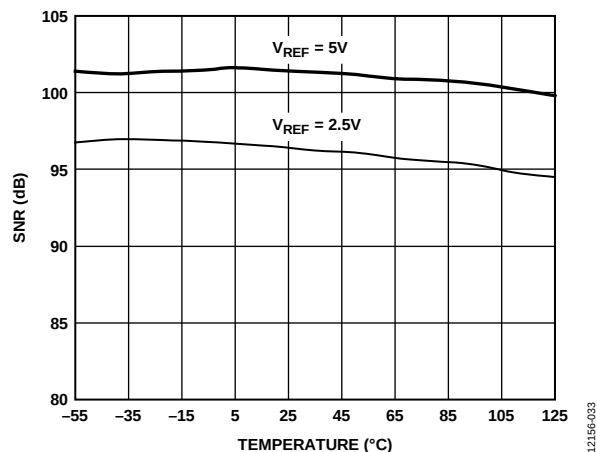


Figure 13. SNR vs. Temperature

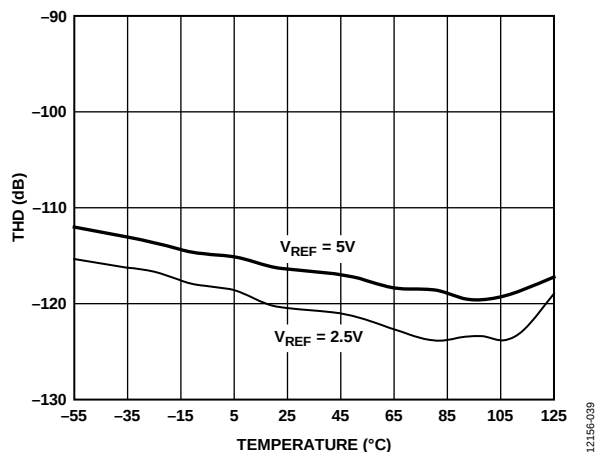


Figure 16. THD vs. Temperature

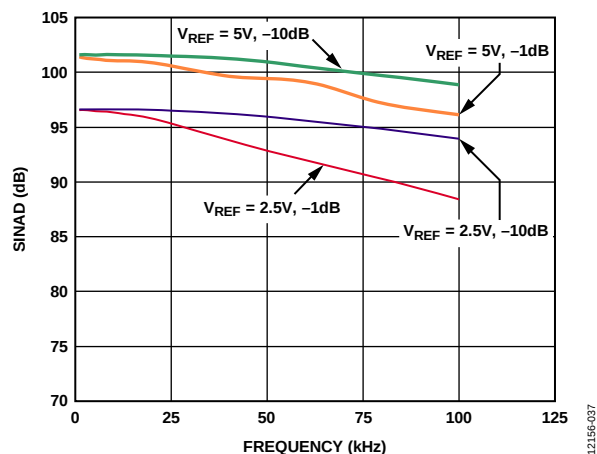


Figure 14. SINAD vs. Frequency

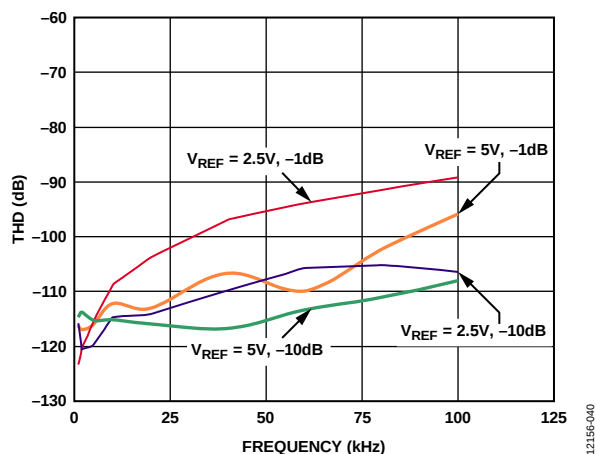


Figure 17. THD vs. Frequency

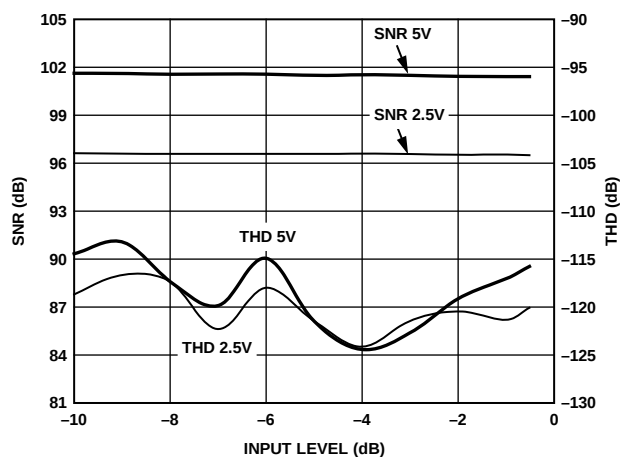


Figure 18. SNR, THD vs. Input Level

12156-041

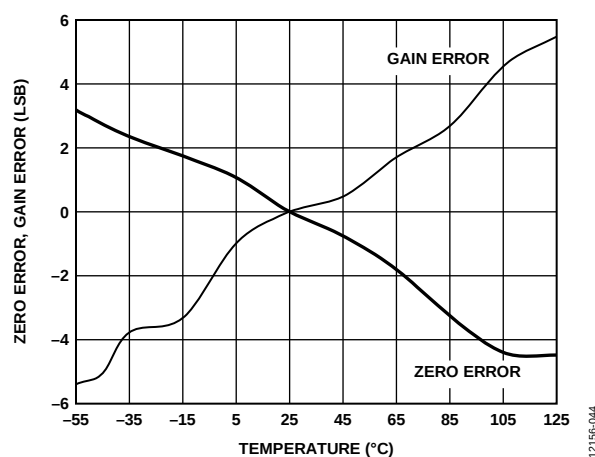


Figure 21. Zero Error, Gain Error vs. Temperature

12156-044

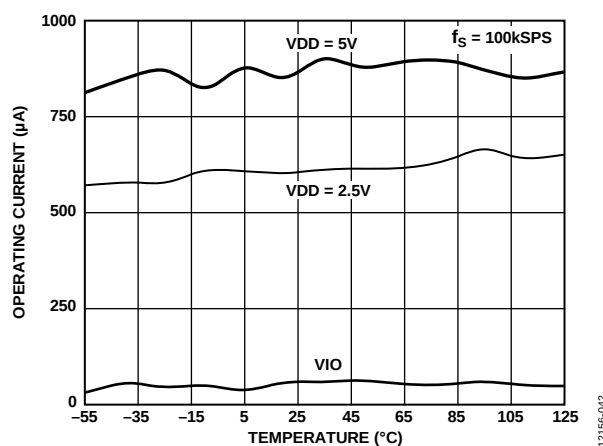


Figure 19. Operating Current vs. Temperature

12156-042

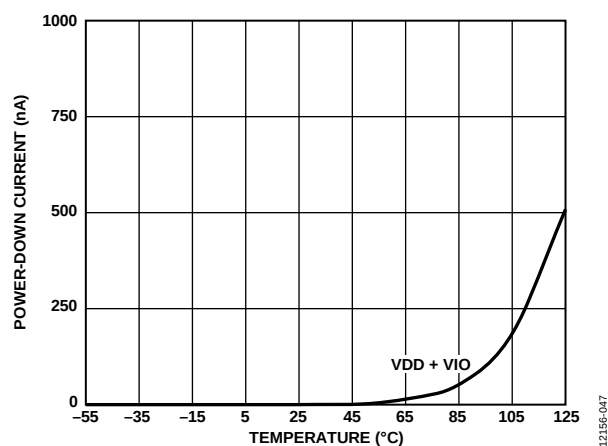


Figure 22. Power-Down Current vs. Temperature

12156-047

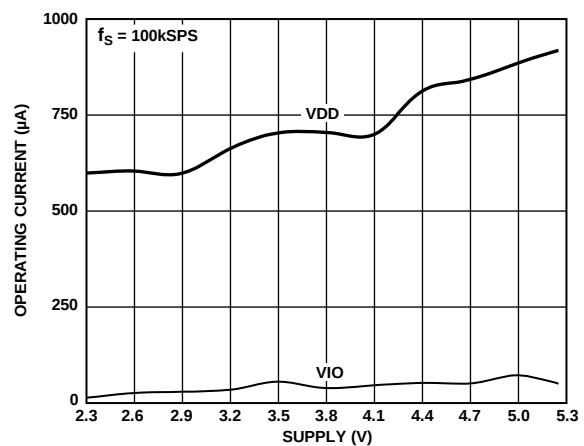
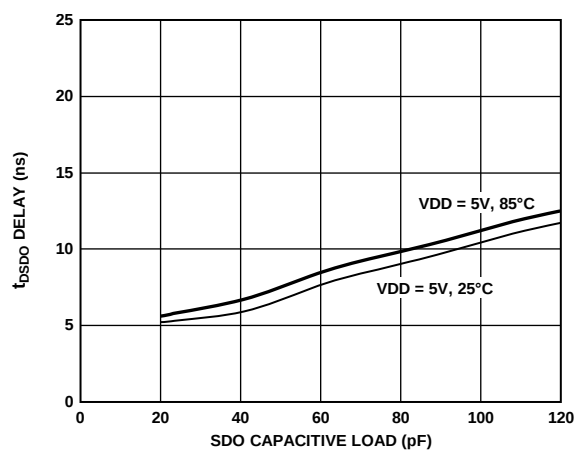


Figure 20. Operating Current vs. Supply

12156-043

Figure 23.  $t_{SDO}$  Delay vs. SDO Capacitive Load and Supply

12156-034

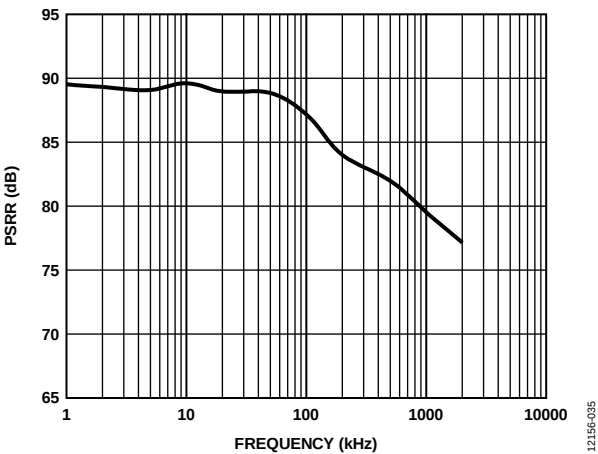


Figure 24. PSSR vs. Frequency

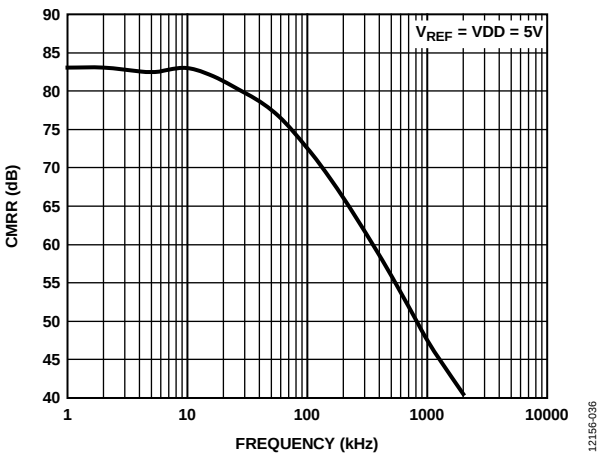
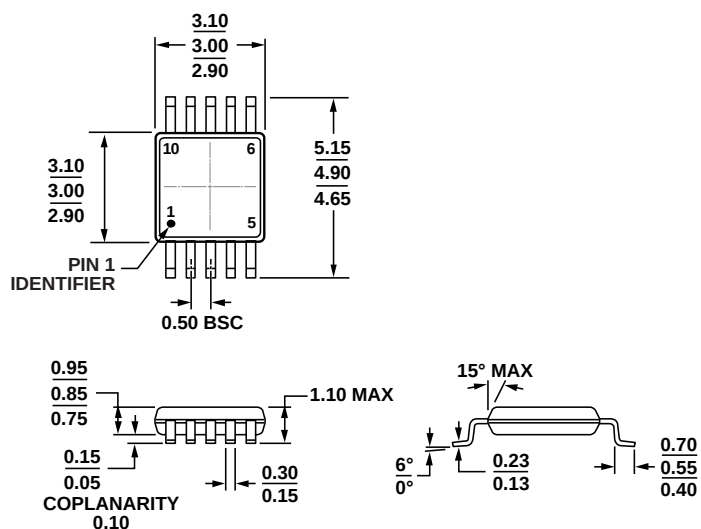


Figure 25. Analog Input CMRR vs. Frequency

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 26. 10-Lead Mini Small Outline Package [MSOP]  
(RM-10)

Dimensions shown in millimeters

091709-A

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description | Package Option | Branding | Ordering Quantity |
|--------------------|-------------------|---------------------|----------------|----------|-------------------|
| AD7691SRMZ-EP-RL7  | -55°C to +105°C   | 10-Lead MSOP, Reel  | RM-10          | C82      | 1,000             |
| EVAL-AD7691SDZ     |                   | Evaluation Board    |                |          |                   |
| EVAL-SDP-CB1Z      |                   | Controller Board    |                |          |                   |

<sup>1</sup> Z = RoHS Compliant Part.