HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

IH5148 - IH5151
High-Level CMOS Analog Switches

GENERAL DESCRIPTION

The IH5148 family of solid state analog switches are designed using an improved, high voltage CMOS technology. Destructive latchup has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present; the IH5148 CMOS technology has eliminated this problem.

Key performance advantages of the 5148 series are TTL compatibility and ultra low-power operation. $R_{DS(on)}$ switch resistance is typically in the 14Ω To 18Ω Area, for signals in the −10V to +10V range. Quiescent current is less than 10μA. The 5148 also guarantees Break-Before-Make switching which is logically accomplished by extending the t_{ON} time (200nsec typ.) such that it exceeds t_{OFF} time (120nsec typ.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

Many of the devices in the 5148 series are pin-for-pin compatible with other analog switches, and offer improved electrical characteristics.

FEATURES

- **Low $R_{DS}(ON)$ — 25Ω**
- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 100μA**
- **Break-Before-Make Switching t_{OFF} 120nsec Typ., t_{ON} 200nsec Typical**
- **TTL, CMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **±5V to ±15V Supply Range**

CMOS ANALOG SWITCH PRODUCT CONDITIONING

- **The Following Processes Are Performed 100% in Accordance With MIL-STD-883**
- **Precap Visual — Method 2010, Cond. B**
- **Stabilization Bake — Method 1008**
- **Temperature Cycle — Method 1010**
- **Centrifuge — Method 2001, Cond. E**
- **Hermeticity — Method 1014, Cond. A, C**
- **(Leak Rate $< 5 \times 10^{-7}$ atm cc/s)**

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range	Harris Equivalent
IH5148MJE	Dual SPST	16 Pin CERDIP	−55°C to 125°C	HI-5048
IH5148CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C	HI-5048
IH5148CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C	HI-5048
IH5149MJE	Dual DPST	16 Pin CERDIP	−55°C to 125°C	HI-5049
IH5149CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C	HI-5049
IH5149CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C	HI-5049
IH5150MJE	SPDT	16 Pin CERDIP	−55°C to 125°C	HI-5050
IH5150CJE	SPDT	16 Pin CERDIP	0°C to 70°C	HI-5050
IH5150CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C	HI-5050
IH5151MJE	Dual SPDT	16 Pin CERDIP	−55°C to 125°C	HI-5051
IH5151CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C	HI-5051
IH5151CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C	HI-5051

NOTES: 1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

7

304300-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+, V^- ..... <36V
V^+, V_D ..... <30V
V_D, V^- ..... <30V
V_D, V_S ..... < ±22V
V_L, V^- ..... <33V
V_L, V_{IN} ..... <30V
V_L ..... <20V
V_{IN} ..... <20V
Current (Any Terminal) ..... <50mA
Storage Temperature ..... −65°C to +150°C

Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

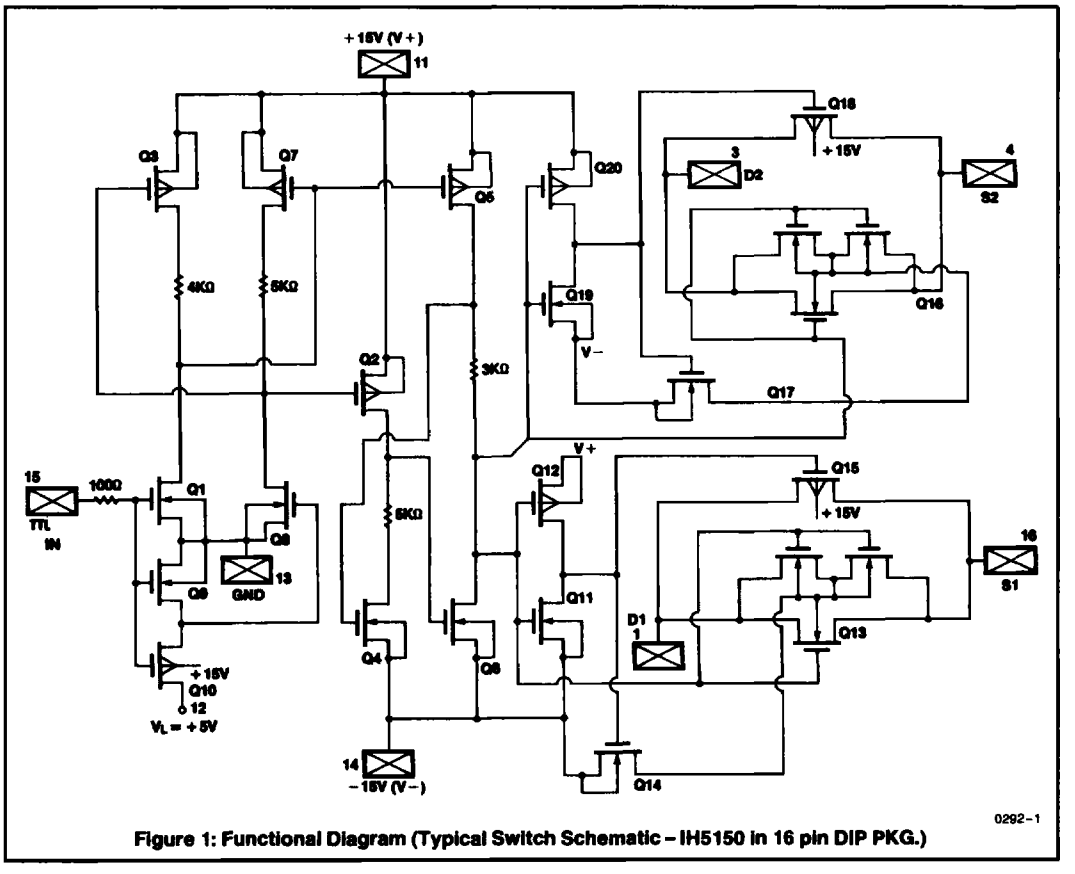


Figure 1: Functional Diagram (Typical Switch Schematic – IH5150 in 16 pin DIP PKG.)

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (T_A @ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Commercial			
Symbol	Characteristic		−55°C	+25°C	+125°C	0	+25°C	+70°C	
$I_{IN(ON)}$	Input Logic Current	$V_{IN} = 2.4V$ (Note 1)	±1	±1	±10		±1	±10	μA
$I_{IN(OFF)}$	Input Logic Current	$V_{IN} = 0.8V$ (Note 1)	±1	±1	±10		±1	±10	μA
$R_{DS(ON)}$	Drain-Source On Resistance	$V_D = \pm 10V$, $I_S = -10mA$	25	25	50		30		Ω
$\Delta R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match			10 (Typ)			15 (Typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±14 (Typ)			±14 (Typ)		V
$I_{D(OFF)}$ $I_{S(OFF)}$	Switch OFF Leakage Current	$V_{ANALOG} = -10V$ to $+10V$		±1.0	100		±2.0	100	nA
$I_{D(ON)} + I_{S(ON)}$	Switch On Leakage Current	$V_D = V_S = -10V$ to $+10V$		±1.0	100		±2.0	100	nA
$Q_{(INJ)}$	Charge Injection	See Figure 4		(10) (Typ)			(10) (Typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, $R_L = 100\Omega$, $C_L \leq 5pF$, See Figure 5		54 (Typ)			50 (Typ)		dB
SUPPLY									
I^+	+Power Supply Quiescent Current	$V_1 = +15V$, $V_2 = -15V$. $V_L = +5V$, $V_R = 0$	10	10	100		10		μA
I^-	−Power Supply Quiescent Current		10	10	100		10		μA
I_L	+5V Supply Quiescent Current		10	10	100		10		μA
I_{GND}	Gnd Supply Quiescent Current		10	10	100		10		μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Figure 8		54 (Typ)			50 (Typ)		dB

NOTE 1. Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce "ON" or "OFF" state.

7

SWITCHING TIME SPECIFICATION

IH5148 SPST SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1K\Omega$, $V_{ANALOG} = -10V$		250	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		200	ns

IH5149 DPST SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1K\Omega$, $V_{ANALOG} = -10V$		350	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		250	ns

IH5150 & IH5151 SPDT SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1K\Omega$, $V_{ANALOG} = -10V$		500	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		250	ns

NOTE 2. For IH5150 & IH5151 devices, channels which are off for logic input ≥ 2.4V (Pins 3 & 4 on 5150, & Pins 3 & 4, 5 & 6 on 5151) have slower t_{on} time, than channels on Pins 1, 16, & 8, 9. This is done so switch will maintain break-before-make action when connected in DT configuration, i.e. Pin 1 connected in Pin 3.

NOTE: All typical values have been characterized but are not tested.

IH5148-IH5151

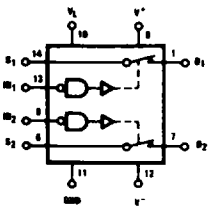
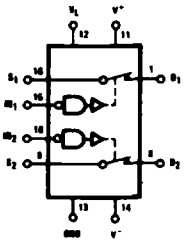
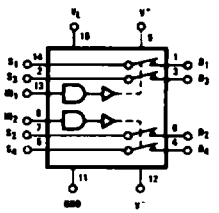
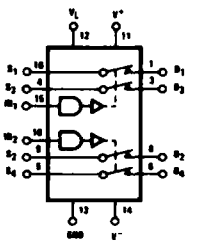
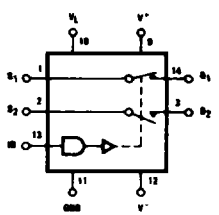
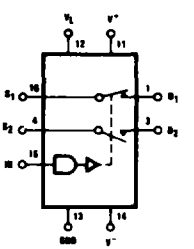
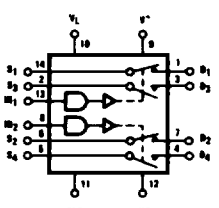
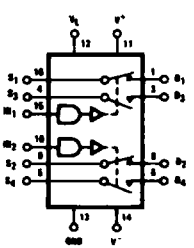
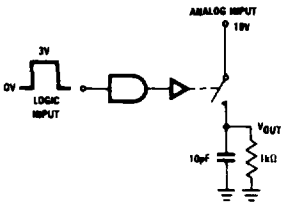
SWITCH STATES ARE FOR LOGIC "1" INPUT	FLAT PACKAGE	DIP (DE) PACKAGE
DUAL SPST IH5148	 0292-2	 0292-3
DUAL DPST IH5149	 0292-5	 0292-6
SPDT IH5150	 0292-7	 0292-8
DUAL SPDT IH5151	 0292-10	 0292-11

Figure 2: Switching State Diagrams

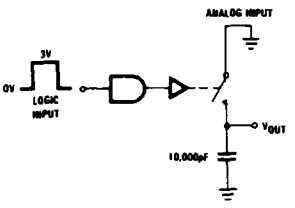
NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



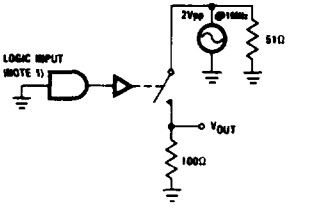
0292-12

Figure 3



0292-13

Figure 4

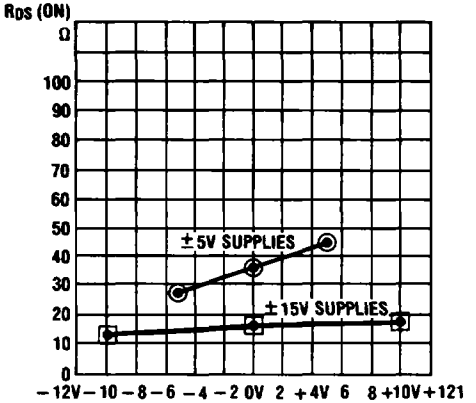


0292-14

Figure 5

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

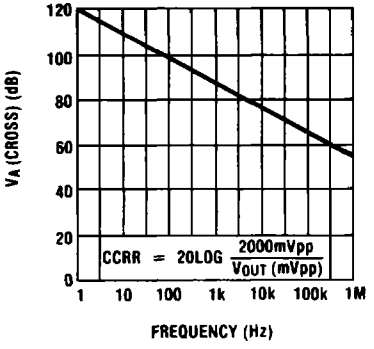
$R_{DS(ON)}$ @ ±15V, ±5V SUPPLIES



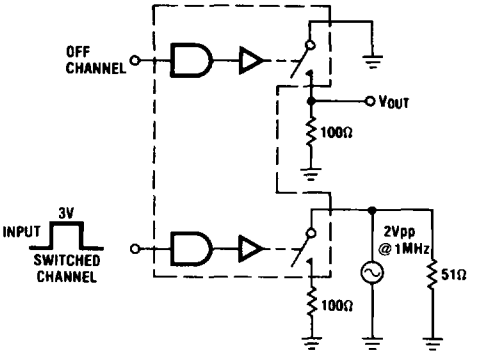
$R_{DS(ON)}$ vs
ANALOG INPUT VOLTAGE

0292-15

CROSS COUPLING
REJECTION vs FREQUENCY



0292-16



0292-17

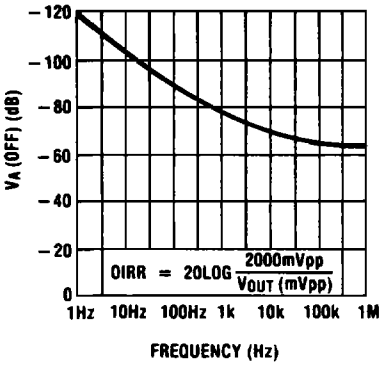
CROSS COUPLING
REJECTION TEST CIRCUIT

NOTE: All typical values have been characterized but are not tested.

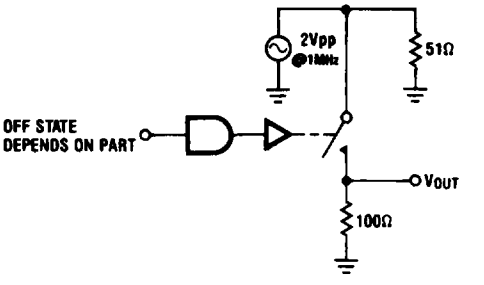
IH5148-IH5151

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) (Continued)

OFF ISOLATION vs FREQUENCY



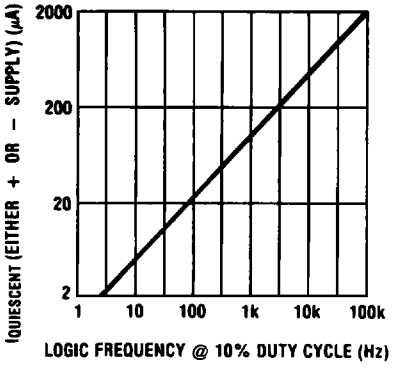
0292-18



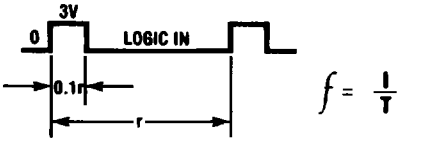
0292-19

OFF ISOLATION TEST CIRCUIT

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

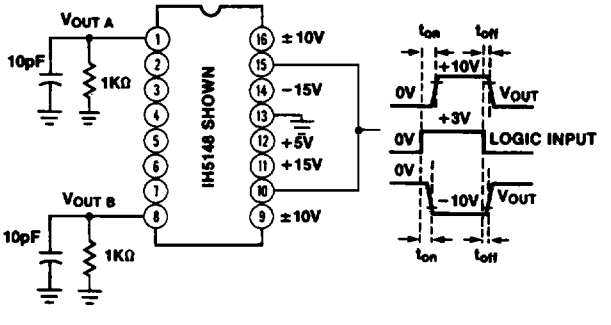


0292-20



0292-21

LOGIC INPUT WAVEFORM



0292-22

Figure 6: Switching Time Test Circuit

NOTE: All typical values have been characterized but are not tested.

Nulling Out Charge Injection:

Charge injection (Qinj. on spec. sheet) is caused by gate to drain, or gate to source capacitance of the output switch MOSFET. The gates of these MOSFETs typically swing from −15V to +15V as a rapidly changing pulse; thus this 30Vpp pulse is coupled through gate capacitance to output load capacitance, and the output "step" is a voltage divider from this combination. For example:

$$Q\text{inject (Vpp)} \cong \frac{C_{gate}}{C_{Load}} \times 30\text{V step.}$$

i.e.

$C_{gate} = 1.5\text{pF}$, $C_{Load} = 1000\text{pF}$, then

$$Q\text{inject(Vpp)} = \frac{1.5\text{pF}}{1000\text{pF}} \times 30\text{V step} = 45\text{mVpp}$$

Thus if you are using switch in a Sample & Hold application with $C_{sample} = 1000\text{pF}$, a 45mVpp "Sample to Hold error step" will occur.

To null this error step out to zero the following circuit can be used:

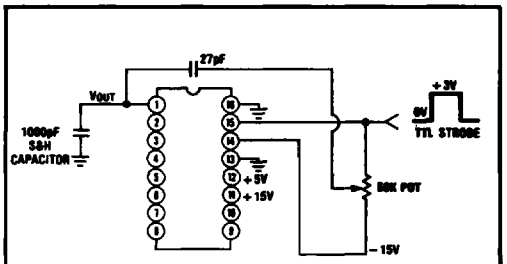


Figure 7: Adjustable Charge Injection Compensation Circuit

The circuit shown above nulls out charge injection effects on switch pins 1 and 16; a similar circuit would be required on switch pins 8 and 9.

Simply adjust the pot until $V_{OUT} = 0\text{mVpp}$ pulse, with $V_{ANALOG} = 0\text{V}$.

If you do not desire to do any adjusting, but wish the least amount of charge injection possible, then the following circuit should be used:

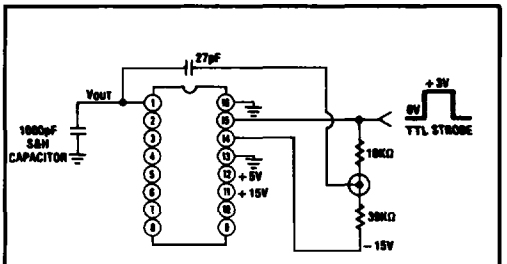


Figure 8: No-Adjust Charge Injection Compensation Circuit

This configuration will produce a typical charge injection of $V_{OUT} \leq 10\text{mVpp}$ into the 1000pF S & H capacitor shown.

Fault Condition Protection

If your system has analog voltage levels which are independent of the ±15V (Power Supplies), and these analog levels can be present when supplies are shut off, you should add fault protection diodes as shown below:

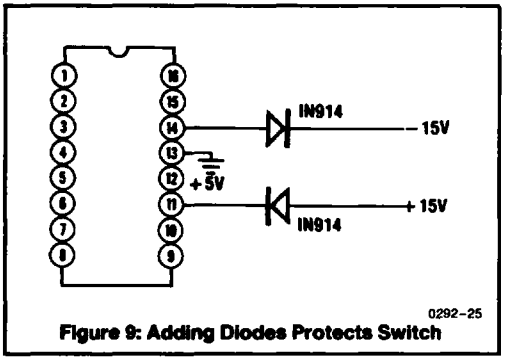


Figure 9: Adding Diodes Protects Switch

If the analog input levels are below ±15V, the pn junctions of Q13 & Q15 are reversed biased. However if the ±15V supplies are shut off and analog levels are still present, the configuration becomes:

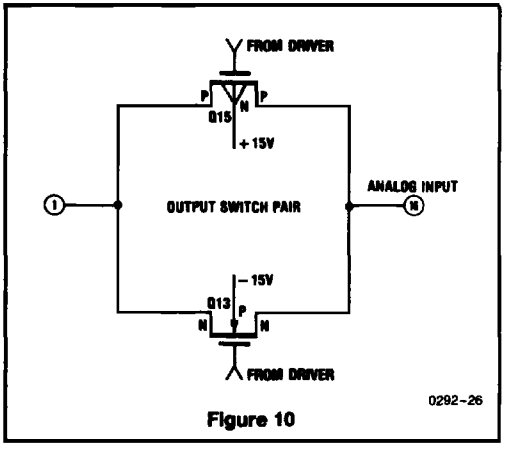


Figure 10

7

NOTE: All typical values have been characterized but are not tested.

IH5148-IH5151

The need for these diodes, in this circumstance, is shown below:

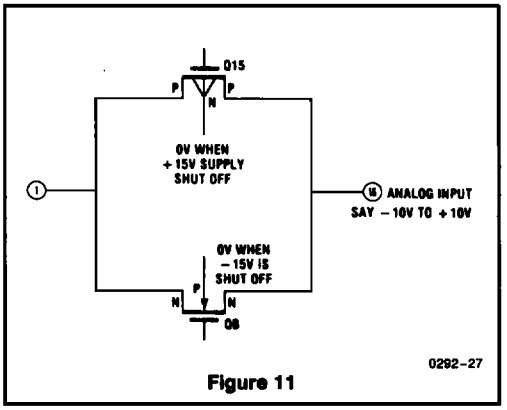


Figure 11

If ANALOG in is greater than 1V, then the pn junction of Q15 is forward biased and excessive current will be drawn. The addition of IN914 diodes prevents the fault currents from destroying the switch. A similar event would occur if ANALOG in was less than or equal to −1V, wherein Q13 would become forward biased. The IN914 diodes form a "back to back" diode arrangement with Q13 & Q15 bodies.

This structure provides a degree of overvoltage protection when supplies are on normally, and analog input level exceeds supplies.

This circuit will switch up to about ±18V ANALOG overvoltages. Beyond this drain(N) to body(P) breakdown VOLTAGE of Q13 limits overvoltage protection.

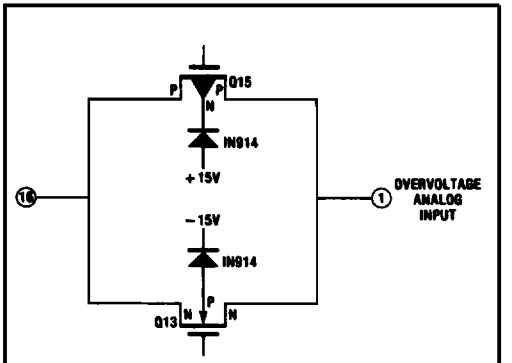


Figure 12

NOTE: All typical values have been characterized but are not tested.