Integrated 500 mA Load Switch with Quad Signal Switch

Data Sheet **ADP1190A**

FEATURES

- **Low input voltage range: 1.4 V to 3.6 V**
- **Load switch**
  - **Low RDS_{ON_L} of 65 mΩ at 3.6 V**
  - **500 mA continuous operating current**
- **4 SPST normally open signal switches**
  - **RDS_{ON_S} of 3 Ω at 1.8 V**
- **Internal charge pump for constant signal switch RDS_{ON}**
- **Output discharge resistance (R_{DIS}): 215 Ω at the output side of the load switch and each analog signal switch output**
- **Built-in level shift for control logic that can operate by a 1.2 V logic**
- **Ultralow shutdown current: 0.7 µA**
- **Ultrasmall 1.2 mm × 1.6 mm × 0.5 mm, 12-ball, 0.4 mm pitch WLCSP**

APPLICATIONS

- **Mobile phones**
- **SIM card disconnect switches**
- **Digital cameras and audio devices**
- **Portable and battery-powered equipment**

FUNCTIONAL BLOCK DIAGRAM

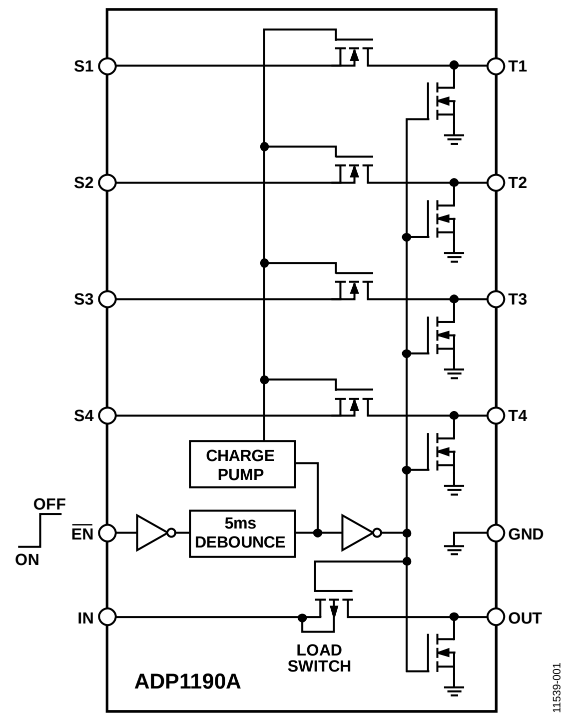

Figure 1.

GENERAL DESCRIPTION

The ADP1190A is an integrated high-side load switch with four signal switches designed for operation from 1.4 V to 3.6 V. This load switch provides power domain isolation for extended power battery life. The load switch is a low on-resistance P-channel MOSFET that supports up to 500 mA of continuous load current and minimizes power loss. Integrated with the load switch are four normally open, 3 Ω single pole, single throw (SPST) signal switches controlled by the charge pump.

Beyond its excellent operating performance, the ADP1190A occupies minimal printed circuit board (PCB) space with an area less than 1.92 mm^2 and a height of 0.50 mm. The ADP1190A is available in an ultrasmall 1.2 mm × 1.6 mm × 0.5 mm, 12-ball, 0.4 mm pitch WLCSP.

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Technical Support **www.analog.com**

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REVISION HISTORY

9/13—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, I_{LOAD} = 200 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +85°C	1.4		3.6	V
$\overline{EN}$ INPUT						
$\overline{EN}$ Input Threshold	V_{EN_TH}	1.4 V < V_{IN} < 1.8 V, T_J = −40°C to +85°C (active low)	0.35		1.2	V
		1.8 V ≤ V_{IN} ≤ 3.6 V, T_J = −40°C to +85°C (active low)	0.45		1.2	V
Logic High Voltage	V_{IH}	1.4 V ≤ V_{IN} ≤ 3.6 V	1.2			V
Logic Low Voltage	V_{IL}	1.4 V ≤ V_{IN} ≤ 3.6 V (chip enable)			0.35	V
CURRENT						
Shutdown Current	I_{OFF}	$\overline{EN}$ = V_{IN} or open		0.7		µA
		$\overline{EN}$ = V_{IN} or open, T_J = −40°C to +85°C			2	µA
Analog Switch Off Current	I_{A_OFF}	Into S1, $\overline{EN}$ = V_{IN}		0.2		µA
LOAD SWITCH, V_{IN} TO V_{OUT} RESISTANCE	RDS_{ON_L}	V_{IN} = 3.6 V, I_{LOAD} = 200 mA, $\overline{EN}$ = GND		65		mΩ
		V_{IN} = 2.5 V, I_{LOAD} = 200 mA, $\overline{EN}$ = GND		80		mΩ
		V_{IN} = 1.8 V, I_{LOAD} = 200 mA, $\overline{EN}$ = GND, T_J = −40°C to +85°C		100	200	mΩ
SIGNAL SWITCH RESISTANCE	RDS_{ON_S}	Maximum value of analog input sweep				
		V_{IN} = 3.6 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		3		Ω
		V_{IN} = 2.5 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		3		Ω
		V_{IN} = 1.8 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		3		Ω
RDS Flatness		V_{IN} = 3.6 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		0.2		Ω
		V_{IN} = 1.8 V, I_{LOAD} = 10 mA, $\overline{EN}$ = GND		0.2		Ω
SIGNAL SWITCH INPUT CAPACITANCE	C_{IN}			10		pF
OUTPUT DISCHARGE RESISTANCE	R_{DIS}	At the output side of the load switch and each analog signal switch output, T1, T2, T3, and T4		215		Ω
−3 dB BANDWIDTH	$BW_{-3\ dB}$	V_{IN} = 3.3 V, R_{LOAD} = 50 Ω, C_{LOAD} = 5 pF		50		MHz
V_{OUT} TIME						
Turn-On Delay Time	t_{ON_DLY}	I_{LOAD} = 200 mA, $\overline{EN}$ = GND, C_{LOAD} = 0. 1 µF		5		ms
Turn-Off Delay Time	t_{OFF_DLY}	V_{IN} = 3.6 V, I_{LOAD} = 200 mA, $\overline{EN}$ = 1.5 V, C_{LOAD} = 0.1 µF		2		µs

Timing Diagram

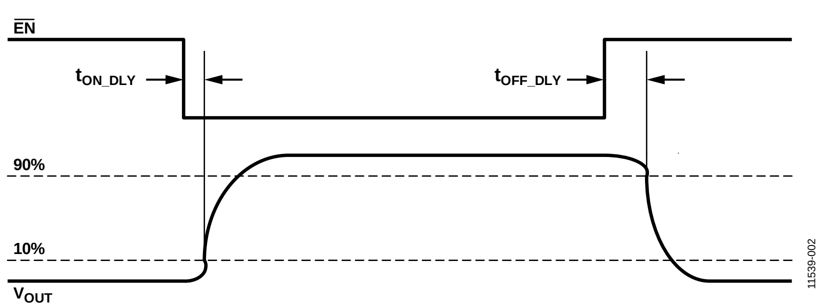

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{IN} to GND	−0.3 V to +4.0 V
V_{OUT} to GND	−0.3 V to V_{IN}
Sx to GND	−0.3 V to +4.0 V
Tx to GND	−0.3 V to +4.0 V
$\overline{EN}$ to GND	−0.3 V to +4.0 V
Continuous Load Switch Current	
T_A = 25°C	±1 A
T_A = 85°C	±500 mA
Continuous Diode Current	−50 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Operating Temperature Range	
Junction Temperature Range	−40°C to +125°C
Ambient Temperature Range	−40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP1190A can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The T_J of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum T_J is calculated from T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} can vary, depending on PCB material, layout, and environmental conditions. The specified value of θ_{JA} is based on a 4-layer, 4 inch × 3 inch circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum T_J is calculated from the board temperature (T_B) and P_D using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
12-Ball WLCSP	130	29.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

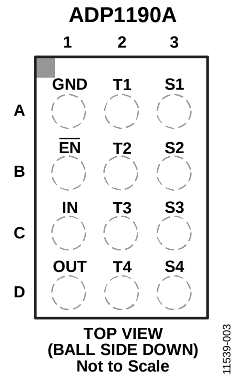

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	GND	Ground.
B1	$\overline{\text{EN}}$	Enable Input, Active Low.
C1	IN	Input Voltage.
D1	OUT	Load Switch Output Voltage.
A2	T1	Channel 1 Analog Switch. Connect Pin A2 to the SIM card socket (has active discharge).
B2	T2	Channel 2 Analog Switch. Connect Pin B2 to the SIM card socket (has active discharge).
C2	T3	Channel 3 Analog Switch. Connect Pin C2 to the SIM card socket (has active discharge).
D2	T4	Channel 4 Analog Switch. Connect Pin D2 to the SIM card socket (has active discharge).
A3	S1	Channel 1 Analog Switch. Connect Pin A3 to the microcontroller.
B3	S2	Channel 2 Analog Switch. Connect Pin B3 to the microcontroller.
C3	S3	Channel 3 Analog Switch. Connect Pin C3 to the microcontroller.
D3	S4	Channel 4 Analog Switch. Connect Pin D3 to the microcontroller.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.8 V, V_{EN} = V_{IN}, I_{LOAD} = 200 mA, C_{IN} = C_{OUT} = 1 μF, T_A = 25°C, unless otherwise noted.

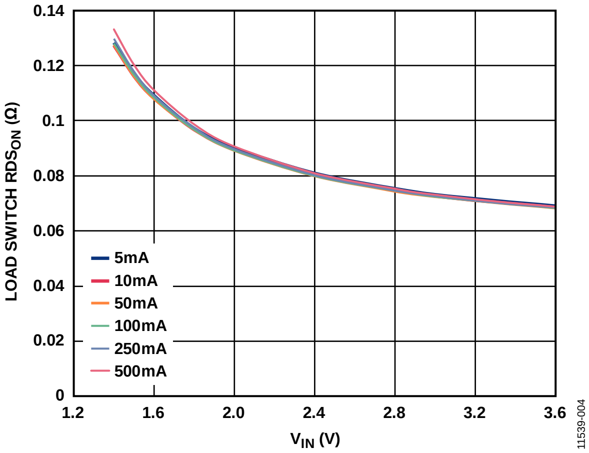

Figure 4. Load Switch RDS$_{ON}$ vs. Input Voltage (V_{IN}) for Different Load Currents

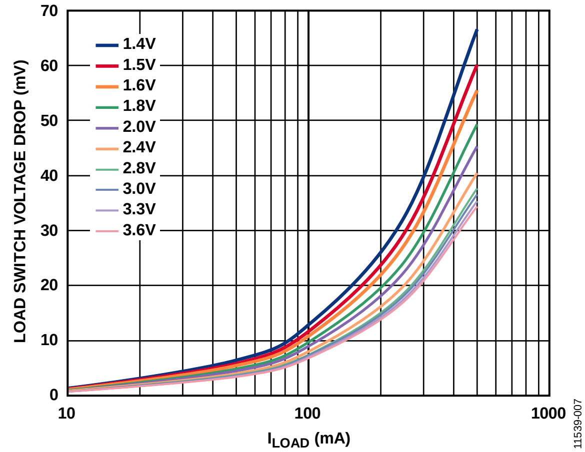

Figure 7. Load Switch Voltage Drop vs. Load Current (I_{LOAD}) for Different Input Voltages

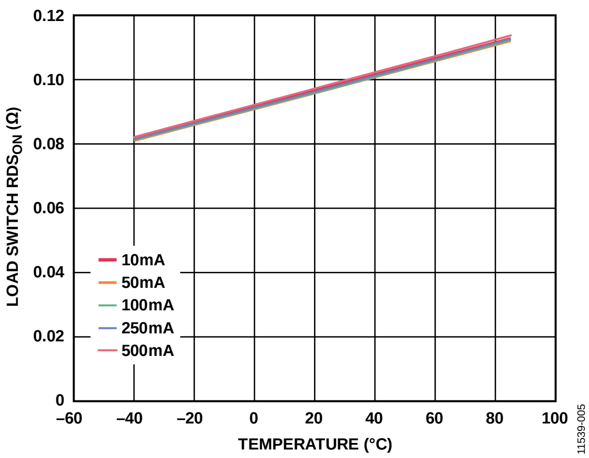

Figure 5. Load Switch RDS$_{ON}$ vs. Temperature for Different Load Currents, V_{IN} = 1.8 V

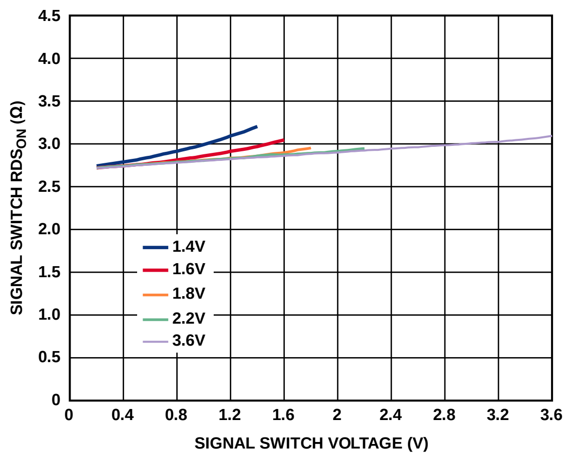

Figure 8. Signal Switch RDS$_{ON}$ vs. Signal Switch Voltage, Different Input Voltages

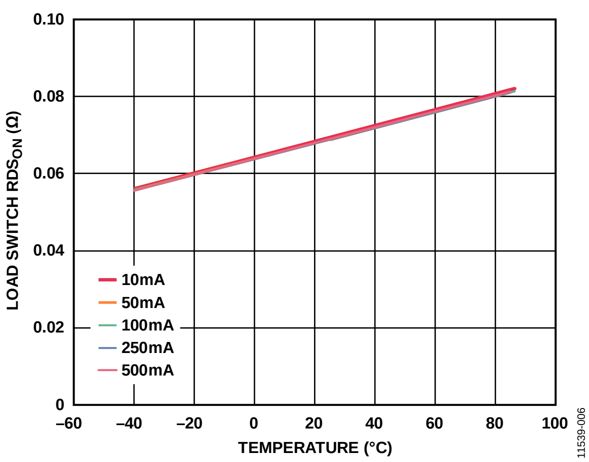

Figure 6. Load Switch RDS$_{ON}$ vs. Temperature for Different Load Currents, V_{IN} = 3.6 V

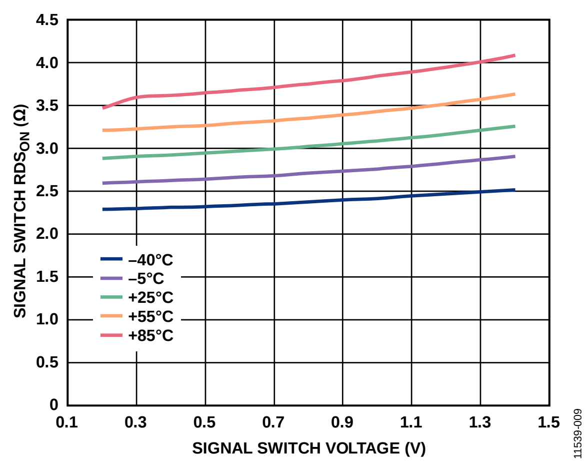

Figure 9. Signal Switch RDS$_{ON}$ vs. Signal Switch Voltage for Various Temperatures, V_{IN} = 1.4 V

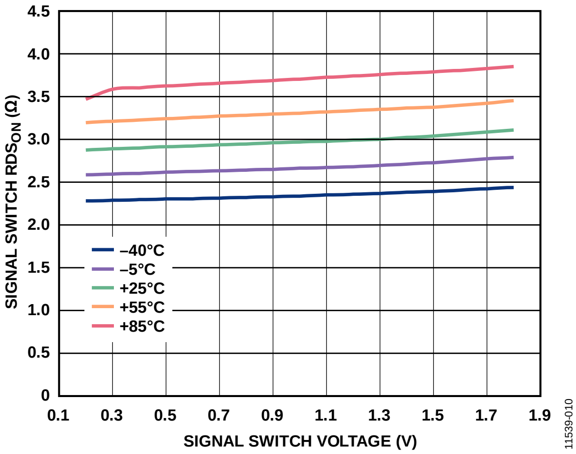

Figure 10. Signal Switch RDS_{ON} vs. Signal Switch Voltage for Various Temperatures, V_{IN} = 1.8 V

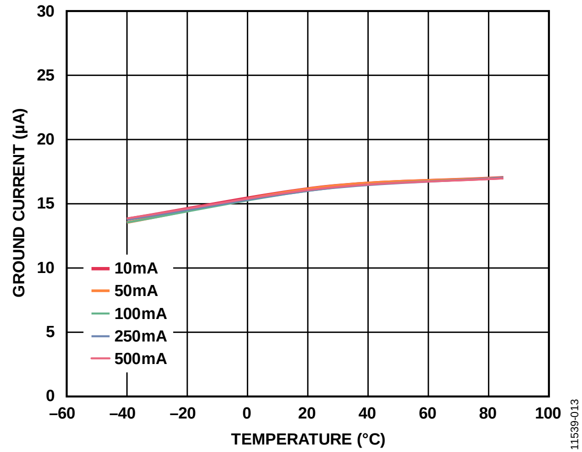

Figure 13. Ground Current vs. Temperature for Different Load Currents, V_{IN} = 1.8 V

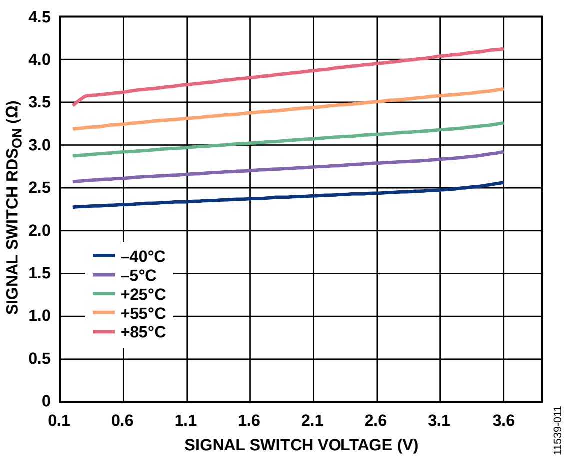

Figure 11. Signal Switch RDS_{ON} vs. Signal Switch Voltage for Various Temperatures, V_{IN} = 3.6 V

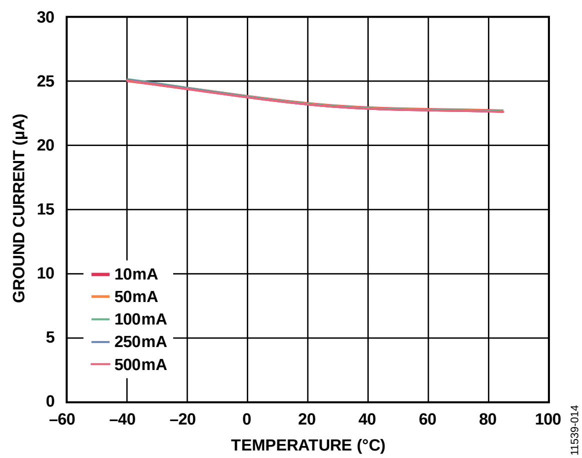

Figure 14. Ground Current vs. Temperature for Different Load Currents, V_{IN} = 3.6 V

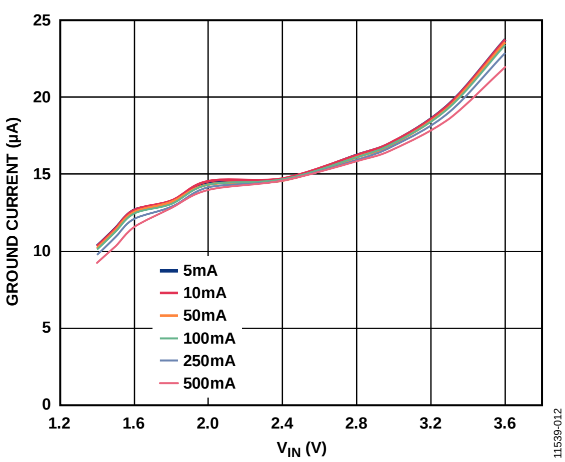

Figure 12. Ground Current vs. Input Voltage (V_{IN}) for Different Load Currents

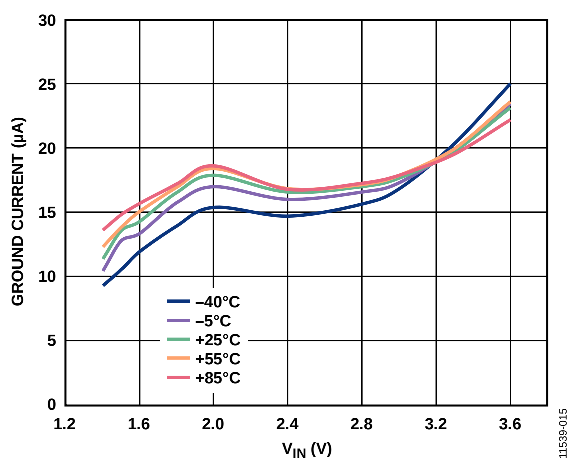

Figure 15. No Load Ground Current vs. Input Voltage (V_{IN}) for Various Temperatures

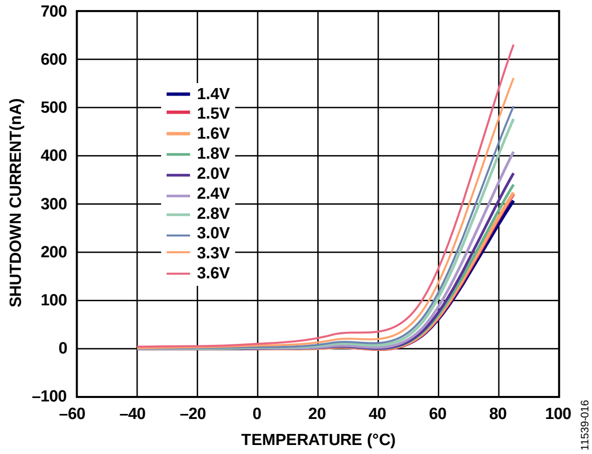

Figure 16. Shutdown Current vs. Temperature for Different Input Voltages

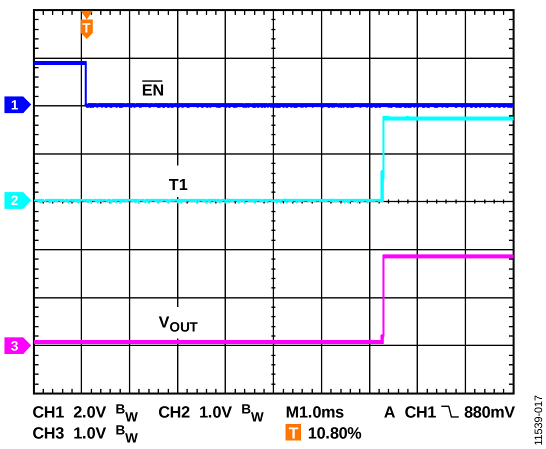

Figure 17. Typical Turn-On Delay Time, V_{IN} = 1.8 V, 50 mA Load

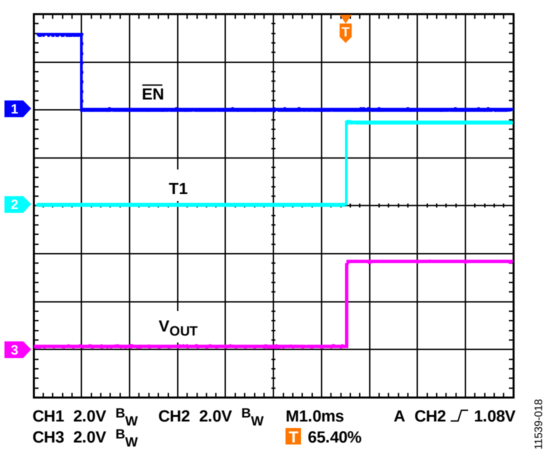

Figure 18. Typical Turn-On Delay Time, V_{IN} = 3.6 V, 100 mA Load

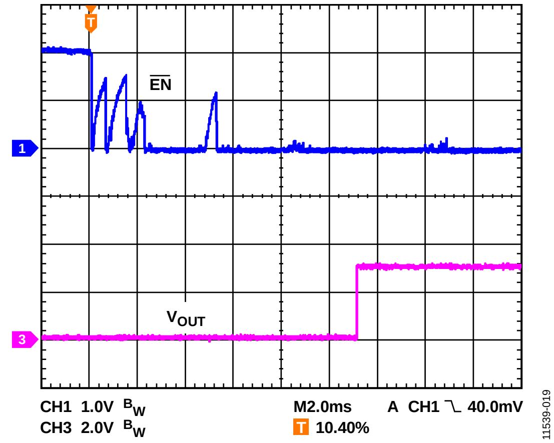

Figure 19. Enable Debounce Behavior, V_{IN} = 1.8 V

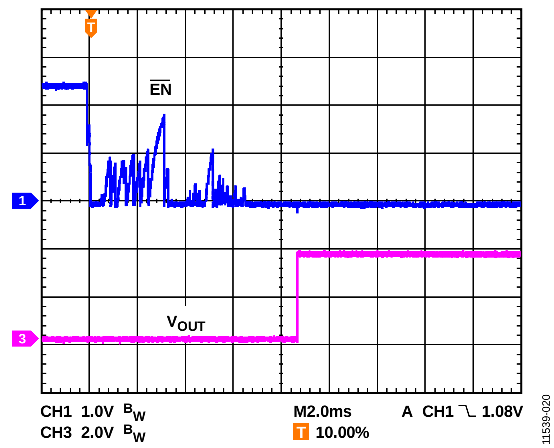

Figure 20. Enable Debounce Behavior, V_{IN} = 3.6 V

THEORY OF OPERATION

The ADP1190A is a high-side load switch integrated with four signal switches. The load switch and signal switches are turned on by a low signal on the $\overline{EN}$ pin. When the device is disabled, the T1 to T4 pins are actively pulled down with a nominal resistance of 215 Ω. There is a 5 ms debounce counter on $\overline{EN}$ for use with a mechanical $\overline{EN}$ switch. That is, hold $\overline{EN}$ low for 5 ms before the device is enabled. If $\overline{EN}$ transitions high before this timeout, the counter is reset and starts a new 5 ms count.

The signal paths are N-channel MOSFETs with 3 Ω on resistance. Break-before-make logic control ensures that the active pull-down is off before the signal path is enabled.

The ADP1190A also has an internal charge pump that provides a regulated voltage at the gates of the N-channel MOSFETs, resulting in a more stable signal switch on resistance over different input voltages and temperature.

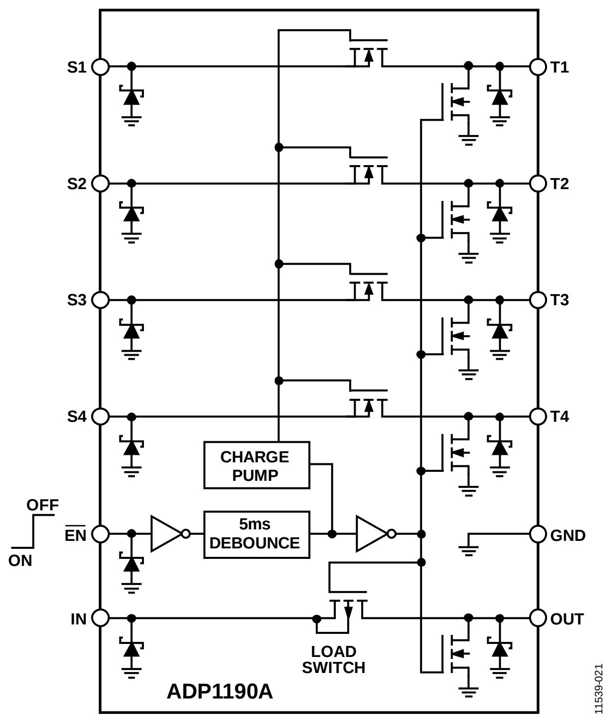

Figure 21. Block Diagram with ESD Protection Devices

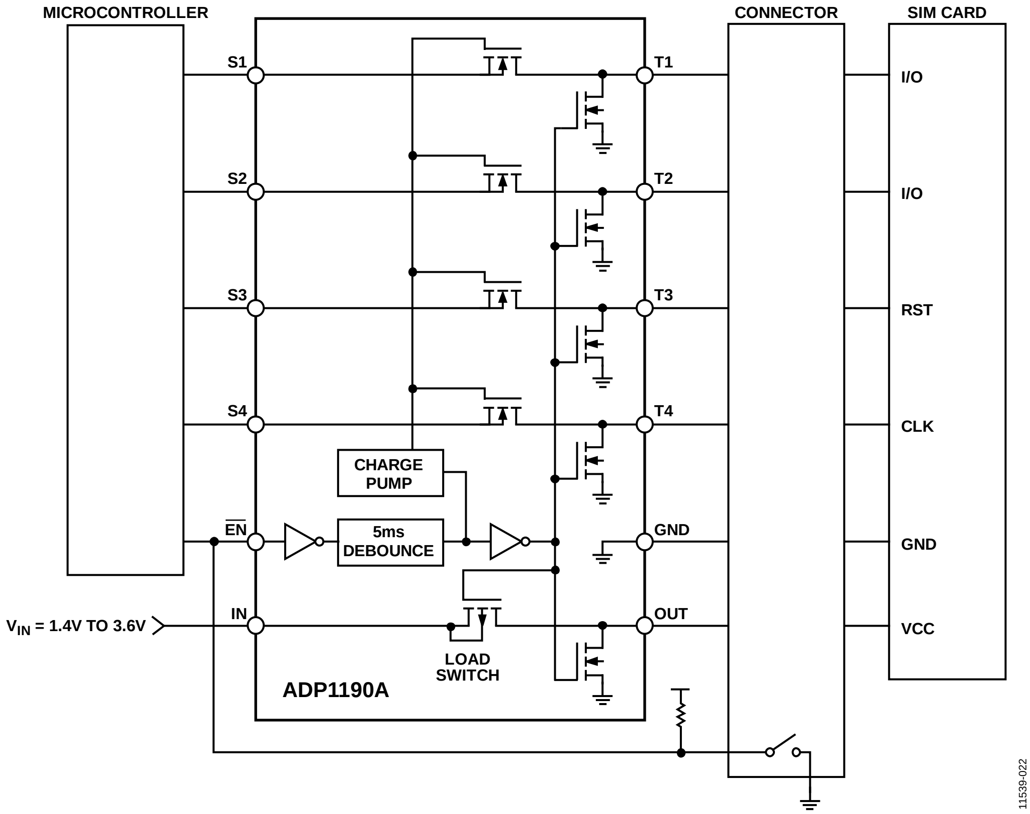

Figure 22. Typical Application Diagram

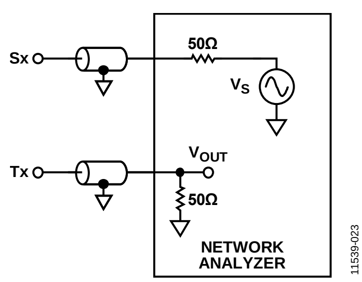

Figure 23. Bandwidth Measurement Setup

OUTLINE DIMENSIONS

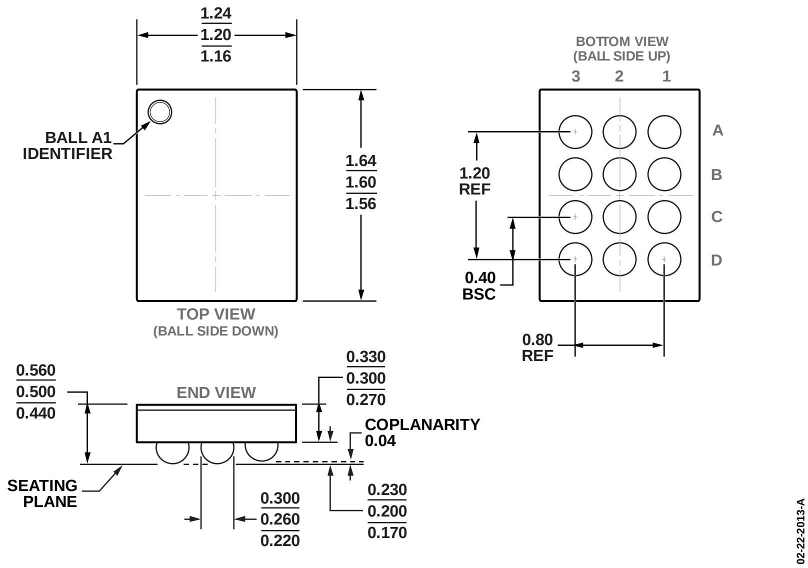

Figure 24. 12-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-12-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADP1190AACBZ-R7	−40°C to +85°C	12-Ball Wafer Level Chip Scale Package [WLCSP]	CB-12-10	LNW

[1] Z = RoHS Compliant Part.

NOTES